A 9.2mW 528/66/50MHz Monolithic Clock Synthesizer for Mobile μP Platforms

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***Abstract*—A low-power monolithic clock synthesizer suitable for use in mobile μP platforms is presented. Clock synthesis is accomplished using an all-Si RF *LC* reference oscillator that does not require an external frequency reference. Fabricated in 0.18μm CMOS, the developed clock synthesizer demonstrates ±1% frequency accuracy over process, voltage, and 0-70°C, exhibits 7.4/21/33ps$_{rms}$ period jitter on 528/66/50MHz clock signals, and achieves a start-up latency of only 3.2μs.**

I. Introduction

Topics of interest in the area of time and frequency synthesis for processor systems include dynamic frequency scaling [1] and external reference (e.g. quartz and ceramic resonators) elimination. When compared to constant frequency operation, dynamic frequency scaling permits a reduction in total system power dissipation. Beyond dynamic frequency scaling, the ability to turn the clock synthesizer OFF and ON with very low latency permits additional power savings. The elimination of external references reduces form factor and can reduce system cost. In this work, it is shown that a RF *LC* reference oscillator enables low-latency start-up and is well-suited to high-accuracy monolithic clock synthesis.

II. Background

Of free-running integrated oscillator topologies including *LC*, phase shift (or *RC*), ring, and relaxation, *LC* oscillators exhibit the best short-term frequency stability and lowest frequency drift over variations in power supply voltage and temperature because unlike the other topologies, the oscillation frequency of an *LC* oscillator is set by a high-*Q* harmonic reference.

High-frequency phase locked *LC* oscillators have been the workhorses of frequency synthesis in RF and high-data-rate (over a GHz) digital electronics for years. However, they have only recently been explored as free-running frequency references for lower-speed and moderate-accuracy digital clock synthesis in applications such as general purpose microcontrollers [2] and mobile μP platforms, the latter of which is target of this work.

In typical clock synthesizers, a low frequency reference oscillator is coupled to a phased-locked loop (PLL) with a large frequency multiplication factor. As shown in [3], such implementations suffer from high jitter due to noise accumulation inherent to frequency multiplication. In contrast, a high frequency reference oscillator permits frequency division which reduces jitter by the same factor in which it is accumulated in the PLL approach. Thus, an RF *LC* reference oscillator, with even a modest division ratio, can be utilized to develop very low jitter clock signals. In the RF *LC* reference oscillator approach, the primary design challenge becomes maintaining high frequency-accuracy over variations in process, power supply voltage, temperature.

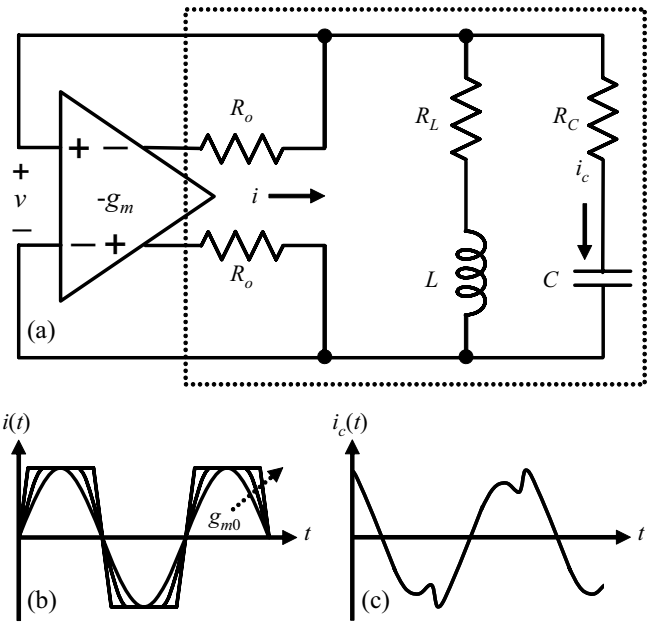

Fig. 1. (a) Generalized schematic of a -g_m *LC* oscillator with a lossy integrated *L* and *C* as well as a finite -g_m amplifier output resistance. (b) As g_{m0} is increased, the harmonic content of $i(t)$ increases as the waveform becomes more square. (c) The injected current is absorbed by the capacitor on each half-cycle distorting $i_c(t)$ and ultimately $v(t)$ and the oscillation frequency (f_o).

Fig. 1a shows the schematic a generalized negative-transconductance (-g_m) *LC* oscillator with finite amplifier output impedance and parasitic inductor and capacitor implementation losses. Ignoring all of the loss in the system, the natural frequency of the system is $\omega_o = \sqrt{1/(LC)}$. However, considering the parasitic losses in the tank, R_L and R_C, the natural frequency of the system, which must be redetermined by solving for the zero phase of the lossy *LC* network, becomes:

$$\omega_o = \sqrt{\frac{1}{LC}\left(\frac{CR_L^2 - L}{CR_C^2 - L}\right)} \tag{1}$$

In monolithic *LC* oscillators, R_L is usually substantially larger than R_C; thus, (1) can be reduced to the following:

$$\omega_o = \sqrt{\frac{1}{LC}\left(1 - \frac{CR_L^2}{L}\right)} \tag{2}$$

To ensure start-up and sustain oscillation, the $-g_m$ amplifier must overcome the loss present in the tank. A simple analysis reveals that the minimum g_m, g_{m0}, required to guarantee that the oscillation is sustained is $g_{m0} = CR_L/L$. In practice, the amplifier's transconductance is designed to be a factor of 3 or more greater than g_{m0} ensuring start-up over process and environmental variation. This overdesign results in a high gain $-g_m$ amplifier, and consequently, the shape of the current waveform injected into the tank network is substantially square and possess high harmonic content as shown in Fig. 1b. Because the current passing through the tank inductor cannot change instantaneously, the injected current is absorbed by the tank capacitor as shown in Fig. 1c. Ultimately, the voltage waveform synthesized by the oscillator and its frequency are distorted by this current injection. This should be clear realizing that the voltage across the tank is derived from the time-domain integral of the current passing through the capacitor.

Considering the aforementioned effects, the entire *LC* network can be considered more generally as a filter with a response determined by the components contained within the dotted lines in Fig. 1a. L, R_L, C, and R_C are determined by the designed frequency of oscillation and resistive parasitics inherent to the process technology, while R_o is determined by the size of active components used to realize the $-g_m$ amplifier. Both L and C exhibit very low temperature sensitivity [4] while R_L and R_C exhibit high temperature sensitivity. Considering (2) and ignoring the effects of the $-g_m$ amplifier, the frequency temperature drift of a free-running *LC* oscillator is dominated by the temperature coefficient of R_L and is negative.

With the above information, the challenge of real-time temperature compensation of the reference oscillator's oscillation frequency (f_o) can be reduced to controlling the transconductance of the sustaining amplifier and its output impedance. The former determines the harmonic content of the current injected into the tank while the latter determines the filter response of the *LC* network. When considering the specifics of a $-g_m$ amplifier implementation, both the g_m and the output impedance can be controlled by the bias current and the aspect ratio of the active devices.

III. Clock synthesizer Reference Oscillator and Architecture

In this work, all clock signals are derived via frequency division from a 1.056GHz voltage-controlled reference oscillator comprised of an *LC* tank and a complementary cross-coupled MOS $-g_m$ amplifier as shown in Fig. 2. The reference oscillator tail device is biased by a supply-independent reference current whose temperature dependence is set by the bias topology and is derived from a diode junction. Because the bias current is temperature dependent, care was taken to ensure that the system g_m was never less than $2g_{m0}$ over all possible variations of process, voltage, and temperature. Two 50kΩ resistors create a low-current voltage divider which are used to bias the backgates of accumulation-mode MOS (A-MOS) varactors to $V_{DD}/2$ and allowing the backgates of the A-MOS varactors to track variations in V_{DD} resulting in low power supply frequency drift. A calibration signal, v_{cal}, can be used to overdrive this voltage and calibrate the absolute frequency of the reference oscillator. The inductor is an octagonal hollow-core topology with a patterned ground shield to maximize the component Q-factor of the device. The MOS devices labeled MR_x are reset transistors of polarity x, which disable the reference oscillator and place it into a low-current sleep state when $\overline{R}$ is low. The reference oscillator is powered from a 1.8V power supply and draws a nominal current of approximately 3mA.

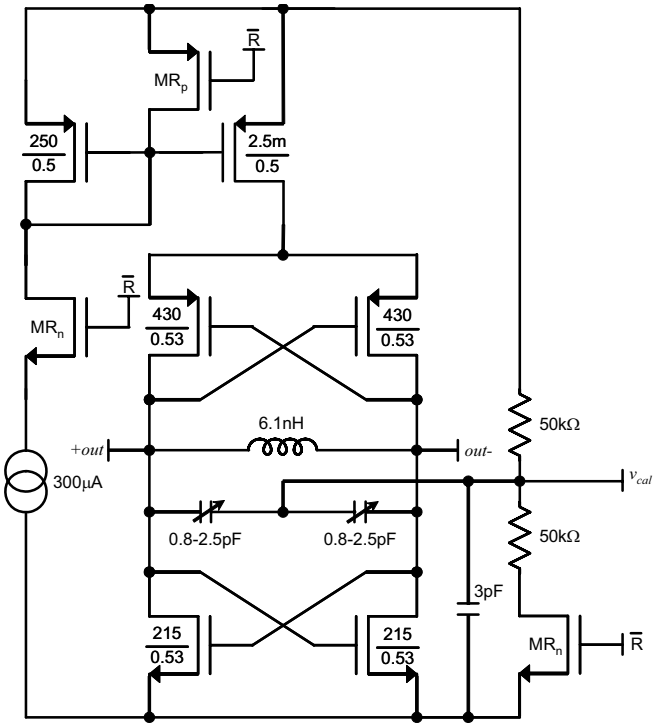

Fig. 2. Schematic of a free-running *LC* clock synthesizer reference oscillator. The aspect ratio of devices in μm unless noted otherwise.

Design considerations include the selection of A-MOS varactors (as opposed to inversion-mode, or I-MOS varactors). A-MOS varactors exhibit a more linear and gradual tuning response with respect to a control voltage as compared to I-MOS varactors. Although this work demonstrates analog frequency calibration, a digital interface is trivial to employ and can be accomplished with a digital-to-analog converter (DAC) that drives v_{cal} or with a switched resistor bank to used set v_{cal}. Additionally, the varactors could be removed and replaced with a switched binary-weighted fixed-capacitor bank. Area and power dissipation tradeoffs are associated with a DAC interface while area is the primary tradeoff associated with a resistor trimming network. A fixed capacitor bank is likely the best calibration interface as it does not dissipate power and requires minimal area to implement; however, monotonicity can be difficult to achieve with a large binary-weighted network. Nevertheless, a digital interface is preferred as it would not require an external calibration voltage. Other design considerations include the use of very large aspect ratio devices in the $-g_m$ amplifier. The aspect ratio of these devices sets the output resistance of the amplifier; the temperature coefficient of this resistance can be utilized along with the bias current, as described previously, to compensate the temperature frequency drift of the reference oscillator.

Fig. 3 shows a schematic of the overall clock synthesizer architecture. The output of the reference oscillator drives a

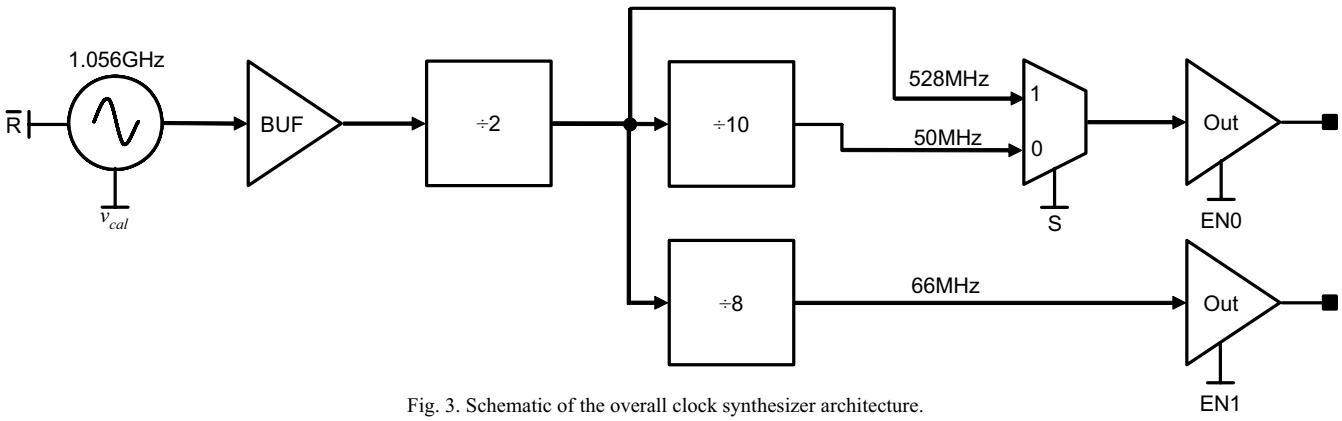

Fig. 3. Schematic of the overall clock synthesizer architecture.

buffer and then a static divide-by-two circuit. The 528MHz clock serves as a µP clock frequency. Subsequent divide-by-10 and divide-by-8 branches derive the 66MHz (for PCI) and 50MHz (when calibrated) clock signals, the latter of which serves as a general purpose time base. The output stages provide rail-to-rail clock signals and include logic to minimize shoot-through current. The output drivers operate from a separate 1.2V power supply, can drive 10pF loads with 100ps rise and fall times, dissipate 20mA$_{rms}$, and can be disabled and either shorted to ground or placed into a high-impedance state.

IV. Experimental Results

The clock synthesizer was fabricated in *IBM Microelectronics'* 0.18µm RF CMOS process (7RF). A die micrograph is shown in Fig. 4. Although fabricated in an RF CMOS process, no process options were utilized in its design which preclude it from being fabricated in a logic process, with the exception of a thick top metal option. In a logic process, where thick top metal is not an option, a high-*Q* inductor structure can be realized by connecting the two top-most metal layers in parallel.

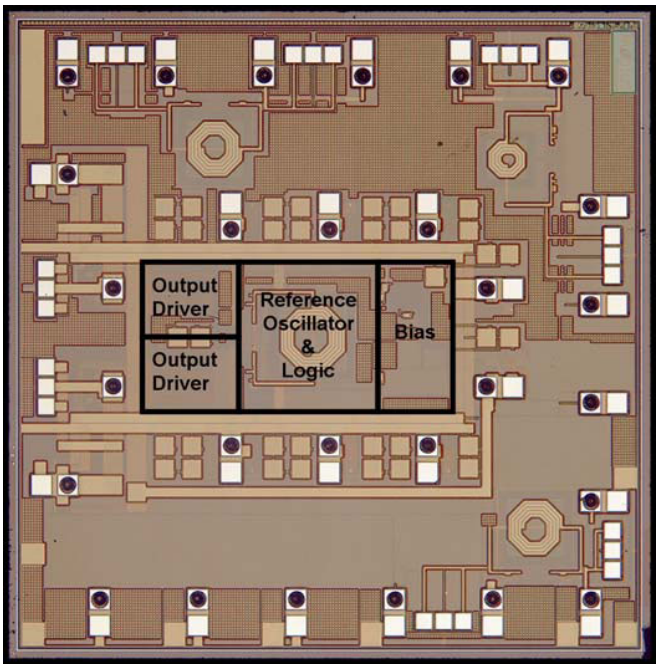

Fig. 4. Die micrograph of fabricated clock synthesizer including Au studs for multi-chip module assembly. Test macros populate the periphery of the die.

The fabricated clock synthesizer was packaged in a ceramic 16-pin DIP and mounted to a double-sided FR4 PCB for initial characterization. Au studding, as shown in Fig. 4, was completed after characterization allowing the device to be flip-chip incorporated into a multi-chip module where it serves as the sole clock reference on a motherboard.

All frequency domain measurements were captured with an *Agilent* E4405B spectrum analyzer. Due to process variation, calibration was required to center the frequency of the reference oscillator. The measured frequency calibration range was ±6.2%. The normalized drift of the reference oscillator's oscillation frequency due to variations in power supply voltage and temperature is shown in Fig. 5. Measurements were made over a ±10% power supply variation and a temperature range of -40°C to 100°C; the worst case power supply frequency drift was ±0.33% at 100°C (at 25°C, the power supply frequency drift was ±0.17%). Over a -40°C to 100°C temperature range, the reference oscillator exhibited a temperature frequency drift of ±1.5%. Over the reduced consumer temperature range of 0°C to 70°C, a frequency drift of only ±0.75% was measured. Combining the effects of power supply, temperature, and process variation, the reference oscillator exhibits a total fre-

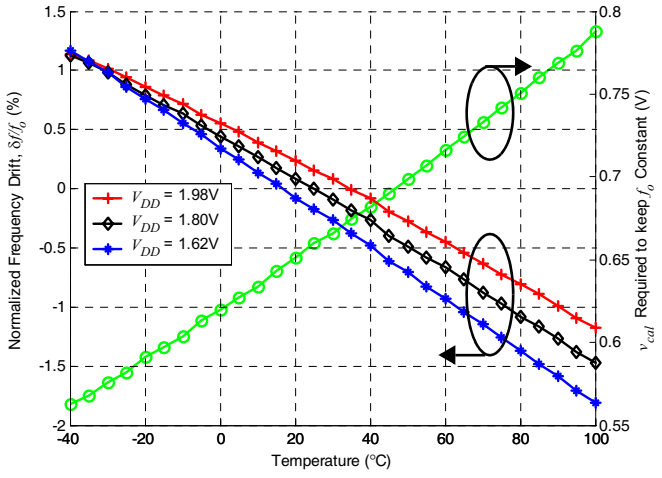

Fig. 5. Normalized frequency drift due to variations in power supply voltage and temperature (left axis). v_{cal} voltage required to maintain a constant output frequency vs. temperature (right axis).

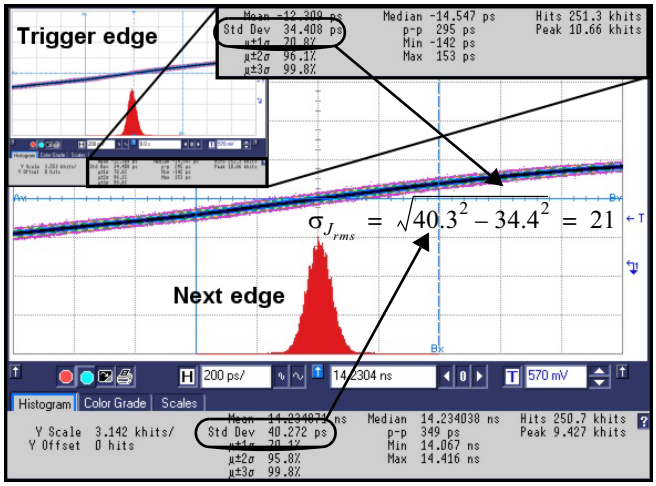

Fig. 6. Statistics captured for jitter calculation on the 66MHz output.

quency drift of less than ±1.8% over all operating conditions and less than ±1% over the range for consumer electronics.

Fig. 5 (right axis) shows that by driving the v_{cal} input with a voltage that exhibits a slope of +1.6mV/°C, the frequency temperature drift of the clock synthesizer can be removed. The least-squares fit of the measured data yields a correlation coefficient of $R^2 = 0.9984$ indicating that very high-accuracy temperature compensation can be achieved by applying a linear temperature-dependent bias voltage to v_{cal}. With this addition, the authors expect that the frequency accuracy of the clock synthesizer can be improved to better than ±0.5% over all operating conditions.

Jitter measurements were made with an *Agilent* Infinium 4GSa/s sampling oscilloscope. RMS period jitter was calculated after collecting statistics on 250k samples of the mid-rail threshold crossing as shown in Fig. 6 for the 66MHz clock. A free-running oscillator exhibits only accumulating jitter; thus, each edge is statistically independent. Therefore, the RMS jitter is calculated by, $\sigma^2_{J_{rms}} = \sigma^2_T - \sigma^2_N$ where σ^2_T is the variance of the trigger edge and σ^2_N is the variance of the subsequent edge [5]. Fig. 6 shows that the measured period jitter was 21ps. Identical measurements were performed for all clock signals.

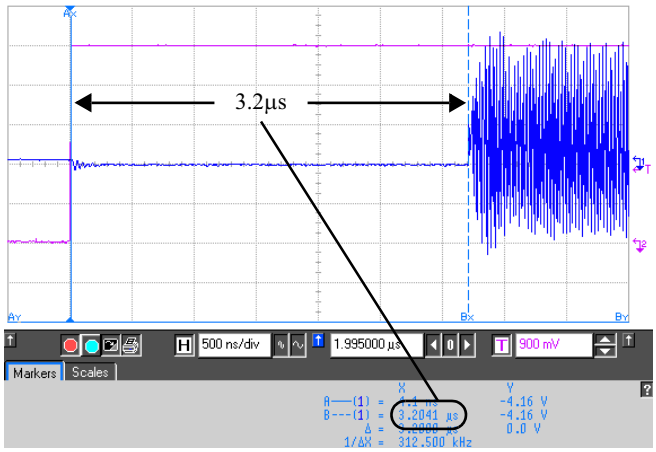

Fig. 7. Measured clock synthesizer start-up latency.

TABLE I CLOCK SYNTHESIZER PERFORMANCE SUMMARY

Parameter	Measured	Unit
Power supply voltage (nom./min.)	1.8/1.12	V
Power supply current (V_{DD} = 1.8V/1.12V)	5.1/3.5	mA
Standby power supply current (V_{DD} = 1.8V)	300	nA
Power dissipation (V_{DD} = 1.8V)	9.2	mW
Output frequencies	49.5-56.2, 61.9-70.2, 495.2-561.6	MHz
Frequency calibration (tuning) range	±6.2	%
RMS period jitter (528/66/50 MHz output)	7.4/21/33	ps
Temperature frequency drift (-40 to 100°C)	±1.5	%
Power supply frequency drift (V_{DD}±10%)	±0.33	%
Total freq. accuracy (process, voltage, temp.)	±1.8	%
Start-up latency	3.2	µs

An intrinsic feature of the proposed clock synthesizer topology that arises because the reference frequency is high as opposed to low is that it can be started with low latency. Fig. 7 shows that approximately 3.2µs of start-up latency was measured. The predominant factor determining this latency is the time constant associated with the start-up of the bias circuitry. In applications where the bias circuitry does not need to be shut down, start-up latency is expected to be less than 1µs. In addition to this low start-up latency, it is worth noting that because the reference is at a high frequency, this topology does not exhibit a lock time as does a phase-locked implementation.

A summary of these measurements, along with DC performance is shown in Table I. The nominal bias current was 5.1mA, and the minimum power supply voltage required to maintain functionality was 1.12V indicating that the clock synthesizer is suitable for voltage, as well as frequency, scaling.

V. CONCLUSIONS AND FUTURE WORK

This work demonstrates the potential use of a compensated RF *LC* oscillator as a low-power, monolithic, low-jitter, and high-accuracy clock synthesizer exhibiting low start-up latency. It was shown that the primary source of frequency drift originated from insufficient compensation of the temperature coefficient which arises primarily from the loss inherent in the integrated inductor. In future work, a programmable compensation interface will be included in order to adjust frequency temperature drift compensation after fabrication.

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