A Low-Power Microinstrument for Chemical Analysis of Remote Environments

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Abstract

The need for small, reliable, and accurate microsystems that can remotely monitor earth and extraterrestrial environments has increased demand for single-chip microinstruments with long lifetimes. This paper presents work toward a monolithic, low-power, mixed-signal microcontroller that is capable of measuring, processing, and storing data from liquid chemical sensors. The system consists of a potentiostatic interface circuit, programmable gain amplifier, analog-to-digital converter, microprocessor core, on-chip memory, and a CMOS-MEMS monolithic clock reference. The microinstrument was designed in *TSMC's* 0.18 µm CMOS process and operates from a nominal 1.8 V supply that is scalable down to 900 mV. The system consumes 50 mW at a nominal operating frequency of 62.5 MHz.

1. Introduction

The reduced size, added sensitivity, and ability to provide redundant or comparative analyses makes miniaturized chemical transducers very attractive for monitoring in extraterrestrial environments and remote earth locations. It has been shown that a wide range of scientifically interesting analytes can be detected *in-situ* using voltammetric sensor systems [1]. These systems combine microsensors with large-scale printed circuit board instrumentation. While continued scaling of sensor dimensions provides improved detection limits, scaling of the instrumentation's size and power consumption are required to extend the lifetimes and reduce the overall dimensions of these systems.

Chemical microinstrumentation serves as the interface between the transducer and the user. It measures the sensor signal, processes the data, and either locally stores or transmits this data to a centralized source. [2] presented a 3.0 V, monolithically integrated microcontroller capable of instrumenting chemical transducers. Microsystem accuracy and lifetime, however, could be increased by improving its resolution and reducing its power dissipation. This paper highlights work toward increasing the instrumentation's resolution while reducing the area and power consumption of the system.

The proposed microinstrument (Fig. 1) consists of an analog-front-end (AFE), a digital core including on-chip memory, and an on-chip CMOS-MEMS clock reference. The AFE includes a sensor interface circuit (a potentiostat), a programmable gain amplifier (PGA), and a ΣΔ analog-to-digital converter (ΣΔ-ADC). The processor consists of a 16-bit, 3-stage pipelined core with 64 KB of on-chip RAM, a memory management unit, and a host of peripheral components. The timebase is generated using a combined CMOS-MEMS *LC*-tank oscillator. The tank capacitor is a MEMS-based, electrostatically controlled varactor, and the inductor is a suspended spiral inductor. The microinstrument was designed in *TSMC's* 0.18 µm process. It operates from a 1.8 V supply but is scalable down to 900 mV with only slight modifications to the sensor interface.

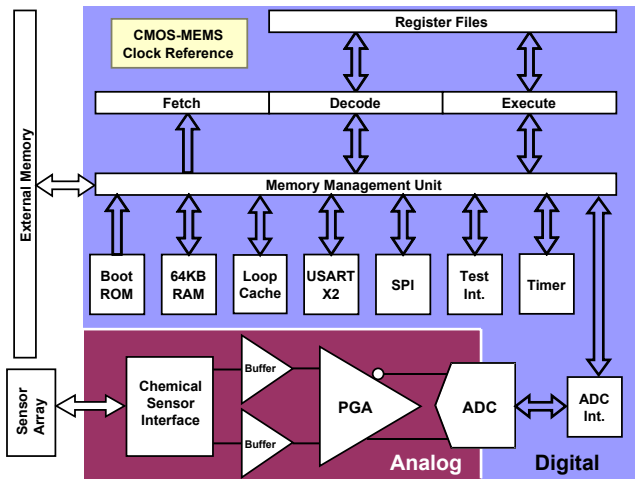

Fig. 1. Microinstrument system architecture.

2. Analog-Front-End

Power consumption in the proposed microcontroller is dominated by the digital components and in particular, by the on-chip memory as shown in Fig. 2. Since power dissipation in digital circuits is proportional to the power supply squared, V_{dd}^2, dramatic power savings can be realized by lowering V_{dd}. To minimize the cost of the integrated system, all of the analog components should also operate from the same reduced supply voltage. Several design techniques were employed to combat the problems associated with operating analog components from a 900 mV supply. The most important design choice was to use a fully-differential (FD) architecture for the entire AFE. The FD architecture increases dynamic range and increases both common-mode and power supply rejection. Since dynamic range (DR) is proportional to power consumption [3], the improved DR of the fully-differential architecture allows the circuit to maintain a constant DR while the power dissipation is reduced. Additional low-power analog techniques such as weak inversion biasing, wide-swing current mirrors, and rail-to-rail inputs and outputs were employed throughout.

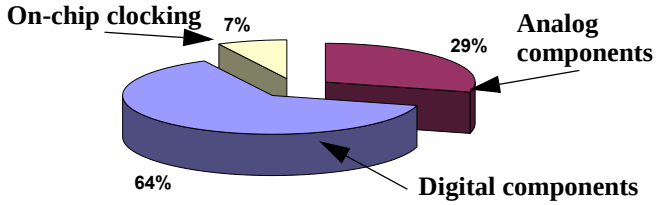

Fig. 2. Percentage power consumption for the components of the proposed microcontroller.

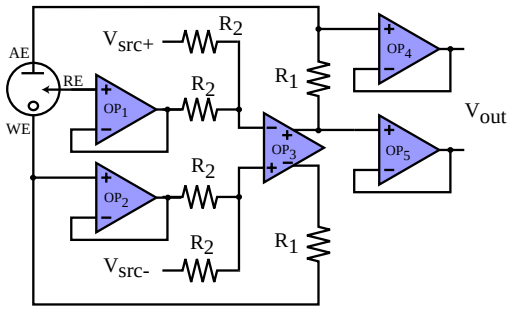

Fig. 3. Fully-differential potentiosat. This potentiosat doubles the output swing of standard potentiostats allowing the supply voltage of the instrumentation to be scaled.

2.1 Potentiostat

Due to the nature of electrochemical voltammetric sensors, scaling of power supply voltages is difficult because the potentials required at the auxiliary (AE) and working electrodes (WE) are defined electrochemically and do not scale. For low-voltage operation, a fully-differential potentiostat (Fig. 3), was designed to interface to the voltammetric sensors. The FD potentiostat enables sensor operation from a 900 mV supply and is well suited for low-voltage operation because it allows the potentials of both the AE and WE to be controlled, doubling the output swing; a standard single-ended (SE) potentiostat only allows the AE to be controlled [4]. Fig. 4 shows the available output swing for both the FD and SE potentiostats.

Table I compares the expected performance of the proposed FD potentiostat and the SE potentiostat designed by our group in [2]. Reducing power dissipation of this circuit is difficult because the potentiostat drives a sensor with a large equivalent capacitance and must maintain closed-loop stability.

2.2 PGA

The purpose of the programmable gain amplifier is to amplify the input signal to the full scale voltage of the ADC ensuring that the maximum signal resolution is achieved. The fully-differential PGA (Fig. 5) uses a capacitive feedback network and switches in capacitors of differing values to produce the variable gains. The capacitive feedback offers distinct advantages over traditional resistive feedback networks. Switched capacitors, which can have large equivalent resistances, provide high gains at lower power since the operational amplifier is not resistively loaded; for comparable performance, an op-amp with capacitive-only loading can be biased with lower currents than a resistively loaded op-amp. Additionally, on-chip capacitors have better matching characteristics than on-chip resistors. This increased matching provides reliable gains across process corners and increases common-mode signal rejection. The differential

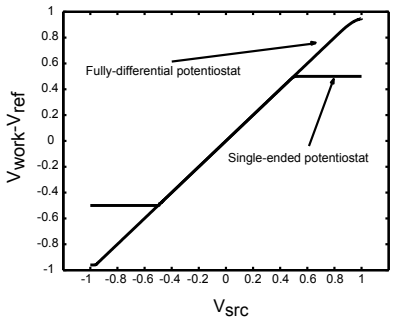

Fig. 4. Normalized output swing delivered to the electrochemical cell by both a FD and a SE potentiostat.

Table I. Comparison of the SE and FD potentiostats.

Parameter	SE Pot	FD Pot
Power Supply	±1.5 V	±0.9 V
I_{supply}	2.2 mA	8.8 mA
Output Swing	±1.5 V	±1.7 V
Max load capacitance	0.2 nF	1.0 nF

architecture of the PGA also reduces the effects of charge injection from the switches, and increases signal swing.

To realize this increased signal range, the op-amp within the PGA must swing from rail to rail. In addition to this requirement, the op-amp was designed for high slew rate and power efficiency. To meet these requirements, the op-amp employed class AB input and output stages. The expected open-loop performance of the PGA is summarized in Table II.

2.3 ΣΔ-ADC

A ΣΔ-ADC was chosen for this design due to its superior resolution and possible low-power implementations. The ΣΔ-ADC trades much of the power-consuming analog sophistication required in Nyquist-rate ADCs for digital complexity [5]. These digital components are well suited for power scaling. A second-order ΣΔ modulator was chosen to meet the desired resolution and bandwidth of the microsystem. The second-order, ΣΔ topology utilizes feedback to provide noise shaping, pushing the signal's quantization noise produced by the 1-bit ADC to out-of-band frequencies. This noise shaping yields higher resolution data conversion at lower power.

In most high resolution data converters, a true, fully-differential architecture is used. In this design, however, a pseudo differential (PD) architecture is implemented. This allows the use of highly efficient integrators and common-mode feedback [6]. The PD architecture maintains the increased signal swing of standard FD architectures. Table III summarizes the performance characteristics of the ADC. Fig. 6 shows the combined simulated results for the PGA and the ΣΔ-ADC.

3. Digital Components

As described previously, large savings in power consumption can be achieved by simply scaling the operating voltage for digital circuits. The proposed microinstrument scales the power supply of [2] from 3.0 V to 1.8 V with 900 mV operation possible. The architecture was also completely reworked with a focus on minimizing the power consumption of the digital components. Memory accesses are responsible for a majority of the power dissipated in the digital components. Consequently, particular attention was given to reducing the number of accesses to memory.

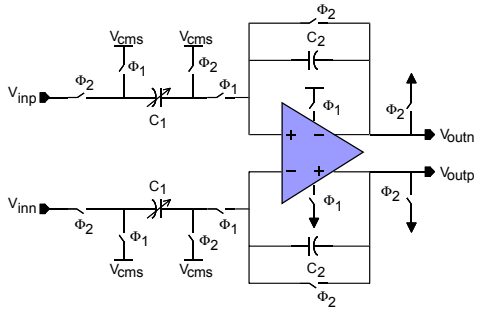

Fig. 5. Programmable gain amplifier. The capacitive feedback consumes less power than standard resistive feedback.

Table II. Expected performance for PGA amplifier.

Parameter	Value
Unity Gain Bandwidth	2 MHz
Open Loop Gain	93 dB
Output Swing	1.7 V
Power	40 µW

Table III. Expected performance for ΣΔ-ADC.

Parameter	Value
Effective Number of Bits	14 Bits
Voltage Full Scale	1.64 V_{pp}
Peak SNDR	86 dB
Average Power	2 µW

3.1 Microcontroller core

A 16-bit load/store architecture with dual-operand, register-to-register instructions was chosen to satisfy the power and performance requirements of the microinstrument. The 16-bit datapath reduces the complexity and power consumption of the core while providing adequate precision in sensor measurements and data calculations. In [2], an 8-bit datapath was implemented. This, however, proved power inefficient for manipulating sensor data with more than 8 bits of resolution. To reduce power consumption, a 16-bit, 3-stage pipeline architecture was chosen that can achieve equivalent throughput at lower clock frequencies. Adding more pipeline stages would improve performance at the cost of increased complexity and power [7]. For most sensor applications, low power consumption is more important than high throughput.

The controller's 16 general-purpose data registers and 4 address registers are evenly split into 2 access windows. The windowing scheme permits 16-bit instruction encoding by reducing the number of bits required to encode register operands. Without register windowing, a larger instruction word would be required, resulting in increased memory accesses and power dissipation. A low-power standby mode was also implemented. This mode will be critical for extending the lifetime of environmental sensor systems that are likely to remain idle between sporadic sensor measurements.

3.2 Memory architecture

A 24-bit address space of unified data and instruction memory satisfies the potentially large storage requirements of remote sensor systems. The core has 64 KB of on-chip SRAM and a memory bus interface to allow utilization of the 16 MB of possible memory space. The on-chip SRAM is divided into eight separate 8 KB blocks which can be independently powered on or off with no latency. This memory structure consumes less power than a single 64 KB block, but occupies more area, as shown by RAM structuring simulations (Fig. 7). This increased area is due to the duplicated sense amplifiers and address decoders for each memory block.

Further power savings were achieved by adding a 512-byte loop cache to reduce the power consumption of the commonly executed instructions [8]. An access to the loop cache uses 49.5% less power than an access to one of the 8 KB memory banks. The contents of the loop cache are determined through compiler profiling, and power savings are therefore, application dependent.

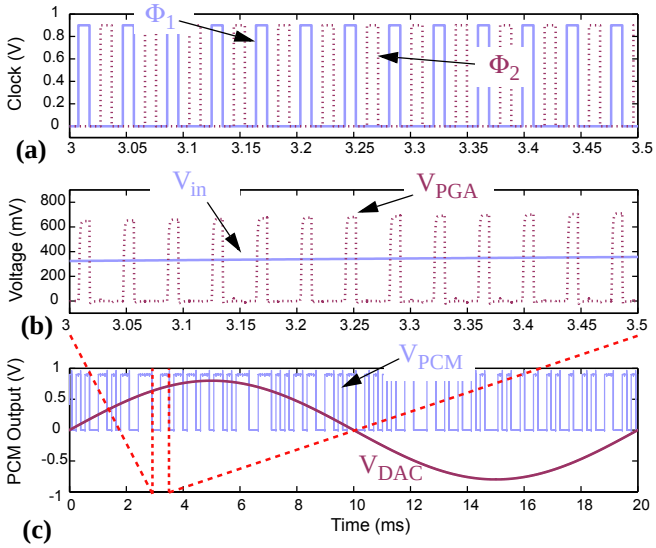

Fig. 6. Simulated SPICE results of the PGA and ΣΔ-ADC. (a) Two-phase clocking scheme where Φ_1 is the gain phase and Φ_2 is the reset phase. (b) Section of the 50 Hz sinusoidal input signal, V_{in}, and the output of the PGA, V_{PGA}, with a gain setting of 2. (c) Pulse code modulated (PCM) output, V_{PCM}, of the ΣΔ-ADC and this PCM output reconverted into an analog signal, V_{DAC}.

3.3 Interfaces

The variety of digital interfaces shown in Fig. 1 were provided to facilitate integration of this microinstrument with external components. The USARTs are supported by many commercial chips, including RF transceivers for wireless data transmission. The Serial Peripheral Interface (SPI) is ideal for communicating with multiple sensors that share a single sensor bus [9]. A test interface allows for remote verification of the system's operation.

4. CMOS-MEMS monolithic clock generation

Clock generation for synchronous processors is often overlooked in the design effort since the clock signal is often considered to be arbitrarily available. Significant performance gains and reduced power consumption, however, can be realized by including clock generation on-chip. The state-of-the-art for clock generation includes a quartz crystal reference and supporting electronics. These supporting electronics may be included within a discrete package along with the crystal, or they may be integrated into the circuit, in which case the crystal is the only off-chip component. In both the discrete and hybrid case, the sup-

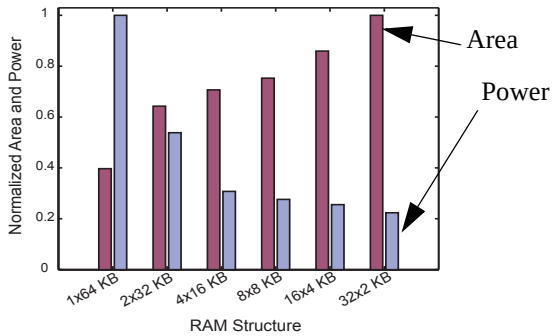

Fig. 7. Trade-off between area and power consumption when dividing the 64 KB RAM into separate memory blocks.

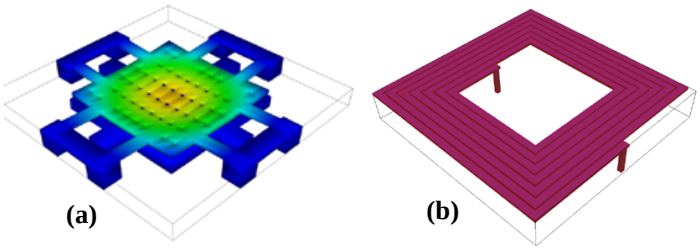

Fig. 8. MEMS-LC components. (a) Finite element analysis of the varactor actuation. (b) Perspective of suspended inductor

porting electronics include the circuitry required to sustain oscillations and often a phase-locked loop (PLL) for frequency multiplication. An alternative option for clock generation is to include a precision monolithic reference that requires no external components and thus is smaller and consumes less power. Such a reference has been developed here.

4.1 Architecture

The monolithic clock generator utilizes a high quality factor MEMS-based coupled inductor (*L*) and varactor (*C*), in an *LC*-tank circuit. MEMS devices have a higher quality factor than alternate integrated technologies and thus achieve better frequency stability. Moreover, the varactor affords tuning of the clock frequency. The inductor is suspended in air above the substrate in order to minimize loss due to induced eddy currents from magnetic coupling into the substrate. The varactor is a mechanically deflectable parallel plate device that is actuated with a DC tuning voltage. These devices are illustrated in Fig. 8.

A low noise oscillator circuit sustains the generated clock. It has been developed with a focus on jitter minimization, as presented in [10]. A series of flip-flops are then used to divide the clock to the desired frequency. This top-down approach to clock synthesis is significantly simpler than PLL-based systems, requires less area, consumes less power, and reduces the relative jitter from the reference. In PLL-based systems, the jitter is accumulated due to multiplication of the reference frequency.

4.2 Process Technology

The monolithic clock generator has been developed in a commercial CMOS process and the inductor and varactor have been constructed using the standard interconnect layers. A maskless post-process releases the devices. Therefore, the clock generation function can be easily incorporated onto the substrate of the system that it supports.

4.3 Results

Power, area, and clock jitter were considered when comparing the monolithic clock generator to state-of-the-art alternate clock references. The monolithic MEMS clock generator consumes 4 mW and occupies an area of 0.09 mm^2, while synthesizing frequencies from 31 MHz to 1 GHz. The frequency stability was analyzed, and results were acquired using *Agilent's ADS* time domain noise analysis. The period jitter was 2.1 ppm for a 62.5 MHz clock. These results are presented in Table IV, along with a comparison to the alternative methods discussed above for clock generation assuming that a 1 MHz crystal reference is utilized. Substantial gains are realized using the monolithic clock.

5. Conclusion

A low-power microcontroller is presented to meet the goals of instrumenting microtransducers in remote environments such as the human body and outer space. The microinstrument includes a low-voltage, fully-differential analog-front-end including a potentiostat, programmable gain amplifier, and over-

Table IV. Comparison of performance metrics for two types of clock generation and the developed monolithic generator.

Parameter	Discrete[a]	Hybrid[b]	Monolithic
Power Dissipation	225 mW	> 30 mW	4 mW
Area	35 mm^2	8 mm^2	0.09 mm^2
Jitter (62.5MHz)	±50 ppm	±50 ppm	±2.1 ppm

[a] *Epson SG-8002JF*
[b] *Epson FA-238* + PLL (estimated)

sampled ΣΔ analog-to-digital converter. The 16-bit digital core includes a loop cache to lower the power consumption of the processor and partitions the on-chip RAM to minimize the area and power of the memories. The processor core also includes a versatile set of peripherals that make it well-suited for long-term, reliable experimentation. The system's timebase is generated on-chip using a low-power, combined CMOS-MEMS reference circuit. The MEMS components are defined during normal processing and require only a single, maskless release step after normal processing. Based on simulation results, the microsystem is expected to dissipate only 50 mW from a 1.8 V supply at an operating frequency of 62.5 MHz. Fabrication of the proposed device has just been completed and experimental verification is currently underway.

6. Acknowledgements

This work was supported in part by the Engineering Research Centers Program of the US National Science Foundation under Award Number EEC-9986866 and under a National Science Foundation Graduate Research Fellowship. The authors thank the MOSIS service for fabrication of the proposed microsystem.

7. References

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