A DSP Architecture for Cochlear Implants

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Abstract—**This paper describes a low-power DSP architecture for use in cochlear implants. The microsystem, fabricated in *TSMC* 0.18μm CMOS, consumes 1.79mW from a 1.2V supply and occupies an area of 9.18mm^2 while providing the necessary programmability for high speech comprehension by patients. Standby power consumption is 330μW.**

I. Introduction

The primary design considerations for battery powered bio-medical implant systems are safety, reliability, area, and power consumption. The work discussed here focuses on reducing the area and power consumption of cochlear implants (CIs) by integrating the signal processing capability required into an SoC. Increased integration of components into a single SoC will enable fully-implantable CIs in the near future; something that is not possible with traditional CI approaches.

The microsystem described here combines an energy-efficient microcontroller unit (MCU), a low-power DSP core, and a monolithic self-referenced hybrid temperature-compensated LC oscillator (TC-LCO) and ring oscillator clock reference into a single bulk CMOS SoC. This work is being developed as part of the Wireless Integrated MicroSystems (WIMS) Engineering Research Center (ERC) [1].

The next section gives a brief description of CIs, followed by the architecture of the microsystem, testing results, and comparisons to other CI approaches.

II. Cochlear Implants

CIs are medical devices implanted in patients who have a degeneration or absence of sensory hair cells in the inner ear. In a properly functioning ear, frequency selective hair cells in the cochlea generate electrical signals that are detected by neurons and transmitted via the auditory nerve to the brain for processing. The purpose of a CI is to bypass non-functional hair cells by directly stimulating the cochlea with current pulses. To date, over 90,000 people worldwide have received cochlear implants [2].

The major components of a CI include a microphone, signal processor, implant electrodes, and batteries. The microphone, fitted into or placed behind the patient's ear, captures the acoustic signal and converts it to an electrical signal. Using this information, the signal processor calculates the type and level of stimulation to deliver through the electrodes, which are surgically inserted into the cochlea. Large variations in signal processing algorithms exist due to diverse implementation methods and differing parameters among patients.

Typical commercial CIs use an off-the-shelf, software-programmable DSP to perform the signal processing. In this paper we report the development of a fully integrated, low-power, DSP core to perform the Continuous Interleaved Sampling (CIS) algorithm. CIS is by far the most popular processing algorithm among patients and manufacturers. Research studies have demonstrated that it provides the highest speech comprehension rates among patients [3]. As shown in Fig. 1, a high-pass filter (HPF) attenuates vowel sounds before the band-pass filters (BPFs) split the signal into n channels (n=16 for this design). Following envelope detection by the low-pass filter (LPF) and rectifier, nonlinear dynamic range compression maps the electrical representation of acoustic signals to a representation of current levels. Lastly, non-overlapping bi-phasic pulses are generated and delivered through the stimulation electrodes as current pulses to the cochlea.

Certain parameters of the signal processing algorithm must be variable in order to provide optimal hearing for the patient [4]. The most important of these are the filter cutoff frequencies, compression function, number of channels,

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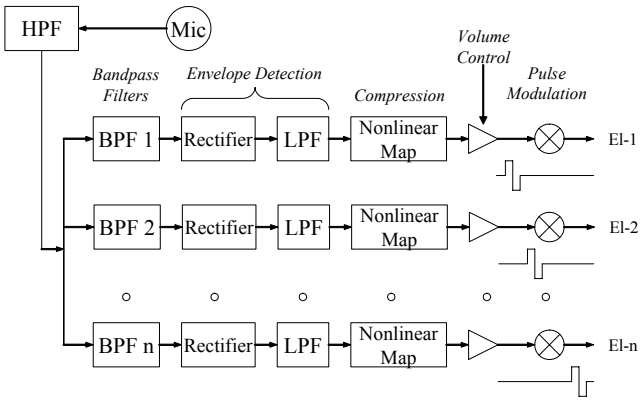

Figure 1. CIS signal processing algorithm

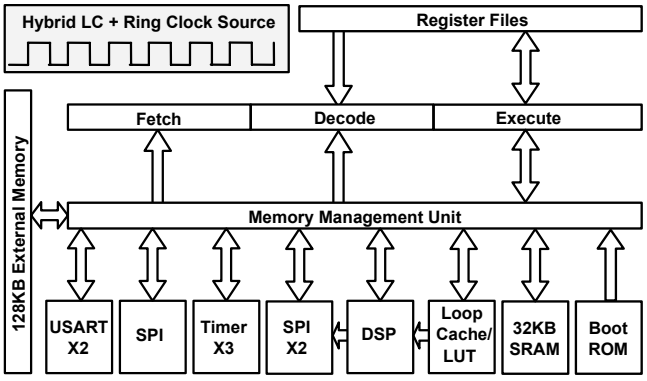

Figure 2. Microsystem architecture

channel to electrode assignment, pulse duration, and pulse rate. Our CI microsystem allows individual patients to be custom fitted by programming each of these parameters via the MCU.

Reference [5] is the lowest reported power consumption for an analog signal processor for CIs. This 16-channel CIS processor consumes 251µW from 2.8V and occupies 88.9mm^2 in an AMI 1.5µm BiCMOS process. This is 7.1 times less power, but nearly an order of magnitude more area than the presented microsystem. While this is an impressive power consumption achievement, the analog system sacrifices programmability and flexibility, especially when it comes to stimulation profiles and dynamic range compression. These two signal processing factors are very important in determining patient speech comprehension.

For software programmable DSPs, 35 million operations per second is an aggressive estimate of the processing capability required to perform a 16-channel CIS implementation that includes the signal processing and communication with the ADC and electrode array. This typically requires 45mW to 90mW of power, depending on the algorithm implementation and processor selection [6][7]. Software programmable DSP approaches consume too much power and area to be part of a fully-implanted CI system.

III. DSP Microsystem Architecture

Fig. 2 shows the complete microsystem architecture consisting of the MCU, DSP, and hybrid clock source. An overview of a prior version of the MCU core has been given in [8]. Improvements upon the previous MCU for this work include a more efficient ISA to relieve compiler bottlenecks, additional communication interfaces, and decreased power consumption. The 16-bit MCU contains a 3-stage pipeline, 32kB of on-chip memory, a loop cache, and several peripheral communication interfaces. This makes the microsystem well suited for other bio-medical or environmental monitoring applications.

The DSP and MCU share control over two SPI interfaces and the loop cache/look-up-table (LUT). The SPI interfaces are intended to communicate with an external ADC and the implanted electrodes. Control registers in the DSP, written by the MCU software, are read by the MCU memory management unit to give control of the read and write data buses for these components to either the DSP or MCU. These control bits also determine the clock domain in which the peripheral ports and the loop cache operate. The microsystem software can select different operating frequencies for the MCU and DSP separately to provide maximum operating point flexibility [9].

The self-referenced hybrid clock source consists of a highly-accurate TC-LCO and an independent tunable ring oscillator. No external crystal or PLL is required. The synthesizer supports a reduced-power standby mode in which the TC-LCO is powered down while the system operates from the low power, low frequency ring oscillator. The entire clock synthesizer occupies 0.25mm^2 of silicon area.

Fig. 3 is a block diagram of the fully-synthesizable signed-magnitude fixed-point DSP core. The HPF, BPFs, and LPFs are implemented as cascaded infinite impulse response (IIR) stages due to the low memory requirements and simplicity of the hardware. They are 1st, 6th, and 4th order, respectively. All filter coefficients are programmable by the MCU to provide the required flexibility for patient fitting procedures. All filters obtain a vast reduction in area, due to the multiply-intensive nature of filters, by sharing the same cascade stage hardware. Storage for the filter coefficients and output data from each datapath stage is a significant requirement on the architecture. Clock gating is performed on these registers to reduce the power consumed by the clock tree.

Compressing the dynamic range, and therefore the number of bits required to encode the signal amplitude, saves power and area by reducing the datapath width from sixteen to eight bits for all downstream calculations and storage.

This logarithmic compression is done using the low-power loop cache to store the LUT data. By allowing the MCU software to control the data in the 512-entry LUT, the patient can have the compression function individually optimized.

Pulse rate, channel to electrode assignment, and pulse duration are all programmable in the modulator via the MCU interface. The current implementation allows for any bi-phasic pulse stimulation information to be sent to the electrodes through one of the system's SPI interfaces. The maximum pulse rate is 3000 pulses per second per channel. In addition, if more complex stimulation profiles are desired, the MCU can read the data coming out of the DSP volume stage and perform computations to calculate the appropriate pulse characteristics. It can then take control of the SPI interface and send information to the implanted electrodes, bypassing the DSP modulator finite state machine (FSM). This makes the microsystem a useful tool for investigating experimental stimulation profiles.

The parallel nature of the CIS algorithm provides for a significant reduction in hardware by pipelining the datapath and allowing all channels to share the same hardware for filters, LUT, volume control, and pulse modulation. Control circuitry is also simplified by allowing the FSMs in the control unit to reuse states for each channel.

The DSP core has four operating modes: stimulation, programming, test, and sleep. For typical operation, the DSP will be in stimulation mode and will process samples and generate stimulation pulses automatically. The MCU can be in standby mode during this time. Input data is received from the external ADC through one of the shared SPI interfaces. Programming mode will allow the MCU to set up all filter coefficients, LUT data, and the stimulation profile. Test mode allows for any of the datapath stages to be bypassed via the multiplexors at each output node to provide observability and controllability over each component in the DSP. Sleep mode allows all DSP components to be shut down in order to conserve power. While in stimulation mode, any unused datapath stages are shut down through the control unit by utilizing the existing sleep mode circuitry.

Assuming a 24kHz front-end ADC, which is standard for speech processing within the human audible range of 0 to 10kHz, the DSP must operate at 3MHz to provide adequate output data for high pulse rate stimulation. This calculation is based on the DSP processing time of a single sample and the data transmission rate to the electrodes.

IV. Measured Results

Fig. 4 shows the fabricated microsystem in *TSMC* 0.18µm mixed-mode bulk CMOS containing 2.3 million transistors and occupying 9.18mm^2. Table 1 shows the measured data, averaged across ten devices, taken on an HP82000 D200/D400 digital tester. 1.79mW is the lowest reported active power consumption for a CI specific DSP.

Fig. 5 shows the capability of the DSP to scale frequency as well as supply voltage. Operating with fewer than sixteen active channels will allow the DSP to reduce its operating frequency and power consumption. When improving electrode technology allows more electrodes to be inserted into

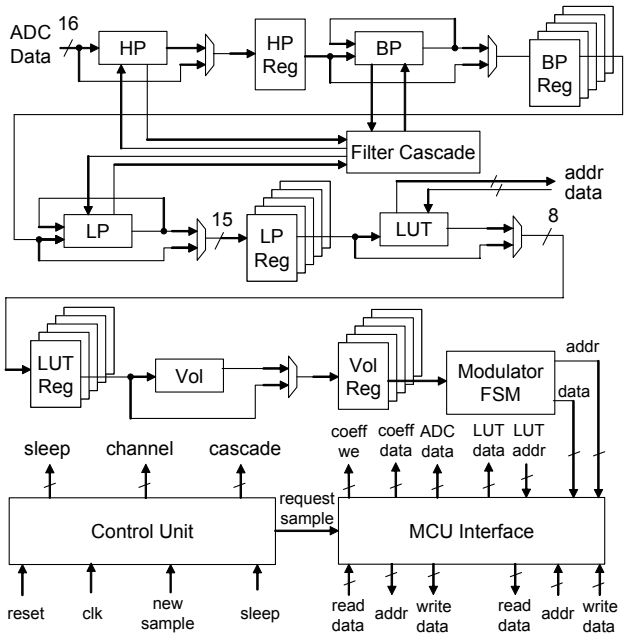

Figure 3. CIS DSP architecture block diagram

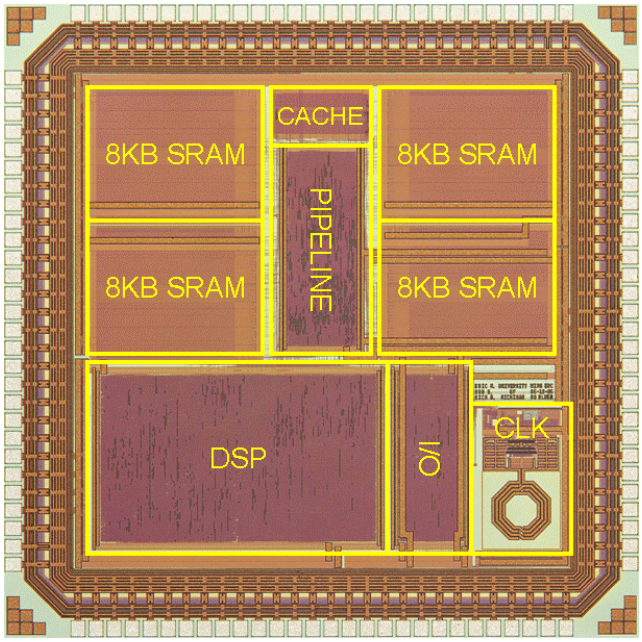

Figure 4. Die micrograph of fabricated microsystem

TABLE 1. MEASURED POWER CONSUMPTION DATA.

Simulation Conditions	VDD = 1.8V		VDD = 1.2V	
	DSP Mode[a]	*Standby*	*DSP Mode*[a]	*Standby*
Core (μW)	1630	170	440	60
Mem (μW)	120	120	30	30
DSP (μW)	2460	270	1140	60
CLK (μW)	760	760	180	180
Total (μW)	4970	1320	1790	330

a.The DSP operating frequency is 3MHz.

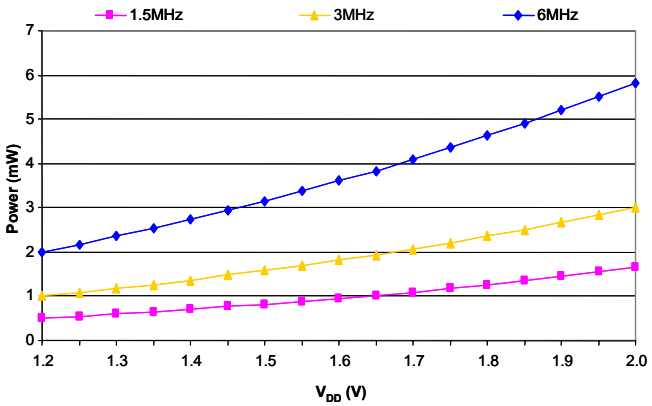

Figure 5. Measured power versus V_{DD} scaling at different frequencies

the cochlea, requiring more signal processing from the system, increasing the number of channels in this DSP architecture to more than 16 channels requires only the addition of more register storage for the additional filter coefficients and data outputs. No additional control or computational hardware would be required due to the pipelined nature of the architecture. Because this architecture is fully-synthesizable, migration to a more advanced bulk CMOS or SOI process will require minimal work while achieving large reductions in power and area.

V. CONCLUSION

This paper describes an expandable, programmable, fully-synthesizeable, low-power, low-area DSP architecture that performs the CIS algorithm. This microsystem achieves the lowest reported digital CI power consumption of 1.79mW in active mode and 330μW in sleep mode; it occupies 9.18mm^2 of Si area. Future improvements to the register storage will reduce area and power consumption. The amount of on-chip memory can also be reduced to decrease the area in a CI-only application implementation.

Future expansion to more than sixteen channels will increase the power and area of analog signal processing systems on a linear scale, while the digital WIMS CI system architecture achieves a superior scaling factor. Migration to a more advanced process will improve the performance of the digital system, but analog systems will not obtain the same benefits [10].

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