

HIGH-Q INTEGRATED INDUCTORS ON TRENCHED SILICON ISLANDS

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HIGH-Q INTEGRATED INDUCTORS ON TRENCHED SILICON ISLANDS

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SUMMARY

This thesis reports on a new implementation of high quality factor (Q) copper (Cu) inductors on CMOS-grade (10-20 Ω .cm) silicon (Si) substrates using a fully CMOS-compatible process. A low-temperature (<300°C) fabrication sequence is employed to reduce the loss of Si wafers at RF frequencies by trenching the Si substrate. The high aspect-ratio (30:1) trenches are subsequently bridged over or refilled with a low-loss material to close the open areas and to create a rigid low-loss island (Trenched Si Island) on which the inductors can be fabricated. The method reported here does not require air suspension of the inductors, resulting in mechanically-robust structures that are compatible with any packaging technology. The metal loss of inductors is reduced by electroplating thick (~20 μ m) Cu layer.

Fabricated inductors are characterized and modeled from S-parameter measurement. Measurement results are in good agreement with SONNET electromagnetic simulations. A one-turn 0.8nH Cu inductor fabricated on a Trenched Silicon Island (*TSI*) exhibits high Q of 71 at 8.75 GHz. Whereas, the identical inductor fabricated on a 20 μ m thick silicon dioxide (SiO₂) coated standard Si substrate has a maximum Q of 41 at 1.95GHz. Comparing the Q of inductors on *TSI* with that of other micromachined Si substrates reveals the significant effect of trenching the Si in reduction of the substrate loss. This thesis outlines the design, fabrication, characterization and modeling of spiral type Cu inductors on the *TSI*'s.

CHAPTER I

INTRODUCTION AND MOTIVATION

With the rapid growth of the wireless communication market, silicon technology has matured to meet the demand for low-cost, high performance, and high level of integration. High- Q integrated inductors can improve the performance and integration-level of radio frequency (RF) integrated circuits (IC) while reducing their power consumption and cost. Inductors are vastly used in voltage controlled oscillators (VCO), low noise amplifiers (LNA), power amplifiers (PA), mixers, filters and matching networks. However, on-chip inductors in commercially available CMOS processes exhibit poor Q 's (<15) due to the high-frequency loss of standard Si substrate and ohmic loss of thin metal layers [1]. While metal loss can be reduced by using thick high-conductivity metals, the loss of Si substrate has remained the major barrier in reaching Q 's comparable to that of off-chip inductors.

Common techniques employed to reduce the metal loss in inductors include the use of high conductivity metal layers [2], in particular, electroplating thick Cu layer [3, 4]; utilizing multi-level metal interconnects to increase the effective thickness of inductor, and series connection of multi-layer inductors in vertical direction to reduce area [5-10]. A 2.88-nH inductor is described in [2] that has a measured Q of 12.1 at 3.3 GHz in Si bipolar process using thick gold metal and high resistivity silicon wafer (150~200 Ω .cm). In [5-10], the approach is to increase the effective thickness of the spiral inductor and simultaneously reduce the inductor area by shunting spiral inductors in adjacent levels.

The highest reported Q 's using this technique are 9.3 at 4GHz for a 1.95nH inductor with a self-resonance frequency of 20GHz [5] and 13.1 at 5.65GHz with inductance of about 5nH [8]. The major draw back of using multi-layer metal is simultaneous increase of the parasitic capacitance introduced between the layers. Nonetheless, the most effective way of reducing the metal loss is through electroplating a thick layer of high conductivity metal (e.g., Cu).

Micromachining techniques have been utilized to reduce the substrate loss and increase the Q . Previously reported techniques include the use of thick isolating oxide layer [11, 12], use of porous silicon to increase the substrate resistance [13, 14], suspension of the inductors [15-17], use of 3-D structures such as toroids and self assembled solenoids [18-20], and use of thick low-K dielectrics [21, 22]. Approaches taken to reduce the substrate loss can be divided in to two major categories: Reducing the loss of Si itself (e.g., oxidizing the Si), or suppressing the effect of lossy Si substrate on the inductor. In [21, 22], the substrate loss is suppressed by using a thick BCB layer. The use of thin low-K dielectric materials alone is not sufficient to effectively reduce the substrate loss. Using suspended inductors, the highest reported Q is 70 at 6GHz for an inductance value of 1.38nH [16]. However, suspension may cause susceptibility to shock and vibrations and can complicate die packaging. Quality factor of 3-D and suspended inductors also drops because of the encapsulating material used for packaging [23].

No work has been done to reduce the loss of Si substrate through a low-temperature CMOS-compatible process. Silicon gets oxidized at more than 1000°C and the process of making porous Si is not CMOS compatible.

In [24], the Si loss is reduced by making deep high-aspect ratio trenches into the Si and subsequently oxidizing the Si left in-between the trenches at 1100°C. Although this technique has a significant effect on the reduction of Si loss, the high processing-temperature makes it unsuitable for post-CMOS processing. On the other hand, oxidizing the remained Si is neither necessary to reduce the substrate loss nor it is required to seal the open areas. In fact, trenches can be bridged over by depositing a thin layer of SiO₂ at 300°C. Making trenches in the substrate reduces the substrate loss through disrupting the path of current flowing in the bulk of Si at high frequencies.

In this thesis, we have investigated the effect of trenching the Si on the inductor's quality factor. The height and width of the trenches as well as the area of the Trenched Si Islands are characterized by fabricating several spiral type inductors on *TSI*. Metal loss in the inductors is reduced by electroplating thick (~20µm) Cu layer. Quality factor of the inductors on *TSI* is compared to the Q 's of identical inductors on other types of micromachined substrates including Oxide Islands. A 0.8nH Cu inductor fabricated on *TSI* exhibits high Q of 71 at 8.75 GHz [26], while the maximum Q of the same inductor on 20µm thick SiO₂ is only 41 at 1.95GHz. Comparison of Q 's shows the remarkable effect of trenching the Si on improving the performance of the inductors at RF frequencies.

This thesis is organized into five chapters. Chapter 1 provides literature review, introducing a new technique to reduce the substrate loss as the motivation behind this work. Chapter 2 reviews the physical model of planar spiral inductors on Si substrate. This chapter discusses their design and optimization, outlining the technique of reducing the Si loss by making trenches in the substrate. Chapter 3 describes the high- Q Cu inductors on Trenched Si Islands fabrication process. Chapter 4 presents the measured and characterization results of the high- Q inductors, and provides discussion of these results. Finally, chapter 5 concludes the thesis and provides suggestions on future research direction.

CHAPTER II

DESIGN AND SIMULATION

2.1. Inductor Physical Model

Figure 2-1 shows the layout of a planar micromachined spiral inductor [26]. The first metal layer, the routing layer, is sandwiched between two insulating layers. In this work, silicon dioxide is used as the insulation layer. In order to efficiently identify the optimal inductor layout and account for its parasitic in circuit simulations, an accurate equivalent model is required. A few equivalent electrical models for spiral inductors are available that describe the inductor behavior in a wide range of frequencies [27-34]. The simplest model is shown in Fig. 2-2, where L_s represents the inductance of the spiral and is computed using either of the equations discussed in section 2.2.2.

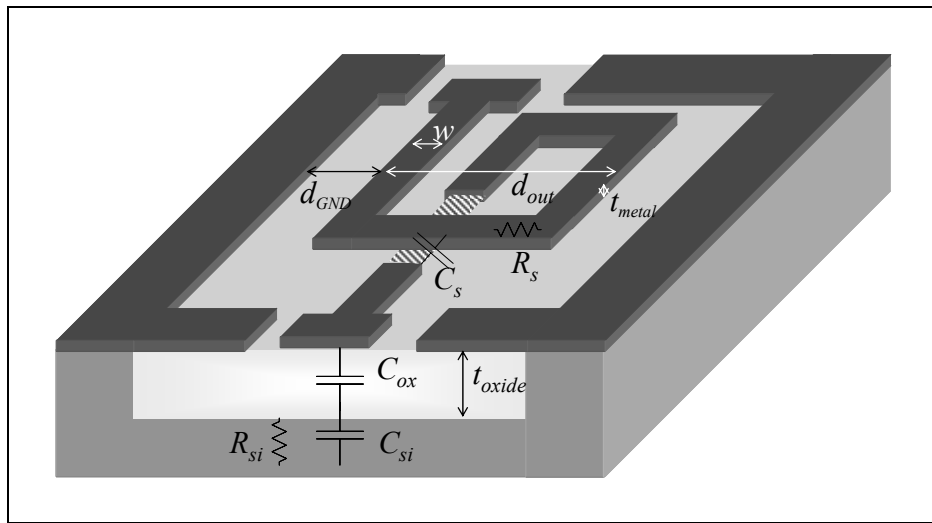


Figure 2-1. Layout of a micromachined planar spiral inductor.

The resistance of the two metal layers is expressed by R_s . An approximate formula for R_s is shown in Fig. 2-2, taking into account the skin depth of the conductor with finite thickness and current distribution in an isolated strip conductor [35]. The overlap between the metal layers allows direct capacitive coupling between the two terminals of the inductor. This feed-through path is modeled by the series capacitance; C_s . C_{ox} models the silicon dioxide capacitance between the spiral turns and the silicon substrate. C_{si} and R_{si} model the capacitance and resistance of the Si substrate, respectively [28]. C_{sub} and G_{sub} are properties of the Si substrate and are extracted from measured data.

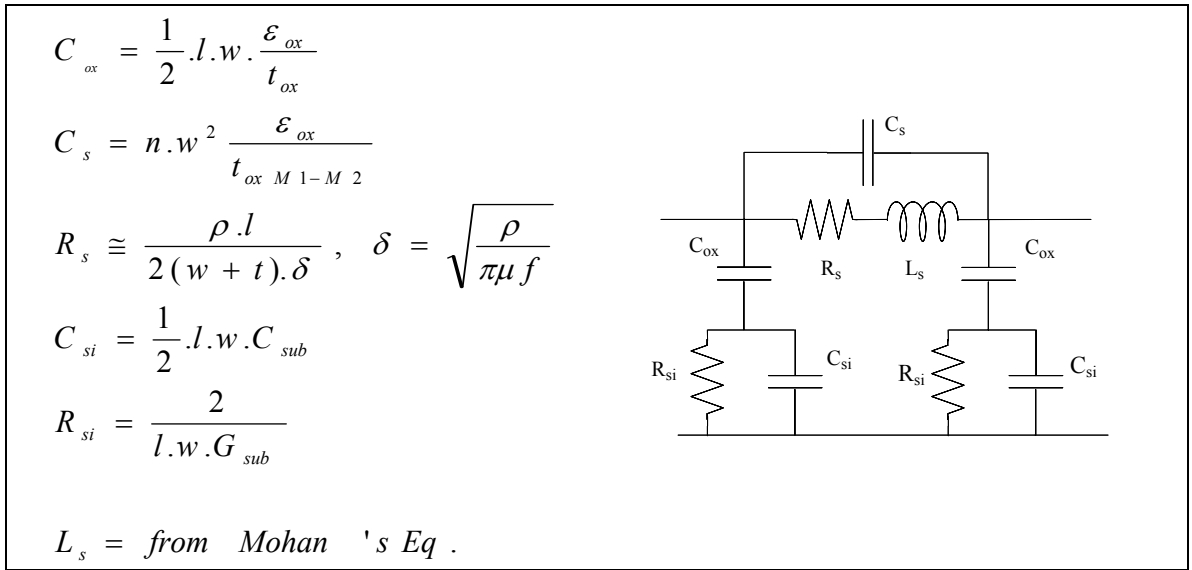


Figure 2-2. The electrical model of an on-chip spiral inductor (l =overall length of the inductor, w =line width, t_{ox} = SiO_2 thickness between 2^{nd} metal layer and substrate, ϵ_{ox} = SiO_2 permittivity, n = number of crossover between the two metal layers, $t_{ox M1-M2}$ = SiO_2 thickness between the metal layers, δ =metal skin depth, t =metal thickness, ρ =metal resistivity, μ =metal permeability, C_{sub} =substrate capacitance per unit area, G_{sub} =substrate conductance per unit area, f =operation frequency).

A more accurate model also includes the effect of the electromagnetic coupling between the substrate and the metal turns [29].

2.2 Inductor Model Parameter Extraction

2.2.1 Series Resistance

The current density in a conductor strip is uniform at dc. However, as frequency increases, the current density becomes non-uniform due to the formation of eddy currents. The eddy current effect occurs when a conductor is subjected to time-varying magnetic fields and is governed by Faraday's law [36, 37]. Eddy current manifest itself as skin and proximity effects. According to the Lenz's law, eddy currents produce their own magnetic fields to oppose the original field. In the case of the skin effect, the time-varying magnetic field due to the current flow in a conductor induces eddy currents in the conductor itself. The proximity effect takes place when a conductor is under the influence of a time-varying field produced by a nearby conductor carrying a time-varying current. In this case, eddy current is induced whether or not the first conductor carries current. If the first conductor does carry a time-varying current, then the skin-effect eddy current and the proximity-effect eddy current superpose to form the total eddy current distribution. Regardless of the induction mechanism, eddy currents reduce the net current flow in the conductor and hence increase the ac resistance. Since a spiral inductor is a multi-conductor structure, eddy currents are caused by both proximity and skin effects.

The distribution of eddy currents depends on the geometry of the conductor and its orientation with respect to the imposing time-varying magnetic field. The most critical parameter presenting the skin effect is the skin depth. The skin depth is also known as the "depth of penetration" since it describes the degree by which the electromagnetic field

penetrates into the thickness of a conductor at high frequencies. The severity of the skin effect is determined by the ratio of skin depth to the conductor thickness. The eddy current effect is negligible only if the depth of penetration is much greater than the conductor thickness (e.g., at frequencies close to dc).

Current distribution in a conductor is strongly dependent on the location of the ground plane. In case of the isolated conductor, at low frequencies where the skin depth is in the order of the strip thickness, the current distribution is almost uniform across the thickness of the conductor. If this condition is satisfied, the ac resistance of the conductor per unit length can be calculated from:

$$R_{ac_{f \rightarrow 0}} = R_{dc} = \frac{1}{\sigma w t} \quad t \leq 2\delta \quad \text{Eq. 2-1}$$

where σ is the metal conductivity, and w and t are the conductor width and thickness, respectively.

At high frequencies however, when the skin depth is much smaller than the strip thickness (say $t > 4\delta$), a nearly exponential penetration of the electric field distribution in the conductor can be observed. This behavior of the current distribution is used to find the approximate formula for the ac resistance of an isolated strip [35].

$$R_{ac_{f \rightarrow 0}} = k \frac{l}{2\sigma\delta(w+t)} \quad t \geq 4\delta \quad \text{Eq. 2-2}$$

where l , w and t are the conductor length, width and thickness, respectively. σ is the conductivity of the strip, and δ is the metal skin depth. k is the correction factor, which depends on w and t .

On the other hand, for a microstrip line with large w/h ratio, current recedes to the bottom surface of the conductor [38-41]. The w and h are the width of the conductor and the thickness of the substrate (distance of the inductor structure to the ground plane), respectively. The current distribution is otherwise almost uniform across the height of the conductor. Figure 2-3 compares the current density distribution for two extreme cases of w/h ratio. For microstrip conductors at high frequencies the effective thickness can then be approximated by

$$t_{eff} = \delta.(1 - e^{-t/\delta}) \quad Eq. 2-3$$

And as a result, the series resistance, R_s , can be expressed as

$$R_s = \frac{\rho.l}{w.t_{eff}} \quad Eq. 2-4$$

Based on Eq. 2-4, resistance of a microstrip line does not decrease by increasing its thickness in excess of $5 \times$ skin depth. On the contrary, having an isolated strip structure for the inductor allows reduction of the series resistance by increasing the thickness of the conductor, even in excess of $5 \times$ skin depth.

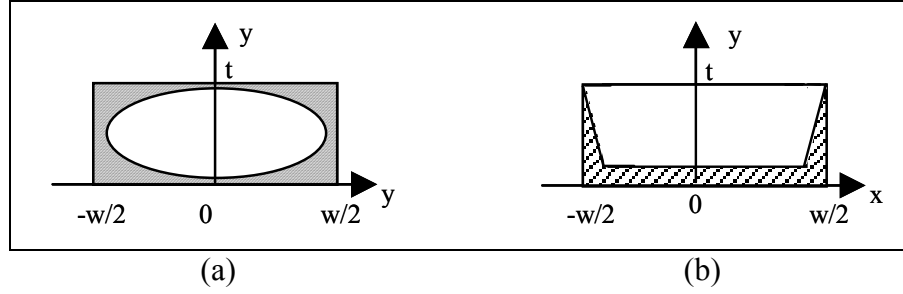


Figure 2-3. Effective area of current flow at high frequencies where (a) $w/h \rightarrow 0$ and (b) $w/h \rightarrow \infty$.

To take advantage of this phenomenon, inductor structures used in this thesis are coplanar with distant ground, knowing that coplanar structures with distant ground behave like isolated strips. Therefore, the equivalent series resistance can be calculated from:

$$R_s = \sqrt{\left(\frac{l}{\sigma w t}\right)^2 + \left(\frac{k l}{2\sigma\delta(w+t)}\right)^2} \quad \text{Eq. 2-5}$$

SONNET simulation results also confirm that for coplanar structures with distant ground, current also flows on the top surface of the conductor. The verification of this fact is shown in Fig. 2-4 (red color shows the highest current density). At 10GHz the current is confined closer to the metal walls, showing the effect of the skin depth.

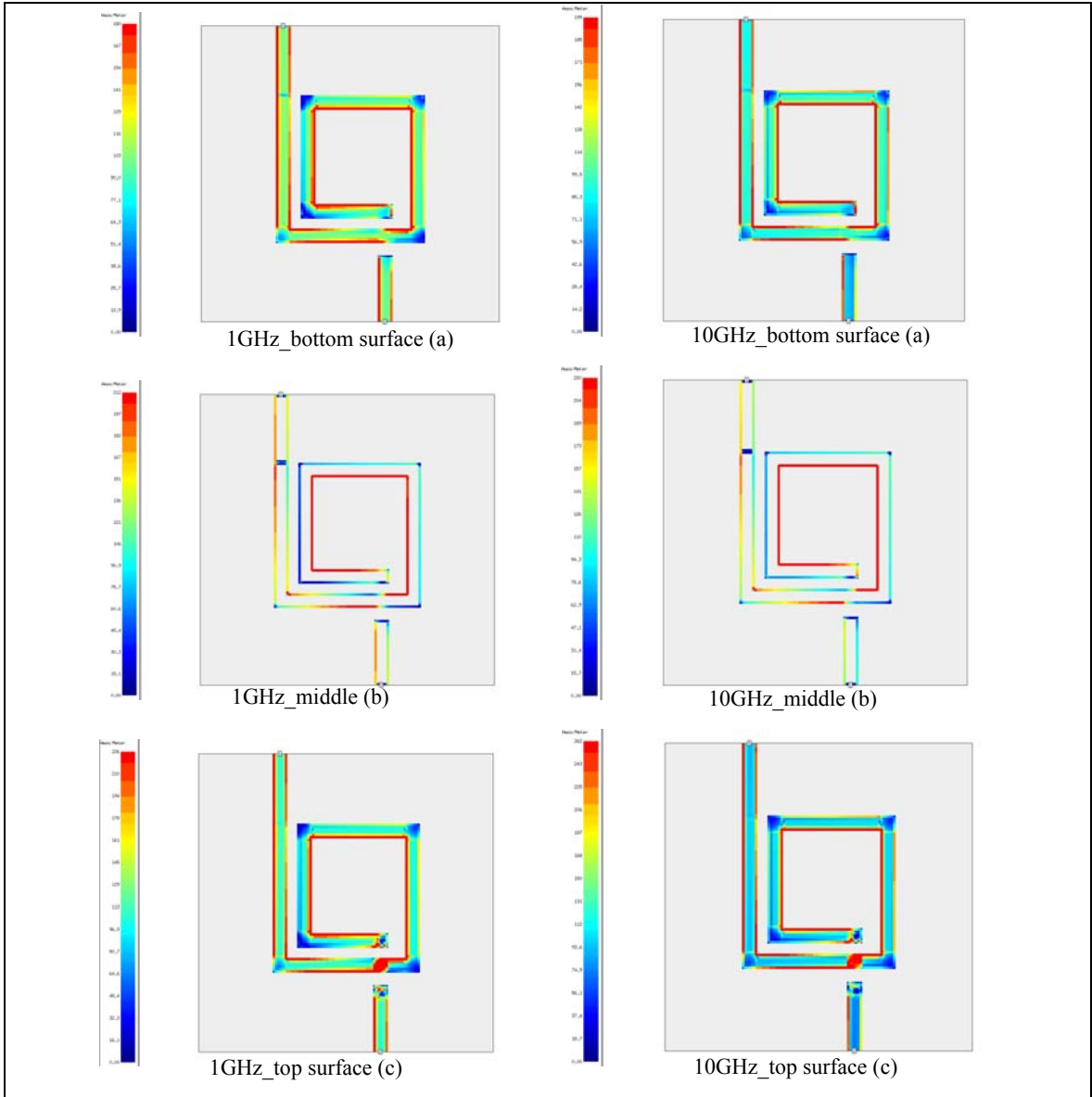


Figure 2-4. Current density of a 1.5-turn inductor at 1 GHz and 10 GHz (a) at the bottom surface of metal, (b) at half the thickness of metal, and (c) at the top surface of metal.

2.2.2 Series Inductance

Many equations have been established to calculate the total inductance of a spiral inductor, based either on the Greenhouse theory or on the experimental results. Table 2-1 summarizes some of the proposed formulas. Greenhouse considers an n -turn rectangular spiral inductor as a set of $4n$ straight segments. The overall inductance of this inductor can be calculated by adding up the self-inductance of each straight segment and the mutual inductance between each two parallel segments [34]. Mohan's equation is based on experimental results and contains most geometrical features of the inductors [42]. This equation is verified by SONNET simulations and is used in this thesis. Figure 2-5 compares the inductance predicted by Mohan's equation with SONNET simulation results for 5 different inductors at the frequency of peak Q . The maximum inductance deviation is less than 20%.

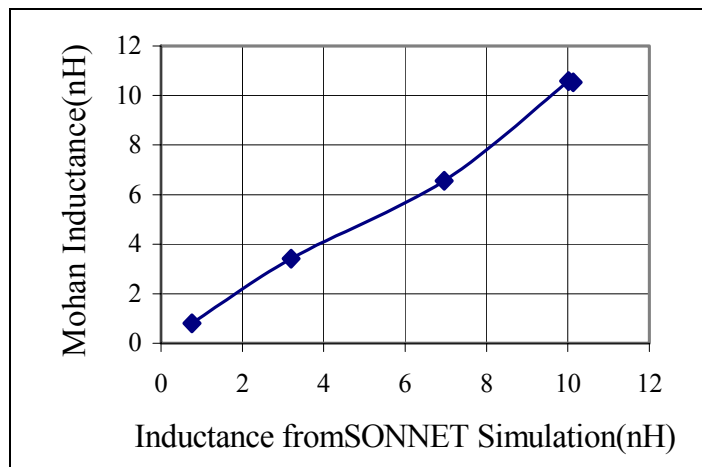


Figure 2-5. Mohan's predicted inductance vs. SONNET simulation results for 5 different inductors.

Table 2-1. Inductance Formulas [43], [44]

Voorman	$L_{Voo} = 10^{-3} n^2 d_{avg}$
Dill	$L_{dill} = 8.5 \times 10^{-4} n^{5/3} d_{avg}$
Bryan	$L_{bry} = 2.41 \times 10^{-3} n^{5/3} d_{avg} \log \frac{4}{\rho}$
Ronkanien	$L_{ron} = 1.5 \times \mu_0 n^2 e^{-3.7(n-1)(w+s)/d_{out}}$
Cros	$L_{cro} = 1.3 \times 10^{-4} \left(\frac{d_{out}^3}{w^2}\right) \eta_a^{5/3} \eta_w^{1/4}, \eta_a = \frac{\text{metal area}}{\text{total area}}, \eta_w = \frac{w}{w+s}$
Terman	$L = 0.0467sn^2 \{\log[2s^2/(t+w)] - \log 2.414s\} + 0.02032n^2 \{0.914 + [0.2235(t+w)/s]\}$
Expanded Grover (Green house)	$L_T = L_0 + M_+ - M_-$, $L_0 = \sum L_x$ $L_x = 2l_x \{\ln[2l_x/(w+t)] + 0.50049 + [(w+t)/3l_x]\}$
Mohan's Empirical expression	$L(nH) = \beta d_o^{\alpha_1} w^{\alpha_2} d_{avg}^{\alpha_3} n^{\alpha_4} s^{\alpha_5}$ $\beta = 0.00162$, $\{\alpha_i\}_{i=1}^5 = \{-1.21, -0.417, 2.40, 1.78, -0.03\}$
<i>t: conductor thickness, w: conductor width, s: line-line spacing, n: number of turns, l_x: length of each segment, M₊ and M₋: positive and negative mutual inductances, $\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}}$, $d_{avg} = \frac{d_{out} + d_{in}}{2}$</i>	

2.2.3 Series Capacitance and Substrate Parasitics

As it was previously mentioned, C_s represents the feed-through effect as well as the sidewall parasitic capacitances. The contribution of sidewall parasitic is negligible due to the insignificant voltage difference between the two adjacent strips, and C_s can be calculated from:

$$C_s = \frac{\epsilon_{dielectric} A_{overlap}}{d} = n.w^2 \frac{\epsilon_{ox}}{t_{oxM1-M2}} \quad \text{Eq. 2-6}$$

The high frequency loss of Si substrate is represented in C_{si} and R_{si} . Specifically, R_{si} is originated from the creation of eddy currents in the low resistivity Si substrate and C_{si} models the high frequency capacitive effect occurring in the semi-conductors. To extract the substrate characteristic, dummy structures should be included on the substrate. Assume a rectangular dummy pad to have a measured impedance of Z_{pad} . R_{si} and C_{si} can be approximated by:

$$Z_{pad} = R_{pad} + \frac{1}{j\omega C_{pad}} \quad \text{Eq. 2-7}$$

$$R_{si} = R_{pad} \times \frac{\text{pad area}}{\text{total inductor area}} \quad \text{Eq. 2-8}$$

$$C_{si} = C_{pad} \times \frac{\text{total inductor area}}{\text{pad area}} \quad \text{Eq. 2-9}$$

2.2.4 Spiral Inductor Quality Factor

The general expression for the quality factor is:

$$Q = \frac{\text{energy stored}}{\text{energy lost}} \quad \text{Eq. 2-10}$$

For inductors, the only desirable source of storing energy is magnetic field and hence any source of storing electric energy such as capacitances is considered as a parasitic. As a result, Q of an inductor can be simplified as follow:

$$Q = 2\pi \frac{\text{peak magnetic energy} - \text{peak electric energy}}{\text{Energy dissipated per cycle of oscillation}} \quad \text{Eq. 2-11}$$

The frequency at which the peaks of electric and magnetic energies are equal is called the self-resonance frequency (*SRF*). Quality factor becomes zero at *SRF*. At frequencies higher than *SRF*, the inductor does not behave as an inductor anymore. There are two separated-source of energy dissipation in an inductor:

I. Metal loss:

This loss is due to the finite conductivity of the metal conductors together with the skin and proximity effects presented at high frequencies. R_s in the equivalent circuit model represents the metal loss.

II. Substrate loss:

At RF frequencies, induced currents in the Si substrate limit the Q by converting the electromagnetic energy into heat. Equations 2-12 and 2-13 show components of the induced current in the substrate at the presence of electromagnetic fields [45].

$$\nabla \times H = j\omega\varepsilon' E + \omega\varepsilon' \tan \delta E + \sigma E \quad \text{Eq. 2-12}$$

$$\nabla \times E = -j\omega\mu H, \quad J = \sigma E \quad \text{Eq. 2-13}$$

where σ and $\tan\delta$ represent the substrate conductivity and loss tangent, respectively; ω is the angular frequency, ε' and ε'' are the real and imaginary part of the substrate permittivity and μ is the permeability. For low-resistivity substrates such as CMOS-grade Si, the electrically-induced current (σE) dominates over the dipole loss ($\omega\varepsilon' \tan\delta E$). However, for high-resistivity substrates the dipole loss is the determining loss

mechanism. At higher frequencies, creation of the magnetically induced eddy current in low-resistivity substrates (Eq.2-13) also limits Q .

These two sources of loss are independent and the unloaded Q can be expressed by [43]:

$$\frac{1}{Q} = \frac{1}{Q_{substrate}} + \frac{1}{Q_{metal}} \quad Eq. 2-14$$

where $Q_{substrate}$ and Q_{metal} represent the substrate loss and the ohmic loss of metal strips, respectively. At very low frequencies, the DC series resistance of the metal layers is the dominant mechanism for determining the Q . At higher frequencies, skin effect and proximity effects reduce the effective area of current flow and thus further limits the Q . At even higher frequencies, loss mechanisms present in the substrate settles the lower limit on the Q .

To investigate the validation of Eq.2-14 and to better understand the contribution of each loss-mechanism in Q , SONNET simulations were carried out. Two sets of simulation were performed to study the effect of each source of loss. Metal loss was determined by assuming that the inductor is elevated in vacuum. On the other hand, the substrate loss was considered by using ideal metal conductors. Figure 2-6 illustrates the SONNET simulation results. As can be seen, metal loss is the dominant loss mechanism at low frequencies, while the substrate loss sets the lower limit on the Q at higher frequencies.

To obtain high- Q inductors, the effect of both the substrate and the metal loss has been effectively suppressed.

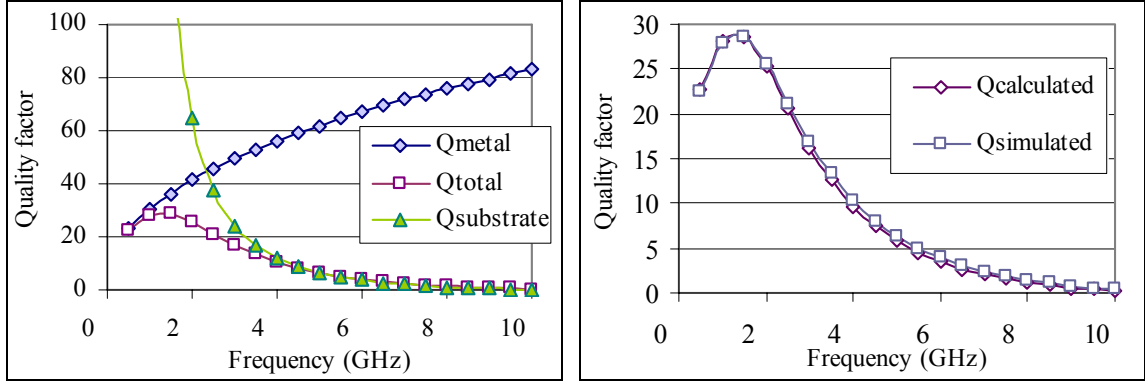


Figure 2-6. (Left) Quality factor vs. frequency for a one-turn spiral inductor and (right) Comparison of the calculated Q (by Eq.2-14) and simulated Q ($d_{out}=500\mu\text{m}$ $w=50\mu\text{m}$, and $t_{metal}=15\mu\text{m}$. $\rho=10\Omega\cdot\text{cm}$).

2.3 Trenched Si Island for Reduced Substrate Loss

The substrate loss is reduced by trenching the Si. As it was mentioned earlier, the creation of currents in the bulk of Si substrate reduces the $Q_{substrate}$. Disrupting the path of current by slicing the substrate with deep high-aspect-ratio trenches reduces the substrate effective permittivity and conductivity, which in turn reduces the electrically- and magnetically-induced currents as well as the dipole loss. The trenches are made underneath the inductors to create an island of low-loss substrate (Trenched Si Island). Two low-temperature approaches are taken to create a rigid and smooth substrate by covering the trenched areas. These approaches include refilling the trenches with a low-loss dielectric material and bridging-over the trenches with a PECVD dielectric layer. Chapter 3 will fully elaborate on the technique taken to reduce the substrate loss.

2.4 Thick electroplated Cu for Reduced Metal Loss

In this work, metal loss is reduced by electroplating thick Cu ($\sim 20\mu\text{m}$) and eliminating the effect of ground plane by increasing the signal to ground distance in the inductor layout. The thickness of routing metal (first metal) and the insulating SiO_2 layers are said by processing constrains. To alleviate the effect of routing layer on the overall Q , the length of this layer must be kept as short as possible.

2.5 Optimization of the inductor physical dimensions

In order to obtain the highest possible Q for inductors fabricated on Trenched Si Islands (*TSI*), all physical dimensions of inductor are optimized using SONNET simulation tool. To find the optimized value of each parameter, all other parameters are kept constant.

The optimized parameters are:

- 1) Metal thickness
- 2) Trench depth
- 3) Number of turns
- 4) Trenched island area
- 5) Outer diameter
- 6) Metal width
- 7) Metal spacing
- 8) Shape of the inductor (round/rectangular/octagon)
- 9) Position of the ground plane

2.5.1 Metal Thickness

SONNET calculates the total surface impedance, impedance per unit area, of a thick metal by [41]:

$$Z_s = \frac{(1+j)\rho}{1 - e^{-\frac{(1+j)t}{N\delta}}} \quad \text{Eq. 2-15}$$

where ρ is the metal resistivity, δ is the skin depth, t is the metal thickness and N is the number of conductor sheets that SONNET requires to estimate the thickness of the metal. By increasing t , surface resistance drops exponentially and therefore Q increases. Figure 2-7 illustrates the dependency of the Q on the metal thickness. Simulation results confirm the Q improvement with metal thickness in excess of $5 \times \delta$.

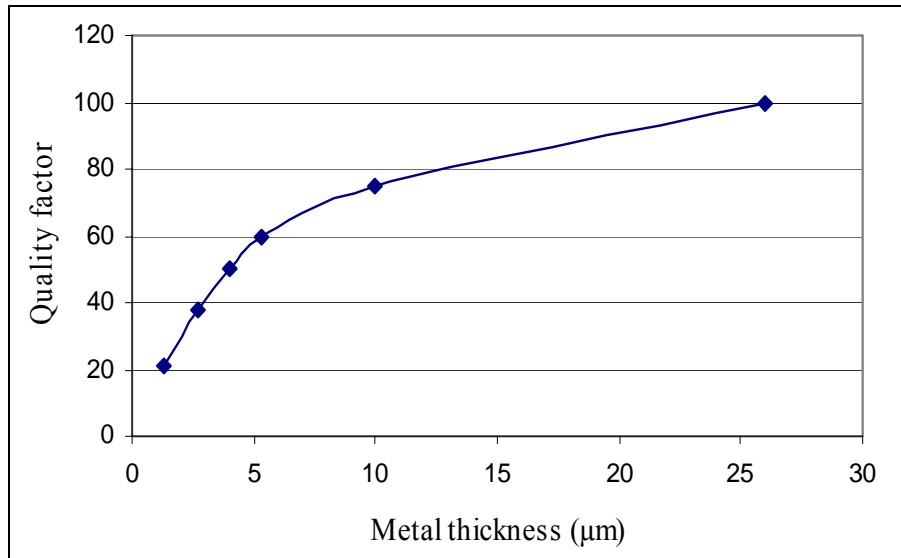


Figure 2-7. Q vs. metal thickness using SONNET thick metal model. $N=20$ for $26\mu\text{m}$ thick inductor and $N=5$ for $6\mu\text{m}$ metal.

2.5.2 Trench Depth

Optimum value for the trench depth cannot be obtained by SONNET simulation tool as it is computationally intensive. To have an estimate of the required trench depth, simulations were done assuming the substrate is covered with a thick oxide layer. SONNET simulations indicate an increase in the inductor Q with oxide thickness up to $50\mu\text{m}$ for a 2.9nH inductor (Fig. 2-8). The optimum value of the trench depth could be close to $50\mu\text{m}$ but needs to be obtained experimentally.

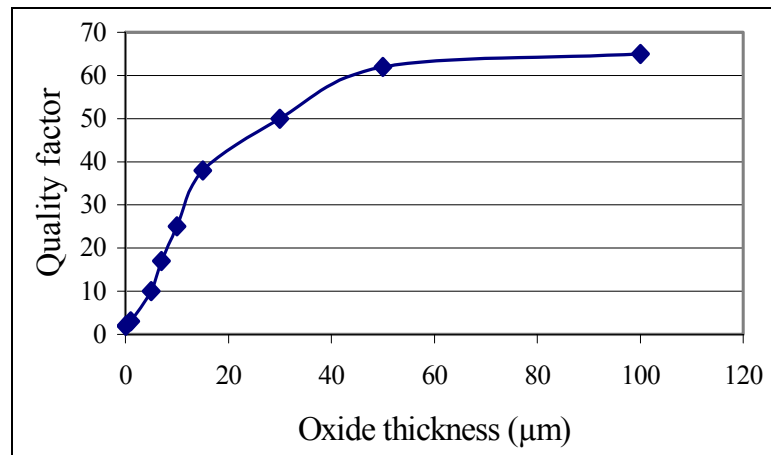


Figure 2-8. Q vs. oxide thickness ($t=4\mu\text{m}$, $w=40\mu\text{m}$, $s=10\mu\text{m}$, $d_{out}=400\mu\text{m}$ $L=2.9\text{nH}$).

2.5.3 Number of Turns

Increasing the number of turns results in smaller outer diameter for a specific inductance value. Accordingly, the inner diameter of the inductor reduces. Since the magnetic field is maximum at the center of the spiral inductor, the unwanted substrate current density is

high near the center of the inductor. This induced current in the substrate will cause a reverse current to flow in the inner most conductors, resulting in an increase in the series resistance and decreases in the Q [27]. Figure 2-9 demonstrates the validation of the above argument.

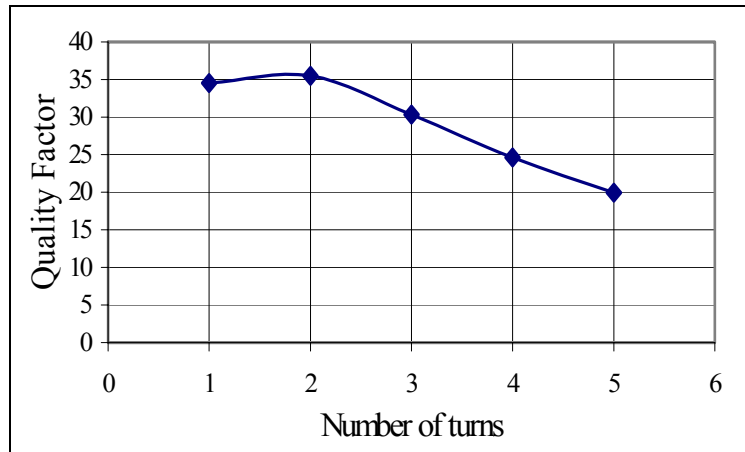


Figure 2-9. Q vs. Number of turns ($f=2.4\text{GHz}$, $L=2.9\text{nH}$, $s=5\mu\text{m}$ and $w=20\mu\text{m}$, $t=6.75\mu\text{m}$).

In our case, where the first metal layer is thin, one-turn inductors exhibit higher Q compared to the multi-turn inductors of the same inductance value.

2.5.4 Trenched Island Area

SONNET cannot be used to optimize for the minimum required trenched area due to a bug in the tool. The minimum required trenched area must be attained experimentally.

2.5.5 Outer Diameter

Smaller-size inductors have smaller substrate parasitic capacitance and thus higher self-resonance frequency. Increasing the outer diameter increases the series resistance and inductance. Since the inductance and resistance values increase at the same rate, the peak Q remains almost constant. Figure 2-10 show the shift in the frequency of peak Q versus frequency as the outer diameter of a one-turn spiral inductor changes. For a better comparison, frequency of peak Q is sketched versus d_{out} in Fig. 2-11. Maximum Q occurs at lower frequency as the outer diameter increases [46].

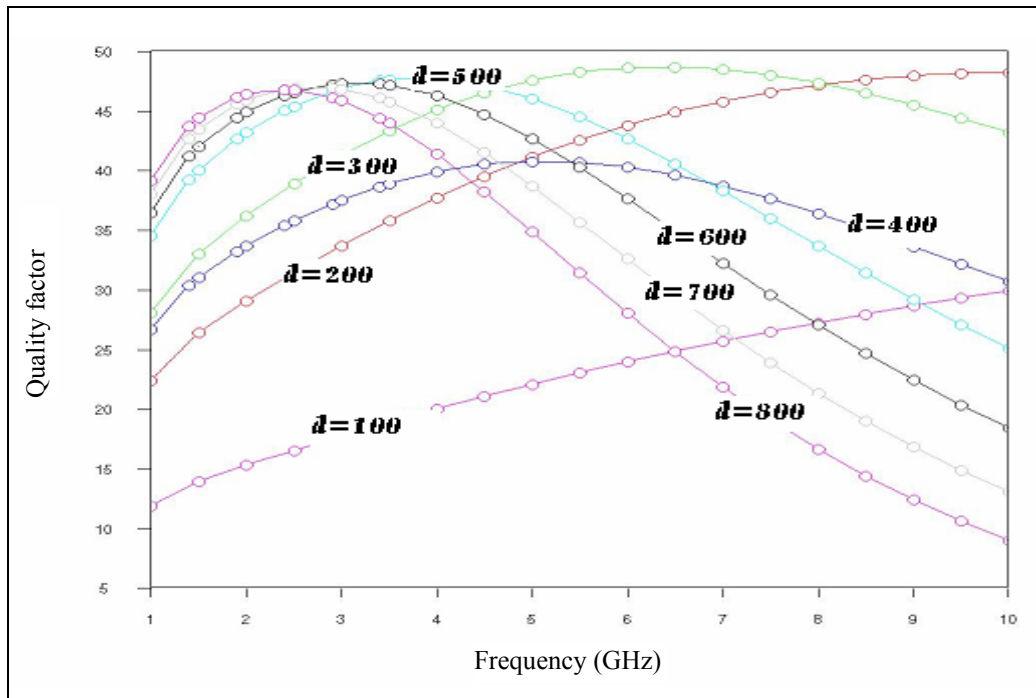


Figure 2-10. Q vs. frequency for a one-turn inductor with various d_{out} ($w=40\mu m$).

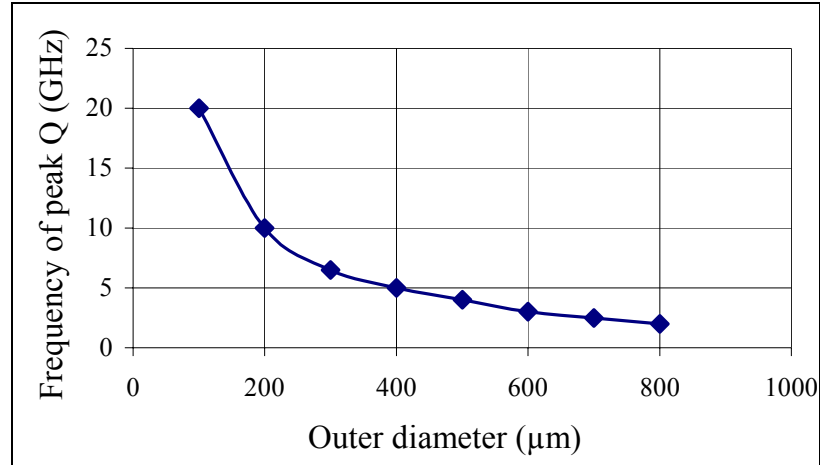
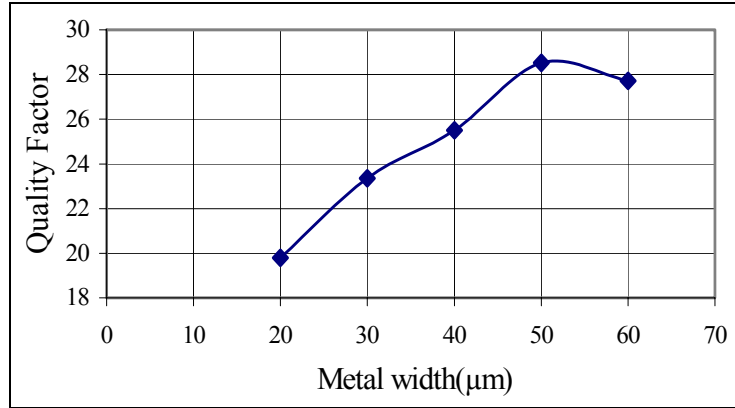


Figure 2-11. Frequency of peak Q vs. d_{out} for one turn inductors with $w=40\mu m$.

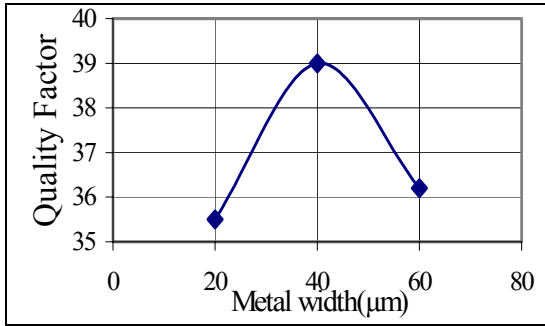
2.5.6 Metal Width

Variation of the conductor width (w) affects the Q in several ways. The primary consequence of increasing w is reduction of the conductor's series resistance. On the other hand, increasing the conductor width has a negative effect on the Q due to the simultaneous enlargement of the substrate parasitic capacitance. Metal width has an optimum value that must be designed for each specific inductor. Figure 2-12 shows the change in Q as a function of w for two different inductors.

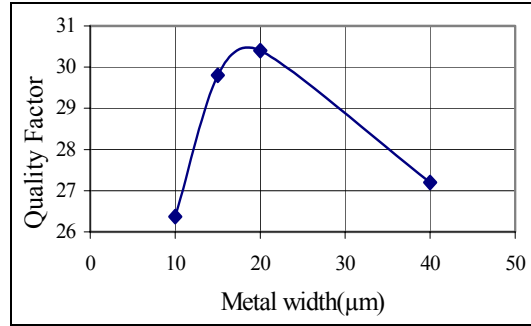
Another consequence of increasing the metal width is reduction of the SRF given that the substrate capacitance increases accordingly.



(a)



(b)



(c)

Figure 2-12. Q vs. conductor width for (a) one-turn $1nH$ inductors (b) $2.9nH$ inductors ($s=5\mu m$ and $n=2$), and (c) $2.9nH$ inductors ($s=5\mu m$ and $n=3$).

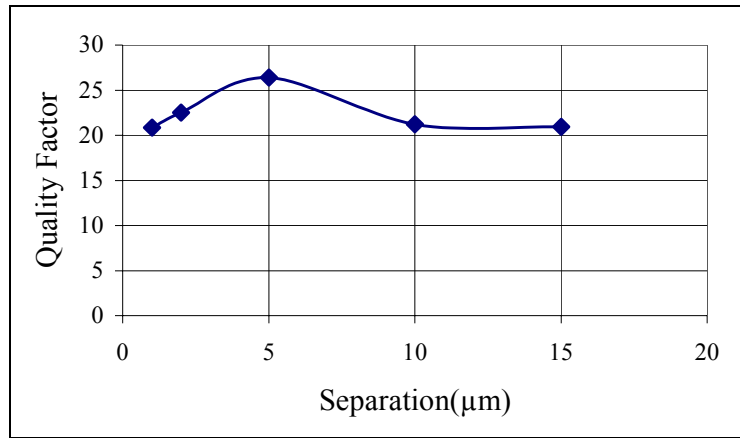
2.5.7 Metal Spacing

When working at low frequencies, minimum possible spacing determined by lithography resolution is favored to maximize the magnetic coupling (Eq. 2-16).

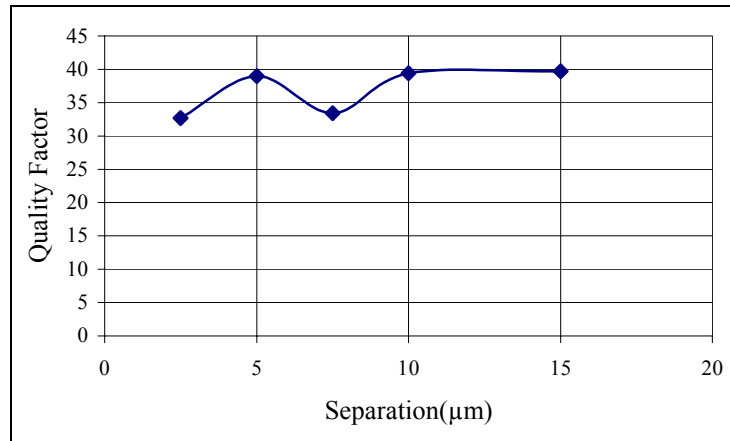
$$2s_{\min} = 3\sqrt{\lambda\left(g + \frac{1}{2}z\right)}$$

Eq. 2-16

where s_{min} is the minimum feature size, λ is the light wavelength, g is the gap between the mask and the substrate and z is the thickness of the photoresist. At high frequencies proximity effects and magnetic coupling favor a larger value of spacing [27]. At 2.4 GHz two sets of inductors with two and three number of turns were simulated. The results are shown in Fig. 2-13.



(a)



(b)

Figure 2-13. Q vs. separation for 2.9nH inductors with (a) $w=10\mu\text{m}$, $n=3$ and (b) $w=40\mu\text{m}$, $n=2$.

2.5.8 Shape of the Inductor (Round/Rectangular/Round-edge)

Current crowding at the sharp edges of the conductor reduces the effective width and increases the metal loss. Round spiral inductors exhibit higher Q compared to the rectangular inductors due to the reduced current crowding effect. For the same reason, rectangular inductors with round edges show an improved Q compared to inductors with sharp edges. Q of a round inductor is about 25% better compared to its rectangular counterpart (Fig. 2-14).

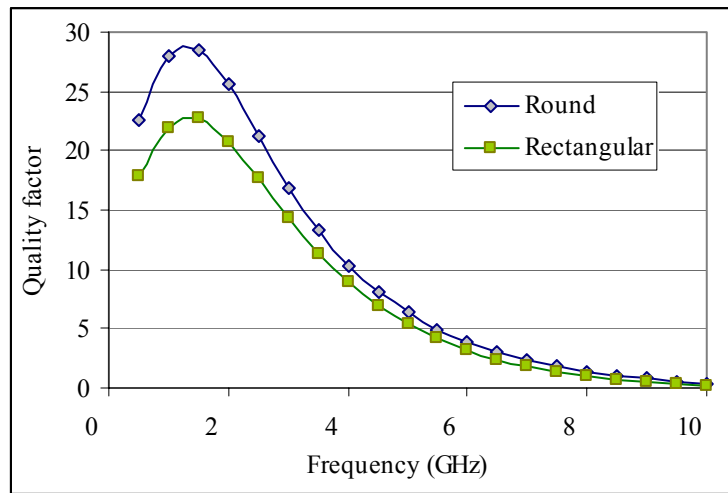


Figure 2-14. Q vs. frequency ■-■ round spiral and ◆-◆ rectangular spiral ($s=50\mu\text{m}$, $w=50\mu\text{m}$, $d_{out}=500\mu\text{m}$ and $n=1$).

Rectangular inductors have a slightly higher inductance than round inductors with same physical dimensions. In Fig. 2-14 for instance, $L=0.96\text{nH}$ at 0.5 GHz for the rectangular and $L=0.90\text{nH}$ for the round inductor.

2.5.9 Position and Shape of the Ground Plane

Coplanar ground plane has less effect on the current distribution in the signal line compared to the ground plane underneath the inductor even when the ground plane is patterned. To minimize the effect of ground plane, the signal to ground distance must be increased. In this work, the distance of the coplanar ground to the closest conductor is kept at $500\mu\text{m}$.

CHAPTER III

FABRICATION

3.1. Process Flow

Figure 3-1 shows the fabrication process flow for the Cu inductors on Trenched Si Islands. The substrate is CMOS grade Si with resistivity of 10-20 Ω .cm.

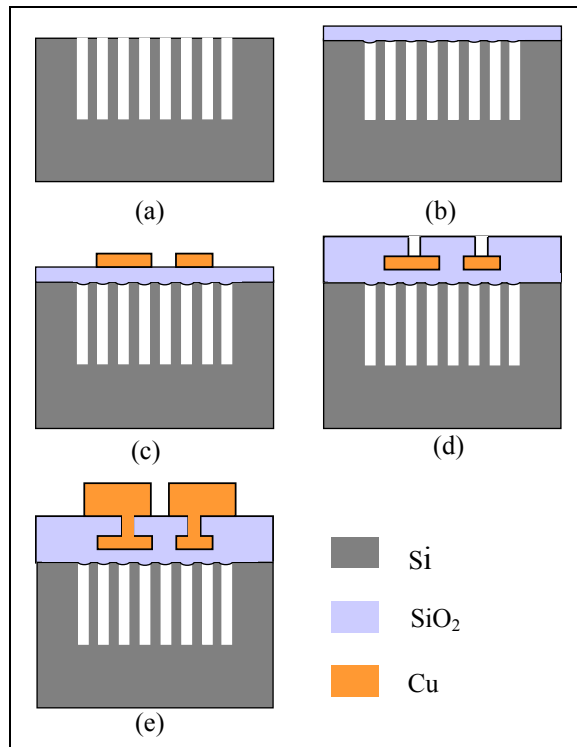


Figure 3-1. Schematic of the process flow.

The fabrication process has four masks. First, deep high-aspect-ratio (30:1) trenches are etched in the Si substrate using the Bosch process in the STS ICP tool.

The standard factory recipe was modified to reduce the anisotropy of the Bosch process in order to further decrease the substrate loss. The etch recipe in the STS ICP is shown in Table 3-1. The etch time is increased from 10sec to 11sec while the passivation time is decreased to 7sec (from 8sec) to increase the undercut.

Table 3-1. Recipe to etch trenches in the STS ICP system.

Passivation time (sec)	Etch time (sec)	Pressure (mTorr)	RF Platten power (watts)	RF Generation power (watts)
7	11	8	12	600

A 2-3 μm thick PECVD SiO₂ layer is then deposited at 300°C to cover the openings and lower the substrate parasitic capacitances. The PECVD silicon dioxide deposition is non-uniform and therefore the deposited SiO₂ bridges over the openings. The detailed recipe used in the UNAXIS PECVD system is shown in Table 3-2. The deposition rate is about 0.66 $\mu\text{m}/\text{min}$.

Table 3-2. Recipe to deposit SiO₂ in the UNAXIS PECVD tool.

Temperature (°C)	Pressure (mTorr)	N ₂ O pressure (sccm)	He pressure (sccm)	SiH ₄ pressure (sccm)	RF power (watts)	DC power (watts)
300	950	500	560	500	65	22

Figure 3-2 shows the cross-section SEM view of a 90 μm deep *TSI*. The etch time of the trenches is 1hour and the required deposition time for PECVD SiO₂ layer is 45min. As it is shown in this figure, width of the Si bars is less than width of the trenches, due to the isotropic etching of the Si.

The first metal layer is subsequently formed by evaporation and patterning of a 2 μm thick Chromium (Cr) -Cu-Cr layer. CVC E-beam evaporator was used for this purpose. The deposition rates of Cr and Cu are 3 $\text{\AA}/\text{sec}$ and 6 $\text{\AA}/\text{sec}$, respectively. Chromium layer of 300 \AA thick was used as the adhesion layer between Cu and SiO_2 since copper has a very poor adhesion to SiO_2 .

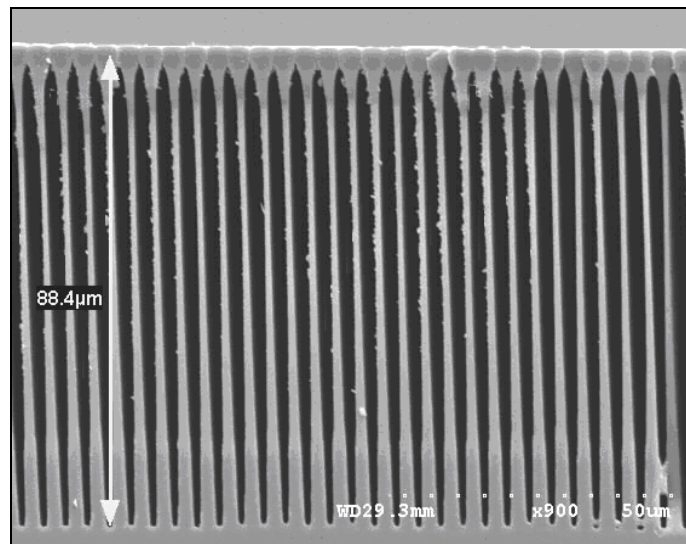


Figure 3-2. Cross-section SEM of a 90 μm deep TSI.

To isolate the two metal layers, a 2 μm thick PECVD SiO_2 is deposited at 300 $^\circ\text{C}$ using the same recipe given in Table 3-2. Vias are subsequently opened using Plasma therm ICP system. The ICP etch process temperature is 60 $^\circ\text{C}$. The recipe used in the Plasma-therm ICP system to anisotropically etch the SiO_2 layer is given in Table 3-3. The etching rate is about 0.13 $\mu\text{m}/\text{min}$ using this recipe.

Table 3-3. Dry etch recipe of SiO₂ in Plasma-therm ICP system.

RF1 power	RF2 power	Pressure	H ₂ flow rate	CF ₄ flow rate
100W	250W	5mTorr	2sccm	20sccm

A 300A°-1000A° seed layer of Cr-Cu is then sputter-deposited, followed by spin-coating and patterning of the electroplating mold. Thick NR4-8000P negative-tone photoresist from Futurrex Inc. has been used for this purpose, which produces high-aspect-ratio (4.5:1) and straight-sidewall columns as shown in Fig. 3-3 [47].

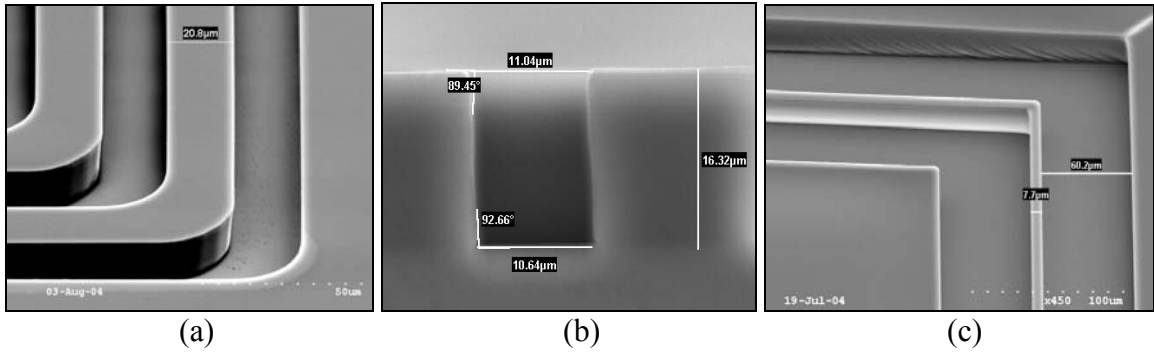


Figure 3-3. SEM pictures of (a) a 17µm thick NR4-8000P used as the electroplating mold; (b) close-up view of the straight photoresist side-walls, and (c) high aspect-ratio (30:8) photoresist column.

Next, thick layer of Cu is electroplated in an electroplating tank. The electroplating current should be about 25mA/cm² in order to have fine Cu grids [48]. The electroplating solution was prepared by mixing the chemicals shown in Table 3-4 in the vertical order. To enhance the Cu grid size and the electroplating rate, the electrolyte is agitated by nitrogen gas bubbles (Fig.3-4). After electroplating for a period of time, the solution level in the electroplating bath goes down and the surface of electroplated Cu layer becomes

rough (the Cu is not shiny anymore). By adding 10ml of Brightener and 10ml of Carrier (both from Techni PC 75) and sufficient amount of DI water this problem would be fixed.

Table 3-4. Electroplating solution, the chemical should be mixed in the order presented.

Component	To make 20 liters
DI water	15.8 liter
Copper sulfate ($\text{CuSO}_4 \cdot 5\text{H}_2\text{O}$)	1.5kg
51% sulfuric acid (H_2SO_4)	4 liter
PC 75 Brightener	0.1 liter
PC 75 Carrier	0.1 liter

The required electroplating current flow in this case is 800mA and the electroplating rate is $0.25\mu\text{m}/\text{min}$. After electroplating, the photoresist and the seed layer are removed. The photoresist is removed in Acetone and the solution used to remove the Cr layer is described in section 3.3.3. The thin Cu seed-layer is finally removed in a dilute mixture of $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2$ (1:1).

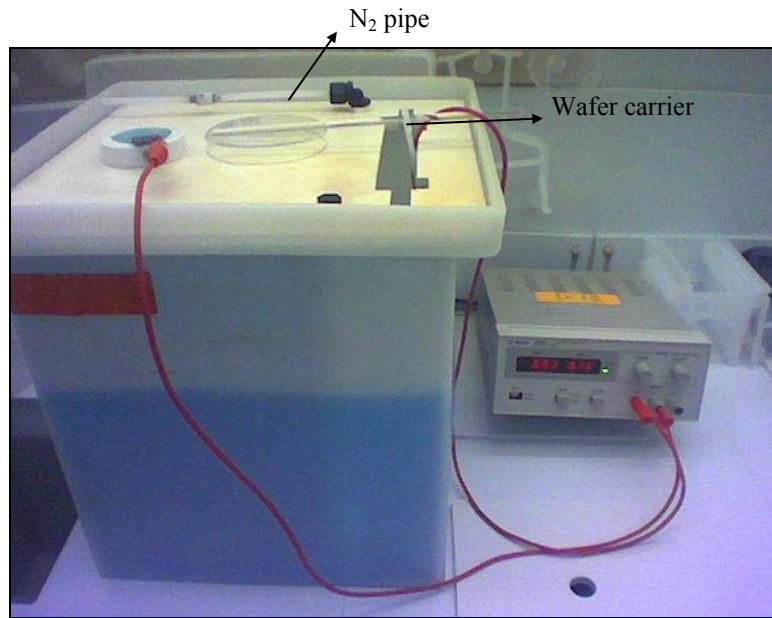


Figure 3-4. Picture of the electroplating tank, showing the electroplating set-up.

Figure 3-5 shows SEM picture of a one-turn rectangular inductor on *TSI*. The Cu trace is separated from the substrate during the cleaving process. Figure 3-6 shows SEM picture of a one-turn round inductor on 60 μm deep *TSI*.

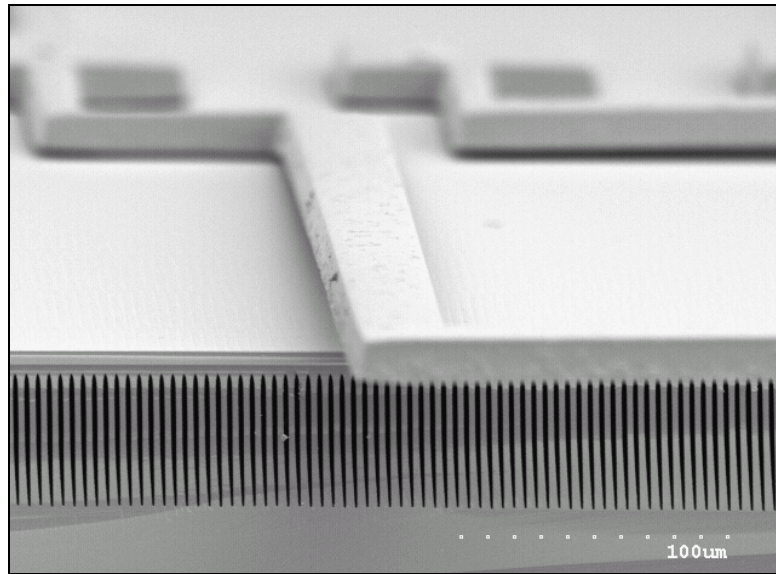


Figure 3-5. SEM picture of a one-turn inductor on top of *TSI* ($w=40\mu\text{m}$, $d_{out}=860\mu\text{m}$, $t_{metal}=26\mu\text{m}$, $Q=45$).

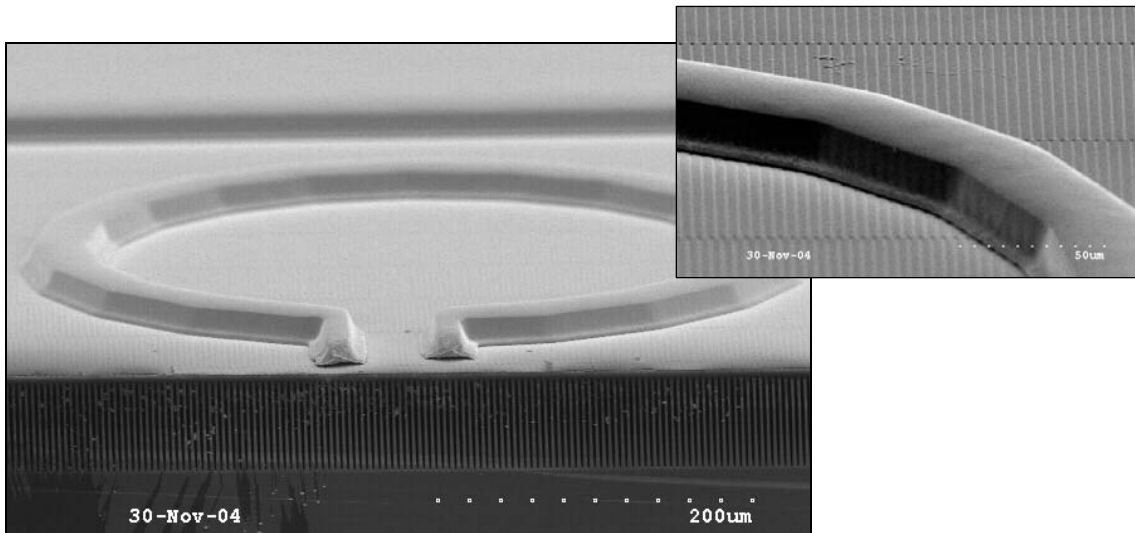


Figure 3-6. SEM picture of a one-turn round inductor on *TSI* with a close-up view of the thick electroplated Cu ($w=50\mu\text{m}$, $d_{out}=500\mu\text{m}$, $t_{metal}=20\mu\text{m}$, trench depth=60 μm , $Q=71$).

To evaluate the effectiveness of *TSI* in reducing the substrate loss, similar inductors were also fabricated on thick SiO_2 islands (*OI*) created by thermal oxidation of silicon left in between the trenches (@ $\sim 1100^\circ\text{C}$) [15, 24]. The SEM and microscope pictures of a three-turn spiral inductor on an *OI* are shown in Fig. 3-7.

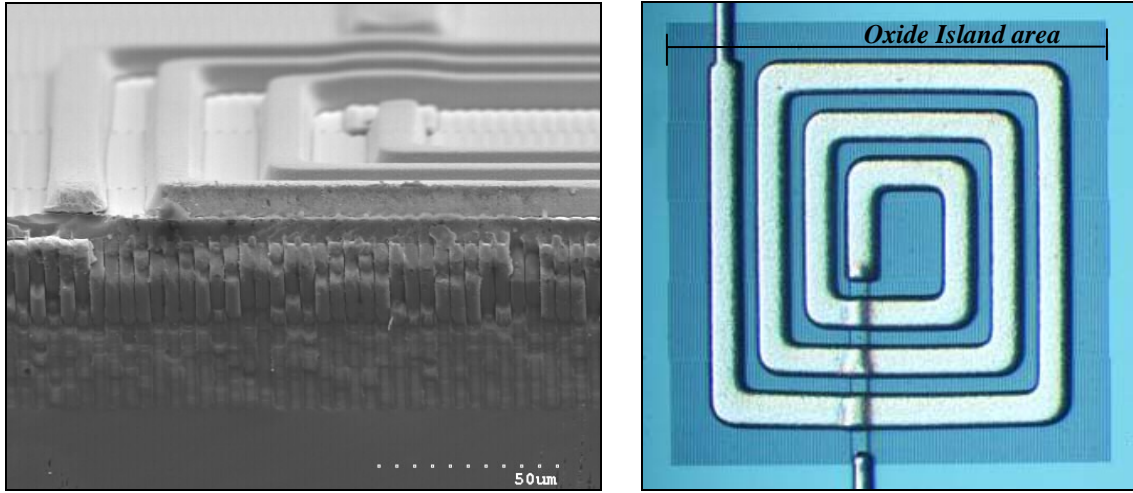


Figure 3-7. SEM (left) and microscope (right) picture of a 3-turn round-edge inductor, $w=15\mu\text{m}$, $d_{out}=400\mu\text{m}$, $s=15\mu\text{m}$, $t_{metal}=8\mu\text{m}$.

3.2. Covering the Trenches

Two low-temperature approaches are adopted in this research to cover the trenches and create a rigid low-loss substrate on which the inductors can be firmly supported.

3.2.1 Silicon Dioxide Bridge-over

The main approach, as discussed in the fabrication process flow, is bridging over the open areas through deposition of a low loss-tangent PECVD dielectric layer (e.g., SiO_2).

The required film thickness to bridge over the open areas and create a smooth surface is in the order of the trench width. The width of the openings should be optimized for low substrate-loss and reasonable bridge-over film thickness. For a Trenched Si Island (TSI) with repeated trench width of $2\mu\text{m}$ and Si width of $2\mu\text{m}$, the required PECVD SiO_2 thickness is about $3\mu\text{m}$. Figure 3-8 shows cross-section SEM view of a $50\mu\text{m}$ deep TSI. The opening width is $2\mu\text{m}$ and the bridge-over SiO_2 layer is $2.7\mu\text{m}$ thick.

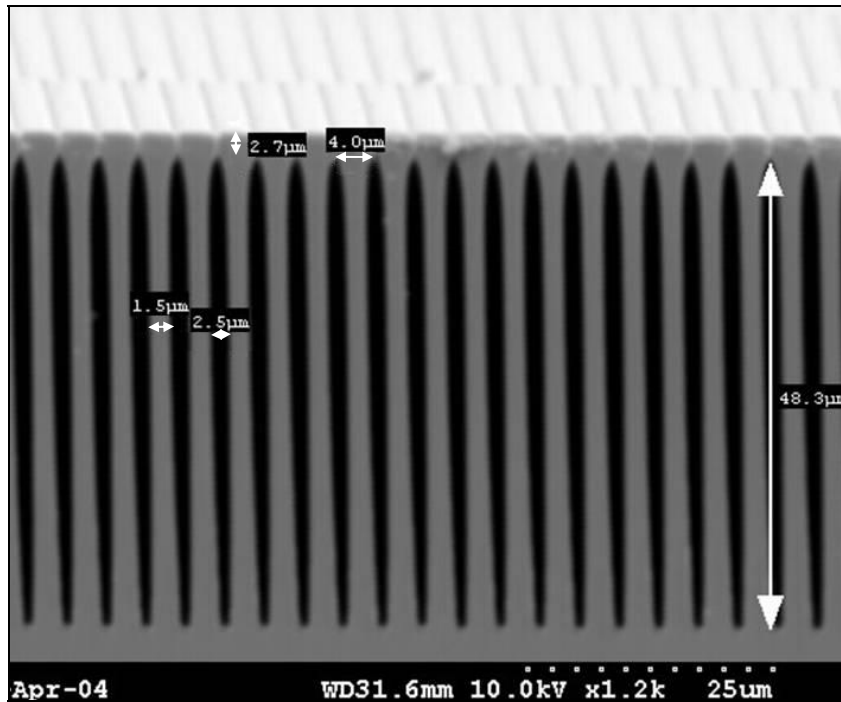


Figure 3-8. SEM picture of a $50\mu\text{m}$ deep Trenched Silicon Island (TSI)

Figure 3-9 demonstrates that the required SiO_2 film thickness to bridge over a $2.5\mu\text{m}$ wide opening and to create a smooth surface (surface roughness of $0.3\mu\text{m}$) is about $3\mu\text{m}$.

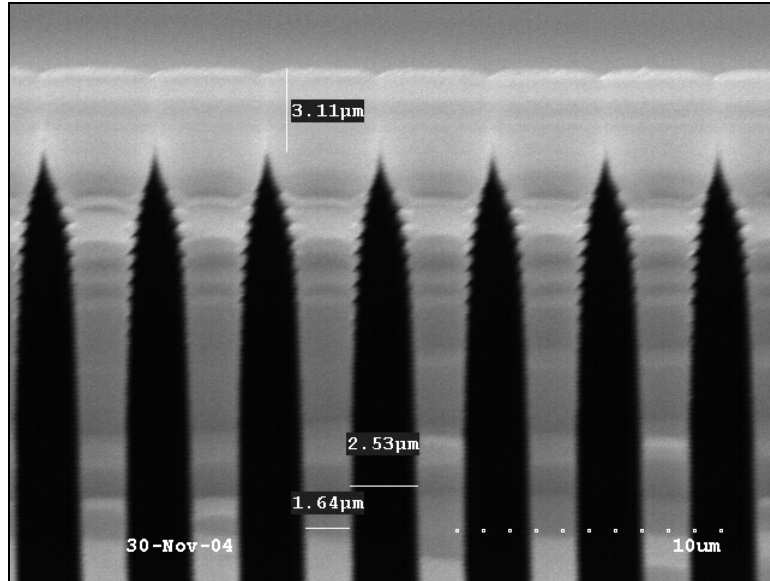


Figure 3-9. Close –up view of the smooth surface of a TSI (surface roughness<0.3µm).

3.2.2. Avatrel Polymer Trench Refill

An alternative low-temperature approach is to refill the trenched areas with a low loss dielectric material. Avatrel 2000P polymer from Promerous Inc. has been selected for this purpose since it has a low dielectric permittivity compared to other dielectric materials [49]. Table 3-4 compares the loss-tangent and permittivity of Avatrel with two other low-K dielectrics commonly used as isolating layers.

Table 3-4. Comparison of electrical properties of Avatrel with BCB and polyimide[49,50].

	Avatrel*	Polyimide	BCB
Moisture uptake, %	<0.1	0.5-3	0.23
Permittivity (ϵ_r)	2.50	3.1- 4.1	2.7
$\tan \delta @ 1\text{GHz}$	0.009	0.01-0.015	0.015

The recipe used to fill the trenches with spin-coating of Avatrel is as follow:

- Spin speed: 3000rpm, 500rpm/sec for 40sec
- Soft bake: on hotplate at 110°C for 10min
- Expose: 500mJ (100sec with lamp intensity of 5mJ/sec, I-line (wave length: 365nm))
- Post Exposure Bake (PEB): in oven at 100°C for 20min

Followed by 60min in oven at 160°C

The resulting thickness of Avatrel on the non-trenched areas using this recipe is 20 μ m. A 1 μ m thick SiO₂ layer is then deposited to enhance the adhesion of the first metal layer to the substrate. The deposition temperature is reduced to 160°C to avoid bubbling of the Avatrel layer. Other SiO₂ deposition parameters are as shown in Table 3-2. Figure 3-10 illustrates SEM picture of a 20 μ m thick layer of Avatrel on *TSI* after deposition of SiO₂ at 300°C, showing this deposition temperature results in bubbling of the Avatrel layer.

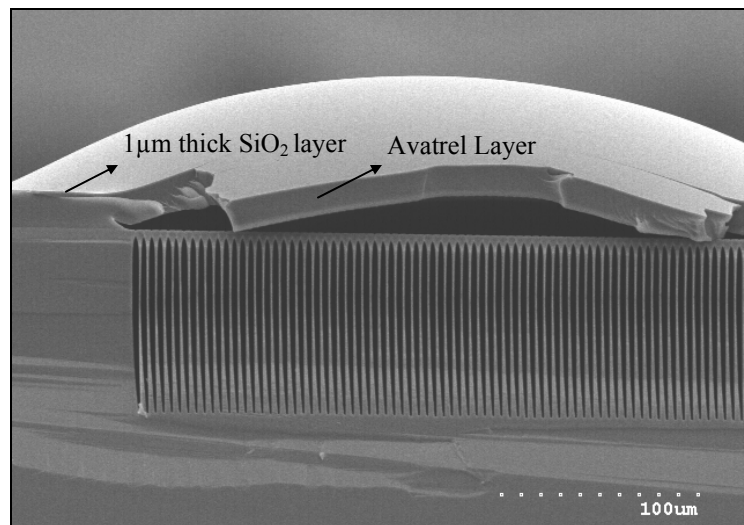


Figure 3-10. Flaking of Avatrel layer due to high-temperature processing (300 °C).

Figure 3-11 shows a 90 μm deep *TSI* refilled by spin-coating of Avatrel polymer. The thickness of SiO_2 over-coat is 1 μm and the SiO_2 deposition temperature is 160 $^\circ\text{C}$.

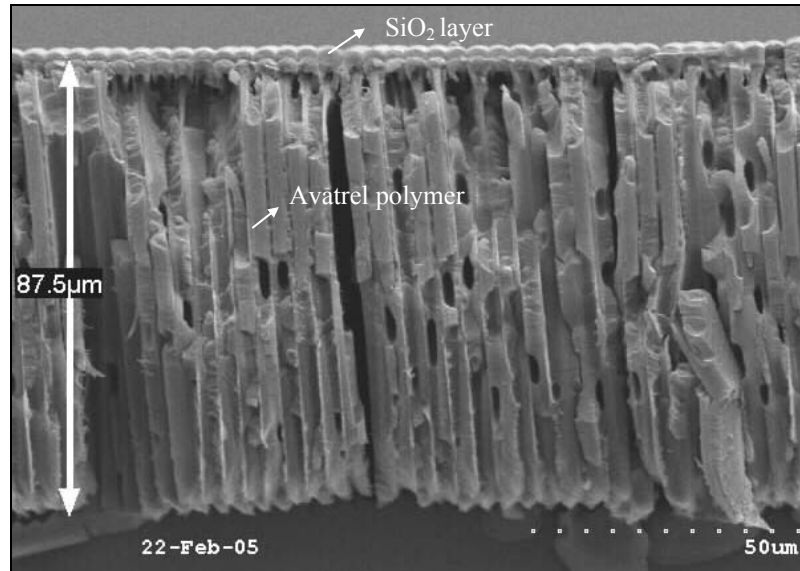


Figure 3-11. SEM picture of a 90 μm deep *TSI* refilled by Avatrel polymer.

3.3. Process Issues

3.3.1. High Aspect-Ratio Si Etch

Width and depth of the trenches determine the required SiO_2 film thickness and the substrate loss, respectively. High-aspect-ratio trenches with opening-width in the range of 2-3 μm are required to effectively reduce the substrate loss, while keeping the subsequent bridge-over SiO_2 film thickness practical. The highest achievable aspect-ratio determined by the STS ICP processing constrains is about 1:30. Deep trenches having this aspect

ratio (3:90) are very brittle and can be easily broken in the photo-resist stripper due to the capillary forces. Capillary forces result from trapped liquid that, due to Laplace pressure differences and surface tension forces produce an attractive force [51]. Solution to this problem is to dry etch (ash) the photoresist used as the mask right after the Si-etching step. Bridge-over SiO₂ layer provides a firm support for the trenches and solves this issue for the subsequent processing steps.

3.3.2. Electroplating Mold

The most critical step is patterning the electroplating mold. The electroplating mold should be thick with straight sidewalls. Negative-tone photoresists are more appropriate for this purpose as they have improved sidewall profile over positive-tone photoresists with same film thickness. The electroplating mold should also have a proper adhesion to the Cu seed-layer. Therefore, the photoresist used as the electroplating mold needs an extensive characterization. The NR-4 8000P photoresist employed in this research worked well using the following recipe:

- Spin speed: 600rpm, 1500rpm/sec for 5sec
1200rpm, 500rpm/sec for 40sec
- Soft bake: on hotplate at 80°C ramps to 110°C for 10min
- Expose: 360mJ (60sec with lamp intensity of 6mJ/sec, I-line (wave length: 365nm))
- Post Exposure Bake (PEB): on hotplate at 80°C ramps to 100°C for 5min
- Develop: in RD-6 resist developer for 3min

This photoresist does not need to be hard-baked before electroplating to ensure its adhesion to the Cu seed-layer and thus the photoresist can be easily removed in Acetone after the electroplating step. Possible residues of the photoresist are removed in the acidic solutions used to etch the seed-layer afterward.

3.3.3 Chromium Etchant

Chromium is used as an adhesion promoter between Cu and SiO₂. Solvent used for etching the Cr seed layer, after the electroplating step, must have a good selectivity to Cu. A mixture of 10g Potassium Ferricyanide (K₃Fe(CN)₆), 10g Sodium Hydroxide (NaOH), and 100ml DI water was developed for this purpose [52]. This wet etchant worked well and provided an etch rate of approximately 500Å/min.

The detailed processing steps are included in the Appendix A.

CHAPTER IV

MEASUREMENT AND CHARACTERIZATION

Rectangular and circular type inductors of various dimensions were fabricated and tested on low-loss micromachined trenched Si substrates. On-wafer S-parameter measurements were carried out using an *hp8517B* vector network analyzer and ground-signal-ground Cascade micro-probes. The pad size used for on-wafer measurements is $100\mu\text{m}\times 100\mu\text{m}$ with $150\mu\text{m}$ pitch. The pad-only characteristics were measured on the open pad structures. The pads parasitics were then de-embedded from the overall inductor characteristic by subtracting the Y-parameters of the pads from the Y-parameters of the embedded inductors [53]. The equivalent circuit model shown in Fig. 2-2 is used to extract the electrical parameters. For one-turn one-port inductors, the second port in the model was grounded. Inductance and Q are extracted using the following equations:

$$L = \frac{\text{Im}(1/Y_{11})}{2 \times \pi \times f} \quad \text{Eq. 4-1}$$

$$Q = \frac{\text{Im}(1/Y_{11})}{\text{Re}(1/Y_{11})} \quad \text{Eq. 4-2}$$

The dependency of Q on inductor physical parameters including oxide thickness, metal thickness, trench depth of *TSI*, and dielectric material have been extracted from the measured data.

4.1. Effect of TSI on Q

Figure 4-1 demonstrates the effectiveness of the Trenched Si Islands in increasing the Q . As it is shown in Fig. 4-1(b) the S_{11} -parameter of the inductor fabricated on 50 μm deep TSI (low-temperature processing) is very close to the one fabricated on 50 μm thick solid OI (high-temperature processing), and the inductor has a significant higher Q compared to when it is fabricated on a 4 μm thick SiO_2 -covered Si.

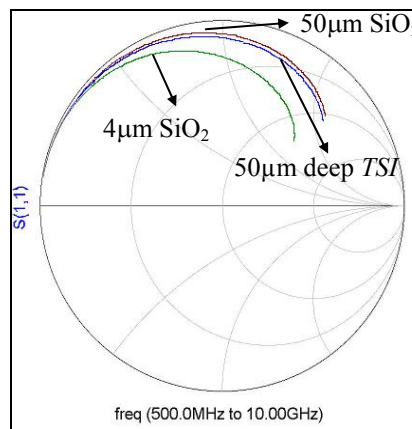
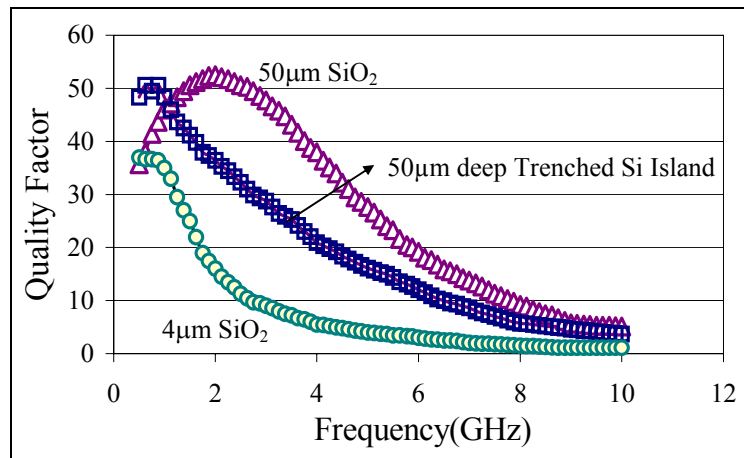


Figure 4-1. Comparison of (a) measured Q , and (b) S -parameter of inductors on OI, TSI and 4 μm SiO_2 -covered Si substrate. ($t_{\text{metal}}=25\text{-}30\mu\text{m}$, $w=60\mu\text{m}$, $d_{\text{out}}=825\mu\text{m}$).

At high frequencies, where the substrate loss is dominant, Q is improved significantly. From Fig. 4-1(a), it is also clear that the substrate loss has a considerable effect on the frequency of peak Q . To improve Q and increase the frequency of maximum Q , while keeping the process CMOS compatible, the depth of trenches should be increased.

4.2. Effect of Trench Depth

Figure 4-2 illustrates the role of the trench depth in reducing the substrate loss. The Q of a 1.07nH inductor on 40 μm deep Trenched Si Island is 4 \times higher than the similar design (with identical metal thickness) fabricated on 10 μm deep trenched-island ($Q_{40\mu\text{m}}=32$ @2.4GHz, $Q_{10\mu\text{m}}=7.5$ @2.4GHz).

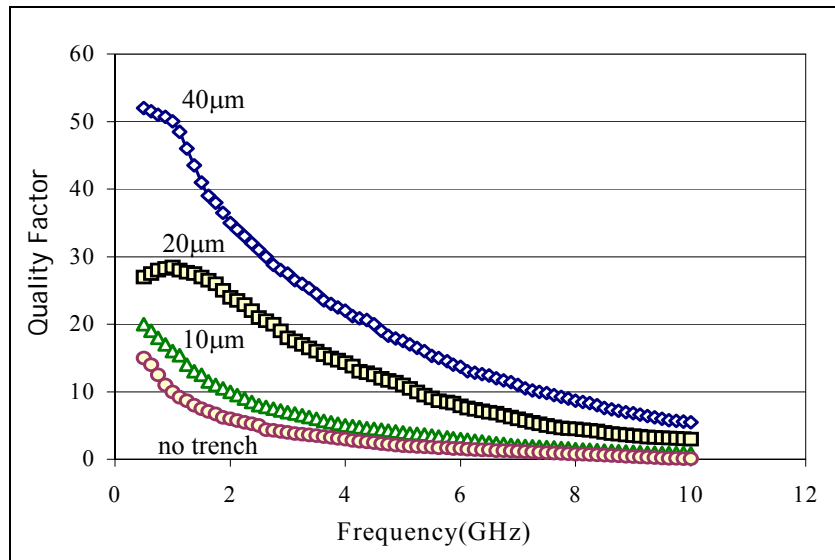


Figure 4-2. Measured Q vs. frequency showing dependency of Q on trench depth. ($t_{\text{metal}}=15\mu\text{m}$, $w=60\mu\text{m}$, $d_{\text{out}}=833\mu\text{m}$).

Similar to the inductors fabricated on thick oxide islands, there is a saturation point for Q versus the trench depth. Quality factor does not increase by increasing the trench depth further than the saturation depth. Measured data indicate an increase in Q with trench depth up to $90\mu\text{m}$. The saturation depth for inductors fabricated on *TSI* is more than the saturation thickness for inductors on *OI* and needs to be determined by fabrication.

4.3. Effect of Oxide Thickness

To identify the dependency of Q on the oxide thickness, identical inductors have been fabricated on

- 1) $50\mu\text{m}$ thick Oxide Islands (*OI*)
- 2) $4\mu\text{m}$ PECVD SiO_2 coated standard Si substrate ($10\text{-}20\Omega\cdot\text{cm}$)
- 3) $7.5\mu\text{m}$ PECVD SiO_2 coated standard Si substrate

Figure 4-3 depicts the effect of the oxide thickness on the measured Q of a 1.3nH inductor on thick *OI*. As can be seen, SiO_2 thickness has a significant effect on the frequency of the maximum Q as well as the Q -values at high frequencies.

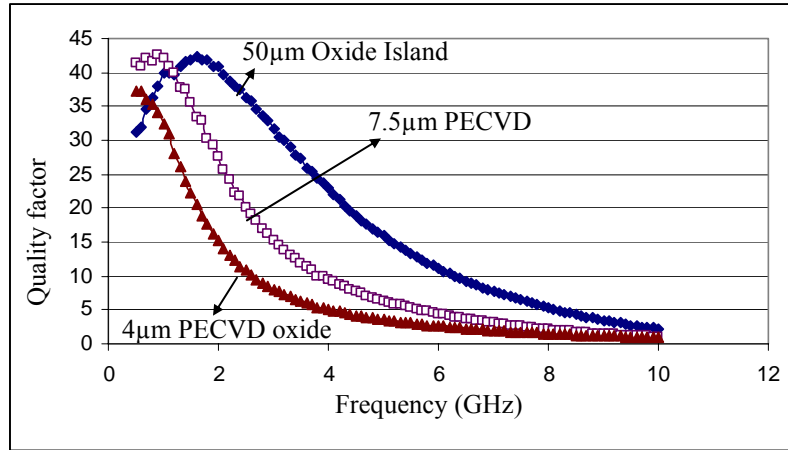
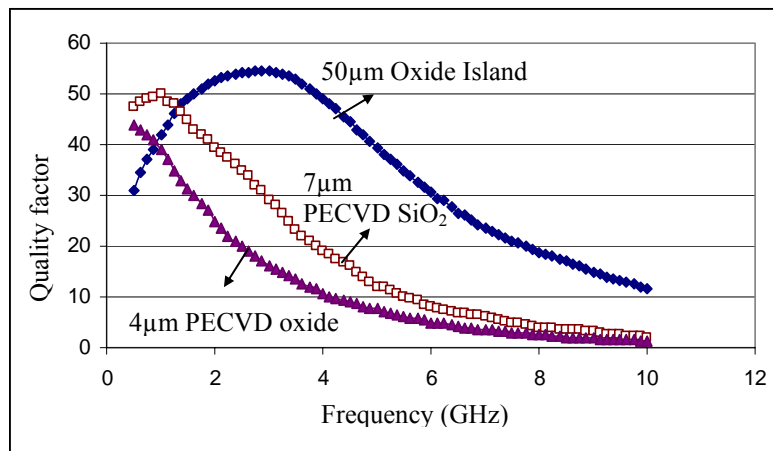
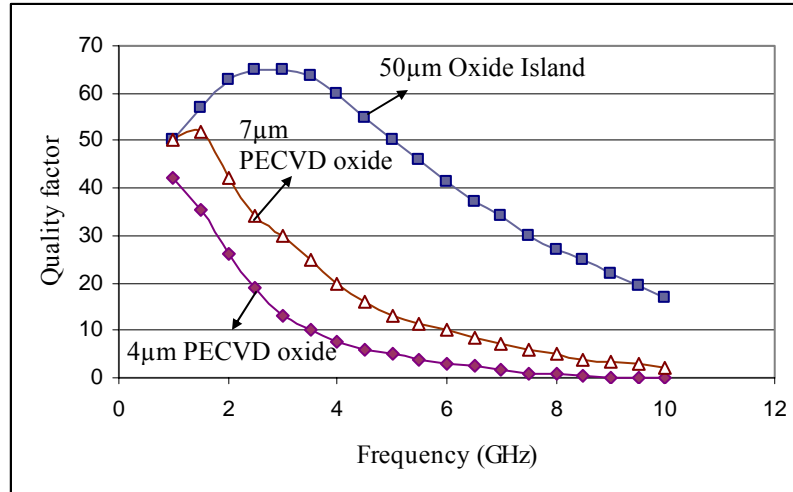


Figure 4-3. Quality factor vs. frequency, showing the dependency of Q on oxide thickness for a one-turn round spiral inductor ($w=60\mu\text{m}$, $t=30\mu\text{m}$, $d_{out}=833\mu\text{m}$ and $L=1.3\text{nH}$).

Figure 4-4(a) depicts the effect of the oxide thickness on the measured Q of a 0.9nH inductor on thick OI , indicating good agreement with simulation results (Fig. 4-4(b)).



(a)



(b)

Figure 4-4. (a) Measured and (b) simulated Q of a 0.9nH inductor with various oxide thicknesses ($t_{\text{metal}}=15\mu\text{m}$, $w=60\mu\text{m}$, $d_{\text{out}}=600\mu\text{m}$).

Nonetheless, measured Q of the inductor on $50\mu\text{m}$ thick OI is slightly different with the simulated values. This may come from the incomplete oxidation of Si bars as shown in Fig. 4-5. As can be seen, trenches are filled prior to the complete oxidation of Si due to the insufficient trench width.

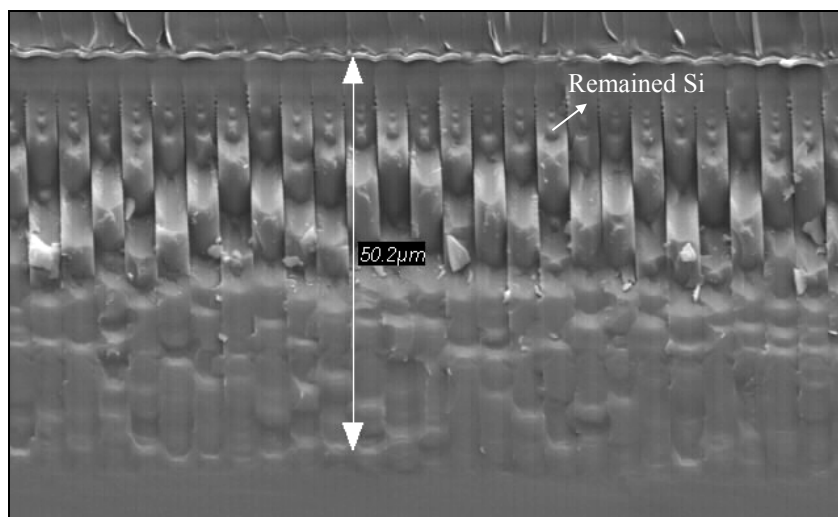


Figure 4-5. Cross-section SEM view of a $50\mu\text{m}$ thick OI , showing the incomplete oxidation of Si.

4.4. Effect of Trenched Area

Another result extracted from measurement is the negligible dependency of Q on the trenched island area. The change in Q is less than 10% (at 2.4GHz) if the trenched island area is extended beyond the Cu track area ($x > 0$ in Figure 4-6), alleviating the need for trenching the entire area beneath the inductor (Fig. 4-6).

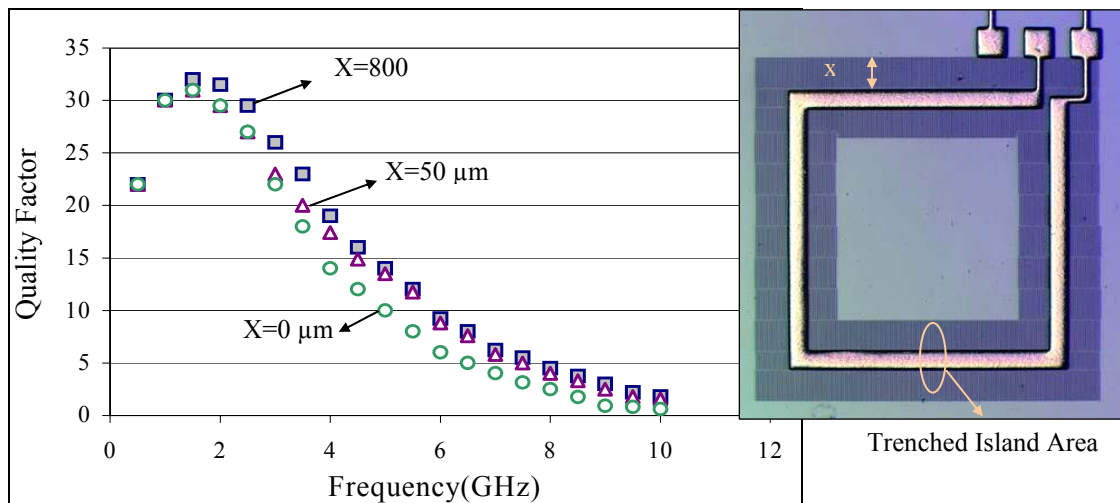


Figure 4-6. (Left) Measured Q of a one-turn inductor on TSI with various trenched island area, and (right) Microscope picture of the inductor showing the definition of x . ($t_{\text{metal}}=30\mu\text{m}$, $w_{\text{metal}}=100\mu\text{m}$, $d_{\text{out}}=1200\mu\text{m}$).

4.5. Effect of Metal Thickness

The Q vs. frequency plots for a one-turn Cu inductor with two different metal thicknesses is shown in Fig. 4-7, confirming improvement in coplanar inductor Q for metal

thicknesses in excess of $5 \times$ skin depth at lower frequencies where metal loss is the dominant Q -limiting mechanism.

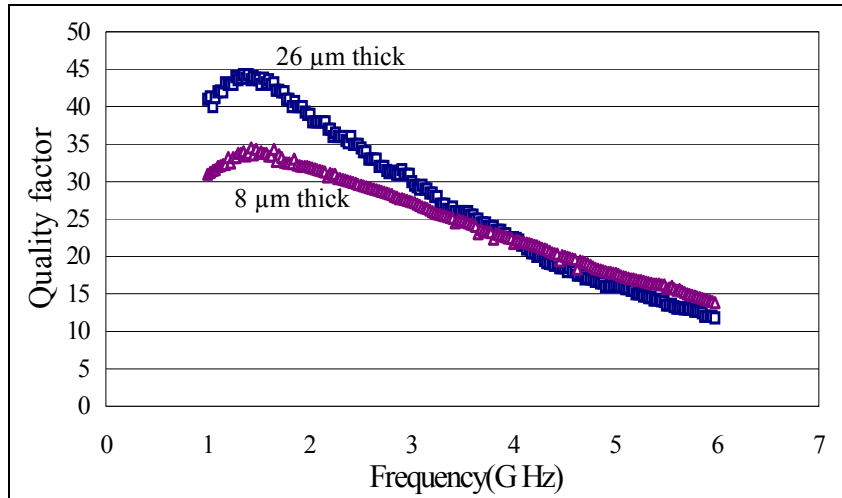


Figure 4-7. Measured Q of a one-turn inductor on TSI with different metal thicknesses.

4.6. Enhanced Design Test Results

To further increase the Q and the frequency at which maximum Q occurs, improved design of inductors have been implemented using a revised mask on 70-100 μm deep TSI and the width of the Si bars has been reduced to smaller values (1.5 μm instead of 2 μm) by increasing the undercut in RIE. Smaller size inductors (smaller outer diameter) with optimized metal width exhibit higher Q 's and are used on the new mask. As a result, the maximum Q has been increased from 23 to 71 at 5GHz for a one-turn inductor fabricated on TSI (compare Fig. 4-4 with Fig. 4-8). However, smaller outer diameter, which resulted in Q -improvement, has the draw back of getting smaller inductance value.

Figure 4-8 shows the embedded and de-embedded Q and inductance of a one-turn round inductor fabricated on 70 μm deep TSI. As it is shown, Q is over 50 in the 5-10GHz range with a maximum of 70.6 at 8.75GHz. The self resonance frequency of this inductor is much higher than 10GHz.

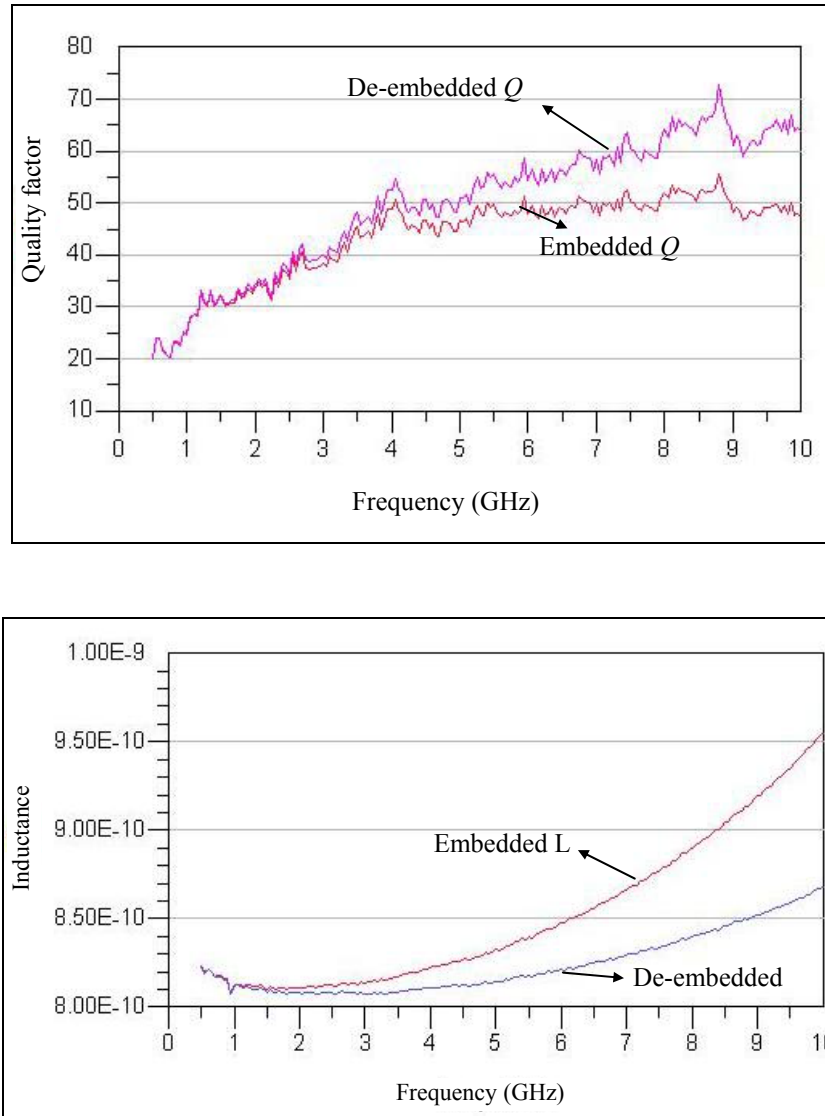


Figure 4-8. Measured (upper) Q , and (lower) inductance of a one-turn inductor on TSI ($t_{\text{metal}}=20\mu\text{m}$, $w=50\mu\text{m}$, $d_{\text{out}}=500\mu\text{m}$, $\rho=100\Omega\text{cm}$).

The measured Q of a 0.9nH inductor on $70\mu\text{m}$ deep TSI is shown in Fig. 4-9. It is notable that inductors fabricated on TSI have high embedded- Q in contrast to the suspended inductors reported in literature (Fig. 4-9) [15]. This is because parasitic capacitances of pads are reduced simultaneously by reduction of the substrate loss underneath them through trenching the Si.

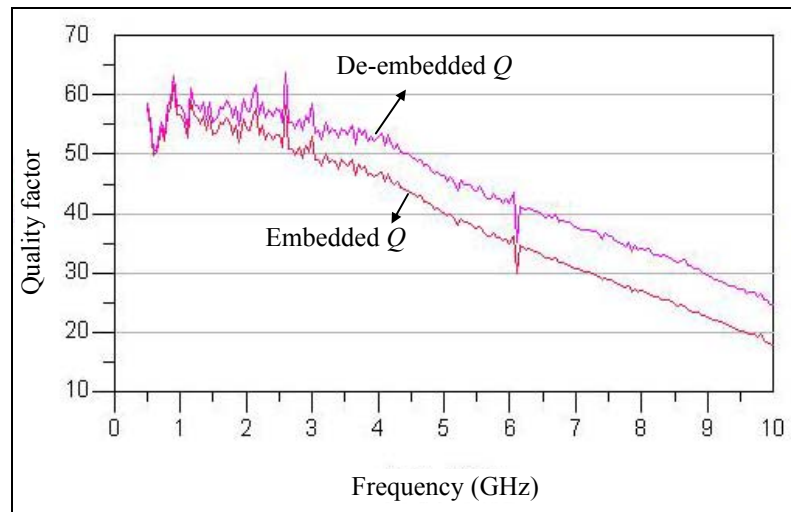


Figure 4-9. Measured Q of a 0.9nH inductor on TSI ($t_{\text{metal}}=20\mu\text{m}$, $w=60\mu\text{m}$, $d_{\text{out}}=600\mu\text{m}$, trench depth= $70\mu\text{m}$).

4.6.1. Avatrel Trench refilled

As it was discussed in section 2.3, the alternate low-temperature method of reducing the substrate loss is disrupting the current path by making trenches in Si and subsequently refilling them with Avatrel Polymer. Figure 4-10 shows the Q of a 0.9nH inductor on Avatrel refilled $90\mu\text{m}$ deep trenches, showing a maximum Q of 60 at 1.75GHz . The inductor is identical to the one in Figure 4-4 (metal width= $60\mu\text{m}$, $d_{\text{out}}=600\mu\text{m}$), and for

comparison the two plots are combined in Fig. 4-11. As it can be seen in this figure, $Q_{substrate}$ in the two cases are almost equal, resulting in similar Q values at high frequencies ($f \geq 4\text{GHz}$).

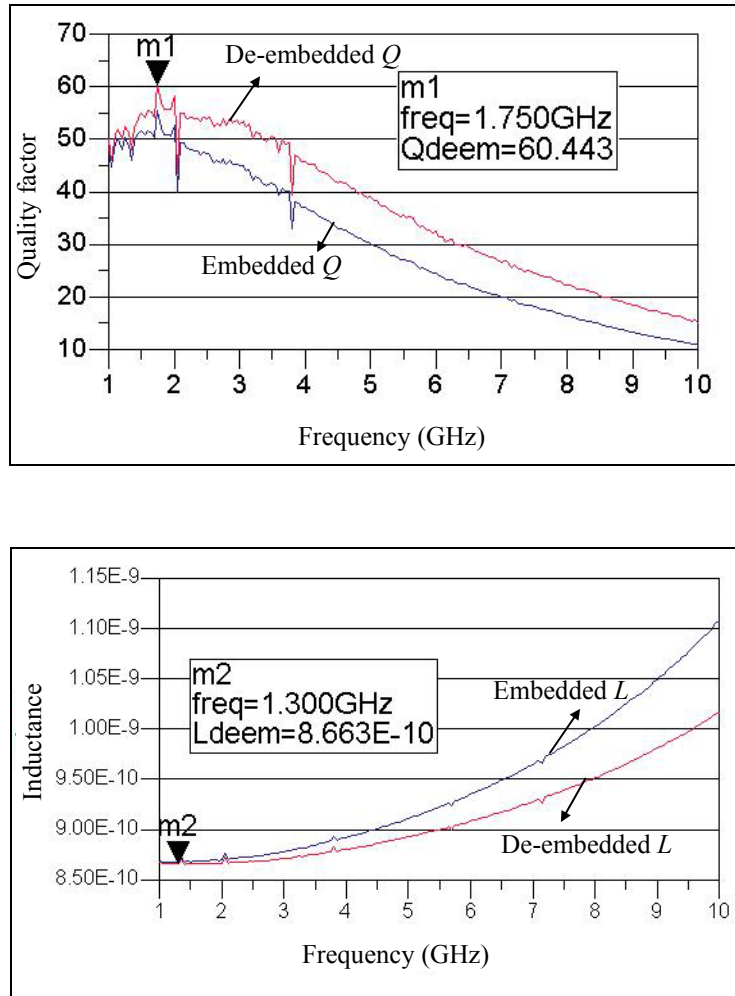


Figure 4-10. Measured (upper) Q and (lower) L of a one-turn inductor on $100\mu\text{m}$ deep Avatrel refilled Trenched Si ($w=60\mu\text{m}$, $d_{out}=600\mu\text{m}$, $\rho=10\text{-}20\Omega\text{.cm}$).

The inductor fabricated on $90\mu\text{m}$ deep Avatrel refilled trenched Si has a slightly improved performance over the identical one fabricated on $50\mu\text{m}$ deep TSI at higher

frequencies ($f > 6\text{GHz}$ in Fig. 4-11). The Q improvement has two reasons. First, the trench depth is increased to $90\mu\text{m}$, and second, the Avatrel polymer is a better dielectric in terms of having lower permittivity and loss tangent compared to PECVD silicon dioxide.

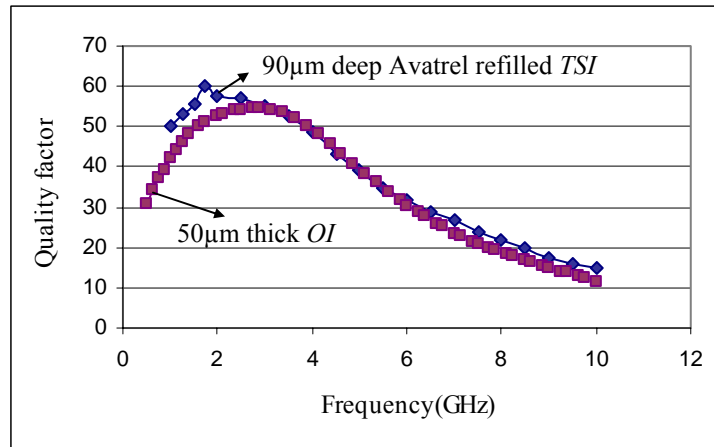


Figure 4-11. Comparison between measured Q of a 0.9nH inductor fabricated on OI and Avatrel refilled TSI.

Figures 4-12 and 4-13 compare the effect of trench depth on the Q when the substrate is coated with a thick layer of Avatrel. In Fig. 4-12, the trench depth is $90\mu\text{m}$ and trenches are filled with Avatrel. The thickness of the Avatrel on the surface of the refilled substrate is negligible (as it was shown in Fig. 3-11). The inductor in Fig.4-13, on the other hand, is fabricated on a $50\mu\text{m}$ deep trenched refilled island. The thickness of Avatrel layer covering the refilled trenches is about $20\mu\text{m}$, as shown in Fig. 4-14. The peak Q is higher for the inductor fabricated on $90\mu\text{m}$ deep trenched Si without extra Avatrel coating. Comparing these two figures demonstrates that the substrate loss cannot be effectively reduced by merely coating it with a low-K dielectric.

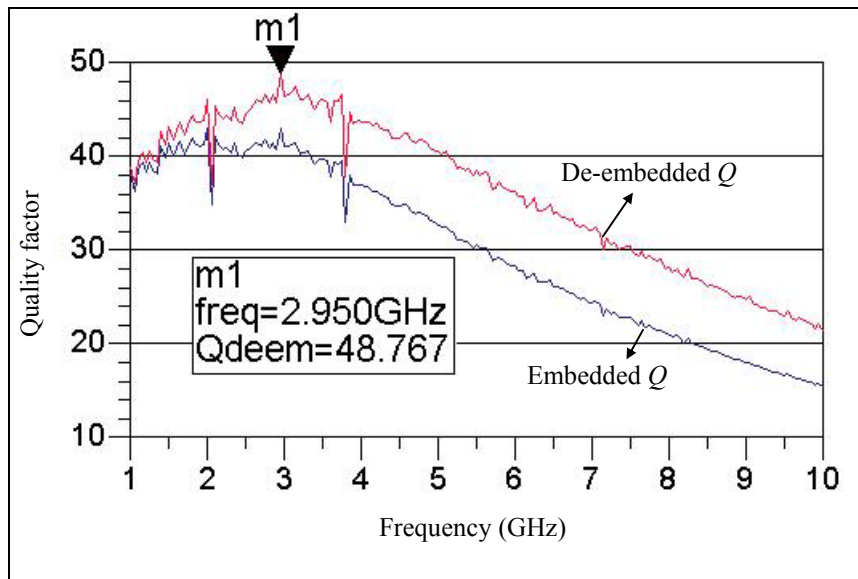


Figure 4-12. Measure Q of a $0.8nH$ inductor on $90\mu m$ deep Avatrel refilled TSI.

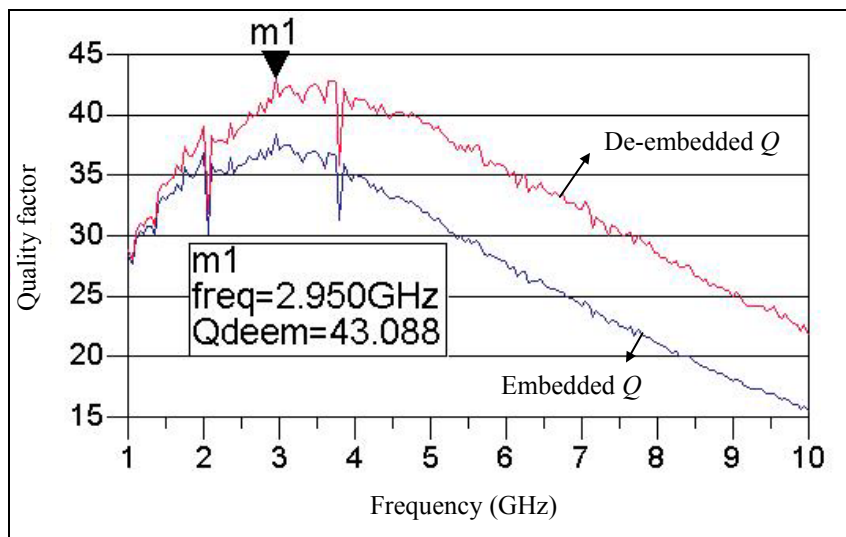


Figure 4-13. Measure Q of a $0.8nH$ inductor on $50\mu m$ deep Avatrel refilled TSI coated with $20\mu m$ thick Avatrel layer.

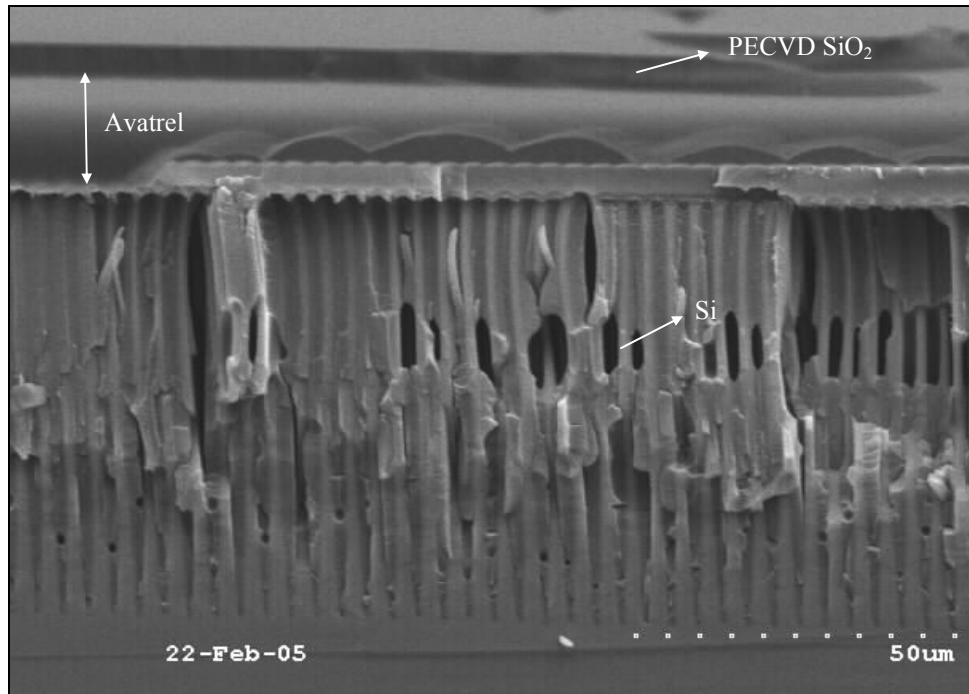


Figure 4-14. Cross-section SEM view of a TSI filled with Avatrel, and coated with a 20µm thick layer of Avatrel and 4µm thick layer of PECVD SiO₂.

Figures 4-15 and 4-16 illustrate the de-embedded Q of a 1nH inductor fabricated on 70µm deep *TSI* (covered with SiO₂) and 90µm deep Avatrel refilled trenched Si, respectively. Quality factor of the inductor on *TSI* is higher by ~30% at 4GHz compared to when it is fabricated on Avatrel refilled trenched Si (Q on *TSI*=55 @ 4GHz, and Q on Avatrel =50@4GHz).

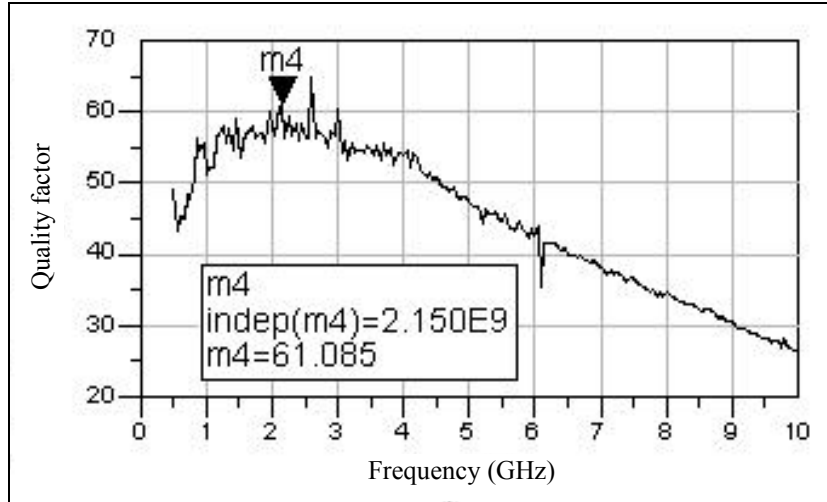


Figure 4-15. Extracted de-embedded Q of a 1nH inductor on $70\mu\text{m}$ deep TSI ($w=60\mu\text{m}$, $d_{\text{out}}=600\mu\text{m}$, $\rho=100\Omega\cdot\text{cm}$).

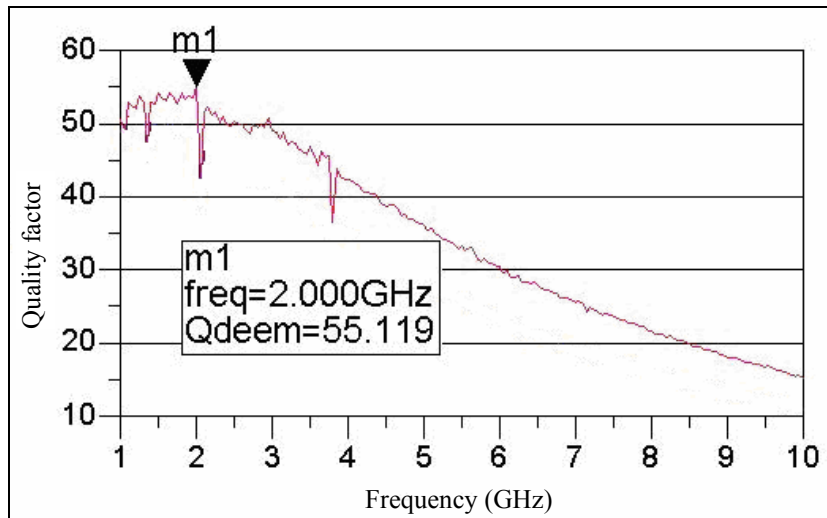


Figure 4-16. De-embedded Q of a 1nH inductor on $90\mu\text{m}$ deep Avatrel refilled trench Si ($w=60\mu\text{m}$, $d_{\text{out}}=600\mu\text{m}$, $\rho=10\Omega\cdot\text{cm}$).

4.6.2. Thick PECVD SiO₂

Although deposition of a thick SiO₂ layer might seem an easy way of reducing the substrate loss, there are some issues associated with it:

- 1) The deposition rate of PECVD SiO₂ is about 1 μ m per 15min. Therefore, it takes about 5hours to deposit a 20 μ m thick SiO₂ layer. Whereas, etching 100 μ m deep trenches using Bosch process takes about 1hour.
- 2) Thick layer of SiO₂ is highly stressed and can crack or peeled off. In addition, it induces stress to the substrate and makes the substrate prone to fracture.

Despite these facts and for the sake of comparison, inductors have also been fabricated on a 20 μ m thick SiO₂ coated standard Si substrate. Figure 4-17 depicts Q of a 0.9nH inductor fabricated on a 20 μ m thick PECVD SiO₂ covered standard Si substrate, showing good agreement with SONNET simulation result (Fig. 4-18).

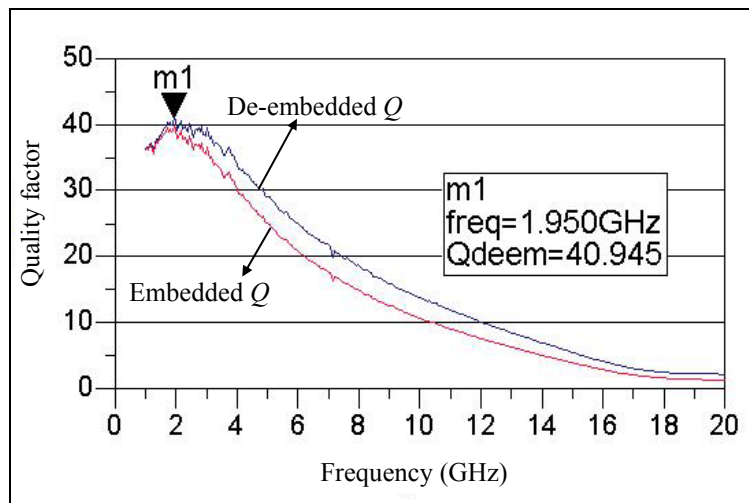


Figure 4-17. Measured Q of a 0.9nH inductor on a 20 μ m thick SiO₂ coated Si substrate ($w=50\mu$ m, $d_{out}=50\mu$ m).

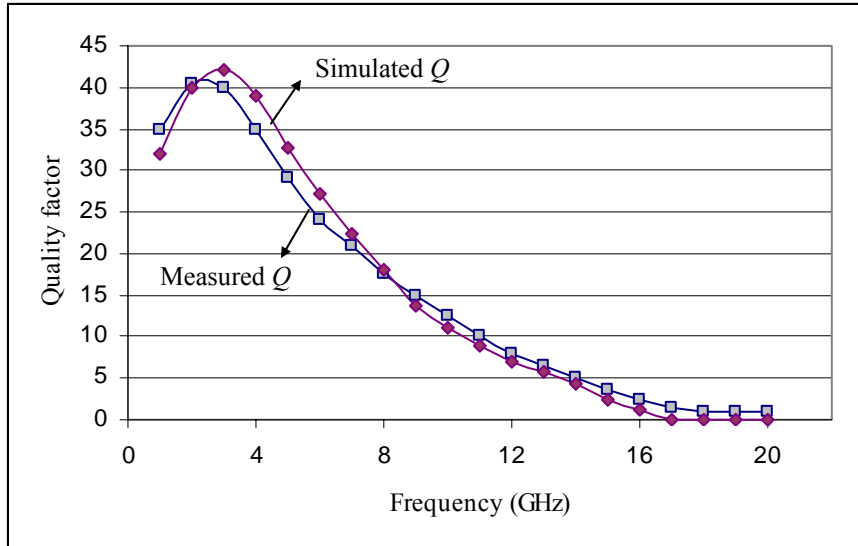


Figure 4-18. Simulated and measured Q of a 0.9nH inductor on $20\mu\text{m}$ thick SiO_2 coated $10\Omega\cdot\text{cm}$ Si substrate.

Quality factor of a 1nH inductor on $20\mu\text{m}$ thick SiO_2 substrate is shown in Fig. 4-19. This inductor is identical to the one in figures 4-15 and 4-16.

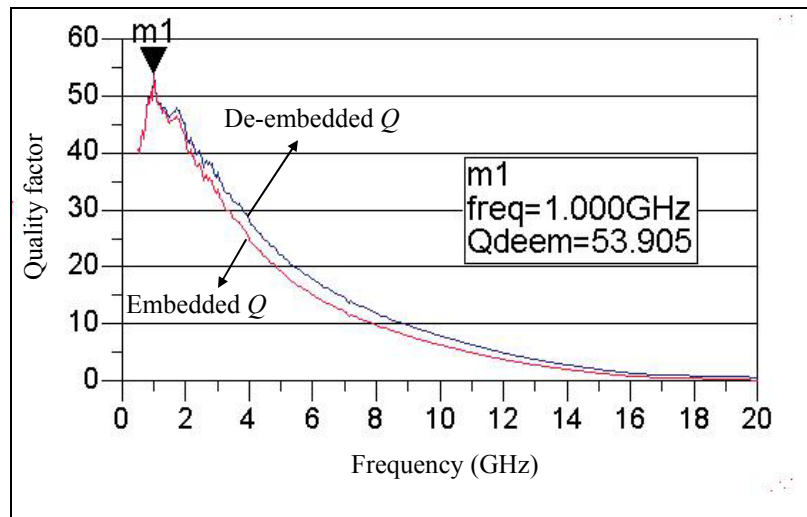


Figure 4-19. Measured Q of a 1nH on $20\mu\text{m}$ thick SiO_2 coated $10\Omega\cdot\text{cm}$ Si substrate.

Comparing the measured Q of identical inductors on different type of micromachined substrates reveals that *TSI* (without refilling) presents the lowest-loss compared to other low-temperature micromachined Si substrates (Fig. 4-20).

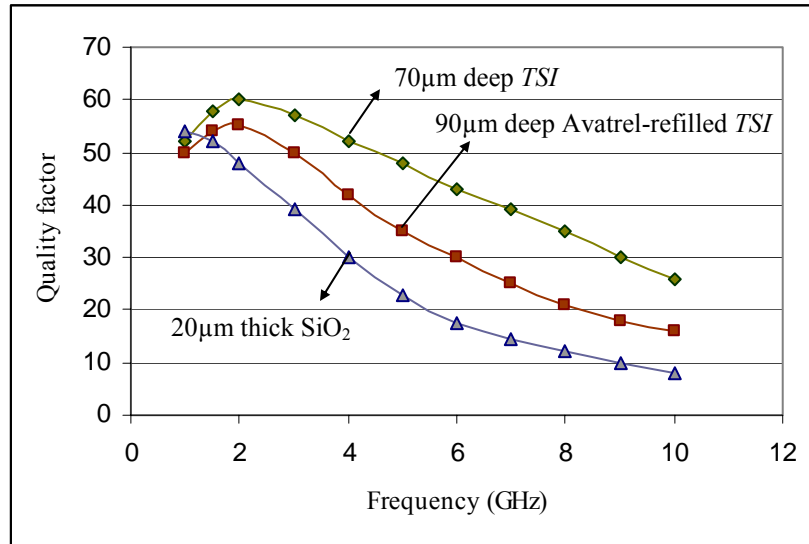


Figure 4-20. Measured Q of a $1nH$ inductor on $70\mu m$ deep *TSI*, $20\mu m$ thick PECVD SiO_2 coated Si, and $90\mu m$ deep Avatrel refilled *TSI* substrate.

4.7. High-turn inductors

High-turn inductors ($n > 1$) suffer from high metal loss, due to the fact that the first metal layer used for routing is only $1.5\mu m$ thick and is located between two SiO_2 layers. For this reason, Q of high-turn inductors is lower than the Q of one-turn inductors. Figures 4-21 to 4-24 are the measured Q 's of some high-turn inductors on different types of micromachined substrates, showing the highest Q of 35 (@ $3.25GHz$) for a 1.5-turn inductor on $20\mu m$ thick SiO_2 coated Si substrate. Although the Q 's presented here are higher than what can be achieved on standard Si substrates due to the reduction of

substrate loss, there is still room to improve this factor by reducing the number of turns to one at the cost of chip area or by increasing the thickness of the first metal layer.

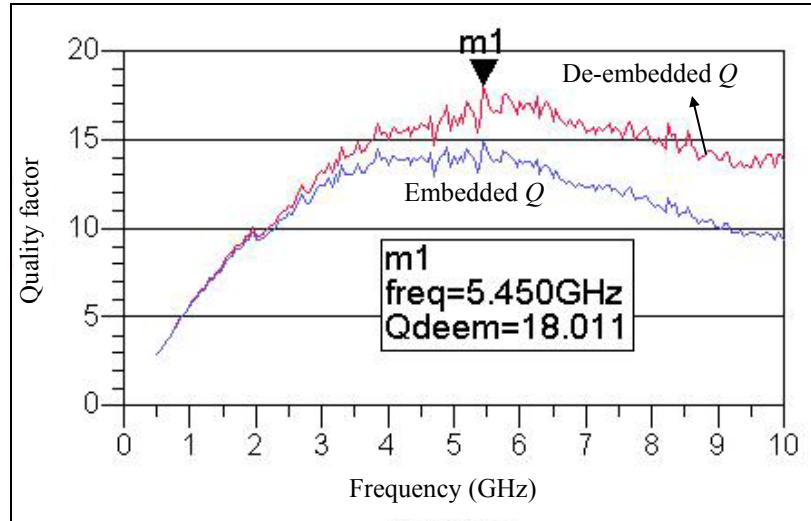


Figure 4-21. Measured Q of a 1.1nH inductor on TSI ($t_{\text{metal}}=1.5\mu\text{m}$, $n=1.5$, $w=40\mu\text{m}$, $s=20\mu\text{m}$, and $d_{\text{out}}=300\mu\text{m}$).

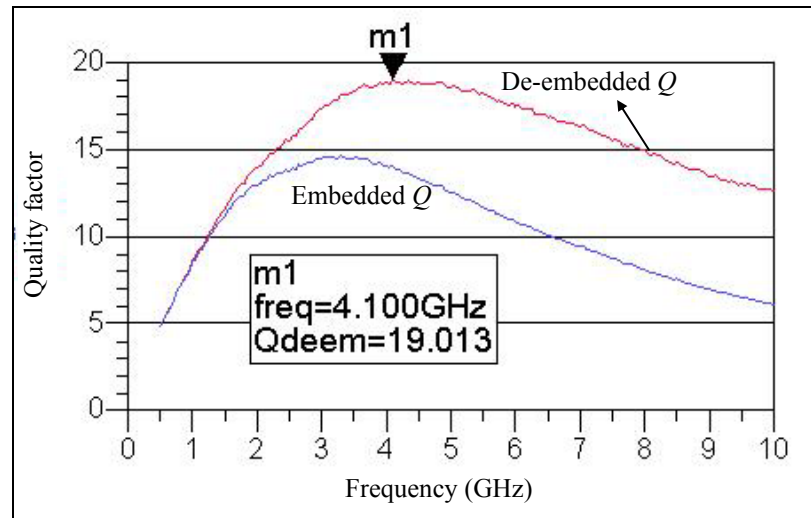


Figure 4-22. Measured Q of a 1.3nH inductor on TSI ($t_{\text{metal}}=1.5\mu\text{m}$, $n=1.5$, $w=30\mu\text{m}$, $s=20\mu\text{m}$, and $d_{\text{out}}=300\mu\text{m}$).

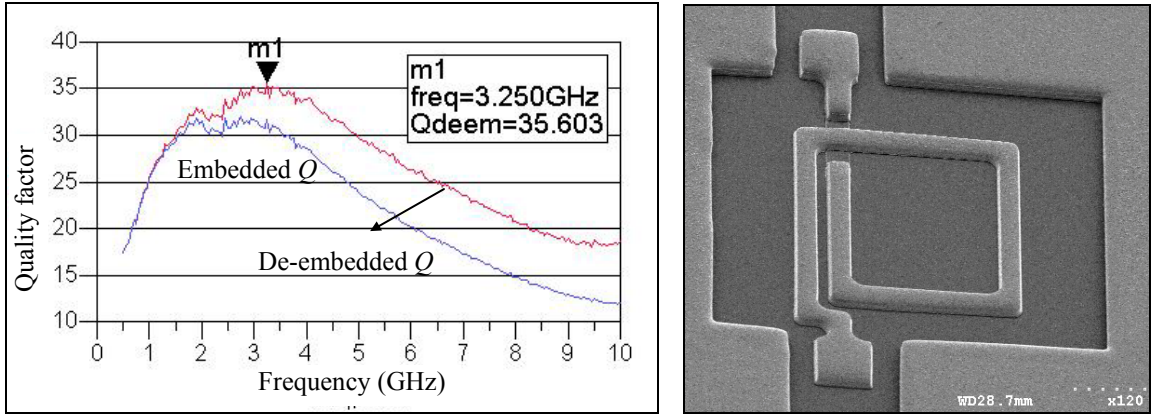


Figure 4-23. (Left) Measured Q of a 1.2nH inductor on $20\mu\text{m}$ thick PECVD SiO_2 , (right) SEM picture of this inductor ($t_{\text{metal}}=1.5\mu\text{m}$, $n=1.5$, $w=30\mu\text{m}$, $s=20\mu\text{m}$, and $d_{\text{out}}=300\mu\text{m}$).

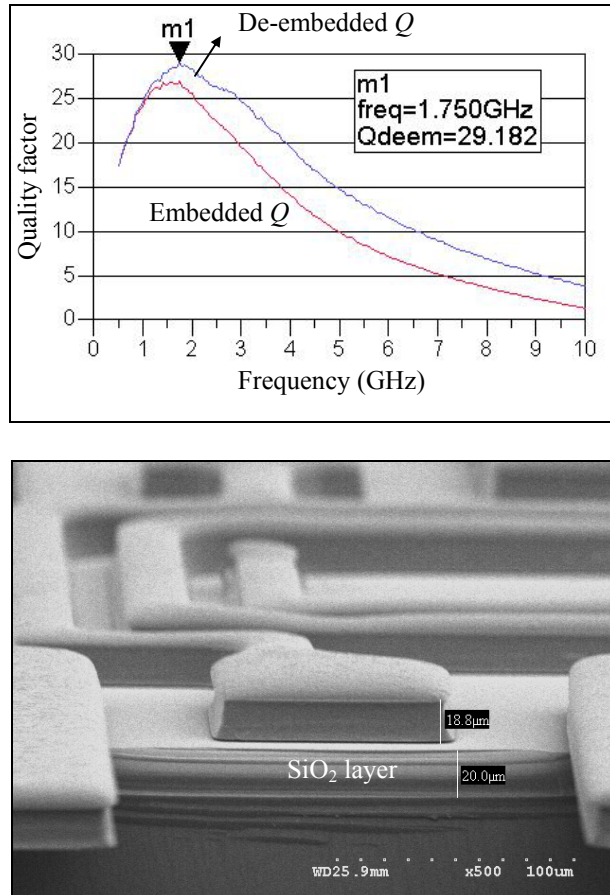


Figure 4-24. (Upper) Measured Q of a 3.3nH inductor on $20\mu\text{m}$ thick PECVD SiO_2 , (lower) SEM picture of the inductor ($t_{\text{metal}}=1.5\mu\text{m}$, $n=2.5$, $w=20\mu\text{m}$, $s=20\mu\text{m}$, and $d_{\text{out}}=400\mu\text{m}$).

4.8. Modeling and Parameter Extraction

Inductors fabricated on *TSI* and *OI* have been modeled using the equivalent electrical model shown in Fig. 2.2. The series resistance is extracted from co-planar model and has an excellent match with the measured data. Figure 4-25 shows the measured and modeled Q of a 1nH inductor on *TSI*.

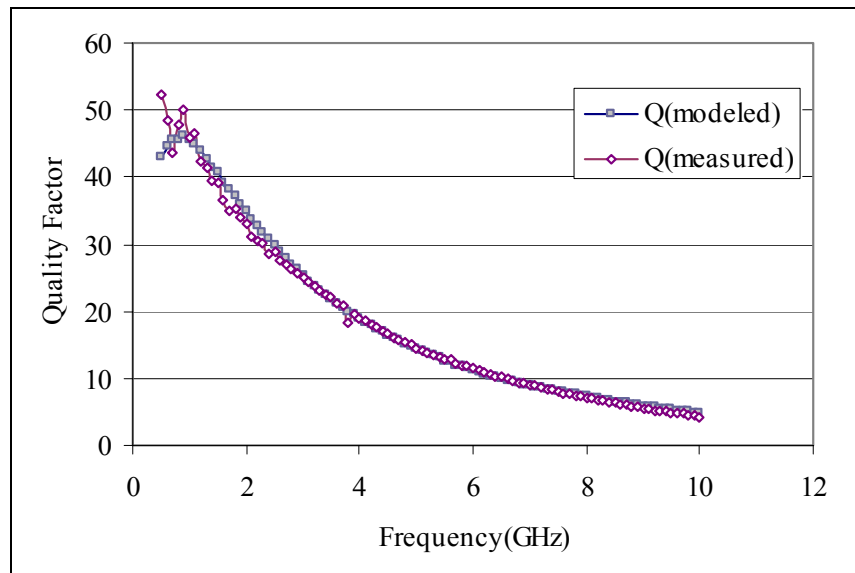
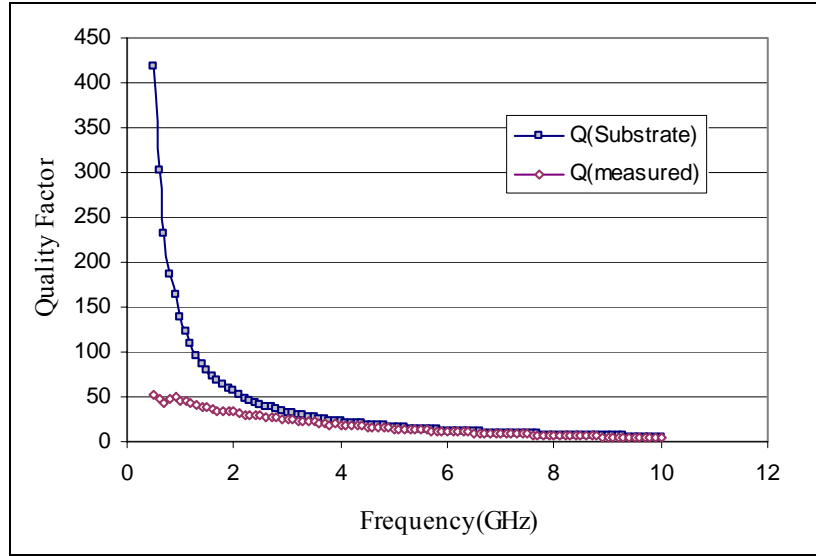
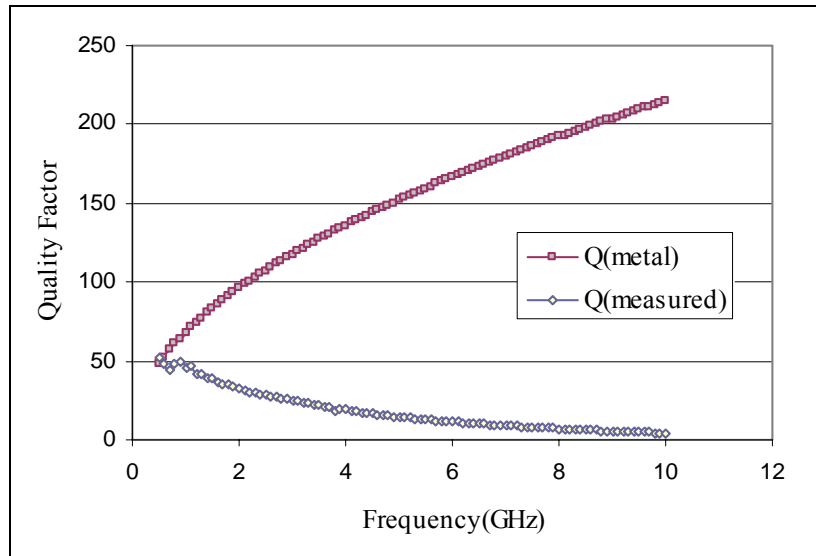


Figure 4-25. Measured and modeled Q vs. frequency of a 1.04nH inductor on *TSI*.

The inductance value is extracted from the measured L at lower frequencies assuming the substrate loss is not present at this frequency range. Figure 4-26 shows the contribution of the metal and the substrate loss on the measured Q , demonstrating that the metal loss is the dominant loss mechanism at lower frequencies.



(a)

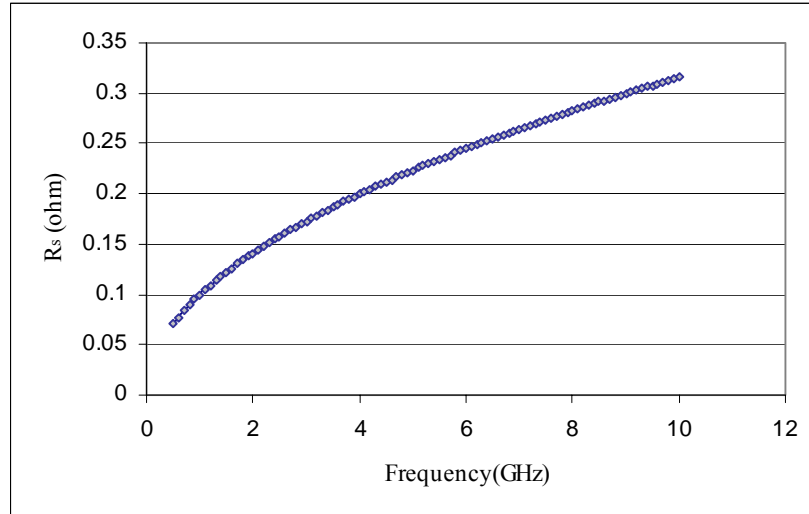


(b)

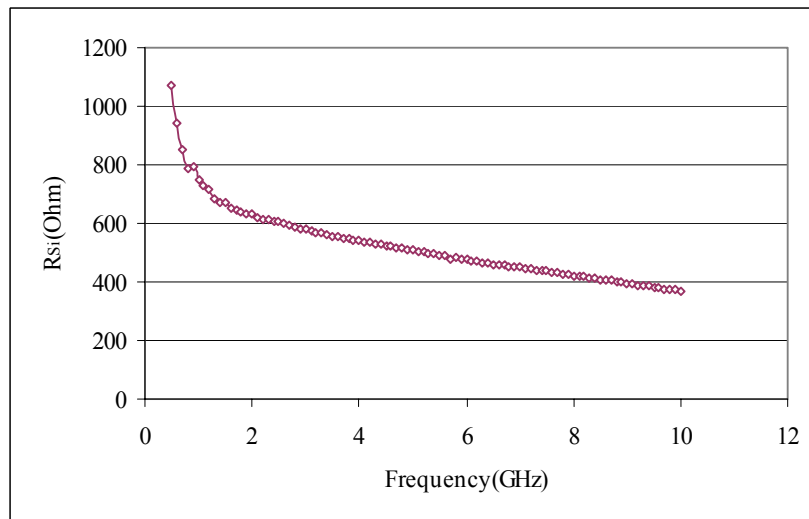
Figure 4-26. (a) Extracted $Q_{\text{substrate}}$, and (b) Q_{metal} of a 1.04nH inductor on *TSI*.

To better understand the effect of trenching the Si on the substrate loss, the equivalent *TSI*'s resistivity has been extracted from the measured data and is plotted in Fig. 4-27(b).

Table 4-1 summarizes the modeled parameter of the inductor fabricated on *TSI*.



(a)



(b)

Figure 4-27. Modeled (a) metal resistance, and (b) substrate resistance of the inductor shown in Fig. 4-25.

Table 4-1. Extracted equivalent parameters of a 1nH inductor fabricated on TSI

f (GHz)	R_s (Ω)	L_s (nH)	R_{si} (Ω)	C_{si} (fF)	C_{ox} (pF)
1	0.0998	1.08	747.65	86.64	0.887
2.4	0.1547	1.08	604.326	77.26	0.887
6	0.2466	1.08	475.74	53.06	0.887

Identical structure on *OI* exhibits lower substrate parasitic (R_{si} and C_{si}) shown in the table below. Modeled Q of this inductor is shown in Fig. 4-28.

Table 4-2. Extracted equivalent parameters of a 0.9nH inductor fabricated on *OI*.

f (GHz)	R_s (Ω)	L_s (nH)	R_{si} (Ω)	C_{si} (fF)	C_{ox} (pF)
1	0.13982	0.883	6909.688	5.963	0.887
2.4	0.21660	0.883	2270.26	5.5782	0.887
6	0.34249	0.883	1168.02	5.0564	0.887

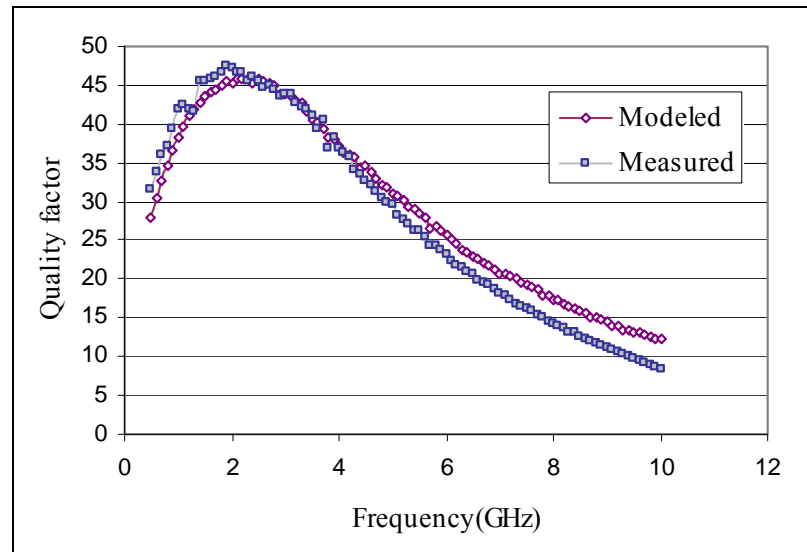


Figure 4-28. Measured and modeled Q vs. frequency of a 0.9nH inductor on *OI*.

CHAPTER V

CONCLUSION AND FUTURE DIRECTIONS

This thesis introduced a new implementation of high- Q integrated Cu inductors on CMOS-grade Si substrates using a fully CMOS-compatible process. A new fabrication sequence has been used to reduce the loss of Si substrate at RF frequencies by trenching the Si. Two approaches were taken to cover the trenches and make a smooth surface: 1) High aspect-ratio (30:1) trenches were bridged-over by depositing a thin layer (3 μm) of SiO_2 at 300°C, and 2) trenches were refilled by spin-coating of Avatrel Polymer. Metal loss of inductors was reduced by electroplating thick (~20 μm) Cu layer.

Several inductors were designed and simulated using SONNET simulation tool. Inductor parameters were optimized to have high Q and small size. For simplicity, inductors were simulated on 4 μm thick SiO_2 coated standard Si substrate, as simulating the behavior of TSI is computationally intensive. A one-turn round inductor with metal width of 50 μm and outer diameter of 500 μm exhibits the highest- Q of 28.5 at 2-10GHz frequency range (assuming the substrate is 10 $\Omega\cdot\text{cm}$ and the thickness of SiO_2 layer is 4 μm). Quality factor and inductance value of simulated inductors is shown in the Appendix B.

The inductors were fabricated on several micromachined standard Si substrates including Oxide Islands, Trenched Si Islands, Avatrel refilled trenched Si and thick PECVD SiO_2 coated Si. Comparing the measured Q of identical inductors on different type of micromachined substrates revealed that the TSI (without refilling) exhibits the lowest-loss

compared to other low-temperature micromachined Si substrates. Measurement results indicate a significant improvement in the Q compared to the inductors fabricated on the conventional low-resistivity Si substrates. A 0.8nH Cu inductor fabricated on Trenched Silicon Islands exhibits high Q of 71 at 8.75 GHz and self resonance frequency of over 15GHz. Whereas, the identical inductor fabricated on a 20 μ m thick SiO₂ coated Si substrate has a maximum Q of 41 at 1.95GHz. A 0.9nH inductor fabricated on Avatrel refilled trenched Si substrate has a high Q of 60.4 at 1.75GHz. Test results show that the same inductor fabricated on 50 μ m deep Oxide Island has a similar Q at high frequencies ($f \geq 4$ GHZ). Therefore, a 90 μ m deep Avatrel refilled trenched Si substrate is the low-temperature (300°C) processed alternative for a 50 μ m deep Oxide Island (processing temperature =1100°C).

Finally, the electrical equivalent circuit of inductors on Trenched Si Islands as well as other substrates was derived. The series resistance was extracted using isolated strip formula. Modeled Q showed an excellent agreement with measured results.

To further increase the inductor Q , the trench depth should be increased. The saturation behavior of the Q versus the trench depth was not observed with trench depth up to 90 μ m and needs to be determined in later fabrications.

Also, the *TSI* coated with a low-K dielectric is expected to exhibit lower loss compared to the *TSI* coated with SiO₂ with the dielectric constant of 3.9. For instance, the substrate shown in Fig. 5-1 is a 90 μ m deep *TSI* coated with a 18 μ m thick layer of Avatrel

polymer($\epsilon_r=2.5$) and has a lower loss compared to the *TSI* with no Avatrel over-coat. Fabrication of inductors on this type of substrate is not yet complete.

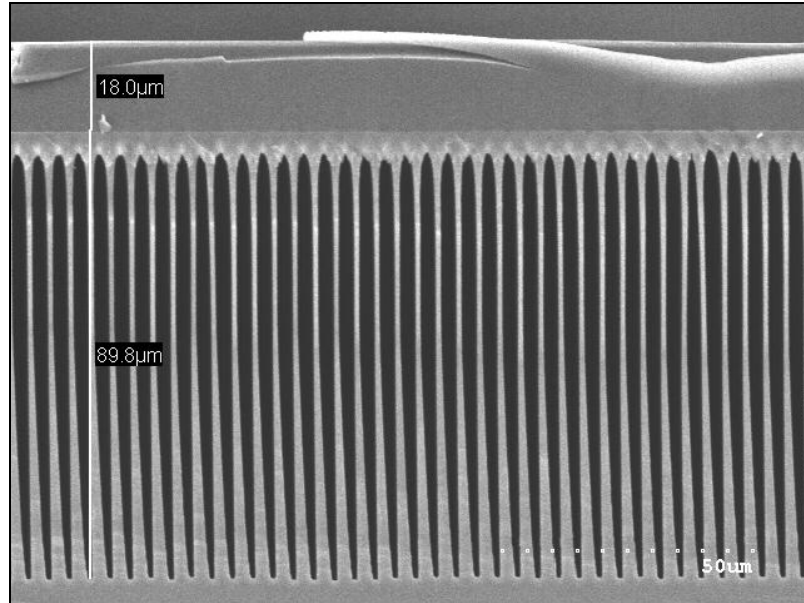


Figure 5-1. Cross-section SEM view of a 90µm deep TSI coated with a 18µm thick layer of low-K dielectric.

A new mask set was also designed to improve Q of the inductors and reduce the inductor size. The trench mask as seen in Fig. 5-2 was modified to have trenches perpendicular to the inductor traces to further reduce the substrate loss. The trench profile as it can be seen is similar to the patterned ground shield profile. Inductors fabricated on perpendicularly trenched Si substrate have not been yet measured to see the effect of the trench direction on the reduction of the substrate loss.

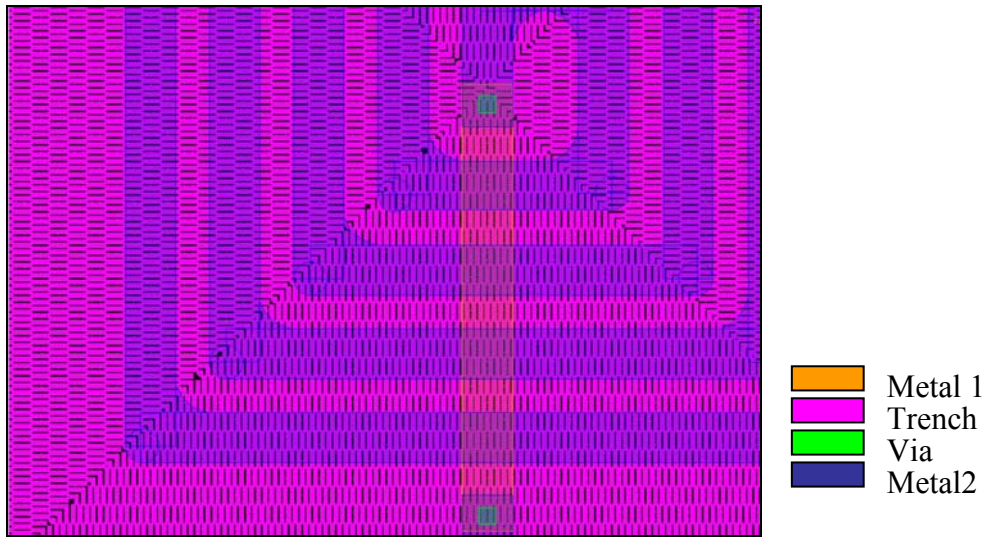


Figure 5-2. Snap-shot of a four-turn inductor mask with trenches perpendicular to the metal trace.

APPENDIX A

PROCESS FLOW

Mask 1. SI TRENCHES

Process step	Process Description	Recipes and Comments
1	Clean wafer	Acetone, Methanol, DI water, dry N ₂ gun
2	Dehydration	3 min at 115°C on hotplate
3	Spin/bake HMDS and Spin Photo-Resist	Cover 1/3 of the wafer with HMDS: 4000rpm, 1000rpm/s, 20 sec. Bake HMDS 115°C for 30 sec. Cover 2/3 of wafer with 1813: 1000rpm, 1500rpm/s, 5 sec. 2000rpm, 500r/s, 30 sec.
4	Soft bake	115°C for 1 min on hotplate
5	Exposure	I-line, intensity 20mJ/sec, vacuum contact, with 25µm alignment gap, 8sec.
6	Develop	MF-319 developer for about 1min Dip in DI water for 1min Wash with DI water
7	Dehydration and bake	dry N ₂ gun , bake 5 min at 115°C on hotplate
8	DRIE	Using STS ICP machine to etch 90um of Si for 1hour
9	Strip	4×30sec in Asher

Mask 2. FIRST METAL LAYER

Process step	Process Description	Recipes and Comments
1	Clean wafer	Acetone, Methanol, DI water, dry N ₂ gun
2	Dehydration	3 min at 115°C
3	SiO ₂ deposition	Using UNAXIS PECVD, Pressure: 950mTorr SiH ₄ : 500sccm N ₂ O :500sccm

		He :560sccm Deposition rate: 1µm/15min RF Power: 65 W Temperature: 300°C
4	Clean wafer and Dehydrate	Acetone, Methanol, DI water, dry N ₂ gun, 3 min at 115°C
5	Spin/bake HMDS Spin Photo-Resist	Cover 1/3 of the wafer with HMDS: 4000rpm, 2000rpm/s, 20 sec. Bake HMDS 115°C for 30 sec. Cover 2/3 of wafer with AZ 4620: 300rpm, 1500rPM/s, 5 sec. 1500rpm, 500rpm/s, 40 sec.
6	Soft bake	80° C ramp to 115°C for 4 min on hotplate
7	Exposure	Using MA-6, I-Line, hard contact, with 25µm alignment gap, 160mJ exposure.
8	Develop	354 developer for 4min
9	Hard bake	115°C for 3 min on hotplate
10	1 st Metal layer deposition	Using CVC E-beam evaporator Cr/Cu/Cr: 300A°/15000A°/300A° Deposition rate: 3 A°/sec-6.5 A°/sec-3 A°/sec
11	Lift-off	Microposit remover 1112 at 80°C, until resist cracks, Acetone in Ultrasonic bath until resist is completely pilled off.
12	Clean wafer	Aceton, Metanol, DI water to remove any metallic residues, Dry N ₂ gun

Mask 3. SILICON DIOXIDE ETCH

Process step	Process Description	Recipes and Comments
1	Clean wafer	Acetone, Methanol, dry N ₂ gun
2	Dehydration	3 min at 115°C
3	SiO ₂ deposition	Using UNAXIS PECVD, 3µm thick Pressure: 950mTorr SiH ₄ : 500sccm N ₂ O :500sccm He :560sccm Deposition rate: 1µm/15min

		RF Power: 65 W Temperature: 300°C
4	Clean wafer	Acetone, Methanol, dry N ₂ gun
5	Dehydration	3 min at 115°C
6	Spin/bake HMDS and Spin Photo-Resist	Cover 1/3 of the wafer with HMDS: 4000rpm, 2000rpm/s, 20 sec. Bake HMDS 115°C for 30 sec. Cover 2/3 of wafer with SPR220: 1500rpm, 500rpm/sec, 5 sec. 3000rpm, 500rpm/sec, 30\5 sec.
7	Soft bake	115°C for 2 min on hotplate
8	Exposure	Using MA-6, I-Line, hard contact, with 25µm alignment gap, 480mJ exposure.
9	Develop	MF-319 developer for 2 min
10	Bake	115°C for 20min on hotplate
11	RIE	Using Plasma therm ICP 25min, etch rate: 1.1µm/sec RF1 power: 100W RF2 power: 250W Pressure: 5mTorr H ₂ flow: 2sccm CF ₄ : 20sccm
12	BOE Dip	Place into BOE: H ₂ O(1:2) for 4min
13	Strip	In 1112A resist remover at 80°C for 6min
14	Rinse and dry	DI water, dry on hot plate at 100°C

Mask 4. SECOND METAL LAYER

Process step	Process Description	Recipes and Comments
1	Clean wafer	Acetone, Methanol, dry N ₂ gun
2	Dehydration	3 min at 115°C
3	Seed-layer deposition	Using CVC DC sputterer Cr/ Cu : 1000A°/3000A°
4	Clean wafer	Acetone, Methanol, dry N ₂ gun
5	Dehydration	3 min at 115°C
6	Spin Photo-Resist	Cover 1/3 of the wafer with NR4-8000P 600rpm, 1500rpm/s, 5 sec.

		1200rpm, 500rpm/s, 40 sec
7	Soft bake	80°C to 110 °C for 10 min on hotplate
8	Exposure	Using MA-6, g-line, hard contact, lamp intensity: 6mJ/sec, expose: 63sec, with 30µm alignment gap.
9	Post exposure bake	80°C to 100 °C for 5 min on hotplate
10	Develop	RD-6 developer for 3 min
11	Copper Oxide removal	Short dip in dilute H ₂ SO ₄ to remove the oxidized Cu layer.
12	Copper electroplating	For 1hour with 750mA current flow In electroplating tank Electroplating rate: 0.25µm/min
13	Strip	Place into Acetone
14	Seed-layer etch	Etch Cu in H ₂ SO ₄ : H ₂ O ₂ :H ₂ O solution until color change, Etch Cr in K ₃ Fe(CN) ₆ :NaOH: H ₂ O solution until color change
15	Clean wafer	Acetone, Methanol, dry N ₂ gun

APPENDIX B

SIMULATED Q AND L OF FABRICATED INDUCTORS

Code number	# of turns	W_{metal}	S_{metal}	d_{out}	Comment	Q_{max} & L
1	1	20	50	300	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm , round edge	21.06@3.5GHz 0.69nH
2	1	20	50	450	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm , round edge	19.83@2GHz 1.12nH
3	1	30	50	300	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm	21.71@2.5GHz 0.7nH
4	1	30	50	400	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm	21.97@2GHz 0.89nH
5	1	30	50	600	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm	21.42@1.5GHz 1.46nH
6	1	50	50	400	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm	22.23@1.5GHz 0.79nH
7	1	40	50	400	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm	22.15@1.5GHz 0.87nH
8	1	40	50	500	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm	22.60@1.5GHz 1.04nH
9	1	40	50	600	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm	22.40@1.5GHz 1.18nH
10	1	50	50	500	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm	22.67@1.5GHz 0.95nH
11	1	50	50	600	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm	23.27@1GHz 1.18nH
12	1	50	50	700	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm	22.95@1GHz 1.31nH
13	1	60	50	500	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm	22.23@1GHz 0.94nH
14	1	60	50	600	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm	23.76@1GHz 1.1nH
15	1	60	50	700	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm	22.88@1GHz 1.21nH
16	1	70	50	600	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm	24.10@1GHz 1.01nH
17	1	20	50	450	On 4 μm SiO ₂ coated Si, metal thickness=15 μm , round	19.74@2.5GHz 1.08nH

Code number	# of turns	W_{metal}	S_{metal}	d_{out}	Comment	$Q_{\text{max}} \& L$
18	1	30	50	500	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm , round inductor	23.35@2GHz 0.98nH
19	1	40	50	500	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm , round inductor	25.50@1.5GHz 0.96nH
20	1	50	50	500	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm , round inductor	28.53@1.5GHz 0.91nH
21	1	60	50	600	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm , round inductor	27.47@1GHz 1.00nH
22	1	60	50	400	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm , round inductor	27.55@1.5GHz 0.55nH
23	1	60	50	450	On 4 μm SiO ₂ coated standard Si, metal thickness=15 μm , round inductor	27.58@1.5GHz 0.62nH
24	1.5	30	20	300	SiO ₂ thickness=5 μm , 1 st metal layer=2 μm , 2 nd metal layer=15 μm , round edge	28.19@2GHz 1.08nH
25	1.5	40	20	300	SiO ₂ thickness=5 μm , 1 st metal layer=2 μm , 2 nd metal layer=15 μm	28.07@2GHz 0.91nH
26	1.5	30	20	400	SiO ₂ thickness=5 μm , 1 st metal layer=2 μm , 2 nd metal layer=15 μm , round edge	28.04@1.5GHz 1.73nH
27	1.5	30	20	200	SiO ₂ thickness=5 μm , 1 st metal layer=2 μm , 2 nd metal layer=15 μm , round edge	27.3@3.5GHz 0.43nH
28	1.5	40	20	400	SiO ₂ thickness=4 μm , 1 st metal layer=1.5 μm , 2 nd metal layer=15 μm , round edge	23.15@1.5GHz 1.4nH
29	1.5	20	20	300	SiO ₂ thickness=5 μm , 1 st metal layer=2 μm , 2 nd metal layer=15 μm	26.7@2.25GHz 1.3nH
30	1.5	50	20	400	SiO ₂ thickness=4 μm , 1 st metal layer=1.5 μm , 2 nd metal layer=15 μm	22.825@1GHz 1.23nH
31	2.5	20	20	300	SiO ₂ thickness=5 μm , 1 st metal layer=1.5 μm , 2 nd metal layer=15 μm	20.70@1.5GHz 2.02nH
32	2.5	20	20	350	SiO ₂ thickness=5 μm , 1 st metal layer=1.5 μm , 2 nd metal =15 μm	20.76@1GHz 2.52nH

Code number	# of turns	w_{metal}	s_{metal}	d_{out}	Comment	$Q_{\text{max}} \& L$
33	2.5	20	20	400	SiO ₂ thickness=5 μm , 1 st metal layer=1.5 μm , 2 nd metal =15 μm	21.05@1GHz 2.94nH
34	2.5	20	20	500	SiO ₂ thickness=5 μm , 1 st metal layer=1.5 μm , 2 nd metal =15 μm	19.65@1GHz 4.1nH
35	2.5	30	20	350	SiO ₂ thickness=5 μm , 1 st metal layer=1.5 μm , 2 nd metal =15 μm	19.79@1GHz 2.15nH
36	2.5	30	20	400	SiO ₂ thickness=5 μm , 1 st metal layer=1.5 μm , 2 nd metal =15 μm round edge inductor	20.54@1GHz 2.6nH
37	2.5	30	20	500	SiO ₂ thickness=5 μm , 1 st metal layer=1.5 μm , 2 nd metal =15 μm round edge inductor	20.04@1GHz 3.43nH
38	2.5	40	20	400	SiO ₂ thickness=5 μm , 1 st metal layer=1.5 μm , 2 nd metal =15 μm round edge inductor	19.23@1GHz 2.14nH
39	2.5	40	20	400	SiO ₂ thickness=5 μm , 1 st metal layer=1.5 μm , 2 nd metal =15 μm round inductor	19.04@1GHz 1.55nH
40	2.5	40	20	500	SiO ₂ thickness=5 μm , 1 st metal layer=1.5 μm , 2 nd metal =15 μm round inductor	19.69@0.5GHz 3.08nH
41	2.5	40	20	500	SiO ₂ thickness=5 μm , 1 st metal layer=1.5 μm , 2 nd metal =15 μm	19.69@0.5GHz 3.08nH
42	2.5	50	20	400	SiO ₂ thickness=5 μm , 1 st metal layer=1.5 μm , 2 nd metal=15 μm , round edge inductor	17.19@1GHz 1.72nH

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