A HIGH-PERFORMANCE, TEMPERATURE-STABLE, CONTINOUSLY TUNED MEMS CAPACITOR

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ABSTRACT

This paper reports on a continuously tunable MEMS capacitor with a wide tuning range of 5:1, high quality factor of better than 100 (at 1 GHz) at each tuned state, and self-resonance frequency of more than 13.5 GHz. The temperature stability of the capacitance in the temperature range of -50 ºC to 60 ºC is better than 7%, which is one of the best reported for continuously tuned capacitors. The maximum tuning speed of the capacitor is measured to be better than 40 µsec.

INTRODUCTION

Electrostatically tuned MEMS capacitors can offer higher actuation speed and lower power consumption compared with piezoelectric, thermal or magnetically actuated capacitors. As such, there has been extensive work on electrostatically tuned capacitors and many wide tuning range devices have been reported [1–6]. However, for successful insertion of the capacitor into RF systems, several other performance aspects of the device need to be simultaneously addressed; some or none of which is considered for most reported tunable capacitors. These include tuning speed, initial capacitance value, quality factor (Q), self-resonant frequency (SRF), and temperature stability.

In this work, all these critical performance parameters of tunable capacitors are addressed. Specifically, a tunable capacitor is designed for stable operation over a wide temperature range and fast tuning stabilization using a dual-gap configuration. The mechanical design of the membrane and springs is optimized to overcome the warping issue due to residual stress and temperature variation, while maintaining a maximum tuning voltage below 30 V. The Q of the capacitor is maintained high across the entire tuning range. Such capacitors can be directly integrated with high-Q inductors [7] to implement continuously tunable filters for reconfigurable radio applications.

DESIGN

The basic structure of the tunable capacitor is shown schematically in Figure 1. In this structure, the RF and DC biasing electrodes are separated and the top membrane is the shared ground electrode. Untying the RF and DC biasing electrodes simplifies the biasing network and improves the power handling capability. To overcome the pull-in limitation of capacitive actuation and achieve wide range of continuous tuning, the capacitor was designed in a dual-gap configuration [1] with actuation gap of 2 µm and capacitive sense gap of 0.5 µm. Increasing the actuation to sense gap ratio beyond 3:1, as is done in this work, not only ensures a wide tuning range, but also results in better tuning linearity and faster stabilization time. The initial capacitance value was designed as 300 fF and the minimum required Q is 100 at each tuned state. To achieve high quality factor, the top membrane was fabricated in thick electroplated gold (4 µm). The size of the entire membrane is decided by the actuation area needed to get the tuning bias below 30 V. The overall size of top membrane is 450 µm by 450 µm.

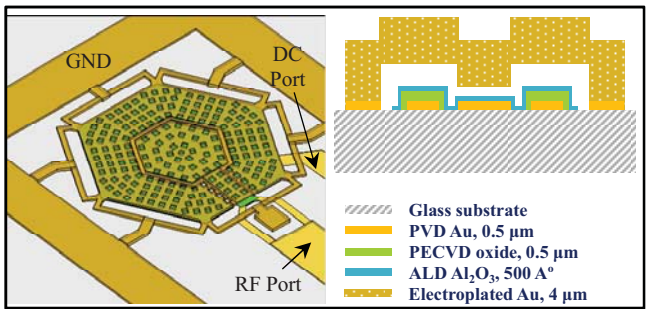


Figure 1: Layout of tunable capacitor. Top-down view (left) and simplified cross-section view (right)

The temperature sensitivity of the capacitor is highly dependent on the residual stress and the stress gradient across the top gold membrane. To determine the value of the residual stress in the electroplated gold layer, a micro-strain gauge [8] was fabricated applying the same fabrication process as that of the tunable capacitor. Figure 2(a) shows a SEM view of the fabricated micro-strain gauge. From the lateral displacement of the micro-strain gauge, the residual stress of electroplated gold was extracted to be ~40 MPa. ANSYS simulation was then used to determine the deformation of the top membrane upon 40 MPa of residual stress and to optimize the physical layout of the springs and the membrane to minimize this deformation (see Figure 2(b)). To this end, the geometrically compensated spring and anchoring design introduced in [9] was adopted. Using this design, the membrane shifts in the lateral direction releasing any residual stress, thereby minimizing the deformation in the vertical direction. Prior stress-tolerant designs based on this compensation technique have used a square-shape membrane. Herein, the design of the membrane was changed to a hexagonal shape, which offers a higher mechanical resonant frequency, good symmetry and comparable stress tolerance compared to a similar size square-shape design. From a modal analysis, the mechanical resonant frequency of the design shown in Figure 2(b) was extracted to be 23 kHz.

Measurement of stress gradient in electroplated gold is a more challenging task. In initial simulations, the stress gradient was assumed to be 2 MPa/µm. As shown in Figure 2(b), the deformation of the top membrane because of the

residual stress of 40 MPa and stress gradient of 2 MPa is less than 86 nm. The center region of the membrane, where the capacitor is sensed, is warped by less than 1.2 nm. This deformation is negligible compared with the initial air gap of 0.5 µm and therefore this design is proved to be stress tolerant. Further, the deflection of the membrane is less than 0.1 µm with temperature variation of 110 ºC (from -50 ºC to 60 ºC). Figure 3 illustrates simulation results with 40 MPa of residual stress at -50 ºC and 60 ºC, respectively. As shown, the difference between the maximum deflection at -50 ºC and 60 ºC is only about 10 nm at the presence of both temperature variation and stress. This would result in capacitance change of less than 1.8%.

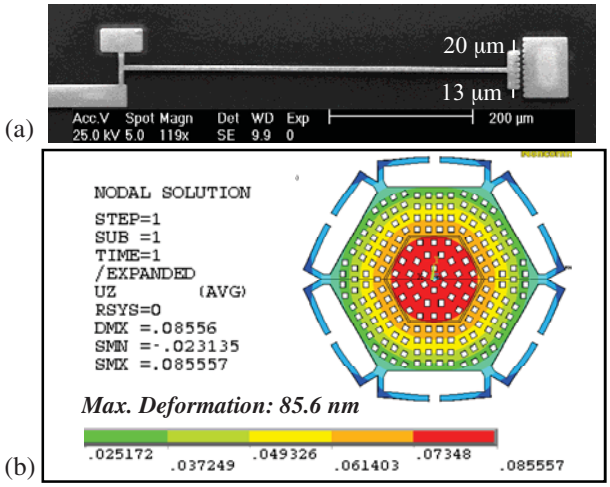


Figure 2: (a) Test structure to measure stress in electroplated gold. (b) Deformation of the top membrane upon 40 MPa of residual stress and 2 MPa/µm of stress gradient in the gold layer at room temperature.

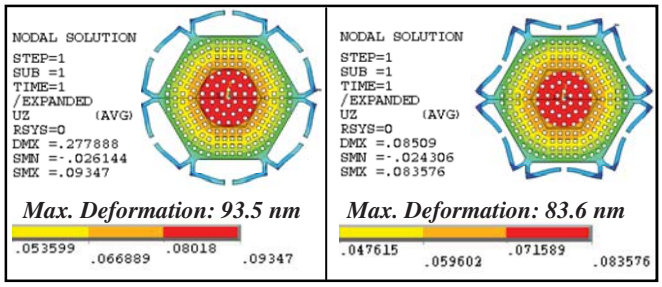


Figure 3: Deformation of the top membrane upon 40 MPa of residual stress and 2 MPa/µm of stress gradient at -50 ºC (left) and at 60 ºC (right).

Capacitance and *Q* were extracted using the HFSS 3D electromagnetic simulation tool [10]. The final capacitance was simulated with a reduced dielectric constant in the aluminum oxide (Al_2O_3) dielectric layer to consider non-ideal factors in fabrication such as surface roughness or minor warping of the top membrane. Substrate properties such as dielectric constant and loss tangent were also considered to reflect the properties of the glass substrate, Borofloat33. As shown in Figure 4, the simulated *Q* is higher than 500 at the initial state and better than 130 at the final state (at 1GHz). Since inductive parasitic of the springs is insignificant, the SRF is high extending the frequency range to more than 15 GHz at the initial state and to about 7 GHz when the capacitor is tuned.

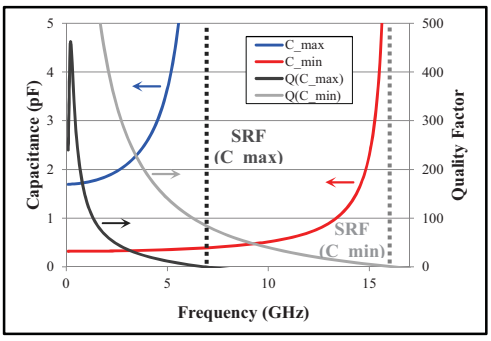
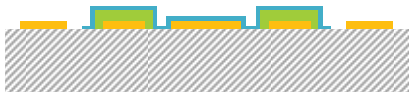


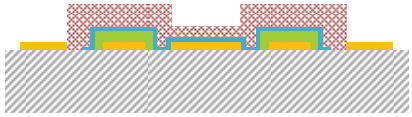
Figure 4: Initial capacitance, maximum capacitance, and Q at initial and final states extracted using the HFSS tool.

FABRICATION PROCESS

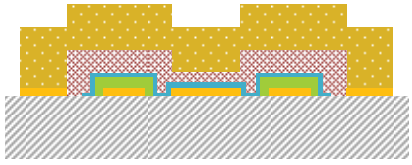
The fabrication process flow is shown in Figure 5. The process is low-temperature (< 300 °C) and thus post-CMOS compatible.



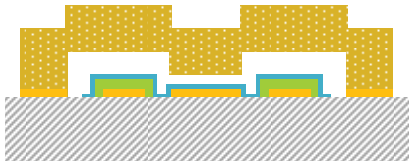
(a) Deposit bottom electrode and dielectric layer



(b) Deposit and pattern sputtered amorphous silicon



(c) Electroplate gold as top electrode



(d)Release device with XeF2

Figure 5: Fabrication process of the tunable capacitors.

The process starts with the deposition and patterning of the gold bottom electrode (0.5 µm thick) on the Borofloat33 glass substrate. A 500 A° thick Atomic Layer Deposited Al_2O_3 layer is used as the capacitance dielectric layer because of its high dielectric constant (ε_r=9.3) and high etch selectivity to the xenon difluoride (XeF_2) gas that is used in the final release step. To increase the breakdown voltage, an additional 5000 A° of silicon dioxide is deposited on the bottom actuation electrode. A low-stress amorphous silicon layer with less than 4 MPa of average residual stress is sputter deposited and patterned to define the capacitance and

actuation gap. Next, 4 µm thick gold is electroplated and devices are dry released using XeF_2. Figure 6 shows a SEM image of the fabricated capacitor. As shown, the membrane and the supporting springs remain flat after release.

MEASURED RESULT & DISCUSSION

On-wafer measurement of devices is carried out using a N5241A Agilent PNA-X network analyzer and Cascade Microtech GSG Z-probes. The fabricated capacitor exhibits *Q* values higher than 100 at 1 GHz at each tuned state and a continuous tuning ratio of more than 5:1 (0.2 pF to 1.0 pF) (Figure 7). The measured capacitance range was slightly lower than the designed value, which was 0.3 pF to 1.5 pF. This is due to the fact that the warping of the top membrane is larger than expected because of higher stress gradient in electroplated gold. The measured self-resonant frequency of the tunable capacitor at the initial capacitance state is more than 13.5 GHz, as shown in Figure 7.

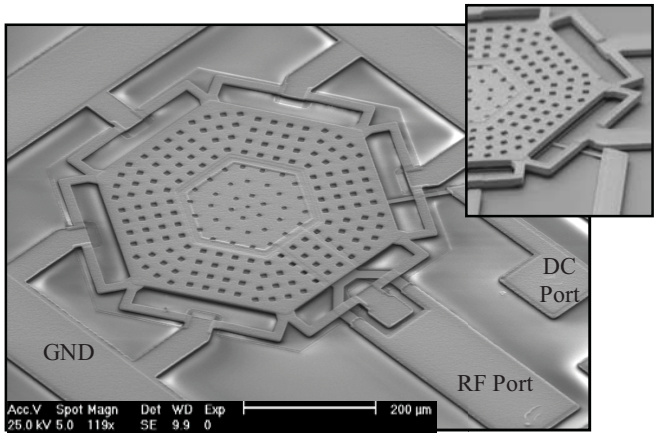


Figure 6: SEM images of the fabricated tunable capacitor.

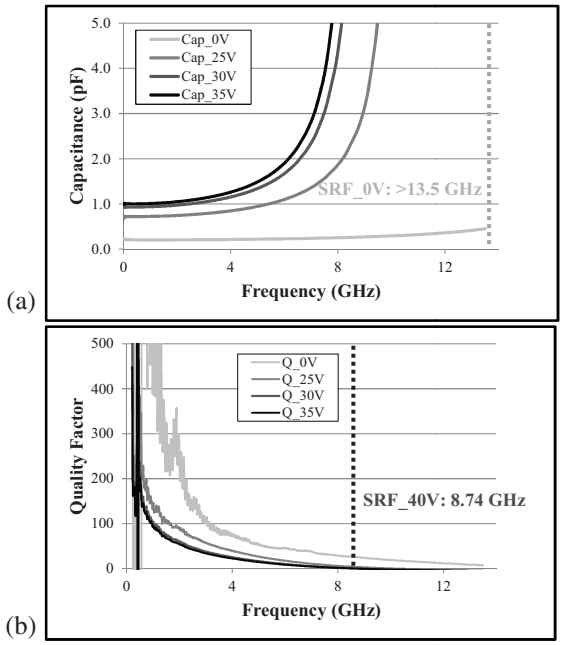


Figure 7: (a) Measured capacitance and (b) quality factor at different tuning bias.

The C-V tuning curve of the capacitor is shown in Figure 8. Due to the minor warping of the top membrane, the capacitor can be tuned in two states. In state one, the whole membrane moves down with the applied bias. After the touchdown at 25 V, the top membrane conforms to the substrate and the capacitance value increases further. The warping in the top membrane can be reduced by reducing the residual stress gradient through optimization of the gold electroplating process. Using optical measurements, the deflection in the top membrane was measured and the stress gradient was extracted to be around 4 MPa/µm, which is twice the value assumed in the initial simulations. To verify the deformation of the top membrane at the presence of 4 MPa/µm of stress gradient, the structure was simulated again in ANSYS (Figure 9). At room temperature, the deformation at the center of the membrane is ~0.2 µm, which explains the shift in the initial capacitance value from 300 fF (designed) to 200 fF (measured).

Although the stress gradient results in a higher deflection in the membrane, this deformation remains similar (within 20 nm) across the temperature range of interest thanks to the temperature tolerant design of the springs. Therefore, the tunable capacitor can still achieve good temperature stability as shown in Figure 10. The initial and final values of the capacitor in the temperature range of -50 °C to 60 °C remain within 5% and 7% of their room temperature values, respectively. The required tuning bias to achieve maximum tuning is stable within 9%, which is one of the best reported in the literature (see Table 1).

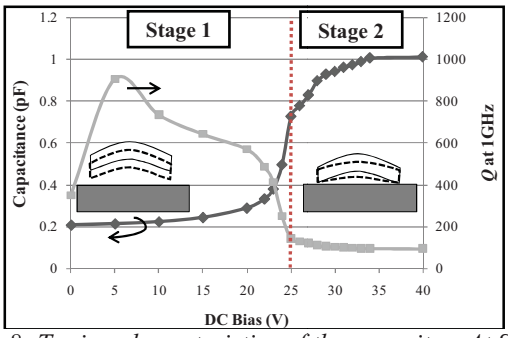


Figure 8: Tuning characteristics of the capacitor. At Stage 1 the air gap closes uniformly. At Stage 2 (after touch-down at 25 V) the membrane conforms to the substrate.

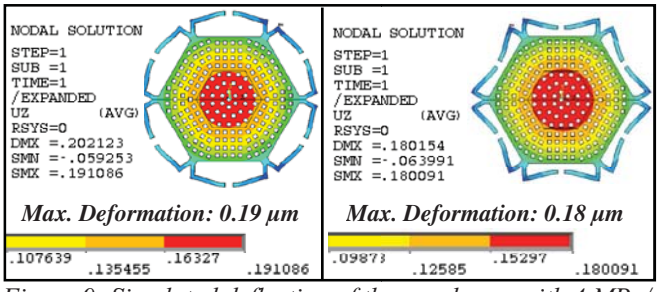


Figure 9: Simulated deflection of the membrane with 4 MPa/µm of residual stress gradient at -50 °C (Left) and 60 °C (Right). The deformation in the membrane stays within 0.20 µm at -50 to +60 °C.

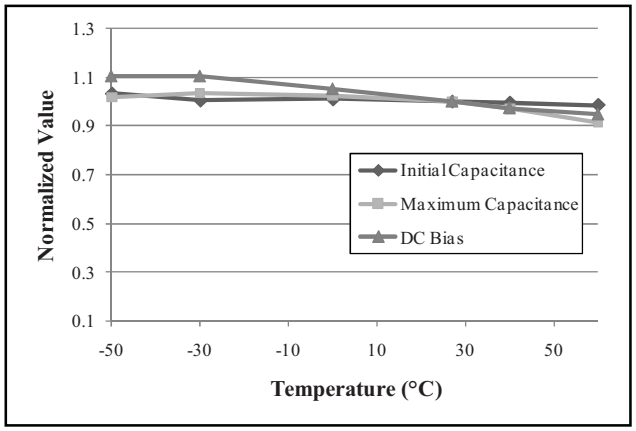


Figure 10: Measured initial and final capacitance values as well as the maximum bias are stable within 5%, 7%, and 9% of their room temperature values.

For the measurement of tuning speed, a 50 MHz RF tone from an Agilent 81150A function generator together with the DC bias were applied to the DC electrode using a bias tee. The corresponding signal at the RF electrode was detected using a KRYTAR 201A power detector that was connected to an Agilent MSO7104A oscilloscope. Figure 11 shows the response of the capacitor (the detected output of the power detector) when 15 V of tuning bias is applied. The mechanical resonance frequency is extracted from the oscillation time to be 25 kHz and the tuning stabilization time is less than 80 µs. The mechanical response is in good agreement with the ANSYS simulation results.

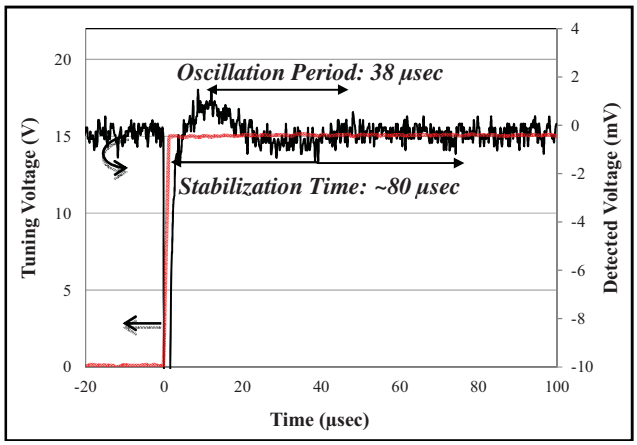


Figure 11: Tuning speed measurement when 15 V of tuning bias was applied.

CONCLUSIONS

A continuously tunable capacitor was designed, fabricated, and characterized. As shown in Table 1, the presented tunable capacitor exhibits high *Q*, high continuous tuning ratio, and good temperature stability. The design of tunable capacitor can be further optimized for improved tuning linearity by further increasing the actuation to sense capacitive gap and reducing the stress gradient in the top membrane. The capacitor can be integrated with other high-performance passives to implement tunable RF modules such as filters and matching networks.

ACKNOWLEDGEMENT

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[10] www.ansoft.com/products/hf/hfss/

Table 1: Comparison between some of the highest performance continuously tunable capacitors.

	Rijks '06 [3]	McFeetors '06 [4]	Mahameed '10 [5]	Shavezipur '10 [6]	**This work**
Initial Capacitance	0.26 pF	0.31 pF	85 ~ 95 fF	1.2 pF	0.2 pF
Tuning Ratio	4.5	6.2	2.8 ~ 3.3	10.5	5.0
Quality Factor (at down-state Cap.)	>100 @4 GHz, 1.17 pF	>100 @20 GHz, 1.4 pF	>100 @5 GHz, 285 to 305 fF	N / A	>100 @1GHz, 1.0 pF
Tuning Speed	< 400 µs, max: 25 µs	N / A	N / A	N / A	< 100 µs, max: 40 µs
Max. Bias	30 V	45 V, 80 V	75 ~ 80 V	40 V	35 V
Temperature Stability	< 20%	N / A	< 10%	N / A	< 9%