High-Q Tunable Silver Capacitors for RFIC's

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Abstract **— This paper presents implementation and characterization of high quality factor (*Q*) silver (Ag) in-plane tunable capacitors on various substrates. A combination of low-loss substrate and the highest conductivity metal is used to achieve very high *Q* at RF frequencies. A high quality factor (*Q*>200 @1GHz) 0.7pF silver capacitor fabricated on a low-loss suspended Avatrel membrane achieved a tuning of 130%.**

Index Terms **— Dual gap, Micromachining, Silver, Quality factor, Tunable capacitor.**

I. Introduction

Tunable capacitors are widely used in RF integrated circuits such as tunable filters, voltage controlled oscillators, and reconfigurable impedance matching networks. Depending on their application, tunable capacitors are required to have large tuning range, high quality factor, and/or high self-resonance frequency (*SRF*). Currently, MOS varactors are used in RFIC's as the tuning element. MEMS (micro-electromechanical system) tunable capacitors, however, could exhibit higher quality factors and therefore outperform MOS varactors at frequencies beyond 1GHz.

Reported MEMS tunable capacitors can be divided into two categories based on their choice of material: silicon-based capacitors, which are usually realized in bulk of silicon (Si) on insulator substrate [1, 2], and metal-based capacitors fabricated on Si or glass substrate [3]. Compared to Si-based capacitors, metal-based capacitors have smaller series resistance and exhibit higher *Q*. To improve the high frequency performance of the metal-based capacitor on Si, the substrate loss should be reduced. In this work high aspect-ratio silver micromachining is used to create in-plane tunable capacitors on low-loss Avatrel membranes. The effect of the substrate is explored by comparing the performance of identical capacitors fabricated on CMOS-grade (10-20Ω .cm) Si, high-resistivity (>1k Ω .cm) Si, and micromachined Avatrel membrane.

II. Design

The continuous tuning range of a conventional parallel-plate MEMS capacitor with electrostatic actuation is limited because of the pull-in effect. The pull-in limitation on the tuning range can be avoided in a dual-gap tunable capacitor, which has different gap sizes at the actuation side and the sense side [2]. In this case, the travel distance is equal to one third of the actuation gap, which can exceed the initial sense gap. Implementation of in-plane (lateral) dual gap actuators is typically easier, since the gap sizes are defined lithographically. In contrast, the gaps of an out-of-plane (vertical) actuator are defined by deposition of sacrificial layers with different thicknesses. In addition, since both plates of in-plane capacitors are suspended in air, they can potentially exhibit higher *Q*. In this work, we chose dual gap actuation scheme to get the highest tuning range with an in-plane (lateral) parallel-plate capacitor design. Dual gap parallel-plate actuation can achieve higher tuning ratio with smaller traveling distance compared to the comb-drive actuation.

III. Fabrication

The fabrication process of tunable silver capacitors is shown in Fig. 1.

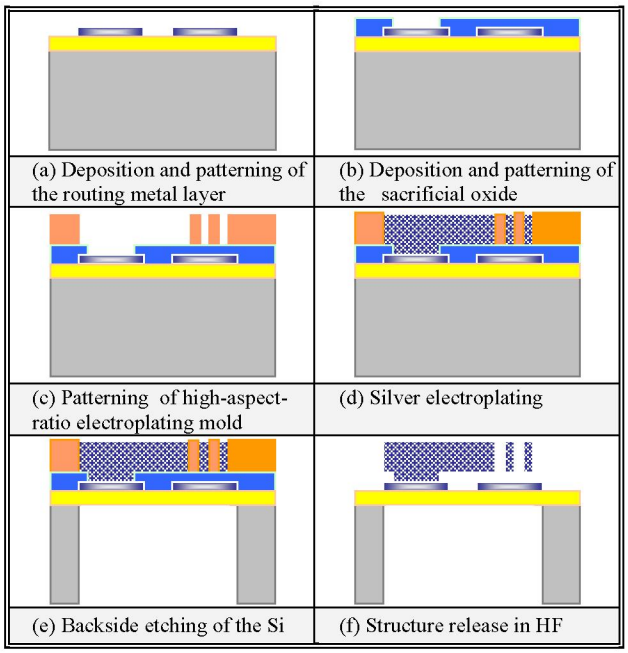

Fig. 1. Fabrication process flow of MEMS silver capacitors

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The substrate is first passivated with a 20µm thick low-loss polymer. We chose Avatrel polymer from Promerus for this purpose because of its low permittivity and loss tangent. Next, a 2µm thick routing layer of titanium/silver is evaporated and patterned. The sacrificial silicon dioxide layer is then deposited at 250°C (the highest processing temperature) and patterned. Next, the electroplating mold is spin-coated and patterned. Figure 2 shows the SEM view of a 50µm thick NR4-8000P negative-tone photoresist from Futurrex used as the mold, showing the straight sidewall profile. Thick silver (40µm) is then electroplated into the photoresist mold. Silver is used as the structural material since it has higher conductivity, lower young's modulus, and lower mechanical stress in thick electroplated film compared to other metals (*e.g.* copper). The loss of Si substrate is then eliminated by selective backside etching of Si underneath the passives, leaving behind an Avatrel membrane. Finally, devices are released in buffer oxide etch.

Figure 3 shows the SEM view of a high aspect-ratio (5:1) silver tunable lateral capacitor with a close-up view of the actuation and sense gap.

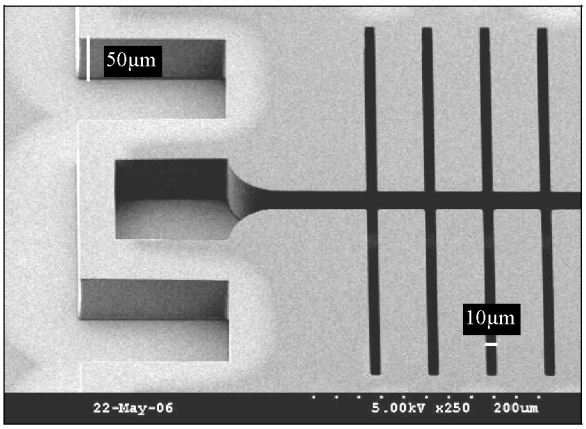
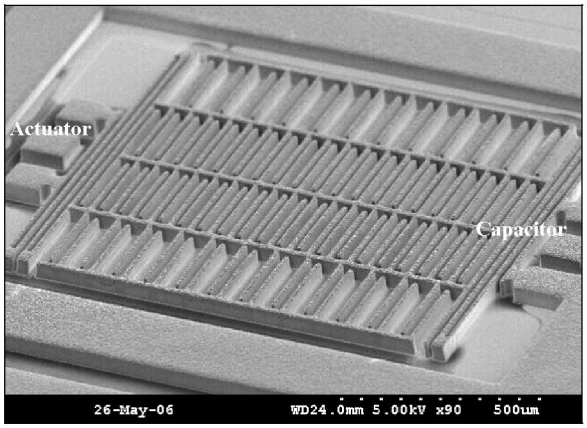
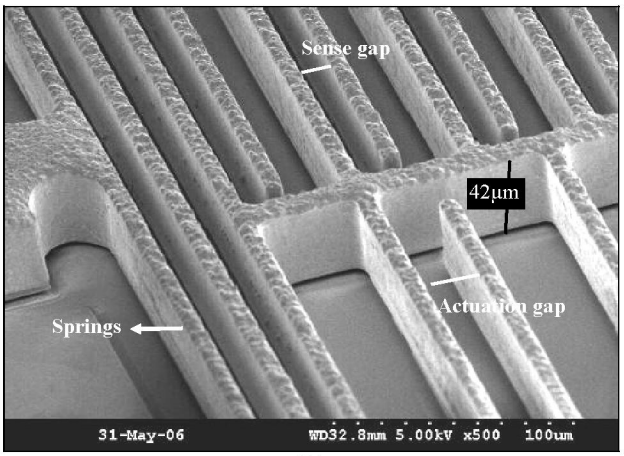


Fig. 2. SEM view of a 50µm thick NR4-8000P negative tone photoresist, showing the straight side walls.



(a)



(b)

Fig. 3. (a) SEM view of a 40µm thick tunable silver capacitor with a (b) close-up view of the actuation and sense gaps.

The micrograph of the tunable silver capacitor taken from the front and backside of the Avatrel membrane is shown in Fig. 4.

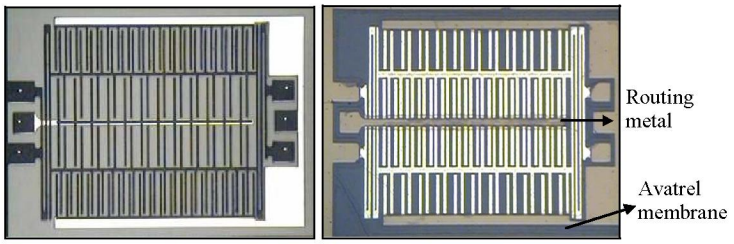


Fig. 4. Micrograph of the capacitor in Fig. 3 taken from (left) the front side and (b) the backside of the Avatrel membrane.

It is worth mentioning that high-Q inductors, fixed capacitors, and vertical tunable inductors can be simultaneously implemented using the same fabrication process [4]. For instance, a 40µm thick silver inductor fabricated on an Avatrel membrane exhibits a very high Q of >110 at 5-25GHz frequency range [5].

VI. Results and Discussion

The silver capacitors have very small series resistance due to the high conductivity of electroplated silver, and can exhibit very high Q. Therefore, special care must be taken in measuring the Q. On-wafer S-parameter measurements of the fabricated devices have been carried out using an *hp*8510C vector network analyzer and Cascade GSG infinity (I-50) microprobes. Measuring Q's in excess of 80 calls for a very thorough calibration. Herein, calibration is done using both SOLT and LRRM calibration procedure and the pad parasitics have not been de-embedded to avoid over estimating of the Q's. Also, to

ensure repeatability in the measurements, the high Q passives are measured several times, and each time the calibration was redone. The deviation of the measurement values is within 10% for Q's in excess of 100. Capacitance value and quality factor are extracted from the measured embedded S-parameters using the following equation:

$$Q = \frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})}, \text{ and } C = \frac{\mathrm{Im}(Y_{11})}{\omega(1-\mathrm{Re}(Y_{11}))} \quad (1)$$

where ω is the angular frequency. Capacitance values are extracted at 50MHz. Figure 5 shows the electrical model of the tunable capacitor on silicon substrate, where C_s is the sense capacitance, R_s is the series resistance of the silver lines, and L_s is mainly the inductance of the folded springs. C_{si} and R_{si} are the parasitic capacitance and resistance of the substrate, respectively. When the substrate is removed below the capacitor body, C_{si} and R_{si} become the parasitics of the pads.

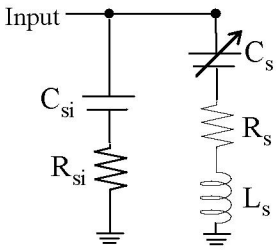


Fig. 5. Electrical model of the tunable capacitor on Si.

Figure 6 is the measured Q of a 40μm thick tunable silver capacitor, showing Q>100 up to 2.4GHz and *SRF*>6GHz. The actuation gap of this capacitor is two times the sense gap. Thus, the ideal tuning of this capacitor, when there is no parasitic capacitance, is 3. The measured parasitic capacitance (C_{si}) of this capacitor is 25fF.

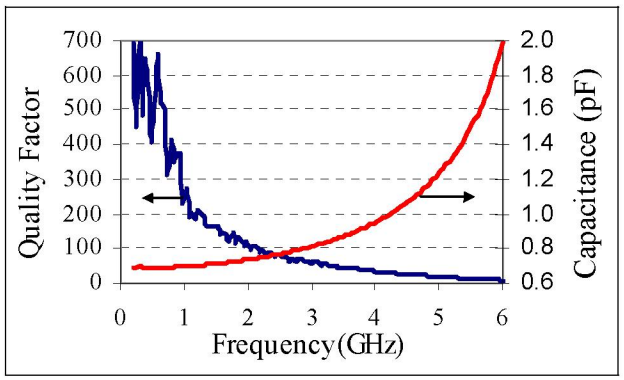


Fig. 6. Measured embedded Q of a 0.68pF Ag capacitor fabricated on Avatrel membrane.

To identify the effect of the substrate on the Q, two identical capacitors were fabricated on Avatrel coated CMOS-grade (ρ = 10-20Ω.cm) Si substrate (Si not etched from back-side), and Avatrel coated high-resistively (ρ>1kΩ.cm) Si (HRS) substrate (Si not removed). The measured Q of these capacitors is shown in Fig. 7. Comparison of Figures 6 and 7 reveals that by removing the substrate Q is improved by an order of magnitude at 1GHz. Also, the parasitic capacitance of the capacitor body to the substrate (C_{si}) is significantly reduced by backside etching of Si. The capacitor exhibits better performance at higher frequencies when fabricated on HRS. On the other hand, the low-frequency Q of the capacitor on HRS is low due to the formation of a conductive layer at the interface of the substrate and the passivation layer, which results in excess values for the equivalent series resistance at low frequencies [6].

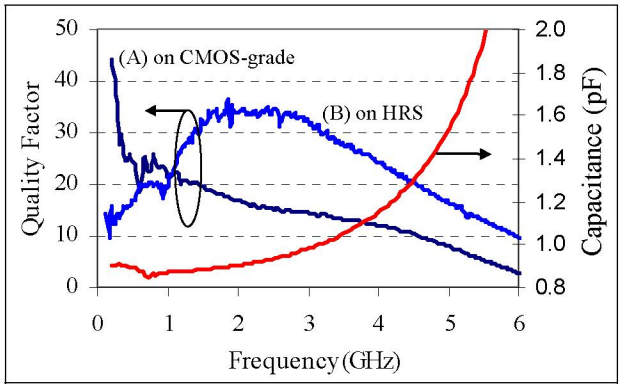


Fig. 7. Measured embedded Q of two identical capacitors to Fig. 6 fabricated on Avatrel coated (A) CMOS-grade, and (B) high-resistivity Si substrate.

The tuning curve of the capacitor on Avatrel membrane is shown in Fig. 8. The capacitance is changed by 2.3x with a tuning voltage of 54V (Fig. 8).

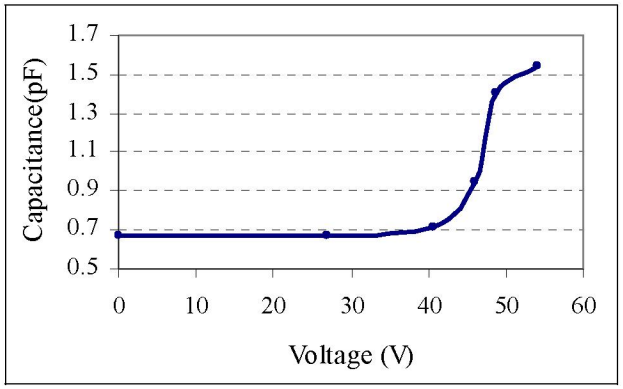


Fig. 8. C-V tuning curve of a 0.68pF Ag capacitor with actuation gap = 2x sense gap.

The tuning curve of another capacitor with the same sense capacitor configuration but smaller actuation gap (10μm) is shown in Fig. 9. As it is shown, when the actuation gap is reduced, the tuning voltage is reduced at the expense of the reduction of the tuning range (x1.45 in this case).

Tuning voltages of these capacitors are high due to the conservative design of the gap size, and can be reduced by decreasing the actuation gap and the spring width. The performance of the capacitors can be further improved by increasing the thickness of the routing layer, decreasing the gap sizes and utilizing one-turn springs to increase the self-resonance frequency by decreasing the series inductance (L_s).

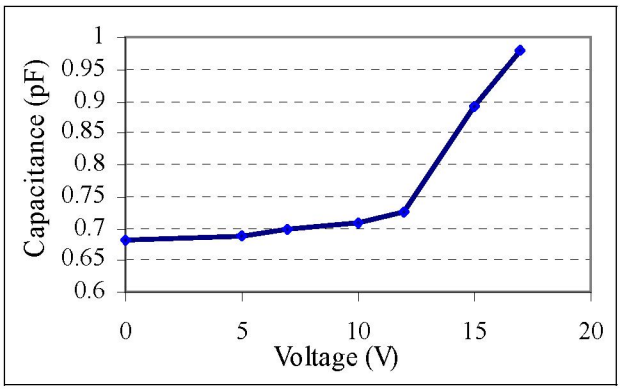


Fig. 9. C-V tuning curve of a 0.68pF Ag capacitor with actuation gap = sense gap.

V. Conclusion

A new implementation of high quality factor tunable MEMS capacitors was presented. Silver was used as the structural material to reduce the metal loss. The loss of the silicon substrate was eliminated by selective backside etching of silicon. A 0.7pF silver tunable lateral capacitor was fabricated and showed a large Q of >200 at 1GHz with a tuning of 2.3x.

Acknowledgement

The authors wish to acknowledge Dr. Paul A. Kohl for his helpful discussion regarding the silver electroplating and the assistance of MiRC cleanroom staff at Georgia Tech.

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