HIGH-Q INTEGRATED INDUCTORS ON TRENCHED SILICON ISLANDS

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ABSTRACT

A new implementation of high quality factor (Q) copper (Cu) inductors on CMOS-grade silicon substrates using a fully CMOS-compatible process is presented. A low-temperature fabrication sequence is employed to reduce the loss of Si wafers at RF frequencies using micromachining technique. This method does not require air suspension of the inductors, resulting in mechanically-robust structures that are compatible with any packaging technology. A 1nH inductor fabricated on this low-loss micromachined Si substrate exhibits a high peak Q of 51 at 1.0GHz (40 at 2.4GHz) with a self-resonant frequency larger than 10GHz.

1. INTRODUCTION

Integrated high-Q inductors can improve the performance and integration-level of RFIC's while reducing their power consumption and cost. On-chip inductors in commercially available CMOS processes exhibit poor Q's (<15) due to the high-frequency loss of silicon (Si) substrate and ohmic loss of thin metal layers. While metal loss can be reduced by using thick high-conductivity metals, substrate loss has remained the major barrier in reaching inductor Q's on Si comparable to that of off-chip elements. Micromachining techniques have been utilized to reduce the substrate loss and increase Q. Previously reported techniques include suspension of the inductor structure or high temperature processes that are not CMOS-compatible [1, 2]. Suspension may cause susceptibility to shock and vibrations and can complicate die packaging.

In this paper, we present a low-temperature CMOS-compatible process sequence to selectively reduce the substrate loss underneath RF passive components while maintaining solid mechanical support for the inductor. Simultaneously, metal loss of inductors is reduced by electroplating thick (~26μm) Cu layer. A 1nH Cu inductor fabricated on this low-loss micromachined silicon substrate exhibits high Q of 51 at 1 GHz. This is the highest Q reported for planar spiral inductors fabricated on CMOS-grade Si substrate.

2. INDUCTOR DESIGN

Figure 1 shows the layout and equivalent circuit model of a planar spiral inductor on silicon [3]. The unloaded Q of an inductor can be expressed by [4]:

$$\frac{1}{Q}=\frac{1}{Q_{substrate}}+\frac{1}{Q_{metal}} \quad (1)$$

where $Q_{substrate}$ and Q_{metal} represent the substrate loss and the ohmic loss of metal strips, respectively.

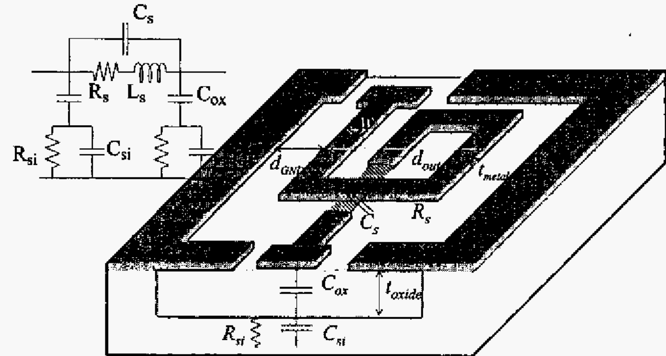

Figure 1. Layout and equivalent electrical model of a planar spiral inductor.

TRENCHED SI ISLAND FOR REDUCED SUBSTRATE LOSS

At RF frequencies, induced currents in the Si substrate limit $Q_{substrate}$ by converting the electromagnetic energy into heat. Equations 2 and 3 show the components of the induced current in the substrate at the presence of electromagnetic fields [5].

$$\nabla \times H = j\omega\varepsilon' E + \omega\varepsilon' \tan\delta\, E + \sigma E \quad (2)$$

$$\nabla \times E = -j\omega\mu H, \quad J = \sigma E \quad (3)$$

where σ and $tan\delta$ represent the substrate conductivity and loss tangent, respectively; ω is the angular frequency, ε' and ε'' are the real and imaginary part of the substrate permittivity and μ is the permeability. For low-resistivity substrates such as CMOS-grade Si, the electrically-induced current (σE) dominates over the dipole loss ($\omega\varepsilon'\ tan\delta\ E$). However, for high-resistivity substrates the dipole loss is the determining loss mechanism. At higher frequencies, creation of the magnetically induced eddy current in low-resistivity substrates (Eq.3) also limits $Q_{substrate}$.

Disrupting the path of current by slicing the substrate with deep high-aspect-ratio trenches reduces the substrate effective permittivity and conductivity, which in turn reduces the electrically- and magnetically-induced currents as well as the dipole loss. A low-loss substrate on which the inductor is firmly supported can then be realized by subsequently bridging over the open areas through deposition of a low loss-tangent PECVD dielectric layer (e.g. SiO_2). The required film thickness to bridge over the open areas and create a smooth surface is in the order of the trench width (1-3μm). Figure 2 shows cross-section SEM view of a 50μm deep Trenched Si Island (*TSI*).

THICK COPPER FOR REDUCED METAL LOSS

Metal loss is reduced by electroplating thick Cu (~26μm) and eliminating the effect of ground plane by increasing the signal to ground distance in the inductor layout.

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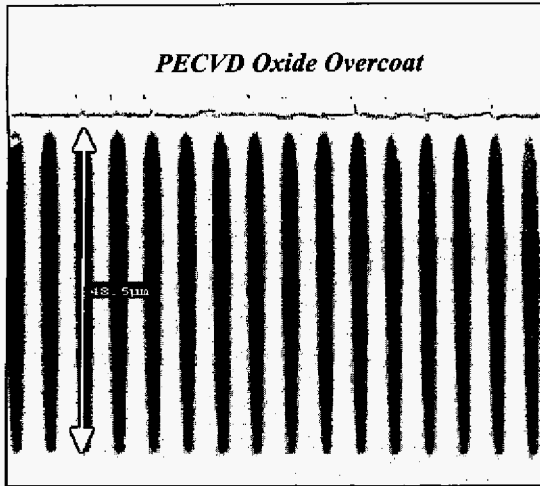

Figure 2. SEM picture of Trenched Silicon Island (TSI).

For coplanar inductors with distant ground, current does not recede on the bottom surface of the conductor, as opposed to microstrip lines with close ground [6], and the series resistance of the conductor can be calculated from:

$$R_s = \frac{k\,l}{2\sigma\delta(w+t)} \quad \text{where} \quad \delta = \sqrt{\frac{1}{\pi f \sigma \mu}} \qquad (4)$$

Conductor width, total length and thickness are represented by *w, l and t*, respectively; *k* is a correction factor, which depends on *t* and *w*, σ is the conductivity of the metal and δ is the skin depth (e.g. δ_{Cu} =1.3µm @ 2.4GHz). Equation 4 justifies the improvement in Q_{metal} for thicker conductors as the series resistance continues to drop even with metal thicknesses in excess of 5 times the skin depth [7].

3. INDUCTOR FABRICATION

Figure 3 shows the fabrication process flow for the Cu inductors on *TSI*. First, deep high-aspect-ratio (25:1) trenches are etched in the Si substrate using the Bosch process. A 2-3µm thick PECVD SiO_2 layer is then deposited at 300°C to cover the openings and lower the substrate parasitic capacitances. The first metal layer is subsequently formed by the evaporation and patterning of a 2µm thick Chrome (Cr)-Cu-Cr layer. To isolate the two metal layers, a 2µm thick PECVD SiO_2 is deposited at 300°C and vias are opened. A 1000A° seed layer of Cr-Cu is then sputter deposited, followed by spin-coat and patterning of the electroplating mold. Thick NR4-8000P negative-tone photoresist has been used for this purpose, which produces high-aspect-ratio (5:1) and straight-sidewall columns as shown in Fig. 4(a). Finally, thick layer of Cu is electroplated and the photoresist and seed layer are removed. Figure 4(b) shows SEM pictures of a one-turn inductor on *TSI*.

To evaluate the effectiveness of trenched Si island in reducing the substrate loss, similar inductors were also fabricated on thick silicon dioxide islands (*OI*) created by thermal oxidation of silicon left in between the trenches (@ ~1100°C) [8]. SEM and microscope pictures of a three-turn spiral inductor on an *OI* are shown in Fig. 5.

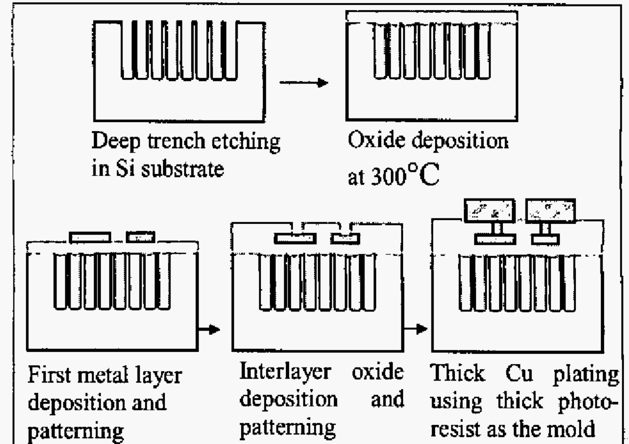

Figure 3. Inductor fabrication process flow on TSI.

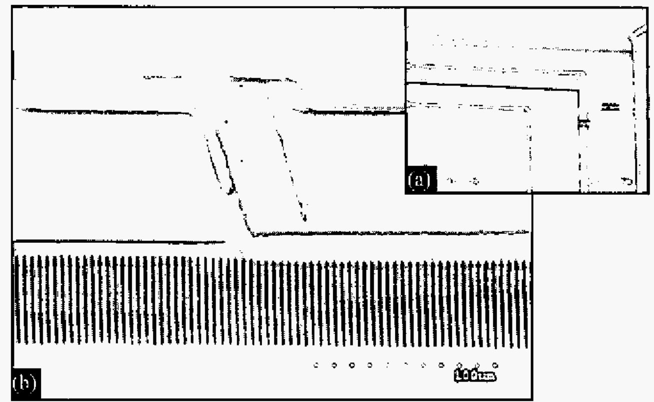

Figure 4. (a) NR4-8000P profile used as electroplating mold and (b) SEM picture of a one-turn inductor on top of TSI, w=40µm, d_{out}=860µm, t_{metal}=26µm, Q=45.

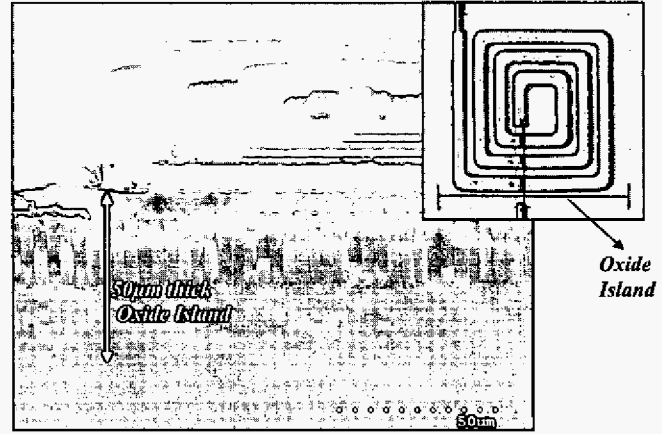

Figure 5. SEM and microscope picture of a 3-turn round-edge inductor, w=15µm, d_{out}=400µm, s=15µm, t_{metal}=8µm.

4. SIMULATION AND TEST RESULTS

Rectangular and circular type inductors of various dimensions were fabricated and tested on low-loss micromachined Si substrates. On-wafer S-parameter measurements were carried out using an *hp*8517B vector network analyzer and ground-signal-ground Cascade micro-probes. The pad-only characteristics were measured on the open pad structures. The pads parasitics were then de-embedded from the overall inductor characteristic by

subtracting the Y-parameters of the pads from the Y-parameters of the embedded inductors. The equivalent circuit model shown in Fig.1 is used to extract the electrical parameters. For one-turn one-port inductors, the second port in the model was grounded. Inductance and Q are calculated from:

$$L = \frac{\mathrm{Im}(Z_{in})}{2 \times \pi \times f} \qquad Q = -\frac{\mathrm{Im}(Y_{in})}{\mathrm{Re}(Y_{in})} \qquad (5)$$

Figure 6 demonstrates the remarkable effectiveness of the trenched Si island in increasing the Q. As it is shown in Fig. 6(b) the S_{11}-parameter of the inductor fabricated on *TSI* (low-temperature) is very close to the one fabricated on 50µm thick solid *OI* (high-temperature), and the inductor has significant higher Q compared to when it is fabricated on a 4µm thick oxide-covered silicon.

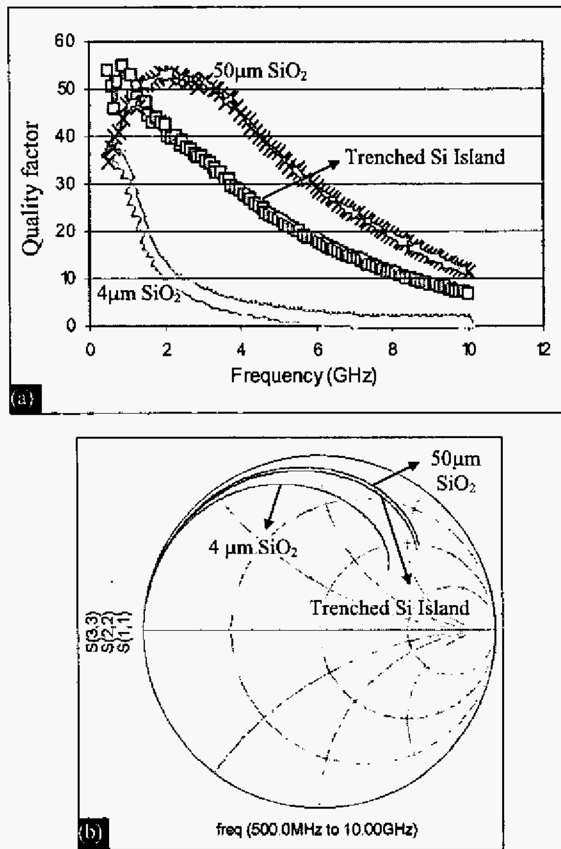

Figure 6. Comparison of (a) measured Q (b) S-parameter, using OI, TSI and 4µm oxide-covered Si substrate. (t_{metal}=25-30µm, w=60µm, d_{out}=825µm).

Figure 7 is another notable result, which specifies the role of the trench depth in reducing the substrate loss. The Q of a 1.07nH inductor on 40µm deep trenched Si island is 4× higher than the similar design (with identical metal thickness) fabricated on 10µm deep trenched-island ($Q_{40\mu m}$=32 @2.4GHz).

Sonnet simulations indicate an increase in the inductor Q with oxide thickness up to 50µm, hence justifying the need for 50µm deep trenches.

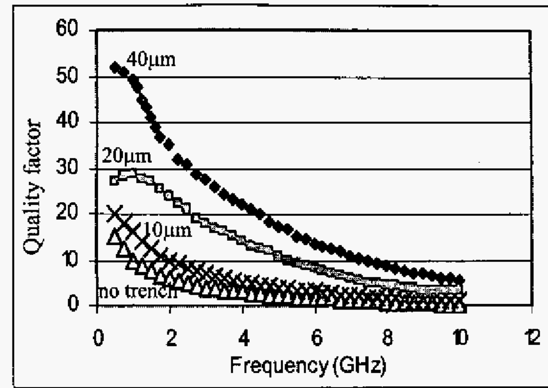

Figure 7. Measured Q vs. frequency showing dependency of Q on trench depth. (t_{metal}=15µm, w=60µm, d_{out}=833µm).

Figure 8(a) depicts the effect of the oxide thickness on the measured Q of a 0.9nH inductor on thick *OI*, indicating good agreement with simulation results (Fig. 8(b)). The modeled electrical parameters and Q of this inductor are shown in Table 1 and Fig. 9, respectively.

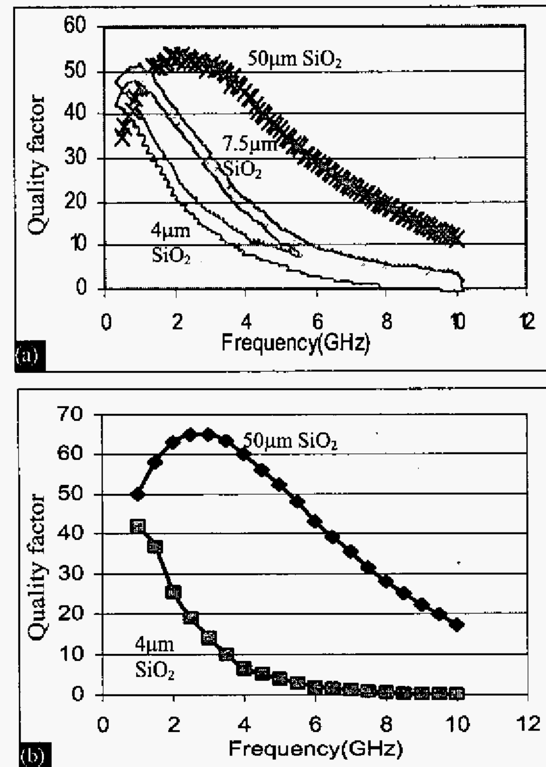

Figure 8. (a) Measured and (b) simulated Q of a 0.9nH inductor with various oxide thicknesses (t_{metal}=15µm, w=60µm, d_{out}=600µm).

Table 1. Modeled parameters of a 0.9nH inductor on OI.

f (GHz)	R_s (Ω)	L_s (nH)	R_{si} (Ω)	C_{si}(fF)	C_{ox} (pF)
1	0.139	0.9	6909	5.963	0.88
2.4	0.216	0.9	2270	5.578	0.88

Another result extracted from measurement is the negligible dependency of Q on the trenched island area. Interestingly, the change in Q is less than 10% (at 2.4GHz) if the trenched island area is extended beyond the Cu track

area ($X>0$ in Fig.10), alleviating the need for trenching the entire area beneath the inductor (Fig.10).

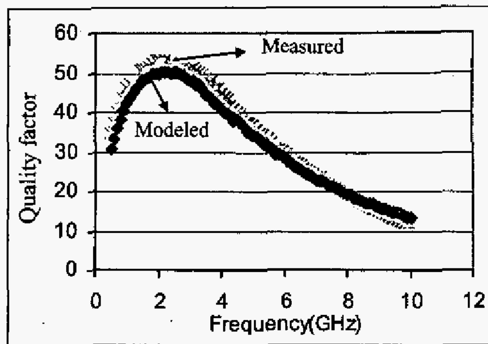

Figure 9. Measured and modeled Q of the inductor in Fig.8 using Eq.4 with k= 0.66.

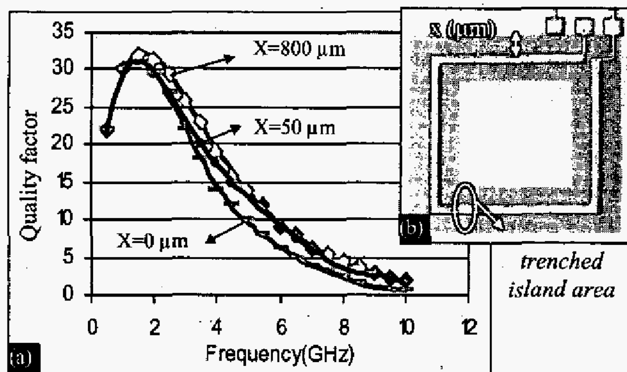

Figure 10. (a) Measured Q vs. frequency for a one-turn inductor TSI with various trenched island area.
(b) Microscope picture of the inductor showing the definition of x. (t_{metal}=30μm, w_{metal}=100μm, d_{out}=1200μm).

The Q vs. frequency plots for a one-turn Cu inductor with two different metal thicknesses is shown in Fig. 11, confirming improvement in coplanar inductor Q for metal thicknesses in excess of five times the skin depth at lower frequencies where metal loss is the dominant Q-limiting mechanism.

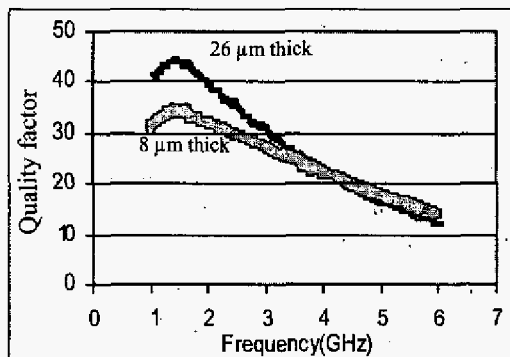

Figure 11. Measured Q of a one-turn inductor on TSI with different metal thicknesses.

It is notable that inductors fabricated on *TSI* have high embedded-Q in contrast to the suspended inductors (Fig. 12) [2]. This is due to the fact that parasitic capacitances of pads are reduced simultaneously by reduction of the substrate loss underneath the pads.

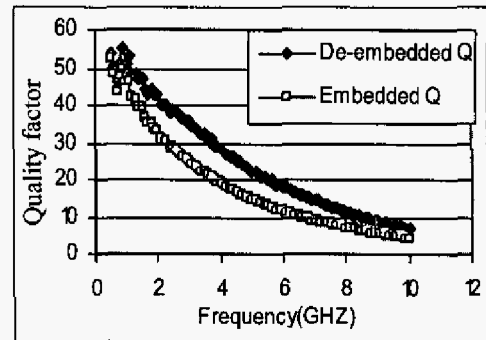

Figure 12. Comparison of embedded and de-embedded Q of a 1nH inductor fabricated on low-loss TSI.

5. CONCLUSION

A new implementation of high-Q integrated Cu inductors on CMOS-grade Si substrates using a fully CMOS-compatible process has been introduced. A new fabrication sequence has been used to reduce the loss of Si substrate at RF frequencies. Several inductors have been fabricated on this low-loss Si substrate. Measurement results indicate a significant improvement in the Q compared to the inductors fabricated on the conventional CMOS-grade Si substrates.

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