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Characterization of high-Q spiral inductors on thick insulator-on-silicon

Mina Rais-Zadeh and Farrokh Ayazi

School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250, USA

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Abstract

This paper reports on the fabrication and characterization of high quality factor (Q) copper (Cu) inductors with thick insulator on standard silicon (Si) substrate ($\rho = 10$–$20\ \Omega$ cm). The thickness and the area of the insulating layer are optimized for high Q by fabricating inductors on very thick ($\sim$50 μm) embedded silicon dioxide (SiO_2) islands and 4–20 μm thick PECVD SiO_2 coated standard Si substrate. The effect of the dielectric permittivity is verified by comparing the performances of identical inductors fabricated on 20 μm thick SiO_2 and 20 μm thick low-k polymer coated standard Si substrate. Measurement results show saturation behavior for the inductor Q versus the area and the thickness of the insulating layer. A 0.9 nH inductor fabricated on a 50 μm thick embedded oxide island (OI) exhibits a high peak Q of 53 at 2 GHz. The Q of an identical inductor on 20 μm thick PECVD SiO_2 is 45 at 2 GHz.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

High-Q integrated inductors are widely used to improve the performance of advanced RF integrated circuits such as voltage-controlled oscillators [1], low noise amplifiers [2], power amplifiers [3], mixers, filters and matching networks. The quality factor of on-chip inductors is limited by the loss mechanisms that convert the electromagnetic energy into heat. There are two separate sources of loss in inductors: the metal loss and the substrate loss. Therefore, the unloaded Q of an inductor can be expressed by [4]:

$$\frac{1}{Q} = \frac{1}{Q_{\text{substrate}}} + \frac{1}{Q_{\text{metal}}}, \tag{1}$$

where $Q_{\text{substrate}}$ and Q_{metal} represent the substrate loss and the Ohmic loss of metal strips, respectively. While metal loss can be reduced by using thick high-conductivity metals, the loss of Si substrate has remained the major barrier in reaching Q's comparable to that of off-chip inductors. Micromachining techniques have been utilized to improve the $Q_{\text{substrate}}$. Approaches taken to reduce the substrate loss and increase the Q can be summarized as the use of a thick insulating layer, whether by suspension of the inductor [5–7] or by the use of a thick dielectric [8–10]. The substrate loss is known to decrease with increasing thickness of the insulating layer [11, 12]. However, there is a saturation thickness for the dielectric beyond which the Q remains constant. On the other hand, the electromagnetic field produced by the current flowing in the inductor vanishes in the close vicinity of the edge of the inductor (tens of microns), resulting in saturation behavior for the inductor Q versus the area of the insulating layer (figure 1). This saturation behavior alleviates the need to insulate the entire area beneath the inductor. This is of special importance when an upper limit exists on the area of the insulating layer due to the processing constraints.

Very little work has been done so far to characterize and optimize the dielectric saturation thickness and area [13]. This paper investigates the effect of the thickness, area and the permittivity of the insulating layer on the inductor performance. The thickness and the area of the insulating layer are characterized by fabricating several spiral-type inductors on thick embedded SiO_2 as well as on thick PECVD SiO_2 coated standard Si substrate. The saturation thickness and the optimum area of the insulating layer are extracted from the measurement results. To investigate the effect of the substrate permittivity, the performances of inductors fabricated on 20 μm thick PECVD SiO_2 and 20 μm thick low-k polymer coated standard Si substrate are compared. Experimental results are in excellent agreement with Sonnet electromagnetic simulations [14].

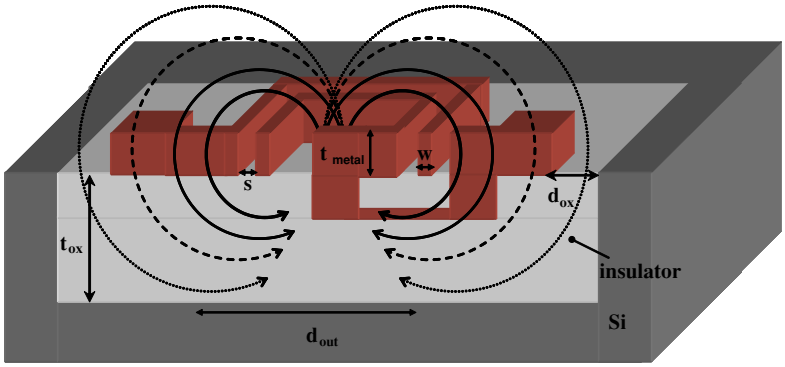


Figure 1. Inductor schematic showing the electromagnetic field.

2. Fabrication

To characterize the effect of the insulating layer on the inductor Q, three types of thick insulating layers are created on and in the Si substrate using micromachining techniques: thick embedded oxide islands, thick PECVD SiO_2 and thick Avatrel polymer [15]. Planar Cu inductors are then fabricated on these pre-processed substrates using the surface micromachining technique introduced in [9].

2.1. Thick embedded oxide islands

In the main approach, a bulk micromachining technique is utilized to create very thick embedded oxide islands (OI) in the standard Si substrate (ρ = 10–20 Ω cm). The embedded OI is realized by etching deep high aspect-ratio (25:1) trenches in select areas of the Si substrate and subsequently oxidizing the Si left in between the trenches at 950 °C [16, 17]. 2 μm thick PECVD SiO_2 is then deposited at 300 °C to improve the surface roughness. A brief fabrication process flow of inductors on thick embedded oxide islands is shown in figure 2. Figure 3 shows a 50 μm thick embedded OI with repeated trench and Si width of about 2 μm.

To have a void-free solid oxide island, the ratio of the trench width to the Si width should be 1:0.818. Insufficient spacing between the Si bars results in early closing of the trenches before the Si bar is fully oxidized. Continuing the oxidation process in this case causes curvature in the wafer due to the stress introduced by oxidation of the remaining Si bars. To reduce the curvature of each individual Si bar during the oxidation process, the length of the bar is reduced by introducing multiple rows and shifting the trench profile of each row with respect to the adjacent row, as shown in figure 4. Using this trench profile, low-stress oxide islands of large areas (3 mm × 3 mm) have been achieved.

The stress in the oxidized Si bars, which in the extreme case causes curving of the wafer, is also dependent on the oxidation temperature. Figure 5(*a*) shows a highly stressed OI before full oxidation of Si, when the wet oxidation temperature was 1100 °C. For comparison, the SEM picture of a low-stress OI processed at 950 °C is shown in figure 5(*b*). The trench profile and the processing parameters become critical when a large percentage of the wafer area is trenched. Therefore, the oxide island area is an important design parameter that needs to be optimized and was not studied in earlier work [7, 8]. Figure 6 shows the cross-section SEM view of a multiple-turn

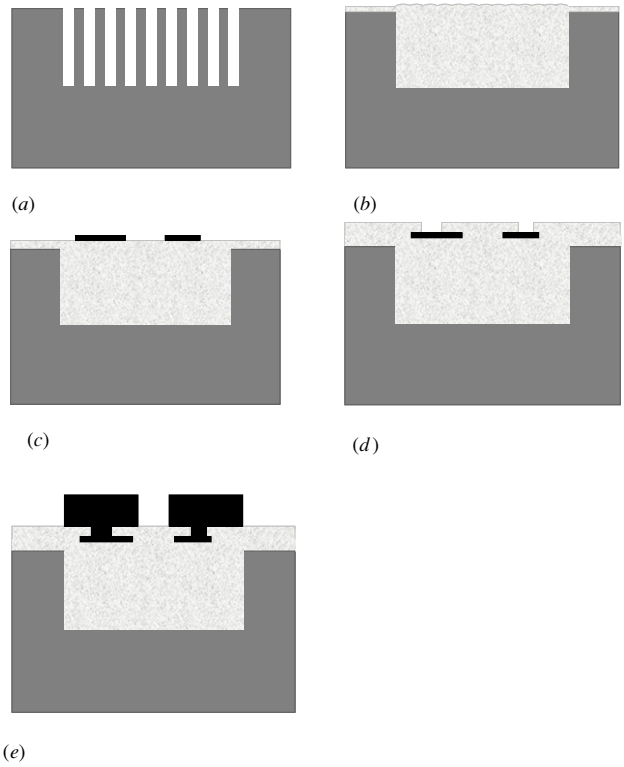


Figure 2. Fabrication process flow of inductors on oxide islands. (*a*) Etching deep trenches in Si, (*b*) oxidizing the remaining Si, (*c*) depositing and patterning the first metal layer, (*d*) depositing and patterning the interlayer dielectric and (*e*) electroplating the second metal layer.

copper inductor fabricated on a 50 μm thick embedded OI. Thick Cu (∼20 μm) is electroplated to increase the Q_{metal} and reduce the effect of metal loss on the inductor performance.

2.2. Thick PECVD SiO_2 coated Si

Although the thick embedded OI has a significant effect on the reduction of the Si substrate loss, the high processing temperature makes it incompatible for post-CMOS processing [8]. The alternative low-temperature approach to create a thick oxide layer is PECVD SiO_2 deposition at 300 °C with a typical deposition rate of 4 μm h^{-1}. The SiO_2 film thickness that can be deposited using the PECVD process is limited, due to the thermal stress introduced between the thick SiO_2 layer and the

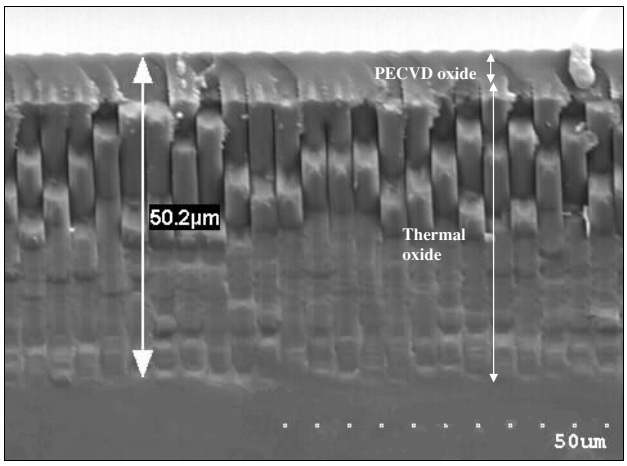


Figure 3. SEM views of a 50 μm thick oxide island showing the smooth surface (oxidation temperature: 950 °C).

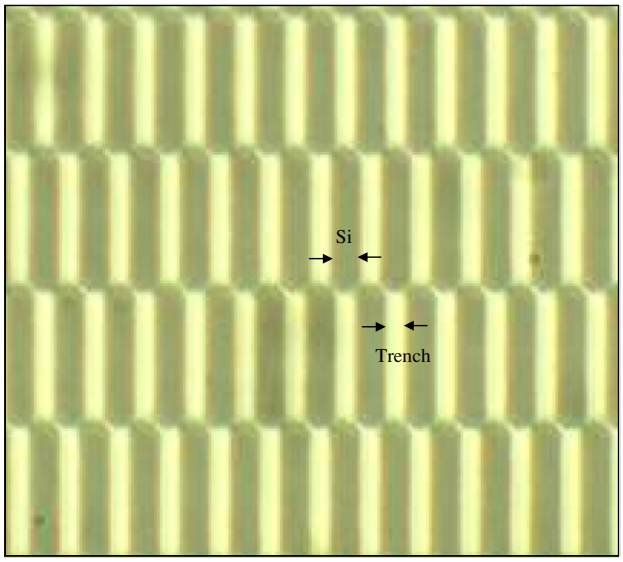
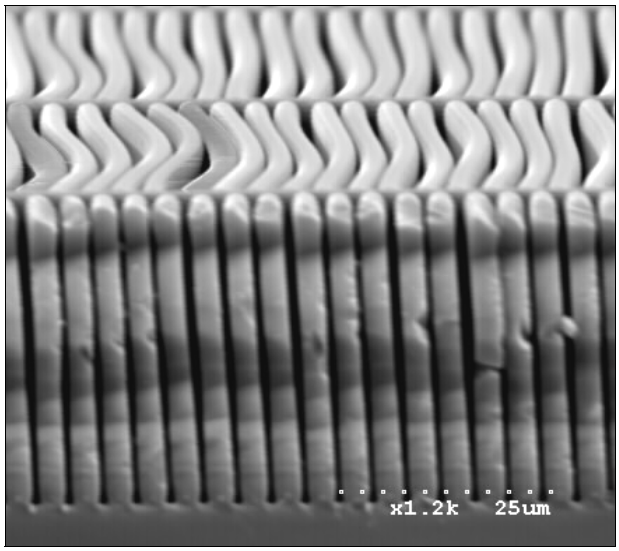


Figure 4. Microscope picture of the trenched area, showing the position of each Si bar with respect to adjacent bars.

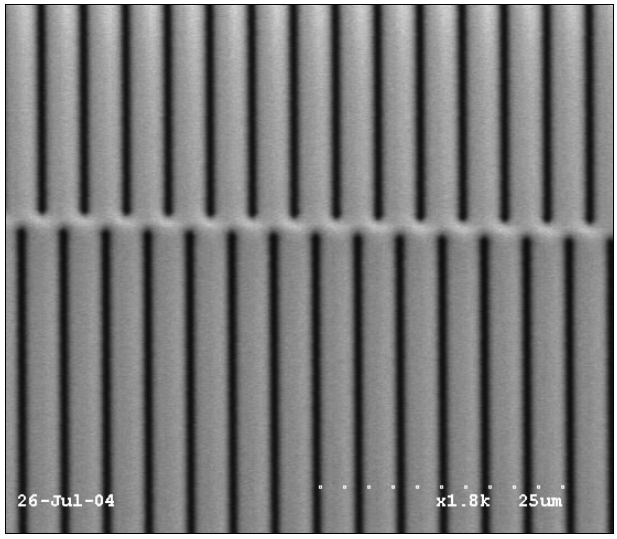
Si substrate. To lower the thermal stress in this work, a 20 μm thick oxide layer is created by repeated deposition of a 4 μm thick oxide layer. Figure 7 shows SEM pictures of a 3.3 nH inductor on a 20 μm thick SiO_2 coated Si substrate.

2.3. Thick low-k polymer coated Si

To study the effect of the dielectric permittivity, inductors are also fabricated on a 20 μm thick low-k polymer spin coated on standard Si substrate. Avatrel 2000P polymer from Promerous Inc. has been selected for this purpose as it has a low dielectric permittivity compared to other dielectric materials [15]. Table 1 compares the electrical properties of Avatrel with two other low-k dielectrics commonly used as insulating layers, showing the small relative permittivity and loss-tangent of this material [18]. Following the spin-coating, the Avatrel polymer is cured at 110 °C and 1 μm thick SiO_2 is deposited at 160 °C to promote the adhesion of successive metallic layers to the polymer. The deposition temperature of SiO_2 is reduced (from 300 °C to 160 °C) to avoid bubbling of the Avatrel.



(*a*)



(*b*)

Figure 5. (*a*) Cross-section SEM view of a highly stressed oxide island (oxidation temperature: 1100 °C), and (*b*) top view of a low stressed OI (oxidation temperature: 950 °C).

Table 1. Comparison of electrical properties of Avatrel with BCB and polyimide [18].

	Avatrel	Polyimide	BCB
tan δ at 1 GHz	0.009	0.01–0.015	0.015
Permittivity (ε_r)	2.55	3.1–4.1	2.7
Moisture uptake	<0.1%	0.5–3%	0.23%

3. Measured results and discussion

Several spiral-type inductors of various shapes and dimensions were fabricated and tested on 50 μm thick OI, 4–20 μm thick PECVD SiO_2 and 20 μm thick Avatrel coated standard Si substrate (ρ = 10–20 Ω cm). On-wafer S-parameter measurements were carried out using an *hp*8517B vector network analyzer and ground–signal–ground Cascade micro-probes. The pad-only characteristics were measured on the

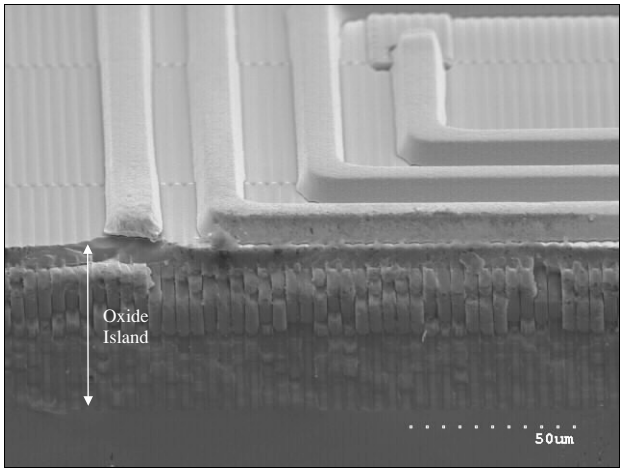
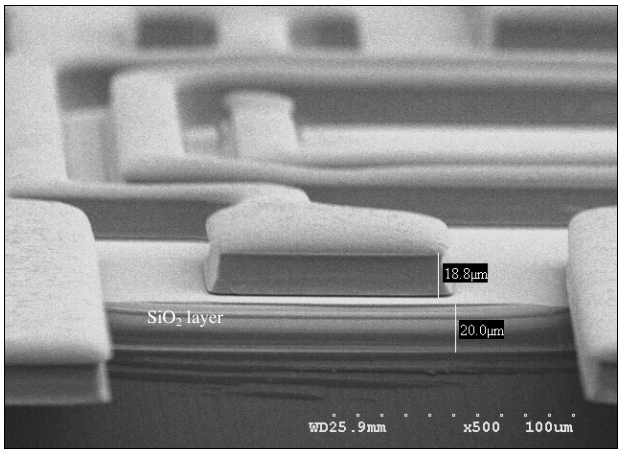


Figure 6. SEM picture of a three-turn inductor on top of OI ($w = 15\ \mu$m, $d_{out} = 300\ \mu$m, $t_{metal} = 20\ \mu$m).



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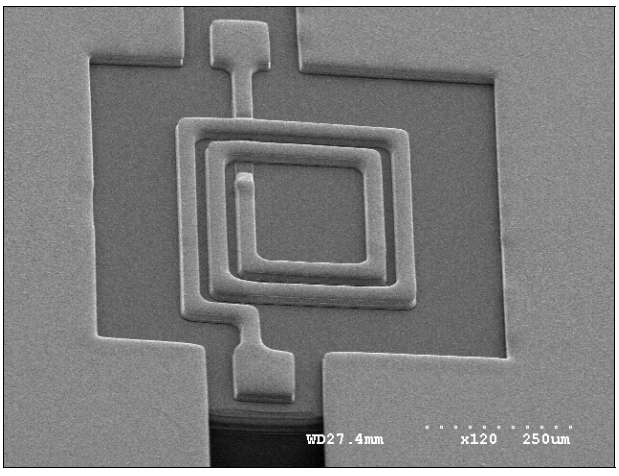
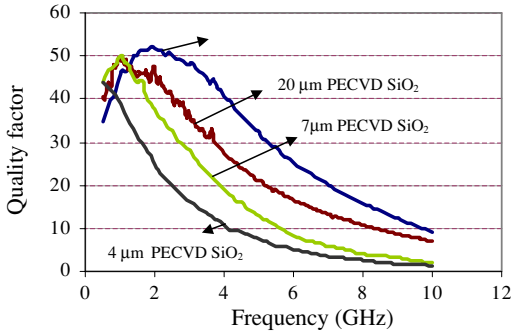


(*b*)

Figure 7. (*a*) Cross-section and (*b*) top SEM view of a 3.3 nH Cu inductor on 20 μm thick PECVD SiO_2 ($t_{metal} = 1.5\ \mu$m, $n = 2.5$, $w = 20\ \mu$m, $s = 20\ \mu$m and $d_{out} = 400\ \mu$m).

open pad structures and de-embedded from the overall inductor characteristic by subtracting the *Y*-parameters of the pads from the *Y*-parameters of the embedded inductors [19].



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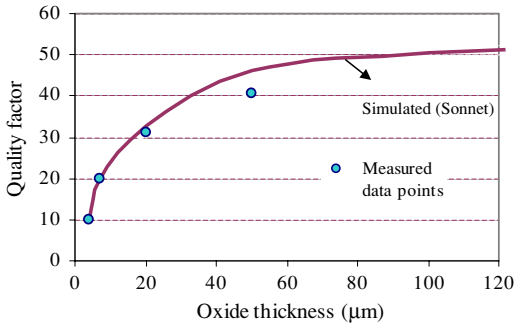

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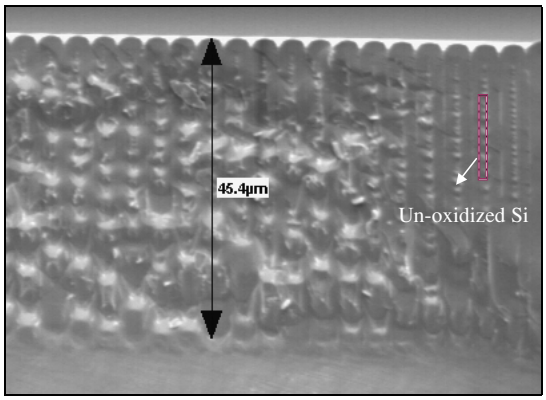


(*c*)

Figure 8. (*a*) Measured *Q* of a 1 nH inductor with various oxide thicknesses, (*b*) comparison of simulated and measured *Q* at 4 GHz and (*c*) cross-section SEM picture of OI showing the incomplete oxidation of Si ($t_{metal} = 20\ \mu$m, $w = 60\ \mu$m, $d_{out} = 600\ \mu$m).

Figure 8(*a*) shows the *Q* of a one-turn 1 nH inductor with various oxide thicknesses. The similar performance observed in the low frequency range ($f < 2$ GHz) is due to the metal loss limitation on the *Q* [4, 9]. At higher frequencies, where the substrate loss is dominant, *Q* increases with increasing oxide thickness. Figure 8(*b*) compares the simulated and the measured *Q* of this inductor at 4 GHz, showing excellent agreement for oxide thickness of up to 20 μm. The deviation of the measured *Q* value from the simulated *Q* for the inductor on 50 μm thick OI is due to the incomplete oxidation of Si (figure 8(*c*)). On account of the agreement observed between simulations and measurements, inductors were not fabricated on thicker oxide islands.

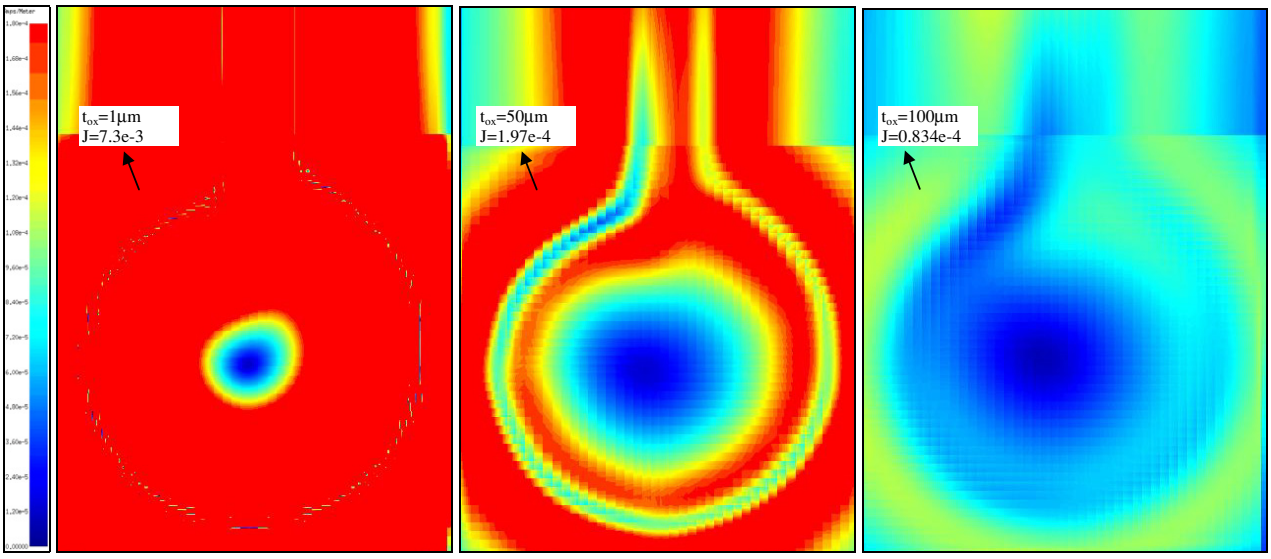
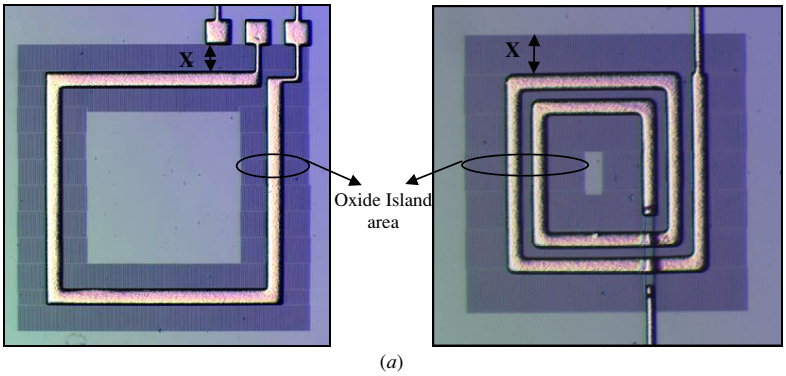


Figure 9. Current density at the common surface of oxide and Si for an inductor fabricated on (*a*) 1 μm, (*b*) 50 μm and (*c*) 100 μm thick oxide coated standard Si substrate at 5 GHz ($t_{\text{metal}} = 20$ μm, $w = 60$ μm, $d_{\text{out}} = 600$ μm).



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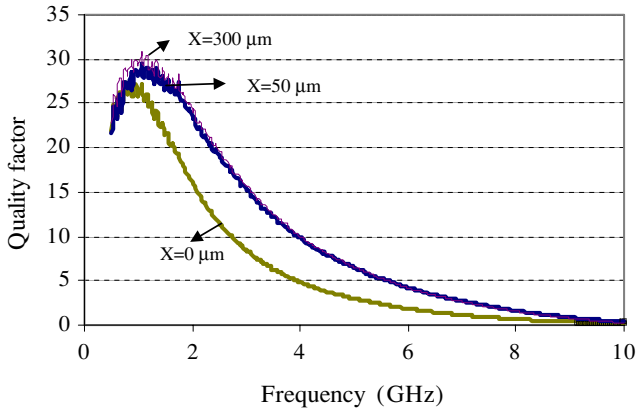


(*b*)

Figure 10. (*a*) Microscope picture of the inductor showing the definition of X, and (*b*) measured Q versus frequency for a 0.8 nH inductor on OI with various oxide areas ($t_{\text{metal}} = 30$ μm, $w_{\text{metal}} = 60$ μm, $d_{\text{out}} = 820$ μm).

The notable result extracted from simulations and measurements is the saturation behavior of the Q versus the oxide thickness. As shown in figure 8(*b*), Q slightly increases with the oxide thickness beyond 50 μm. Sonnet electromagnetic simulations were carried out to verify the measurement results by determining the density of the unwanted current flowing at the common surface of the oxide layer and the Si substrate [20]. The density of the current flowing in the substrate represents the intensity of the substrate loss [9]. Figure 9 shows the current density (J) flowing at the

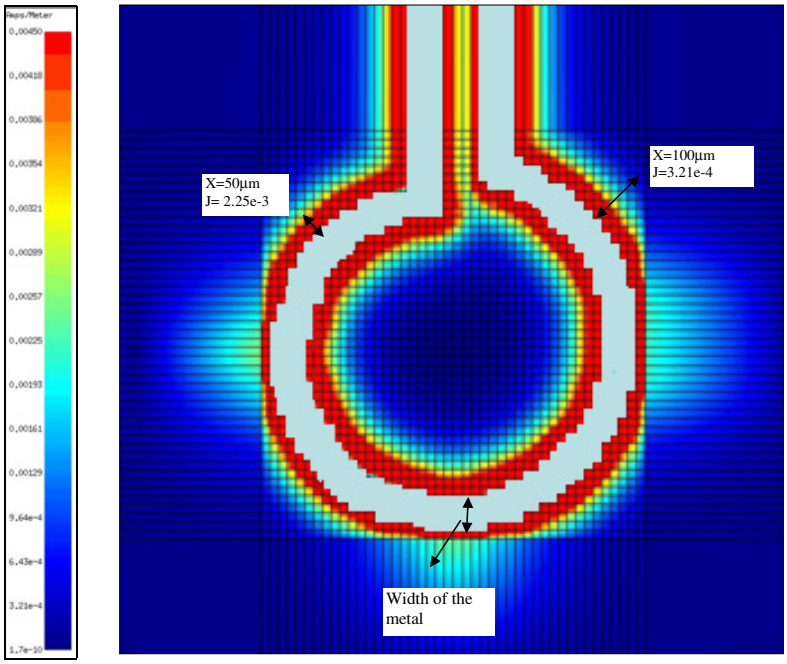


Figure 11. Current density at the depth of 1 μm beneath the inductor in figure 10 ($t_{oxide} = 50\ \mu$m, $f = 5$ GHz).

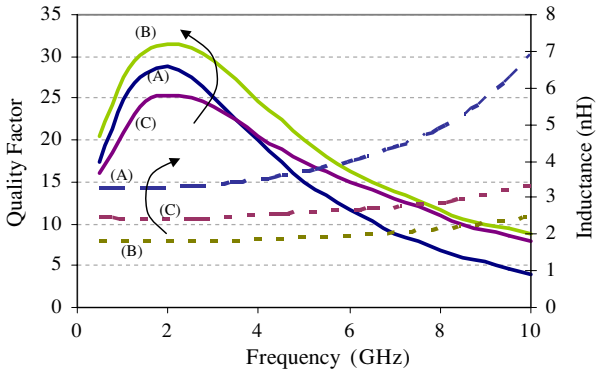
Table 2. Specification of multiple-turn inductors.

Type	$t_{metal\,1}$ (μm)	$t_{metal\,2}$ (μm)	w (μm)	s (μm)	n	d_{out} (μm)	L (nH)
A	1.5	19	20	20	2.5	400	3.00
B	1.5	19	40	20	2.5	400	1.80
C	1.5	19	20	20	3	360	2.6

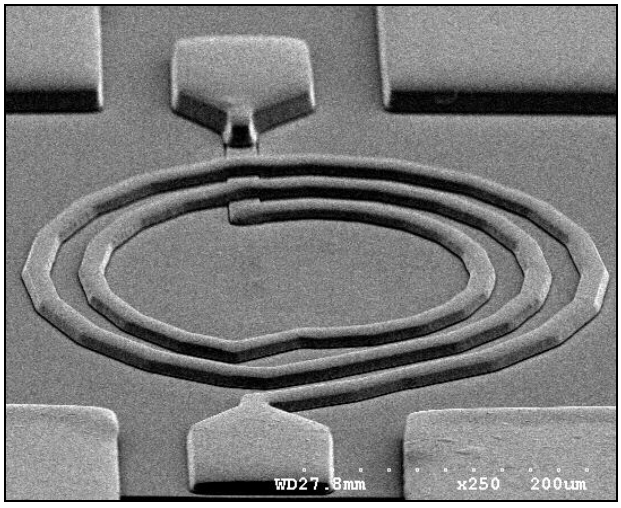
bottom surface of (a) 1 μm, (b) 50 μm and (c) 100 μm thick oxide layer. As shown in figure 9(c), the current density at the depth of 100 μm is much less than the current density at the depth of 50 μm (figure 9(b)). Therefore, at a thickness of 50 μm the quality factor reaches 91% of its final value and further increase in the SiO_2 thickness does not significantly affect the Q. The saturation thickness of the insulator depends on the inductor geometry, size and frequency of operation. For inductors with wider metal strips, the saturation thickness is greater due to the larger parasitic capacitance between the inductor structure and the lossy Si substrate.

Another interesting result extracted from the measurement is the dependence of Q on the oxide island area. A negligible change in Q is observed when the oxide area is extended too much beyond the Cu track area (X in figure 10(a)), alleviating the need for oxidizing the entire area beneath the inductor (figure 10(b)). Figure 11 illustrates the current density flowing in the oxide layer at the depth of 1 μm beneath this inductor. As is shown, the current density at $X = 50\ \mu$m is 10$\times$ higher than the current density at $X = 100\ \mu$m, demonstrating the negligible change in Q for $X > 50\ \mu$m.

To further characterize the effect of the substrate loss, larger size inductors having multiple turns are also fabricated on 20 μm thick SiO_2 coated standard Si substrate. Specifications of the fabricated inductors are shown in table 2. As shown in table 2, the thickness of the first metal layer (routing layer) is about 1.5 μm and thus the sheet resistance



(a)



(b)

Figure 12. (a) Measured Q and inductance of multiple-turn inductors on 20 μm thick PECVD SiO_2 ($t_{metal\,1} = 1.5\ \mu$m, $t_{metal\,2} = 20\ \mu$m) and (b) SEM picture of the inductor type (A).

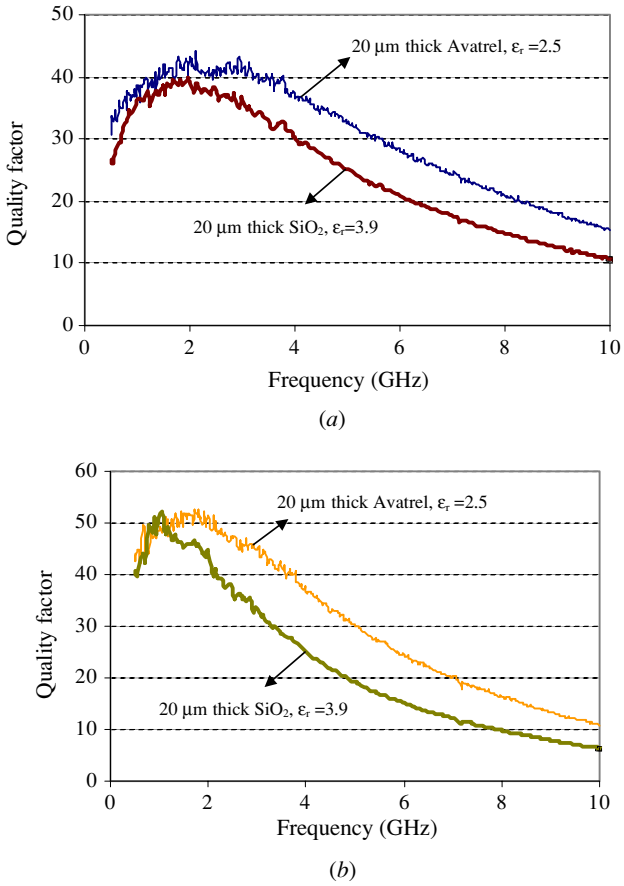


Figure 13. (a) Measured Q of identical inductors on 20 μm thick oxide and 20 μm thick Avatrel coated standard Si substrate (a) $w = 50$ μm, $d_{\text{out}} = 500$ μm, $t_{\text{metal}} = 20$ μm, and (b) $w = 60$ μm, $d_{\text{out}} = 600$ μm, $t_{\text{metal}} = 20$ μm.

of the first metal layer is about 13 times higher than that of the second metal layer. Although the first metal layer is very thin, the quality factor of the multiple-turn inductors is lower than the single-turn inductors due to the Ohmic loss of the first metal layer. Figure 12 compares the performances of inductor types A, B and C. The following has been extracted from the measured data shown in figure 12:

(1) Comparison of inductors A and B shows that inductors with wider metals have higher Q but lower inductance [21].
(2) Smaller size inductors have superior performance at higher frequencies due to their lower substrate loss (inductor A compared to inductor C).

The effect of the insulating layer permittivity is also verified. Figure 13 shows the measured Q of two different types of inductors fabricated on 20 μm thick oxide and 20 μm thick Avatrel coated Si substrate. At high frequencies ($f > 4$ GHz), Q of inductors on Avatrel is higher due to their reduced substrate loss. As shown in figure 13(b), the peak Q of a 0.9 nH inductor is 52 at 2 GHz when the Si substrate is passivated with 20 μm thick Avatrel, while the Q of the exact same inductor fabricated on 20 μm thick oxide is 45 at 2 GHz.

4. Conclusion

High-Q integrated Cu inductors were fully characterized on thick insulator on Si. Thick oxide islands were employed to characterize the effect of the dielectric area on the inductor performance. Measurement results show saturation behavior for the inductor Q versus the dielectric area. For one-turn inductors, negligible change in Q was observed when the oxide area was extended beyond 50 μm from the edge of the inductor. On the other hand, the optimum value of the insulator thickness was obtained by fabricating the inductors on thick PECVD oxide and oxide islands. It was found that the oxide thickness required to effectively reduce the Si loss depends on the inductor geometry and size, and was about 50 μm in this work. The measurement results were verified by Sonnet electromagnetic simulations. The effect of the insulator permittivity on the quality factor of on chip inductors was studied by fabrication of identical inductors on 20 μm thick low-k polymer and 20 μm thick PECVD oxide. Measurement results show superior performance for inductors fabricated on low-k insulating layer due to their reduced substrate loss.

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