Non-linear Characteristics of Passive Elements on Trap-Rich High-Resistivity Si substrates

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***Abstract* — RF losses and non-linear behavior of RF passive elements such as coplanar transmission lines and inductors are analyzed. The investigated trap-rich HR-Si wafers with a fixed oxide layer of 150 nm-thick show true effective resistivity values higher than 4 kΩ-cm up to 5 GHz and harmonic distortion levels lower than -90 dBm for a 900 MHz input with signal level of +25 dBm. High quality factor of 60 is measured for a 2 nH inductor on a trap-rich HR-Si substrate at 2.73 GHz frequency of operation. Our investigations confirm the capability of trap-rich HR-SOI wafer for the integration of passive elements for RF systems.**

***Index Terms* — RF integration, high resistivity (HR) Si, Silicon-on-Insulator (SOI), non-linearity, trap-rich, HR-SOI, SoC.**

I. Introduction

Advanced CMOS technologies provide the opportunity of low-cost integration of analog, digital, and RF functions on the same wafer for System-on-Chip (SoC) applications [1]. Silicon-on-Insulator (SOI) technologies offer added design advantages that include reduced substrate crosstalk and easy integration of high quality passive elements [2]. The presence of the buried oxide layer offers the flexibility of using high resistivity substrate (HR-Si) leading to substantially reduced substrate RF losses. It has been demonstrated in [3] that HR-Si must present an effective resistivity as high as 3 kΩ.cm to be considered low loss for RF applications. However, oxidized HR-Si substrate suffers from parasitic surface conduction (PSC) due to fixed oxide charges which attract free carriers near the Si/SiO_2 interface, thereby reducing the substrate effective resistivity (ρ_{eff}) of the wafer by more than one order of magnitude than the bulk nominal resistivity [3], [4]. In addition, the non-linear behavior of HR-Si substrate increases due to PSC effect and the generated harmonics by the passive components can have higher power levels than those from RF switches or other active devices fabricated on HR-SOI [5], [6]. Several technological solutions have been developed to reduce these parasitic effects and enhance the HR properties of Si handle wafer. The introduction of a trap-rich layer such as amorphous silicon (α-Si) or polycrystalline silicon (polySi) [4], [7] has been proved as the most effective techniques while being compatible with industrial SOI fabrication and standard CMOS process [8].

Transmission lines and integrated inductors are widely used in RF integrated circuits such as voltage controlled oscillators [9], low noise amplifiers [10], power amplifiers [11], mixers, filters and matching networks. The quality factor (Q) of on-chip inductors is limited by metal losses and substrate losses. While metal loss can be reduced by using thick conductivity metals, the loss in substrate has remained the major drawback to reach Q's comparable with off-chip inductors on Si [12]. HR-Si substrate with a trap-rich layer can improve the Q by reducing the eddy current losses in the substrate. The trap-rich layer consists of a polySi layer between the BOX and the HR-Si handle wafer to literally "freeze" the excess of carriers attracted at the Si surface.

The non-linear behavior of CPW transmission lines on Si substrates has been already addressed in [6]. However, the harmonic products generated at integrated inductors on Si due to substrate nonlinearities have never been shown.

This paper investigates the efficiency of trap-rich HR-Si technique in reducing the insertion loss of coplanar waveguide (CPW) line, reducing non-linear behavior of the silicon substrate, and enhancing the quality factor of integrated inductors.

II. Experiments

The passivation efficiency of polysilicon trap-rich layer is investigated using coplanar waveguide (CPW) and integrated spiral inductors. Standard HR-Si (10 kΩ.cm)

substrate is compared with polysilicon trap-rich HR-Si wafer. To provide a high density of traps between the HR-Si handle wafer and the oxide layer we deposited by low pressure chemical vapor deposition (LPCVD) at 625°C a 450 nm-thick polysilicon layer. On both wafers, a 150 nm-thick thermal oxide was grown at 950°C partially consuming the polysilicon layer. The resulting trap-rich layer thickness is 330 nm. The numerous traps created by silicon dangling bonds in polysilicon are able to absorb the free carriers attracted at the SiO_2/Si interface and greatly reduce substrate losses. A 1 µm-thick aluminum layer was then deposited and patterned to form a 50 Ω CPW line. Its dimensions are, respectively, 26, 12 and 208 µm for central, slot space and ground plane. Various inductors are designed and fabricated on HR-Si substrate with (TR) and without (HR) polySi trap-rich layer using the fabrication process described in [13]. The designed 2 nH inductor considered in this paper is fabricated using 40 µm-thick Cu metal layer to obtain sufficiently low ohmic resistance required to observe the effect of the trap-rich layer.

On-wafer small- and large-signal measurements were performed on each passive device using a dedicated setup [6] based on an Agilent 4-port PNA-X vector network analyzer.

III. CPW LINE RF PERFORMANCE

The RF measurements of the CPW line were carried up to 10 GHz and the effective resistivity (ρ_{eff}) of the wafers were extracted from the measured S-parameters using the method depicted in [3]. The extracted effective resistivity in Fig. 1 confirms the true high resistivity (> 4 kΩ.cm) up to 5 GHz of the wafer compared with only 200 Ω.cm for the oxidized HR-Si substrate. It is worth noticing that the nominal resistivity of the initial bulk HR-Si is 10 kΩ-cm, 50 times higher than the resistivity finally seen by the CPW. Such low effective resistivity of HR-Si without the trap-rich layer is explained by the presence of a highly conductive inversion layer underneath the oxide layer. The high ρ_{eff} on the trap-rich HR-Si wafer makes Si material a viable solution for RF integrated SoC applications.

Regarding their linear behavior, CPW harmonic distortions are lower than -90 dBm for an input power of +25 dBm as depicted in Fig. 2. The total harmonic distorsion corresponds to the detected 2nd harmonic component at the output of a 2,146 µm-long CPW when a signal at 900 MHz is injected at the input. The HR-Si non-linear behavior is mainly due to the modulated charge density at the Si/SiO_2 interface. The parasitic surface electron inversion layer change the distribution of free carriers inside the silicon substrate, thereby modulate its correspondent nonlinear capacitance and conductance [5]. The trap-rich polysilicon layer stabilizes the surface potential at the Si/SiO_2 interface and the applied large RF signal does not change the carrier distribution inside the substrate. As shown in [6] there is a correlation between the effective resistivity and the degree of non- linearity introduced by the substrate.

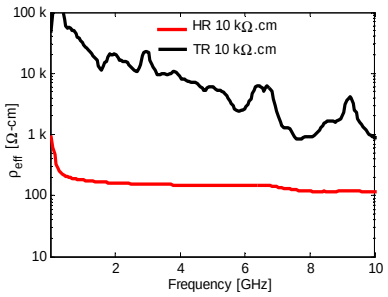

Figure 1. Effective resistivity vs. frequency on HR-Si and polySi trap-rich (TR)

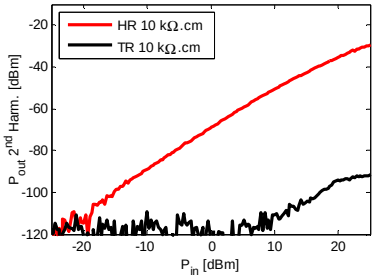

Figure 2. Harmonic distorsion of CPWs on HR-Si and polySi trap-rich (TR) substrates.

IV. INDUCTORS ON TRAP-RICH HR-SI

The impact of passivation polysilicon layer on the Q factor and non-linear behavior of 2 nH single-turn circular inductor is investigated. The inductor is designed to have its peak Q at frequency beyond 2.5 GHz. The measurement results on the trap-rich HR-Si in Fig. 3 show a much higher Q compared with the standard HR-Si when a thick Cu layer is used. The maximum Q on 10 kΩ.cm trap-rich HR-Si is more than 60 at 2.73 GHz while it is only 35 at 1 GHz on standard HR-Si.

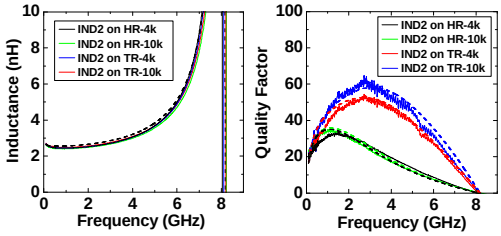

Figure 3. Measured (left) inductance and (right) Q of 2 nH_IND on HR-Si and TR-Si (the dashed line is the simulation result using the lumped element model presented in [14]).

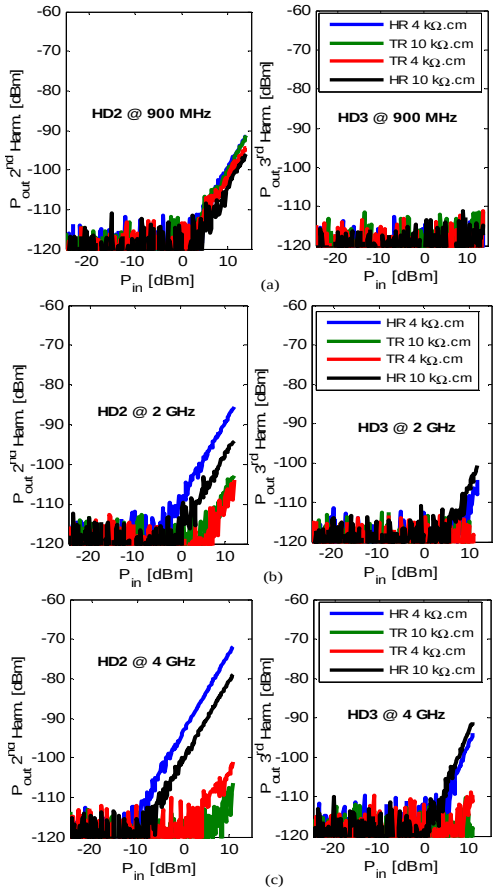

Figure 4. Harmonic distorsion of 2 nH inductor @ fund. tone (a) 900 MHz, (b) 2 and (c) 4 GHz on HR-Si and polySi trap-rich (TR).

As expected the HR-Si substrate has higher harmonic level than the trap-rich HR-Si when the input frequency is close to the inductor operation frequency. The second and third order harmonics (HD2 and HD3) were measured on both wafers, i.e. HR-Si and trap-rich HR-Si (TR) for three different input fundamental frequencies, 900 MHz, 2 GHz and 4 GHz. Fig. 4 (a) shows HD2 level at -90 dBm and HD3 close to the noise floor level when an input fundamental frequency is 900 MHz on both wafers. The non-linear behavior increases on HR-Si substrate when the input fundamental frequency increases to 2 and 4 GHz as shown in Fig. 4 (b) and (c). The passivated trap-rich HR-Si wafer maintains its low harmonic levels over the whole frequency range. These results correlate with the measured quality factor, i.e. reduction of harmonics with the increase of the quality factor.

V. Conclusion

Analysis of RF performance and non-linearity behavior of trap-rich HR-Si wafer show superior characteristics over standard HR-Si substrate. Their true high-resistivity and excellent linear properties convert them to an ideal substrate of choice for the integration of wireless and RF transceivers into SoC. In fact, measurement results indicate a significant improvement such as reduced substrate RF losses, higher linearity and larger inductor Q on the trap-rich passivated HR-Si substrate.

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