WAFER-LEVEL ENCAPSULATED HIGH-PERFORMANCE MEMS TUNABLE PASSIVES AND BANDPASS FILTERS

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WAFER-LEVEL ENCAPSULATED HIGH PERFORMANCE MEMS TUNABLE PASSIVES AND BANDPASS FILTERS

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To my family

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

LIST OF SYMBOLS

Aº	Angestrom
c	Centi-
C	Centigrade
ε_r	Permittivity
f	Femto-
F	Farad
G	Giga-
Hz	Hertz
k	Kilo-
K	Kelvin
m	Meter
M	Mega-
μ	Micro-
n	Nano-
Ω	Ohm
p	Pico-
Pa	Pascal
ρ	Resistivity
S	Siemens
sec	second
V	Volt
W	Watt

LIST OF ABBREVIATIONS

Ag	Silver
BAW	Balk acoustic wave
C	Capacitance
Cr	Chromium
DRIE	Deep reactive ion etching
EM	Electromagnetic
f_0	Center frequency
GSG	Ground-signal-ground
GSM	Global system for mobile communications
HARPSS	High-aspect-ratio polysilicon and single crystal silicon
HF	High frequency
HRS	High-resistivity silicon
ICP	Inductively coupled plasma
L	Inductance
LNA	Low-noise amplifier
LPCVD	Low-pressure chemical vapor deposition
LRRM	Line-reflection-reflection-match
MEM	Microelectromechanical
MEMS	Microelectromechanical systems
MIM	Metal-isulator-metal
PA	Power amplifier
PECVD	Plasma-enhanced chemical vapor deposition
Q	Quality factor

RF	Radio frequency
RIE	Reactive ion etching
SAW	Surface acoustic wave
SEM	Scanning electron microscope
SHF	Super high frequency
Si	Silicon
SOI	Silicon on insulator
SOLT	Short-open-load-through
SRF	Self-resonance frequency
Ti	Titanium
UHF	Ultra high frequency
VCO	Voltage-controlled oscillator
VHF	Very high frequency
VNA	Vector network analyzer

SUMMARY

This dissertation reports, for the first time, on the design and implementation of tunable micromachined bandpass filters in the ultra high frequency (UHF) range that are fully integrated on CMOS-grade (ρ = 10-20 Ω.cm) silicon. Filters, which are designed in the Elliptic and coupled-resonator configuration, are electrostatically tuned using tunable microelectromechanical (MEM) capacitors with laterally movable interdigitated fingers. Tunable filters and high-quality factor (Q) integrated passives are made in silver (Ag), which has the highest conductivity of all materials in nature, to reduce the ohmic loss. The loss of the silicon substrate is eliminated by using micromachining techniques. The combination of the highest-conductivity metal and a low-loss substrate significantly improves the performance of lumped components at radio frequencies (RF), resulting in an insertion loss of 6 dB for a tunable lumped bandpass filter at 1075 MHz with a 3 dB-bandwidth of 63 MHz and tuning range of 123 MHz. The bandpass filters are encapsulated at the wafer level using a low-temperature, thermally released, polymer packaging process. This thesis details the design, fabrication, and measurement results of the filters and provides strategies to improve their performance. The performance of filter components, including the tunable capacitors and inductors, is characterized and compared to the state-of-the-art micromachined passive components. The silver inductors reported in this thesis exhibit the record high Q, and the silver bandpass filters show the minimum insertion loss that has been achieved on a CMOS-grade silicon substrate, to the best of our knowledge. Alternatively, tunable capacitors can be made in the bulk of silicon using a modified version of the high-aspect-ratio polysilicon and single crystal silicon (HARPSS) fabrication technique to obtain a larger capacitance density at the expense of a higher conductive loss. Using this process, a 15 pF two-port tunable capacitor is fabricated and tuned by 240% with the application of 3.5 V to the

isolated actuator. Silver inductors can be post integrated with HARPSS tunable capacitors to obtain tunable filters in the very high frequency (VHF) range. The reported bandpass filters can be monolithically integrated with CMOS and have the potential to replace several transmit and receive acoustic filters currently used in cellular phones.

CHAPTER 1

INTRODUCTION

Recent developments in wireless communications have resulted in handheld cellular phones that can utilize up to seven different wireless standards or bands, including GSM, EGSM, CDMA, WCDMA, GPS, DCS, PCS, and Wi-Fi [1]. Each standard has its own characteristics and constraints. Meeting the stringent RF standards for several bands has greatly increased the complexity of the RF front-end. Adding switches or other components at the front-end of the phone to efficiently route signals creates loss and distortion that impairs performance or increases power consumption. In other words, any component placed between the antenna and the first low-noise amplifier (LNA) results in a higher noise figure, which impacts the overall radio sensitivity. Moreover, the battery life is heavily influenced by the power consumption of the power amplifier (PA). Therefore, any low-Q component used in the PA dissipates power, further reducing the battery life. Thus, a tunable filter technology that can deliver the minimum loss with high linearity while drawing no additional power and occupying the smallest possible area is desired. In addition, this technology should be capable of further integration with a transceiver or other active components.

Currently, most of the high-Q bandpass filters used in cellular modules are realized using off-chip, acoustic-resonant components, such as surface acoustic wave (SAW) devices [2]. While acoustic filters offer very low insertion loss and high quality factor and occupy a small area, they cannot be tuned, and therefore many transmit and receive filters are needed to cover multiple frequency bands. In addition, most acoustic filters require matching networks to efficiently interface with the wireless module [3]. Also, off-chip acoustic components must interface with integrated electronics at the board level. Board-level integration introduces additional loss and creates a bottleneck to the

miniaturization of the wireless modules. Therefore, integrated single-chip solutions to cellular modules are desirable. Tunable MEMS lumped LC filters can be prime candidates for multi-band cellular application if they meet the desired band specification in terms of insertion loss, out-of-band rejection, and bandwidth. Meeting these specifications is directly dependent on the Q of filter components, which should be in excess of 100 for most applications. Such high-Q passives, and specifically inductors, are not available in commercial CMOS processes. MEMS-based passives offer the possibility of achieving high-performance tunable filters that have not been available through conventional silicon technology.

There is also a significant interest in tunable MEMS components, mainly tunable capacitors, for reconfigurable matching networks [4]. Tunable passives can also be used to create wide-band PAs or adaptive antenna matching. Similarly, tunable MEMS components may be used to vary the load impedance match of a PA or LNA, ensuring that the amplifier is operating at the highest possible efficiency at all power levels, thus improving power-added efficiency or noise figure [5]. In addition, lower-frequency radio applications (20 MHz-100 MHz) require high-value tunable capacitors and inductors with relatively high quality factors and high power handling. Micromachined tunable capacitors have been shown to exhibit high quality factors with large capacitance density and high power handling, thus making them suitable candidates for VHF filters.

Figure 1 is a general schematic of an envisioned fully integrated RF transceiver, showing the possible locations where MEMS-based tunable passives and filters can be used. The focus of this thesis is on the bandpass filter that follows the antenna. Our objective is to achieve a continuously tunable filter with an insertion loss of less than 5 dB using on-chip high-Q passive components. Therefore, in this thesis, we develop a micromachining technique that is post CMOS-compatible and offers both high-Q integrated inductors and wide-tuning range tunable capacitors. In addition to the bandpass filter, these high-Q tunable passives can be applied to increase the efficiency of

load matching, to improve the performance, and to add tuning capability to the LNA, PA, and voltage-controlled oscillator (VCO). It is worth mentioning that an insertion loss of 5 dB is reasonably low for an integrated tunable MEMS filter that does not suffer from added parasitics of board interconnects.

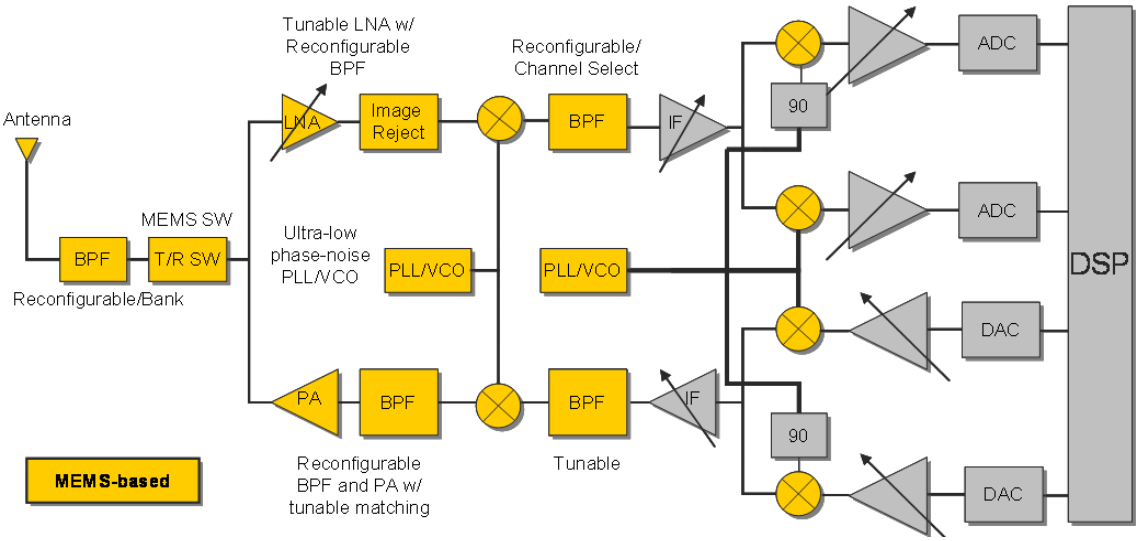


Figure 1: General schematic of a RF transceiver, showing the possible use of MEMS-based devices.

However, some challenges exist when using MEMS devices. For instance, tunable MEMS components and filters require a fair degree of hermeticity for a reliable performance. Tunable MEMS devices are very sensitive to moisture and atmospheric particulates. Therefore, low-cost packaging of the MEMS devices and filters, ideally at the wafer level, is necessary [6]. In addition, tunable MEMS components require high operating voltages (5 V-80 V) that are not available on chip. Ultimately, this is a system architecture problem, since there is no reason why such a voltage could not be made available on chip if the benefits were apparent [1]. In the meantime, this problem can be solved by using charge pumps [7].

Because of the numerous advantages of the MEMS-based components, the integrated MEMS area has attracted a large pool of attention [8]. However, not much work has been done to implement a passive component with a sufficiently high Q (i.e., Q

in excess of 100) that can be employed in a low-loss tunable bandpass filter in the VHF or UHF region. Instead, most reported work in the literature discusses some random-value passive components that, although they exhibit high-performance, are not targeted for a certain frequency range and are not employed in a system (e.g., filters). In this thesis, we demonstrate high-performance fixed- and tunable-frequency lumped filters in the UHF range using high-Q passive components that are designed for an optimum filter performance. In addition, we have devised a fabrication technique that not only results in the record high-Q passive elements, but is also low-temperature and post CMOS-compatible.

In this chapter, we first review some of the previous work that has been done to improve the performance of individual RF components through micromachining technology. Next, we discuss different filter technologies that are commonly used for wireless applications and our motivation for selecting the lumped filter technology.

1.1 High-Q Micromachined Inductors

The poor performance of available on-chip inductors poses a major bottleneck in the realization of low-loss filters in the VHF and UHF range. High-Q integrated inductors can significantly reduce the size and improve the insertion loss of bandpass filters. Besides their application in low-loss filters, high-Q integrated inductors are required to improve the performance and integration level of RF integrated circuits, such as low-noise amplifiers and lumped oscillators. On-chip inductors in commercially available CMOS processes exhibit poor Qs (< 30) because of the high-frequency loss of the standard silicon substrate and ohmic loss of thin metal layers [9]. There are two sources of energy dissipation in an inductor: the metal loss and the substrate loss. These two sources of loss are independent and the unloaded Q can be expressed by [10]

$$\frac{1}{Q} = \frac{1}{Q_{metal}} + \frac{1}{Q_{substrate}}, \tag{1}$$

where $Q_{substrate}$ and Q_{metal} represent the substrate loss and the ohmic loss of metal strips, respectively.

Common techniques employed to reduce the metal loss in inductors include the use of high-conductivity metal layers [11]; in particular, electroplating a thick copper layer [12], utilizing multi-level metal interconnects to increase the effective thickness of the inductor, and series connection of multi-layer inductors in the vertical direction to reduce the area [13], [14]. The most effective way of reducing the metal loss is through electroplating a thick layer of a high-conductivity metal (e.g., copper or silver).

Micromachining materials and techniques have been utilized to reduce the substrate loss and to increase the Q. Reported techniques include the suspension of inductors [15], [16] and the fabrication of 3D microstructures such as toroids and self-assembled solenoids [17], [18]. The materials utilized to reduce the substrate loss include thick isolating oxide [19], porous silicon [20], and thick low-K dielectrics [21], [22].

We had previously shown the implementation of high-Q copper inductors on the CMOS-grade silicon substrate using a bulk micromachining technique [23], [24], [25], [26]. In this technique, a low-temperature (< 300º C) fabrication sequence is employed to reduce the loss of silicon wafers at radio frequencies by trenching the silicon substrate. The high-aspect-ratio (30:1) trenches are subsequently bridged over or refilled with a low-loss material to close the open areas and to create a rigid low-loss island (trenched silicon island) on which the inductors are fabricated. Using this method, we demonstrated a one-turn 0.8 nH copper inductor that exhibits a high Q of 71 at 8.75 GHz.

Using the aforementioned techniques, the performance of inductors has been improved. Table 1 compares some of the high-Q inductors reported in the literature. As shown in Table 1, the combination of a high-conductivity metal and bulk micromachining techniques has considerably improved the Q of on-chip inductors. However, the quality factor of the reported inductors on silicon is still far from sufficient for implementation of a low-loss narrow-band filter in the UHF range. In this frequency

range, the dominant *Q*-limiting mechanism is the metal loss. Consequently, the use of the highest conductivity material would have a significant effect on reducing the ohmic loss and improving the *Q*. Therefore, in this work, we have used silver to minimize the metal loss. In Chapter 2, we provide a more detailed explanation of our motives for using silver as the structural material.

Table 1: Comparison of some of the reported high-*Q* micromachined inductors.

Author	Type	Inductor Value	Q_{max}@ Frequency	Self- Resonance Frequency
P. Carazzetti et al. [11]	Planar silver on glass	5.5 nH	70 @ 3.8 GHz	~10 GHz
J. B. Yoon et al. [15]	Suspended copper spiral	1.32 nH	70 @ 6 GHz	>20 GHz
Chua et al. [17]	Helical on silicon	8 nH	75 @ 1 GHz	8 GHz
D. H. Weon et al. [18]	Helical on glass diaphragm	1.2 nH	140 @ 12 GHz	>40 GHz
Yoon et al. [22]	Helical on glass	1.17 nH	84 @ 2.6 GHz	-
M. Raieszadeh et al. [25]	Planar copper on silicon	0.8 nH	71 @ 8.75 GHz	>10 GHz

1.2 Tunable MEMS Capacitors

The reported tunable lumped filters have either used tunable capacitors or an array of switchable lumped capacitors to achieve frequency tuning. Tunable capacitors are also widely used in RF integrated circuits, such as voltage-controlled oscillators and reconfigurable impedance matching networks. Depending on the application, tunable capacitors are required to have a large tuning range, high quality factor, high self-resonance frequency (*SRF*), and/or high power handling. Currently, MOS varactors are used in RF integrated circuits (ICs) as the tuning element. However, MEMS tunable capacitors can exhibit higher quality factors and therefore outperform MOS varactors at frequencies beyond 1 GHz. In this section, we present a brief overview of the reported

MEMS tunable capacitors based on the choice of material, actuation mechanism, and actuator design.

1.2.1 Material Type

MEMS tunable capacitors can be divided into two categories based on the choice of material: silicon-based capacitors, which are usually realized in the bulk of silicon or silicon on insulator (SOI) substrates [27], [28], [29], [30], or metal-based capacitors fabricated on silicon or glass substrates [31], [32], [33], [34]. Compared to silicon-based capacitors, metal-based capacitors have a smaller series resistance and can potentially exhibit a higher Q. To improve the high-frequency performance of metal-based capacitors on silicon, the substrate loss should be reduced. To reduce the high-frequency loss of silicon, two main approaches have been taken: the removal of silicon underneath the device [32] or the use of high-resistivity silicon (HRS) substrates [33]. While the use of high-resistivity silicon significantly reduces the substrate loss at high frequencies (> 3 GHz), it impairs the quality factor of the device in the UHF range [33]. Needless to say, removing the silicon substrate using a bulk micromachining technique is the most effective way to reduce the substrate loss, and as such, is the method used in this work.

1.2.2 Actuation Method

The methods used for capacitance tuning include electrostatic [31], electromagnetic [35], magnetic [36], piezoelectric [37], [38], and thermal [39] actuation. Electrostatic actuation is usually preferred for its inherent speed and low energy consumption. A drawback to the electrostatic scheme is the high actuation voltage, which is typically in the range of 5 V-80 V. A charge-pump circuit can be used to address the high operating voltage issue in the system level [7]. Lower actuation voltages are possible using the piezoelectric actuation method. Thermal actuation has the disadvantage of relatively high power consumption. Compared to electrostatic actuation, magnetic actuation is harder to realize as it is hard to produce and control a magnetic

field on chip. This work focuses on the electrostatic actuation mechanism because of its dominant advantages, including the simplicity of the actuator design.

1.2.3 Actuator Design

The most commonly used MEMS actuators are based on the electrostatic attraction. In electrostatic actuators, capacitance tuning is achieved by changing the physical parameter in the general capacitor expression

$$C = \varepsilon_0 \varepsilon_r \frac{A}{d}, \tag{2}$$

where C is the capacitance, ε_0 and ε_r are the respective permittivity of free space and dielectric constant of the capacitive gap material, A is the overlapping area of the capacitor plates, and d is the gap between the two capacitor plates. Based on the parameter that is changed, tunable capacitors are categorized as gap-tuning, area-tuning, or dielectric-tuning capacitors. Electrostatic actuators that are based on the change in the inter-electrode spacing (gap) are called parallel-plate (or gap-tuning) actuators. An example of a micromachined parallel-plate actuator is shown in Figure 2 [28].

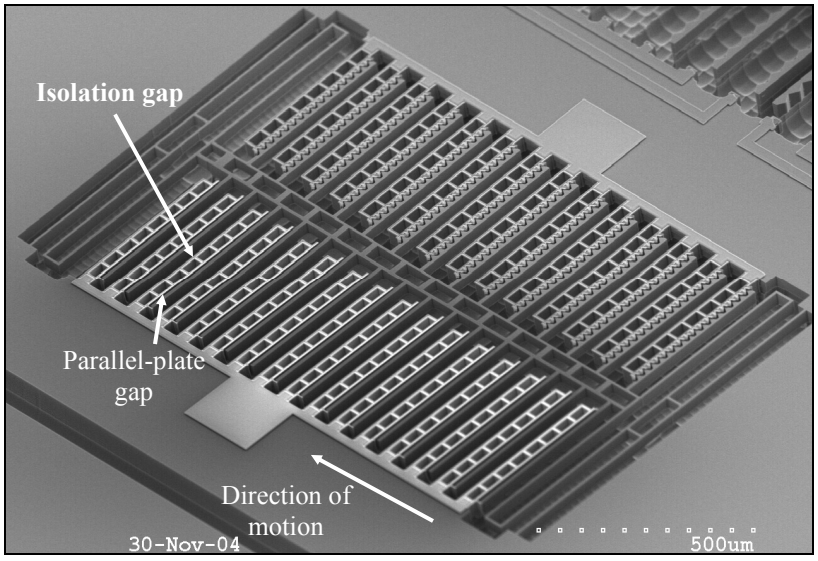


Figure 2: A scanning electron microscope (SEM) view of a parallel-plate capacitor [28].

Comb-drive (or area-tuning) actuators have alternating interdigitated comb fingers that move parallel with each other when a potential is applied. Therefore, in a comb-drive actuator, tuning is achieved by changing the effective capacitance area between the two actuator plates. A SEM view of an exemplary comb-drive actuator is shown in Figure 3 [29].

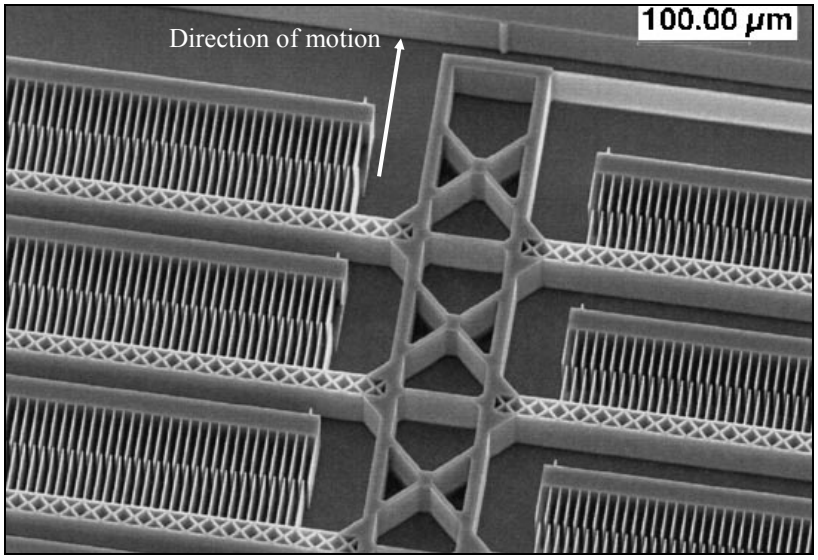


Figure 3: An overview SEM picture of a comb-drive tunable capacitor [29].

The continuous tuning range of a conventional parallel-plate MEMS capacitor with the electrostatic actuation method is limited to 50% because of the pull-in effect. If the actuation voltage exceeds the pull-in voltage, the air gap reduces to less than two-thirds of the original air gap, and the movable plate collapses on the fixed plate. The voltage at which the two plates collapse is found from

$$V_{pull-in} = \sqrt{\frac{8kd_0^{\,3}}{27\varepsilon A}}, \tag{3}$$

where k is the stiffness of the movable plate, d_0 is the initial gap between the two plates, ε is equal to $\varepsilon_0 \times \varepsilon_r$, and A is the overlapping area of the two plates.

The pull-in limitation on the tuning range can be avoided in a dual-gap tunable capacitor in which the parallel-plate actuation gap is larger than the parallel-plate sense (capacitor) gap [28]. Figure 4 shows the schematic view of a dual-gap actuator. The travel range is equal to one-third of the actuation gap (d_1), which exceeds the initial sense gap (d_2). In a case where $d_1 > 3 \times d_2$, the tuning range is ideally infinite. In dual-gap capacitors, the movable actuator and capacitor plates are mechanically coupled. If also electrically connected, the capacitor is one-port; otherwise, the capacitor is two-port.

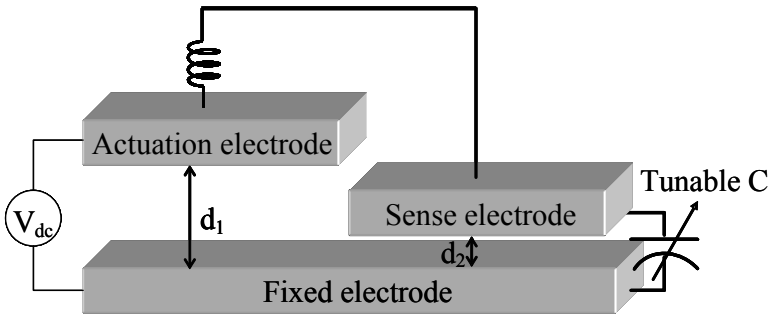


Figure 4: Schematic view of a dual-gap parallel-plate actuator.

The implementation of in-plane (lateral) dual-gap actuators is typically easier as both the actuator and the capacitor gaps are defined in one step, lithographically. In contrast, different gaps of an out-of-plane (vertical) actuator are defined by multiple depositions of a sacrificial layer. In addition, since both the movable and fixed plates of an in-plane capacitor can be suspended in air, in-plane capacitors can potentially exhibit higher *Q*s. If we define the tuning ratio as the final capacitance value divided by the initial capacitance value ($C_{final}/C_{initial}$), dual-gap parallel-plate actuators can achieve a large tuning ratio with a small tuning voltage.

Alternatively, to achieve a large tuning ratio, the actuator can be made in a comb-drive configuration while the capacitor is a parallel-plate. In comb-drive actuators, the maximum displacement (travel range) is limited by the lateral snap-down of the comb

fingers. The lateral snap-down occurs when the lateral distances of a comb finger from the two adjacent fingers are not equal. This is mainly due to fabrication imperfections, which are inherent in any MEMS device. The maximum displacement of a comb-drive actuator before the lateral snap-down occurs is

$$x_{\max} = \frac{-w + \sqrt{w^2 + 2(k_y / k_x) d^2}}{2}, \tag{4}$$

where x_{max} denotes the maximum travel range, and w is the initial overlap between the comb fingers. k_x and k_y are the respective lateral stiffness along and normal to the displacement vector. The lateral distance between the comb fingers is denoted by d (see Figure 5). Comb-drive actuators typically require higher tuning voltages, but their travel distance is linear with respect to the applied tuning voltage.

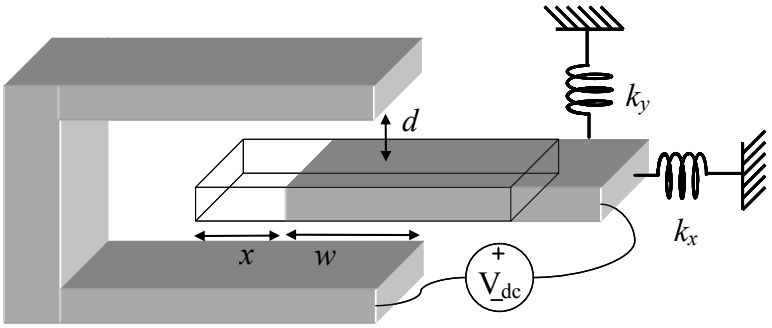


Figure 5: Schematic view of a comb-drive actuator.

Another method of capacitance tuning is changing the material property of the dielectric between the two capacitor plates. This type of tunable capacitors has been implemented in planar [40], [41] or in coupled-line [42], [43] configuration so that a DC bias voltage can change the permittivity of the dielectric. The dielectric material can be a voltage-tunable ferroelectric thin film, such as barium strontium titanate, which is deposited using the laser vapor deposition with proper stoichiometric ratios necessary for

the desired film [44]. Major disadvantages of the dielectric-tunable capacitors are poor power handling and a small break-down voltage.

Table 2 compares the performance of some of the highest-Q electrostatic capacitors reported in the literature. In this work, we have employed both gap-tuning and area-tuning actuators to simultaneously achieve a large tuning range and a high Q.

Table 2: Comparison of some of the reported high-Q micromachined tunable capacitors.

Author	Type	Initial Capacitance (pF)	Tuning Voltage (V)	Percentage Tuning	Q @ 2 GHz	SRF (GHz)
Borwick et al. [27]	Area tuning on glass	1.4	8	740	40	>3
Monajemi et al. [28]	Dual gap tuning on silicon	2.5	2	100	30	10
Nguyen et al. [30]	Out-of-plane area tuning on glass	0.27	40	3000	160	>5
Grichener et al. [31]	Gap tuning on glass	0.091	35	90	>200	>20
Gu at al. [32]	Area tuning on silicon	0.28	4	210	46	9.44
Rijkr et al. [33]	Dual gap tuning on HRS	0.47	20	700	300	>6
Zou et al. [34]	Dual gap on glass	0.046	17	55.6	40	>10

1.3 Tunable Inductors

Since it is much easier to control the electrical field than the magnetic field on chip, it is common to use variable capacitors as the tuning element in tunable filters and reconfigurable impedance matching networks. However, it is desirable to make the inductor also tunable, especially for wide frequency tuning capability. Both discrete and

continuous tuning of passive inductors using micromachining techniques have been reported in the literature. Discrete tuning of inductors is usually achieved by changing the length or configuration of a transmission line using micromachined switches [45]. The incorporation of switches in the body of the tunable inductor increases the resistive loss and hence reduces the quality factor. Alternatively, continuous tuning of inductors is realized by displacing a magnetic core [46], [47], changing the permeability of the core [48], or using movable structures with large traveling range [49], [50]. Although significant tunings have been achieved using these methods, the reported fabrication or actuation techniques are complex, making the on-chip implementation of the tunable inductors difficult. In addition, *Q*s of the reported tunable inductors are not sufficiently high for many wireless and RF integrated circuit applications. To overcome the shortcomings of prior work, we have developed a new implementation of integrated tunable inductors, which is explained in Chapter 2.

1.4 Fixed Bandpass Filters

Figure 6 shows different wireless standards in the UHF and super high frequency (SFH) range. Each standard poses its own specific requirement on the filter characteristic with regard to insertion loss, bandwidth, out-of-band rejection, and roll-off. Based on the required filter specifications with the consideration of the filter size and cost, the most suitable filter technology is selected for each band.

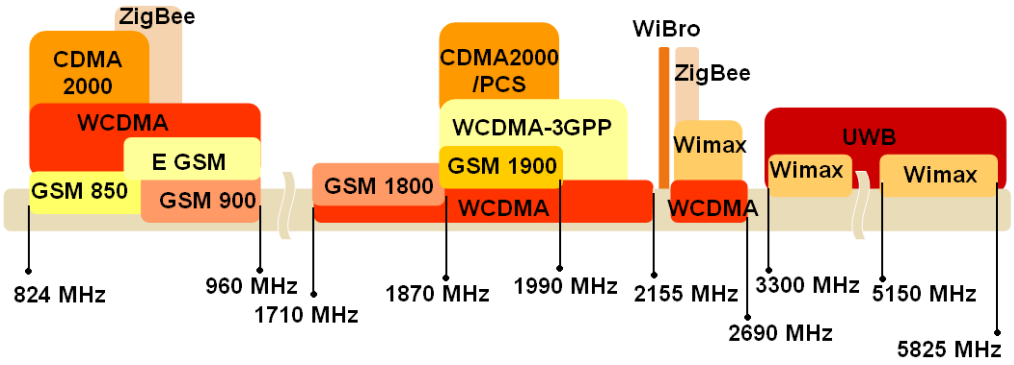


Figure 6: Wireless standards in the 800 MHz-6 GHz frequency range.

The most commonly used filters in the high-VHF, UHF, and SHF range are implemented using SAW, bulk acoustic wave (BAW), distributed filter, or lumped filter technology. BAW filters include FBAR-type filters [51] and micromechanical coupled-resonator filters [52], [53], [54]. As discussed earlier, most of the high-Q bandpass filters used in available cellular modules are realized using the SAW and BAW technology [55], [56]. SAW and BAW filters offer a very high performance in terms of insertion loss, Q, and out-of-band roll off. However, these off-chip filters pose a bottleneck in the integration effort.

Silicon-based capacitive BAW filters like the one reported in [52] exhibit ultra high Qs (>10000) in the low UHF range (up to 500 MHz), but poor insertion loss performances. Therefore, these devices are more suitable for IF filtering, where the requirement on the filter bandwidth is more stringent than that on the filter insertion loss. In addition, the fabrication of capacitive silicon-based BAW filters includes high-temperature (> 900º C) deposition and annealing steps, which make these BAW filters incompatible for post-CMOS integration.

Recently, there have been a few reports on the low-temperature implementations of BAW filters on SOI substrates using the piezoelectric transduction method [53], [54]. Piezoelectrically transduced BAW filters offer moderate to high quality factors in the range of 100-10000. The high Q and low-temperature processing of piezoelectric BAW filters make them attractive candidates for VHF and UHF wireless modules. However, this type of BAW filter requires SOI substrates, making them less compatible for monolithic integration with CMOS circuitry. In addition, there are several applications that necessitate wider-band filtering (e.g., WCDMA and GSM standards), where the required filter Q is less than that offered by the SAW and BAW filter technologies. Most important, acoustic filters cannot be tuned.

For these reasons, lumped filters [8], distributed filters [57], and active circuit resonators [58] have been proposed as solutions for acoustic filter replacement. Although

distributed filters with a practically low (< 4 dB) insertion loss have been shown at frequencies greater than 5 GHz [57], the size of such filters in the UHF and high-VHF range would be much larger than the alternative lumped element filters.

The use of active circuit resonators not only increases the power consumption and decreases the battery life of a cellular phone, but it also decreases its dynamic range. Until recently, high-Q passives, and mainly high-Q inductors, had not been available on chip, and therefore the realization of integrated passive LC bandpass filters that could meet the channel/band specification in terms of insertion loss and Q was impractical. With the introduction of practically high-Q (i.e., $Q > 70$) inductors using micromachining techniques (Table 1), a new horizon has opened for the implementation of high-performance lumped filters that can be made tunable. Table 3 summarizes some of the characteristics of the filter technologies that were discussed.

Table 3: Comparison of the filter technologies used in 30 MHz-30 GHz frequency range.

Filter Type	Frequency Range	Quality Factor	Relative Size	Relative Loss	Tuning Method
Crystal (Acoustic)	IF	High	Large	Moderate-high	Hard to realize
Acoustic	LF-UHF	Very high	Very small	Small-moderate	Hard to realize
Distributed	SHF	Low-moderate	Large	Small-moderate	Easy implementation on chip
Lumped	HF-UHF	Low-moderate	Small-medium	Moderate-high	Easy implementation on chip

A comparison of the different filter technologies shown in Table 3 reveals that for UHF applications, the lumped filter technology is the most suitable candidate that offers tuning capability. For this reason, we have selected the lumped filter topology in this work and have investigated the feasibility of implementing several high-order narrow-bandwidth (< 5%) filters as well as high-order wide-bandwidth (> 10%) filters on silicon.

For lumped filters, it can be shown that the minimum achievable insertion loss is a function of the order of the filter (i.e., number of sections), the unloaded Q of each LC resonator incorporated in the filter, and the relative bandwidth of the filter [59], [60]. Figure 7 gives the minimum unloaded Q (Q_{min}) for each LC resonator, as stated by Fubini et al. [61]. The axes are normalized to the unity bandwidth. That is, instead of plotting Q_{min}, a more general set of curves has been obtained by plotting

$$q_{\min} = Q_{\min} \frac{\Delta f}{f} \quad , \tag{5}$$

where ($\Delta f / f$) is the relative bandwidth of the complete filter connected to proper termination impedances. The number of sections of the filter is determined from the requirements on the filter shape, such as the filter out-of-band rejection and roll-off. In Figure 7, note that for a given bandwidth, the requirements on the component Q increase sharply from the no-ripple (Butterworth) case to the cases where ripples of a few decibels are specified (e.g., Chebychev or Elliptic filters). It must also be noted that, if one were trying to use components whose unloaded Q is barely equal to the minimum required, the desired filter shape could indeed be achieved but with an infinite mid-band loss [61].

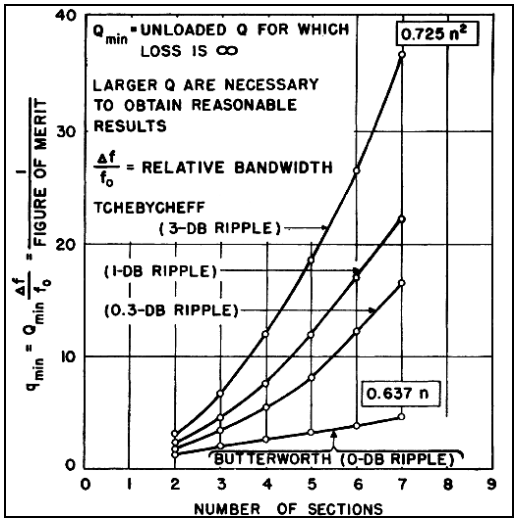


Figure 7: Relative minimum unloaded Q for the Butterworth and Chebychev filters.

Fabiani also calculated the minimum mid-band loss of the Butterworth filter if the unloaded Q of each resonator is more than the minimum required. For the sake of completeness, Fubini's minimum mid-band loss curve is reproduced in Figure 8.

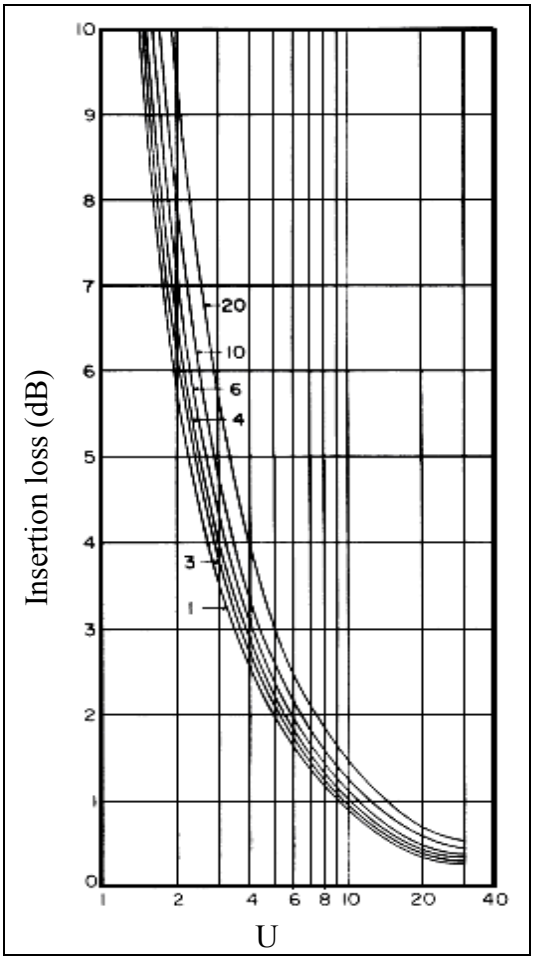


Figure 8: Minimum insertion loss at mid-band in the Butterworth filters of 1, 2, 3, 4, 6, 10, and 20 sections. U is the ratio between the unloaded Q of each section and the minimum Q as defined by Figure 7.

To better understand the purpose of Figure 7 and Figure 8, consider a third-order bandpass filter at 1 GHz with a 3 dB-bandwidth of 300 MHz. If one is to design this filter in the Butterworth configuration, the q_{min} for each resonator will be 1.9, as defined by Figure 7. Therefore, the minimum unloaded Q of each resonator would be 6.4 (i.e, 1.9×(1 GHz/300 MHz)). If each resonator has a Q of 64, which is 10 times the minimum

required Q, the minimum insertion loss determined from Figure 8 would be 1 dB at the filter mid-band. If we estimate the Q of a lumped LC resonator as

$$Q = \left(\frac{1}{Q_{inductor}} + \frac{1}{Q_{capacitor}}\right)^{-1}, \tag{6}$$

to achieve a Q of 64 for the resonator, the individual component Q should be at least 128.

In Figure 8, it is noticeable that if an insertion loss of less than 5 dB is required for a Butterworth filter, the unloaded Q of each section should be at least three times the minimum required Q, where the minimum Q is defined by Figure 7. The same trend is also observed for the Chebychev filters [60].

1.5 Tunable Bandpass Filters

Among the different types of micromachined filters discussed in Section 1.4, lumped filters that employ tunable or switchable capacitors offer the greatest tuning range [62], [63], [64], [65]. However, the size of lumped tunable filters can become large in the VHF and UHF range (30 MHz-3 GHz), particularly when distributed-type inductors are used. On the other hand, as discussed earlier, the quality factor of on-chip lumped inductors (e.g., spiral inductors) on *silicon substrate* has not been sufficiently high (i.e., Q >100 in the UHF range) for applications that require narrow-band filtering with low insertion loss. Consequently, most reconfigurable lumped filters reported in the literature to date have either utilized off-chip inductors or low-loss substrates, such as high-resistivity silicon, FR4, sapphire, or glass, to achieve a low insertion loss [62], [63], [64], [66], [67]. Because of the challenges involved with the integration of high-Q lumped elements in a small form factor on the CMOS-grade silicon (ρ = 10-20 Ω.cm), a low-loss, high-order, narrowband, integrated tunable filter is yet to be shown in this frequency range.

In this thesis, we present continuously tuned filters in the UHF range using a new silver micromachining technique. Filters are tuned by actuating the tunable integrated silver capacitors, electrostatically. The low-temperature fabrication process used in this work to implement the filters enables the simultaneous fabrication of high-performance two-port and one-port tunable capacitors, as well as high-Q planar inductors.

This thesis is divided into six chapters. In Chapter 2, we discuss the design and implementation of individual passive components, which enable the realization of bandpass filters. We document the design methodology of the fixed-frequency lumped bandpass filters in Chapter 3 and demonstrate an array of these filters that is fabricated and encapsulated using the low-temperature silver micromachining technique. In Chapter 4, we detail the design strategies of tunable lumped bandpass filters and provide a comparison of different lumped filter topologies. We also discuss a new approach to maintain a constant bandwidth while the center frequency of the filter is tuned. We present an alternative method for the fabrication of high-value tunable capacitors in Chapter 5. Also in Chapter 5, we demonstrate the measurement results that we have obtained for the large-value tunable capacitors and discuss different strategies to further improve the performance of these devices. We conclude this thesis with Chapter 6. In Chapter 6, we summarize the contributions of this work and provide directions for the future work regarding the different aspects of the research presented in this thesis and in the micromachined integrated lumped filter area.

CHAPTER 2

HIGH-PERFORMANCE TUNABLE PASSIVES

In Section 1.4, we explained that to attain a narrow-band lumped filter with a low insertion loss, we need high-Q LC resonators. This entails that each individual capacitor and inductor incorporated in the resonator must have a high Q. We further described that high-Q tunable passive components have been demonstrated on low-loss substrates using advanced micromachining techniques. However, several challenges have impeded the realization of a low-loss tunable lumped bandpass filter on the CMOS-grade silicon substrate. The main challenge has been to devise a process flow that would enable the *simultaneous* fabrication of high-Q inductors as well as fixed and tunable capacitors. Using a suitable fabrication process, the subsequent task is to design the physical layout of the inductors and tunable capacitors such that their peak Q occurs at the center frequency of the filter while having realizable values for on-chip integration. The last, but not least challenge is to design a tunable component that maintains its high Q over a wide tuning range. To tackle this task, we have developed a low-temperature fabrication process that offers very high-Q wafer-level encapsulated tunable passives on the CMOS-grade silicon substrate. The quality factor of the passive components enabled using this technique is high enough to yield a high-performance tunable filter with a low insertion loss.

In this chapter, we first introduce the fabrication technique. Next, we discuss the measured results that we have obtained for the fabricated devices, namely, integrated high-Q inductors, tunable capacitors, and tunable inductors. In the following chapters, we demonstrate the application of these components in low-loss fixed and tunable bandpass filters.

2.1 Fabrication Technique

In Section 1.1, we showed that to achieve the highest Q, both the metal loss and the substrate loss have to be effectively reduced. To minimize the metal loss, we have used silver as the structural material. Table 4 compares some of the electrical and mechanical properties of silver with the other two high-conductivity metals: copper and gold. In comparison, silver has the highest bulk conductivity and the lowest thin film resistivity. More importantly, it is easier to attain close to the bulk conductivity in the electroplated silver film. Silver has a low level of stress in a thick electroplated layer, which makes it a strong candidate for MEMS as a high level of stress can significantly hamper the performance of a movable device. In addition, silver has a relatively low Young's modulus. A low Young's modulus is preferred as it results in a lower stiffness and thereby a lower tuning voltage for tunable components. Lastly, silver has the highest thermal conductivity of all metals. This is particularly important for applications that necessitate high power handling. A suspended device with a high thermal conductivity rapidly transfers the heat resulted from the high input power to the surrounding structures, alleviating the local temperature increase and improving the life time [68].

Table 4: Comparison of the electrical and mechanical properties of silver with copper and gold.

Metal	Bulk Conductivity @ 20° C (MS/m)	Thin-Film Resistivity @ 20° C (μΩ.cm)	Young's Modulus (GPa)	Stress (MPa)	Thermal Conductivity @ 330° K ($W \cdot m^{-1} \cdot K^{-1}$)
Gold	44	2.7 (gold/chromium)	78	220	318
Copper	59	2.0-2.5 (copper/ chromium)	130	400	401
Silver	62.5	1.6 (silver/titanium)	83	220	429

As shown in Table 4, the use of silver not only improves the ohmic loss [69], but it also offers several added advantages. However, silver has some issues that have impeded its wide application in RFICs. Silver is very sensitive to hydrogen sulfide (H_2S), which forms silver sulfide (Ag_2S), even at a very low concentration of the corrosive gas [70], [71]. The decomposition of the silver contact surface leads to an increase in the surface resistance, hence to a lower Q for the passive components. Another problem with silver is the electrochemical migration, which occurs in the presence of a wet surface and an applied bias. Silver migration usually occurs between adjacent conductors/electrodes, which leads to the formation of dendrites and finally results in an electrical short-circuit failure. The failure time is related to the relative humidity, temperature, and strength of the electric field [69]. These problems can be avoided using a hermetic or semi-hermetic sealing.

In this work, we have incorporated a semi-hermetic packaging technique to decrease the exposure of the silver microstructures to the corrosive gases and to encapsulate the tunable components. The preliminary results of this packaging technique are reported here. If necessary, subsequent over-molding can provide longer-term hermeticity as well as additional strength and resilience.

In addition, to reduce the high-frequency loss of CMOS-grade silicon, we have passivated the substrate with a thick low-loss dielectric. We have chosen Avatrel (Promerus, LLC, Brecksville, OH 44141) for this purpose because of its low permittivity and loss tangent [26], [72]. A comparison of the electrical properties of Avatrel with the other commonly used low-k polymers is shown in Table 5.

Table 5: Comparison of the properties of Avatrel with BCB and Polyimide.

Material	Loss Tangent @ 1 GHz	Permittivity (ε_r)	Moisture Uptake
Polymide	0.01-0.015	3.1- 4.1	0.5-3%
BCB	0.015	2.7	0.23%
Avatrel	0.009	2.55	<0.1%

Using silver as the structural material and Avatrel as the passivation layer, we have developed a new low-temperature fabrication process. The fabrication process flow is schematically shown in Figure 9.

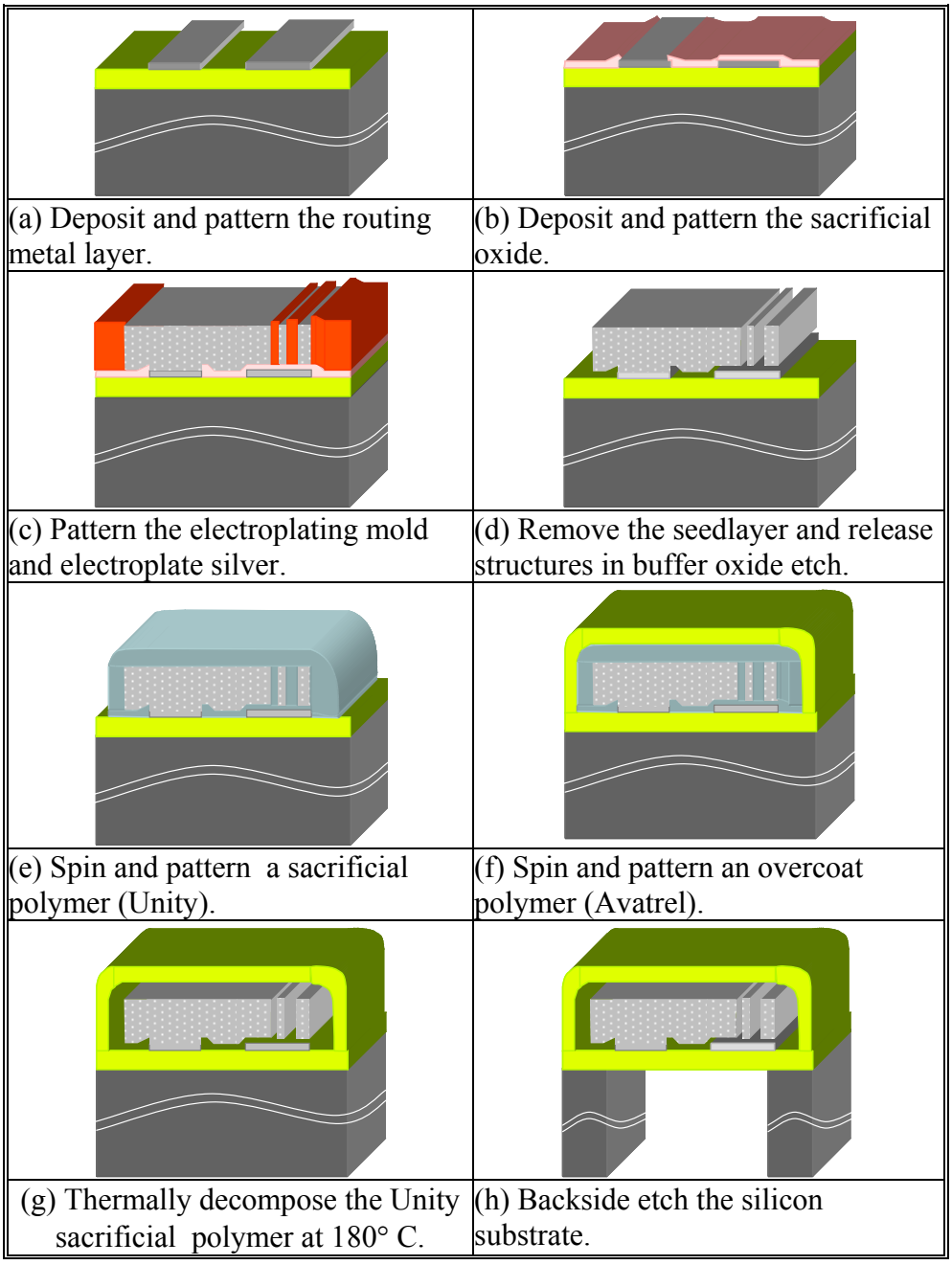


Figure 9: Fabrication process flow of the wafer-level encapsulated MEMS passives and bandpass filters.

In this process, the CMOS-grade silicon substrate is first spin-coated with a 20 μm thick Avatrel layer. A 2 μm thick silver layer is then evaporated to form the routing metal layer (Figure 9(a)). A thin layer (~100 Aº) of titanium (Ti) is used to promote the adhesion between the silver layer and the Avatrel layer. Next, a 4 μm thick plasma-enhanced chemical vapor deposited (PECVD) silicon dioxide layer is deposited at 160º C and patterned (Figure 9(b)). The deposition temperature of silicon dioxide is reduced to preserve the quality of the Avatrel layer, which provides a mechanical support for released devices. A thin layer of Ti/Ag/Ti (100 Aº/ 300 Aº/ 100 Aº) is sputter deposited and serves as the seedlayer for electroplating. The top titanium layer prevents the plating of silver underneath the electroplating mold, and is dry etched from the open areas, prior to electroplating, in a reactive ion etching (RIE) system. The use of the Ti layer is specifically important when the distance between the silver lines is less than 10 μm.

The structures are formed by electroplating silver into a thick (20 μm-50 μm) photoresist mold (Figure 9(c)). Figure 10 shows two SEM views of a 50 μm thick NR4-8000P negative-tone photoresist from Futurrex that is used as the mold, showing the straight sidewall profile.

The plating bath consists of 0.35 mol/L of potassium silver cyanide (KAgCN) and 1.69 mol/L of potassium cyanide (KCN). A current density of about 1 mA/cm^2 is used in the plating process. The electroplating mold is subsequently removed. The seedlayer is removed using a combination of a wet and a dry etching process. Compared to the sputtered silver, the electroplated silver layer has a larger grain size resulting in a higher etch rate using an H_2O_2:NH_4OH wet solution. Hydrogen peroxide oxidizes silver and the ammonium hydroxide solution complexes and dissolves the silver ions. When wet etched, the thick and high-aspect-ratio lines of electroplated silver get etched much faster than the sputtered seedlayer that is between the walls of the thick electroplated silver structures. On the other hand, the dry etching of silver decouples the oxidation and dissolution steps resulting in almost the same removal rate for the small-grained sputtered

layer as the large-grained plated silver. The silver layer is first oxidized in an oxygen plasma (dry etch) and then the silver oxide layer is dissolved in a dilute ammonium hydroxide solution. Using this etching method, the seedlayer is removed without loosing excess electroplated silver. Devices are then released in buffer oxide etch (Figure 9(d)).

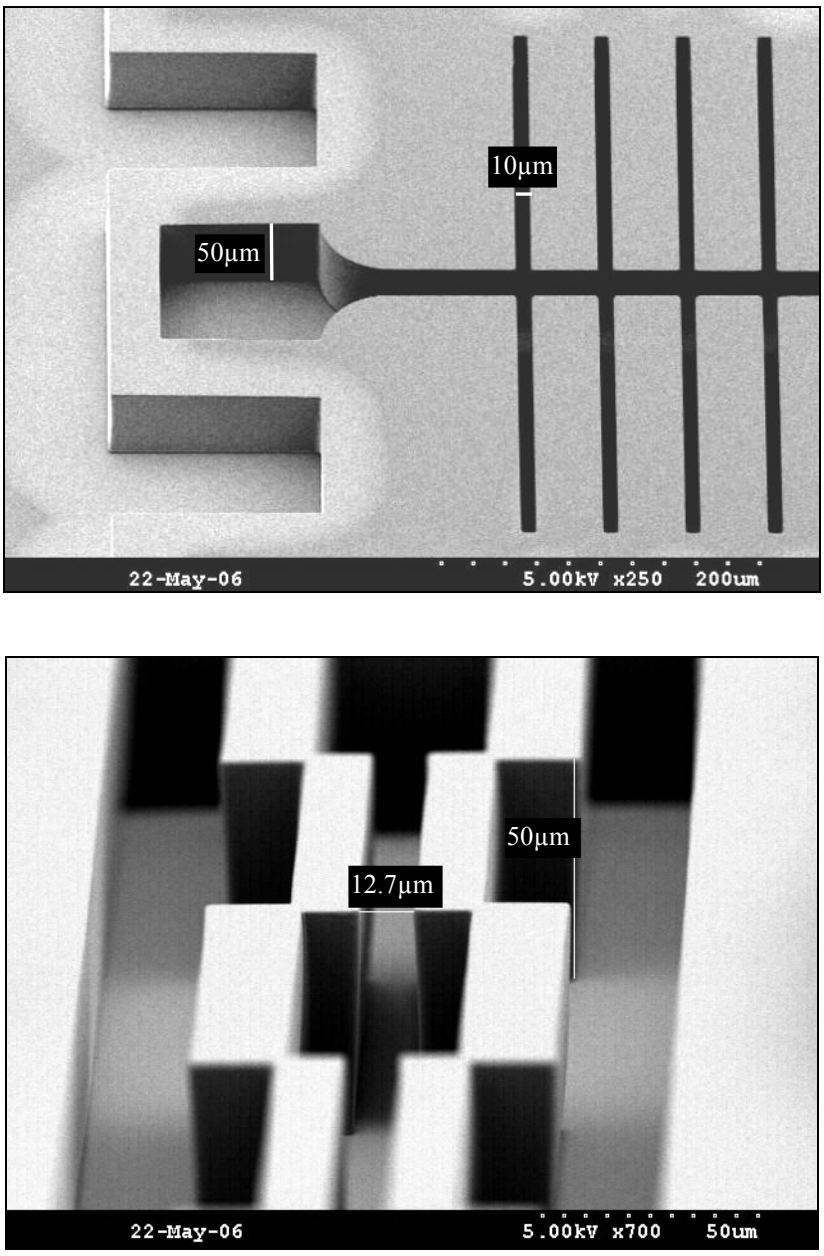


Figure 10: SEM views of a 50 µm thick NR4-8000P negative-tone photoresist, showing the straight sidewalls.

The released device is then wafer-level Encapsulated. A thermally decomposable sacrificial polymer, Unity (Promerus LLC, Brecksville, OH, 44141), is applied and patterned (Figure 9(e)). Then, the over-coat polymer (Avatrel), which is thermally stable at the decomposition temperature of Unity, is spin-coated and patterned (Figure 9(f)). Finally, the Unity sacrificial polymer is decomposed at 180° C (Figure 9(g)). As discussed in [73], the resulting gaseous products diffuse out through a solid Avatrel over-coat with no perforations. The loss of the silicon substrate is eliminated by selective backside etching using a deep reactive ion etching (DRIE) system, leaving a polymer membrane beneath the devices (Figure 9(h)). The highest processing temperature, including the packaging steps, is 180º C, and thus the process is post CMOS-compatible. The fixed inductors, vertical tunable inductors, and lateral tunable capacitors are simultaneously fabricated using this process.

2.2 Measurement Setup

The fabricated silver passives have a very small series resistance because of the high conductivity of the electroplated silver [69] and thus can exhibit very high Q. Therefore, special care must be taken in measuring the Q [18]. If otherwise stated, the on-wafer S-parameter measurements of the fabricated devices are carried out using an *hp*8364B vector network analyzer (VNA) and Cascade ground-signal-ground (GSG) infinity, I-50, microprobes. Figure 11 shows a picture of the on-wafer test setup. Accurate measurements of Qs in excess of 80 call for a very thorough calibration. Herein, the calibration is done using both the short-open-load-through (SOLT) and line-reflect-reflect-match (LRRM) calibration procedures, and pad parasitics are not de-embedded to avoid an over estimation of the Q. Also, to ensure repeatability in measurements, the high-Q passives are measured several times and each time, the calibration is redone. The deviation of the measurement values is within 10% for Qs in excess of 100.

Figure 11: A picture of the measurement test setup.

2.3 High-*Q* Integrated Silver Inductors

Because of the extreme reduction of both the metal loss and the substrate loss, the fabricated inductors have exceptionally high *Q*s. Figure 12 shows a SEM view of a 40 μm thick 0.6 nH inductor that exhibits a high *Q* of > 200 at 8 GHz. The inductance and *Q* are extracted from the measured S-parameter using the relations

$$L = \frac{\mathrm{Im}(1/Y_{11})}{\omega} \quad \text{and} \quad Q = \frac{\mathrm{Im}(1/Y_{11})}{\mathrm{Re}(1/Y_{11})}, \tag{7}$$

where ω is the angular frequency. The S-parameters of the 0.6 nH inductor is simulated in the Sonnet 2.5D electromagnetic (EM) simulation tool, using the Sonnet thick-metal model [74]. The conductivity of the electroplated silver layer in simulation is assumed to be 6×10^7, which is very close to the bulk conductivity of silver shown in Table 4. Figure 13 shows the measured and simulated *Q* of the inductor. As shown in Figure 13, the simulated *Q* validates the accuracy of the high measured *Q*.

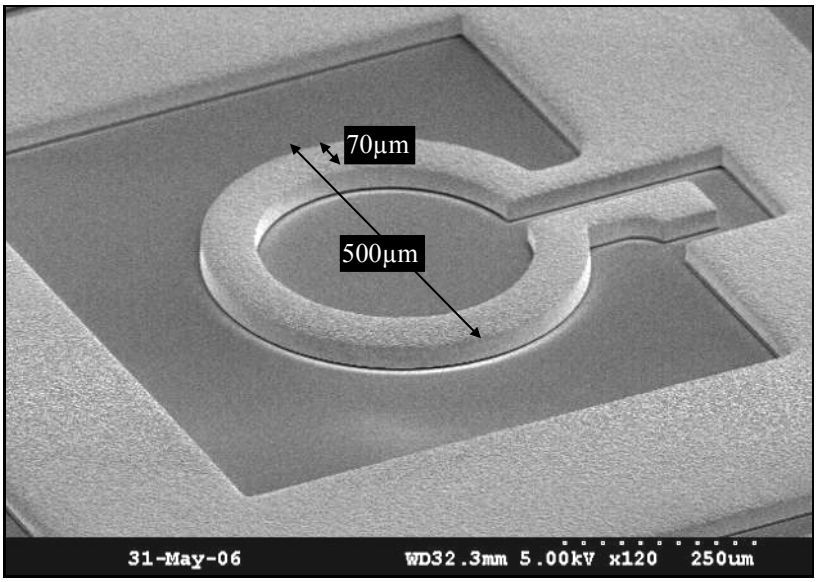


Figure 12: A SEM view of a 40 µm thick 0.6 nH silver inductor.

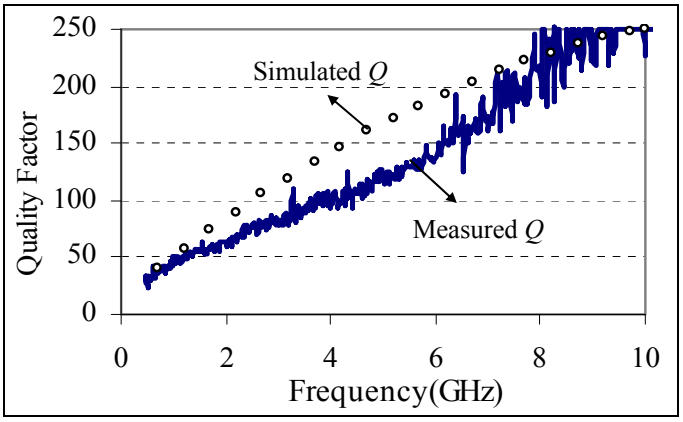


Figure 13: Measured and simulated *Q* of the inductor in Figure 12.

Figure 14 demonstrates the high embedded *Q* of a 1 nH inductor fabricated on an Avatrel membrane. This inductor exhibits an unprecedented performance (*Q* >150) in the 8 GHz - 25 GHz frequency range. To our best knowledge, this is the highest measured embedded *Q* for planar spiral inductors at such high frequency (compare to Table 1) [75].

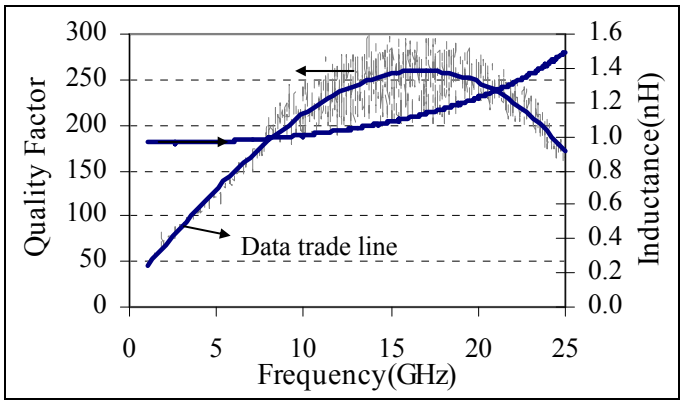


Figure 14: Measured embedded *Q* and inductance of a one-turn 1 nH inductor on an Avatrel membrane, showing a *Q* in excess of 150 in the 8 GHz - 25 GHz frequency range.

To explore the effect of using silver on the reduction of the metal loss, an eight-turn 32 nH inductor is fabricated. The fabricated inductor exhibits a high *Q* of 35 at 1.2 GHz, with a *SRF* of larger than 3 GHz (Figure 15). Figure 16 illustrates a SEM view of this inductor along with a micrograph of the inductor taken from the backside of the wafer, showing the device on an Avatrel membrane.

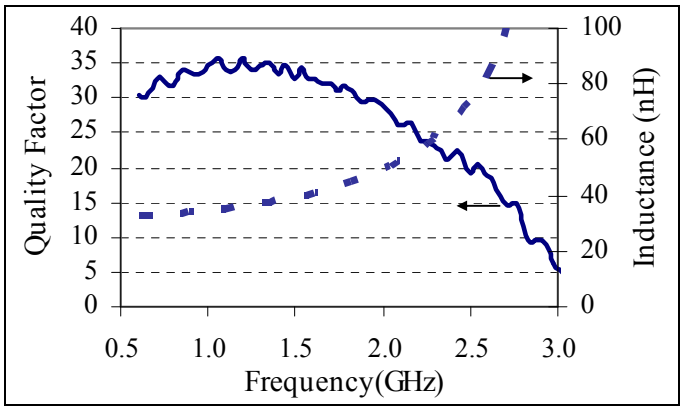
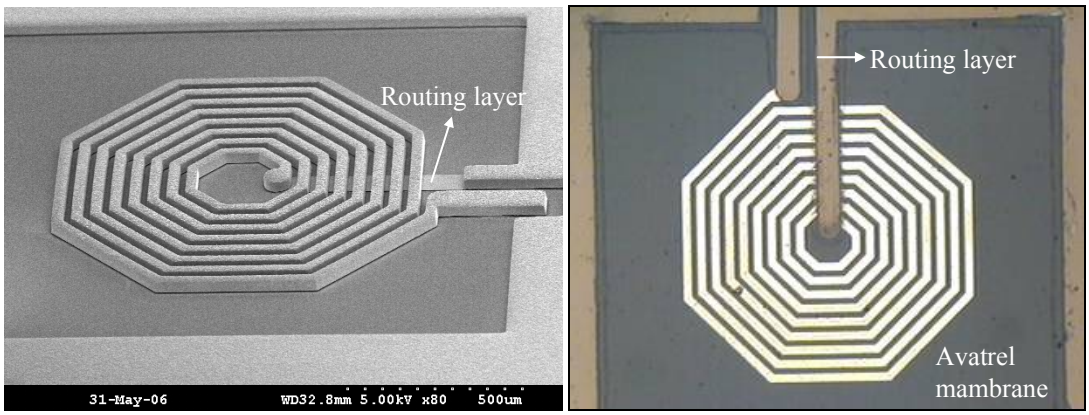


Figure 15: Measured embedded *Q* and inductance of a 32 nH silver inductor.



(a) **(b)**

Figure 16: (a) A SEM view of a 32 nH inductor and (b) a micrograph of the inductor taken from the backside of the wafer.

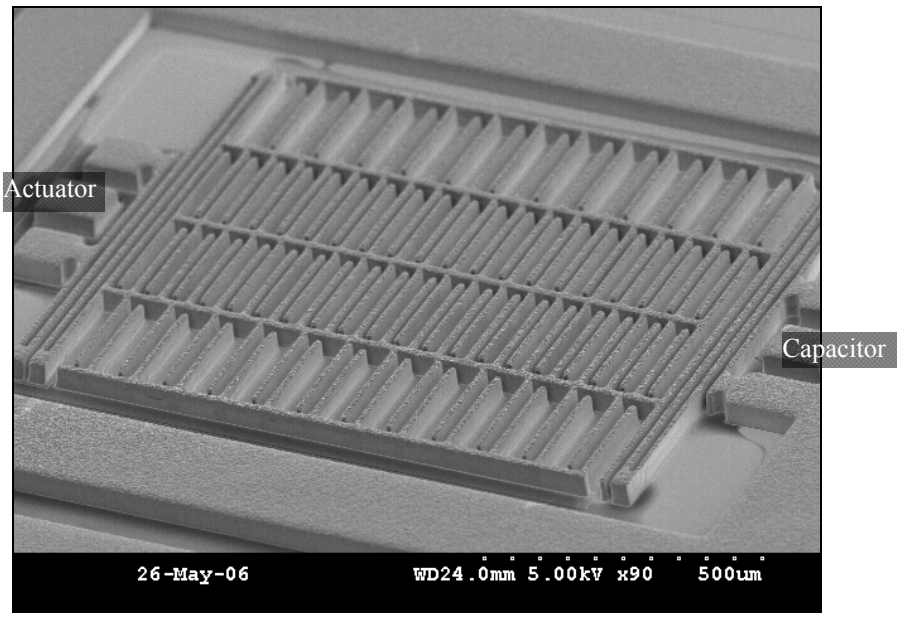
2.4 Lateral Tunable Silver Capacitors

2.4.1 Design

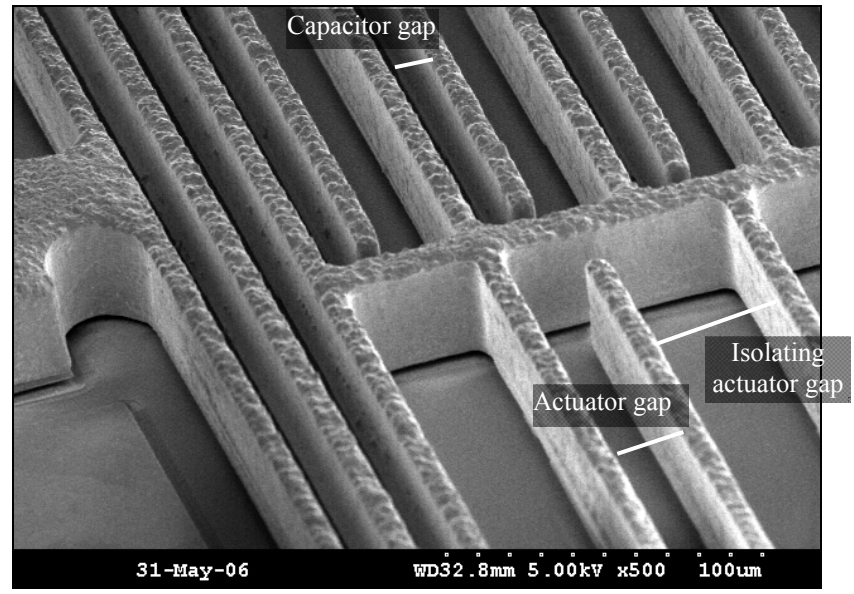
The thick silver micromachining method also enables the implementation of high-performance electrostatic lateral (in-plane) and vertical (out-of-plane) actuators. In this work, the dual-gap actuation scheme is applied to achieve the highest tuning range with an in-plane parallel-plate capacitor design. In the in-plane dual-gap capacitors, the narrow capacitor gaps and the wider actuator gaps are defined simultaneously using the relatively high-aspect-ratio (4:1) electroplating mold. Figure 17 shows a SEM view of a 40 μm thick silver in-plane tunable capacitor along with a close-up view of the actuator and capacitor gaps. In this design, the actuator and capacitor are folded into each other to reduce the die area and the length of the movable shuttle. Therefore, this design offers both a high Q and a small size. As shown in Figure 17, the actuation gap is 20 μm and the capacitor gap is 10 μm. The isolating gap between each set of parallel-plate fingers at the actuator side is 40 μm.

Figure 18 shows a MATLAB simulation, comparing the maximum displacement of the tunable capacitor in the dual-gap configuration when the isolation gap at the

actuator side is set as twice the actuator gap with a case where the isolation gap is infinite. As shown, with an actuator gap of 20 μm, the travel range decreases from 6.666 μm for the infinite isolation case to 6.139 μm for the 40 μm isolation case, resulting in a drop in the tuning range of the actuators with smaller isolation gaps.



(a)



(b)

Figure 17: (a) A SEM view of a 40 μm thick tunable silver capacitor and (b) a close-up view of the capacitor showing actuator and capacitor gaps.

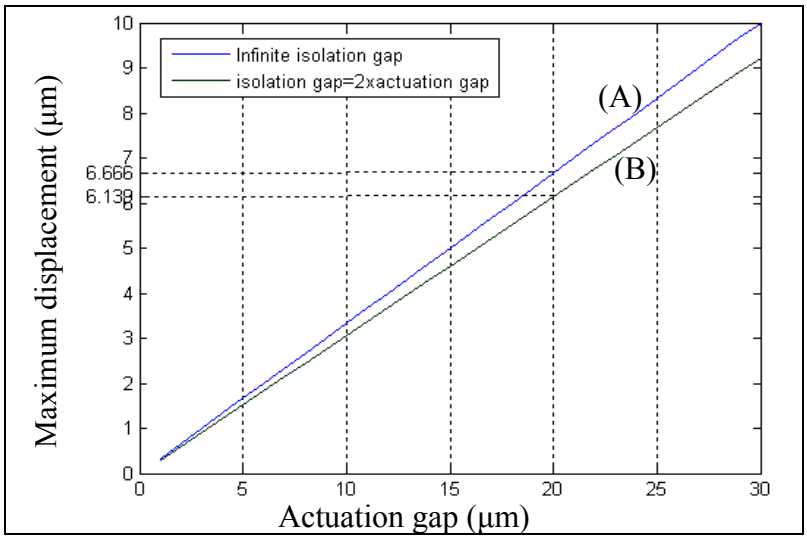
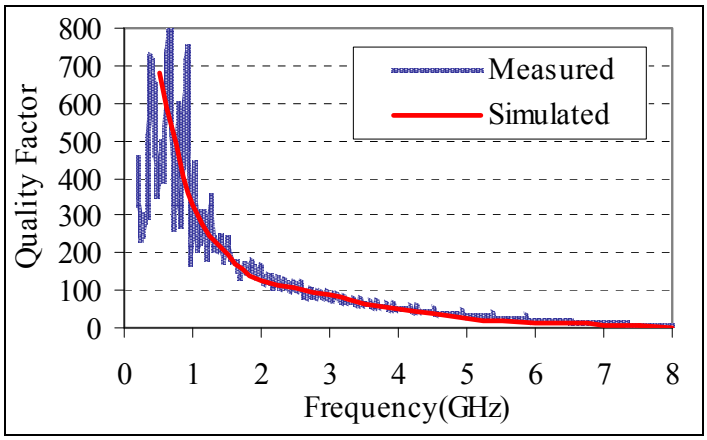


Figure 18: Simulated maximum displacement of a tunable capacitor in the dual-gap configuration when the isolation gap is set as (A) infinite and (B) twice the actuator gap.

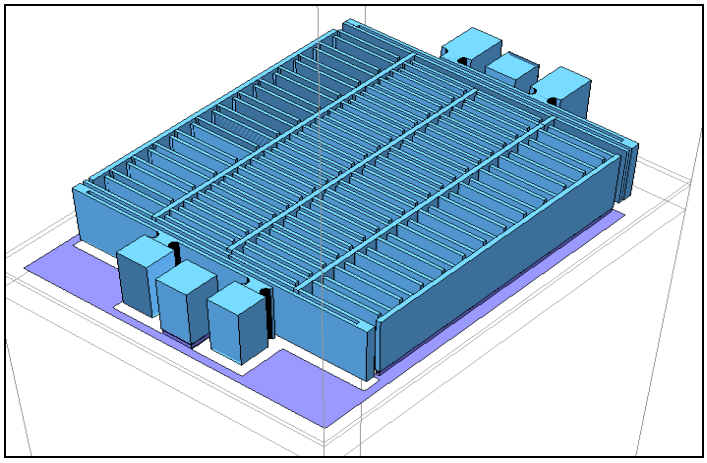
2.4.2 Electrical Performance

The frequency response of the capacitor shown in Figure 17 is simulated in the Sonnet using four metal sheets to account for the thickness of the capacitor. Figure 19(a) compares the measured and simulated Q of this capacitor, showing a good agreement between them. As shown in Figure 19(a), a high Q of > 100 is measured for this capacitor up to 3 GHz. The self-resonance frequency of the capacitor is higher than 6 GHz. The *SRF* of the capacitor is degraded due to the substantial inductance of the folded narrow springs. The actuation gap of this capacitor is three times the sense gap (i.e., 10 μm); therefore, the tuning range of this capacitor is ideally infinite with the application of 150 V. The capacitor exhibits a tuning of 3.3:1 with the application of 100 V (the maximum voltage that can be applied to the bias-tee network). The C-V tuning curve of this capacitor is shown in Figure 20. The Q and capacitance are extracted from the measured S-parameters using the relations shown below.

$$Q = \frac{\mathrm{Im}(Y_{11})}{\mathrm{Re}(Y_{11})} \quad \text{and} \quad C = \frac{-1}{\omega \times (\mathrm{Im}(1/Y_{11}))}. \tag{8}$$



(a)



(b)

Figure 19: (a) Measured and simulated *Q* of a 0.4 pF tunable capacitor fabricated on an Avatrel membrane and (b) the Sonnet simulation model.

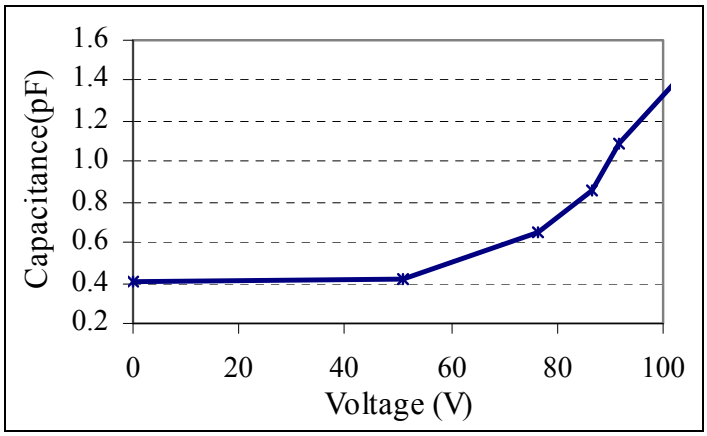
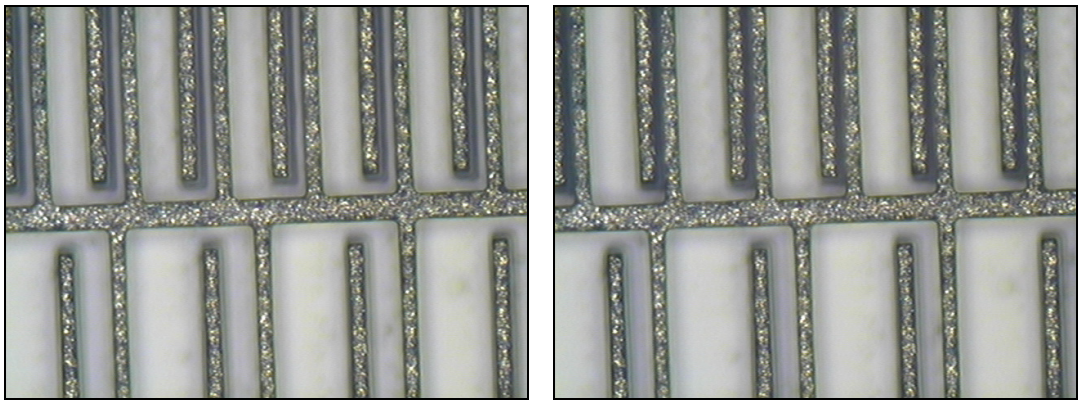


Figure 20: C-V tuning curve of the silver capacitor shown in Figure 19. The capacitance is extracted from the measured S-parameters at 50 MHz.

Figure 21 shows close-up micrographs of the capacitor, showing the gaps at the initial state (a) and at the tuned state (b).



(a) (b)

Figure 21: Micrograph images of the 0.4 pF capacitor showing the gap at (a) the initial state (b) the tuned state.

Figure 22 shows the electrical model of the fabricated tunable silver capacitors. C_s is the sense capacitance, R_s is the series resistance of the silver lines, and L_s is mainly the inductance of the folded springs. C_{si} and R_{si} are the parasitic capacitance and resistance of the substrate, respectively. When silicon is removed from the backside of the capacitor, C_{si} and R_{si} represent the parasitics of the pads.

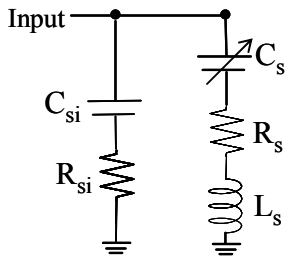
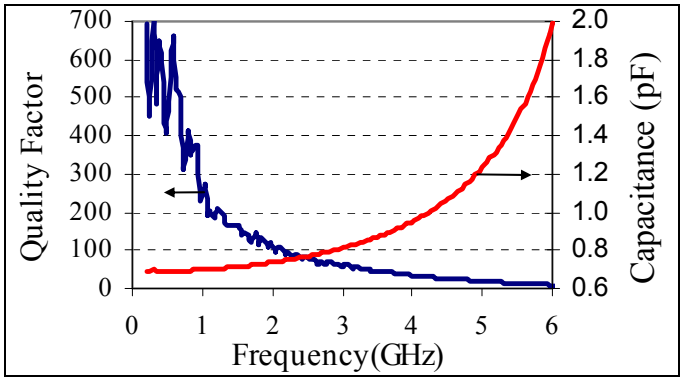


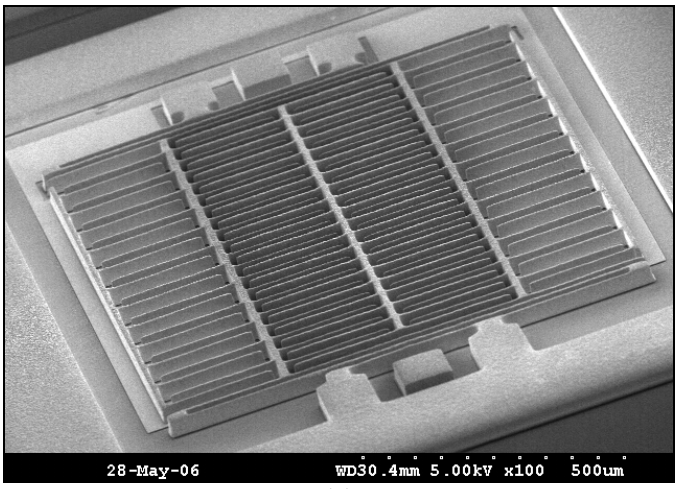
Figure 22: Electrical model of the silver tunable capacitors.

Figure 23(a) is the measured *Q* of a higher-value tunable capacitor that is shown in Figure 23(b). The actuation gap of this capacitor is twice the sense gap. Thus, the maximum displacement of the movable actuator/capacitor plates is 6.139 μm, as inferred

from Figure 18. Accordingly, in the absence of parasitic capacitances the capacitive tuning is 154%. The extracted parasitic capacitance (C_{si}) of this capacitor on an Avatrel membrane is only 25 fF. The measured tuning curve of this capacitor is shown in Figure 24. As shown, the capacitance is changed by 130% with a tuning voltage of 54 V. Tuning voltages of these capacitors are high due to the large size of the actuation gap. The actuation voltages can be reduced by decreasing the gap size and the spring width. Also, the high-frequency *Q* of these capacitors is low due to the parasitic inductance of the folded springs (L_s), which significantly lowers the *SRF*. The use of non-folded springs considerably improves the performance of the in-plane tunable capacitors.



(a)



(b)

Figure 23: (a) Frequency response and (b) a SEM view of a 40 µm thick 0.68 pF Silver capacitor on an Avatrel membrane.

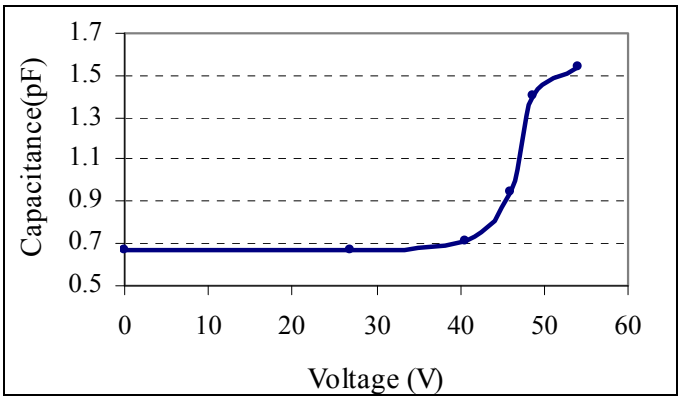


Figure 24: C-V tuning curve of the 0.68 pF capacitor shown in Figure 23(b).

2.4.3 Effect of the Substrate Loss

To identify the effect of the substrate on the Q, two identical capacitors to the one shown in Figure 23(b) are fabricated on an Avatrel-coated CMOS-grade silicon and an Avatrel-coated high-resistively silicon substrate (ρ >1 kΩ.cm) (silicon is not removed from the backside of these two samples). The measured Q of these capacitors is shown in Figure 25.

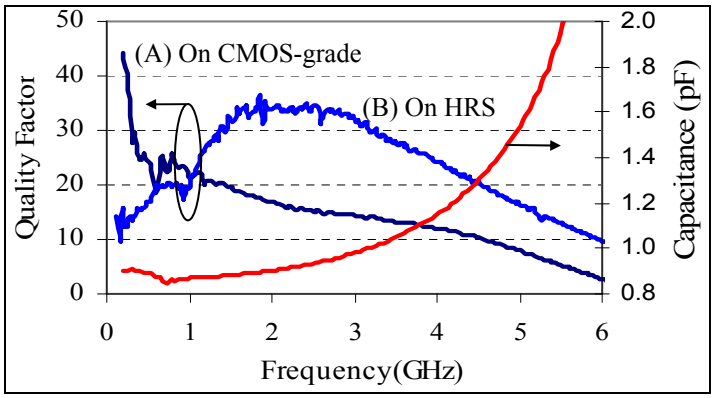


Figure 25: Measured embedded Q of two identical capacitors to the one shown in Figure 23 fabricated on an Avatrel-passivated (A) CMOS-grade and (B) high-resistivity silicon substrate.

A comparison of Figure 23(a) and Figure 25 reveals that by removing the substrate, the Q is improved by an order of magnitude at 1 GHz. Also, the parasitic capacitance of the capacitor body to the substrate (C_{si}) is significantly reduced by the backside etching of silicon. The capacitor exhibits a better performance at higher

frequencies when fabricated on HRS. On the other hand, the low-frequency Q of the capacitor on HRS is low due to the formation of a conductive layer at the interface of the substrate and the passivation layer [76], which results in an excess value for the equivalent series resistance at low frequencies [77].

2.5 Integrated Switched Tunable Inductors

Using the silver micromachining method we introduced in Section 2.1, we have also designed and fabricated switched tunable inductors. These inductors can be used in the tunable filters to achieve a wider frequency tuning and to reduce the required tuning ratio of the tunable capacitors. The design considerations are to achieve a small form-factor and a high Q in the frequency range of 1- 10 GHz. In this frequency range, the permeability of the most magnetic materials degrades [78], making them unsuitable for our application. Also, small displacement is preferred to simplify the encapsulation process of the tunable inductors. With these design objectives, we have developed a new implementation of tunable inductors based on the transformer action and using on-chip micromachined vertical switches with an actuation gap of a few micrometers. To encapsulate the tunable inductors, we have employed the wafer-level polymer packaging technique we introduced in Section 2.1. The switched tunable inductor presented here outperforms the reported tunable inductors with respect to its high embedded quality factor at radio frequencies.

2.5.1 Design

Figure 26 shows the schematic view of the switched tunable inductor [79], [80]. The inductance is taken from Port 1 and a plurality of inductors at Port 2 (secondary inductors) is switched in and out (two inductors in this case). Inductors at Port 2 are different in size; thus, they have different mutual inductance effect on Port 1 when activated. The effective inductance of Port 1 can have $1+n(n+1)/2$ different states, where

n is the number of inductors at Port 2. In the case of two inductors at Port 2, four discrete values can be achieved.

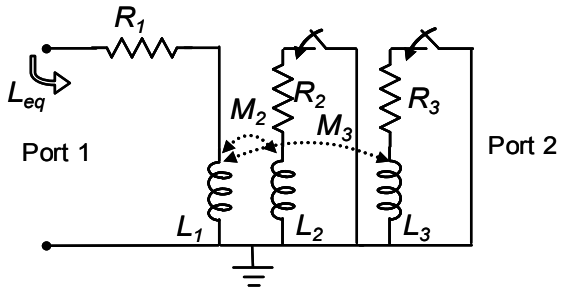


Figure 26: Electrical model of the switched tunable inductor.

The equivalent inductance and series resistance seen from Port 1 are found from

$$L_{eq} = L_1(1 - \sum_{i=2}^{n+1} \frac{b_i k_i^2 L_i^2 \omega^2}{R_i^2 + L_i^2 \omega^2}) \qquad b_i = 0 \text{ or } 1 \tag{9}$$

and

$$R_{eq} = R_1 + \sum_{i=2}^{n+1} \frac{b_i R_i k_i^2 L_1 L_i \omega^2}{R_i^2 + L_i^2 \omega^2} \qquad b_i = 0 \text{ or } 1\ , \tag{10}$$

where L_1 is the inductance at Port 1, L_i is the inductance value of the secondary inductors, R_i represents the series resistance of each secondary inductor plus the contact resistance of its corresponding switch, k_i is the coupling coefficient, b_i represents the state of the switch and is 1 (or 0) when the switch is on (or off), and ω is the angular frequency.

In (9) and (10), the parasitic capacitances are not considered. If we take into account the effect of parasitic capacitances, the equivalent inductance seen from Port 1 when all of the switches at Port 2 are open ($L_{eq(off\text{-}state)}$) is given by

$$L_{eq(off-state)} = L_1(1 + \sum_{i=1}^{n+1} k_i^2 \frac{1 - \frac{\omega^2}{\omega_{SRi}^2}}{\frac{\omega^2}{Q_i^2 \omega_{SRi}^2} - 2 + \frac{\omega^2}{\omega_{SRi}^2} + \frac{\omega_{SRi}^2}{\omega^2}}), \tag{11}$$

where Q_i is equal to $L_i\omega/R_i$ and represents the quality factor of the secondary inductors. ω_{SRi} is defined as

$$\omega_{SRi} = \frac{1}{\sqrt{L_i(C_i + C_{swi})}}, \tag{12}$$

where C_i denotes the self-capacitance of each inductor and C_{swi} is the off-state capacitance of its associated switch. If secondary inductors are high Q and have a self-resonance frequency much higher than the operating frequency (i.e., $\omega << \omega_{SRi}$), $L_{eq(off-state)}$ can be approximated by

$$L_{eq(off-state)} \overset{\omega<<\omega_{SRi}}{\approx} L_1\left(1 + \sum_{i=1}^{n+1} k_i^2 \frac{\omega^2}{\omega_{SRi}^2 - 2\omega^2}\right) \approx L_1 . \tag{13}$$

In this case, the largest change in the effective inductance occurs when all switches at Port 2 are on, and the percentage tuning can be found from

$$\%\ tuning = \sum_{i=2}^{n+1} \frac{b_i k_i^2 L_i^2 \omega^2}{(R_i^2 + L_i^2\omega^2)} \times 100 . \tag{14}$$

From (13) and (14), it can be seen that to achieve a large tuning range, R_i should be much smaller than the reactance of the secondary inductors, $L_i\omega$, which calls for high-Q inductors and low contact-resistance switches that are best implemented using micromachining technology. For this reason, our silver micromachining technique is well-suited for the implementation of a high-performance switched tunable inductor as this technology offers high-Q inductors and micromachined ohmic switches. The switches are actuated by applying a DC voltage to Port 2.

Figure 27 shows a SEM view of a 20 μm thick switched tunable silver inductor. The two inductors at Port 2 are in series connection with a vertical ohmic switch through a narrow spring. The springs are designed to have a small series resistance and a stiffness

of less than 15 N/m. The actuation voltage of the vertical switch with an actuation gap of 3.8 μm is 40 V. This voltage can be reduced to less than 5 V by reducing the gap size to ~0.9 μm. Since the off-state capacitance of a switch with an air gap of 0.9 μm remains in a few femtofarad range, reducing the gap size to 0.9 μm does not affect the electrical performance of the switched tunable inductor (14). A close-up view of the switch showing the actuation gap is shown in Figure 28. A micrograph of an un-packaged inductor taken from the backside of the Avatrel membrane is shown in Figure 29.

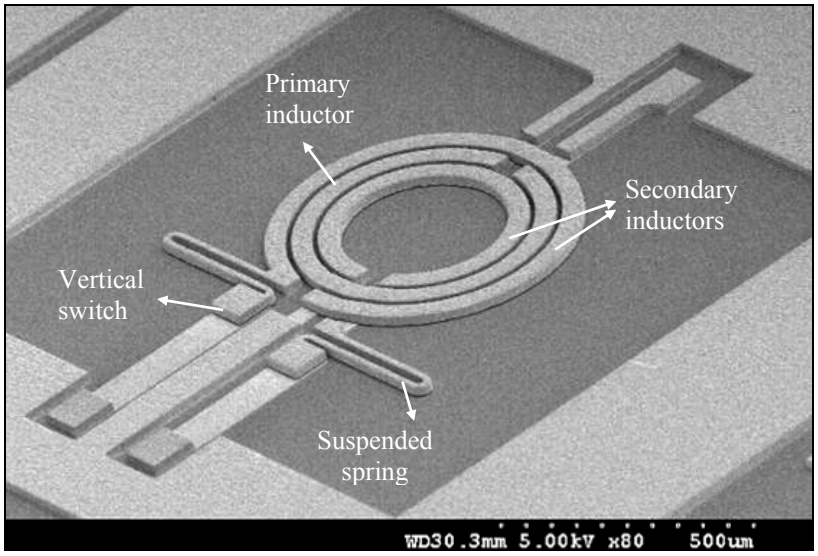


Figure 27: A SEM view of a 20 μm thick silver switched tunable inductor fabricated on an Avatrel membrane.

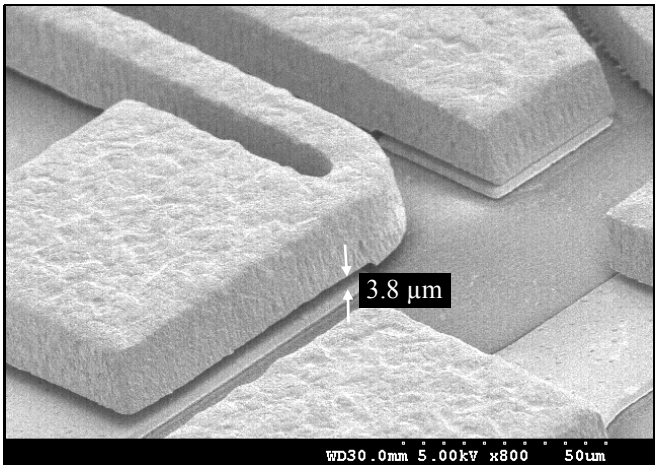


Figure 28: A close-up SEM view of the switch, showing the actuation gap.

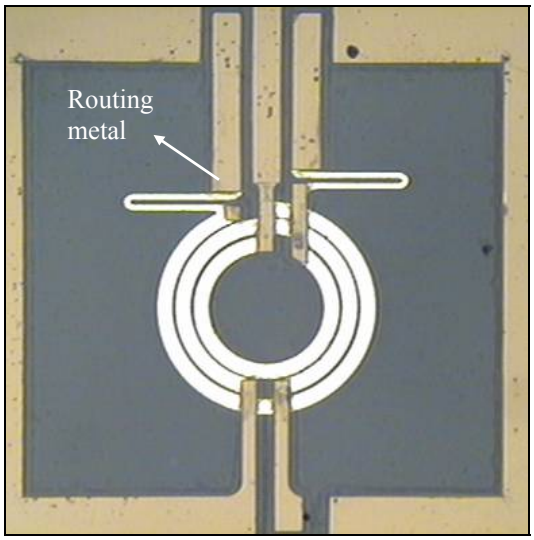
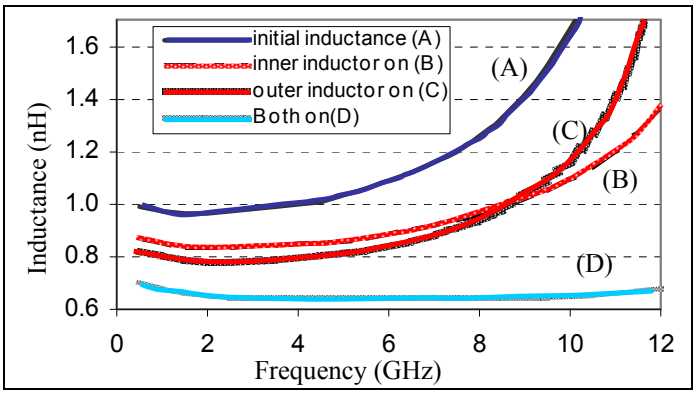


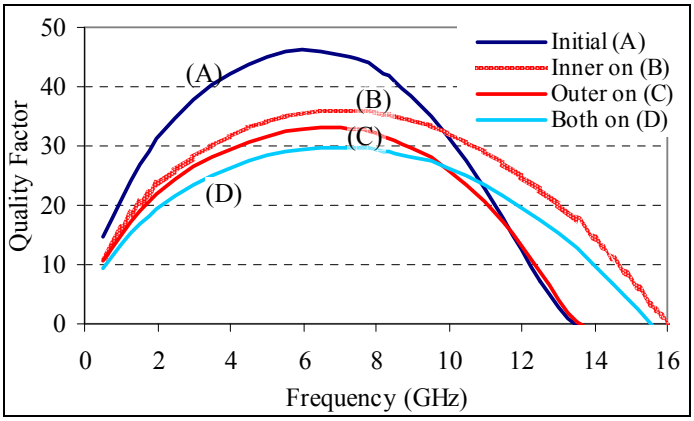
Figure 29: A micrograph of the switched tunable inductor taken from the backside of the Avatrel membrane.

2.5.2 Simulation Results

The tunable inductors are simulated in the Sonnet. Figure 30 shows the simulated effective inductance and Q seen from Port 1 at four states of the tunable inductor (state (A) is when all the switches are off). As shown in Figure 30(a), a maximum inductance change of 47% is expected at the frequency of the peak Q when both switches are on. At low frequencies, R_i is not negligible compared to $L_i\omega$. According, the percent tuning is small (14). At higher frequencies, $L_i\omega$ is much larger than R_i, and the magnetic coupling is stronger. Therefore, the tuning range increases at higher frequencies. The outer inductor is larger in size than the inner one, and its peak Q occurs at lower frequencies. As a result, the outer inductor has a larger effect on the effective inductance at lower frequencies. In contrast, the frequency of the peak Q for the inner inductor is higher. Thus, the inner inductor has a stronger effect at higher frequencies.



(a)



(b)

Figure 30: Simulated (a) inductance and (b) *Q* of the switched tunable inductor on an Avatrel membrane, showing a maximum tuning of 47.5% at 6 GHz.

2.5.3 Measurement Setup

Several switched tunable inductors are fabricated and tested. Herein, on-wafer S-parameter measurements are carried out using an *hp*8510C VNA and Cascade GSG air coplanar probes (ACP). The test setup is schematically shown in Figure 31. Each switched tunable inductor is tested several times to ensure the repeatability of the measurements.

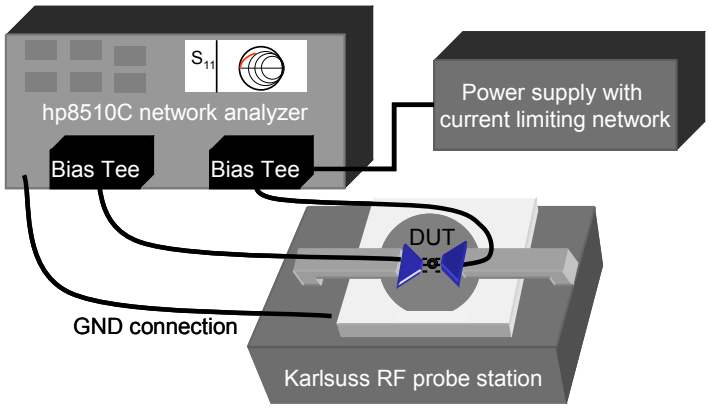


Figure 31: Schematic of the test setup for tunable inductors.

Figure 32 shows the measured inductance of a switched silver inductor fabricated on an Avatrel membrane. The inductance is switched to four different values and is tuned from 1.1 nH at 6 GHz to 0.54 nH, which represents a maximum tuning of 47% at 6 GHz. The maximum tuning is achieved when both inductors are switched on. At 6 GHz, the effective inductance drops to 0.79 nH when the outer inductor is on, and it drops to 0.82 nH when the inner inductor is on. The measured results are in good agreement with the simulated response, as shown in Figure 30(a) and Figure 32. The measured embedded Q of this inductor in different states is shown in Figure 33. As shown, the inductor exhibits a peak Q of 45 when the inductors at Port 2 are both off. The Q drops to 20 when both switches are on. The drop in the Q is consistent with (9) and (10). When any inductor at Port 2 is switched on, L_{eq} decreases, while the effective resistance increases, resulting in a drop in the Q as the inductor is tuned. Figure 34 shows the measured Q of the inductors at Port 2. In Figure 34, it can be seen that the peak Q of the inner inductor is at frequencies above 6 GHz. Thus, the maximum change in the effective inductance resulted from switching on the inner inductor occurs in the 6-10 GHz frequency range, as shown in Figure 32.

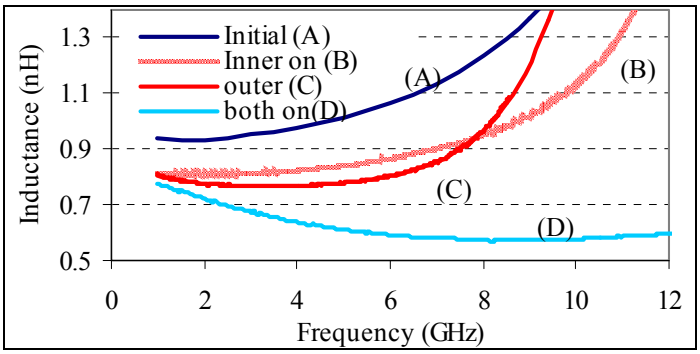


Figure 32: Measured inductance, showing a maximum tuning of 47 % at 6 GHz when both inductors are on.

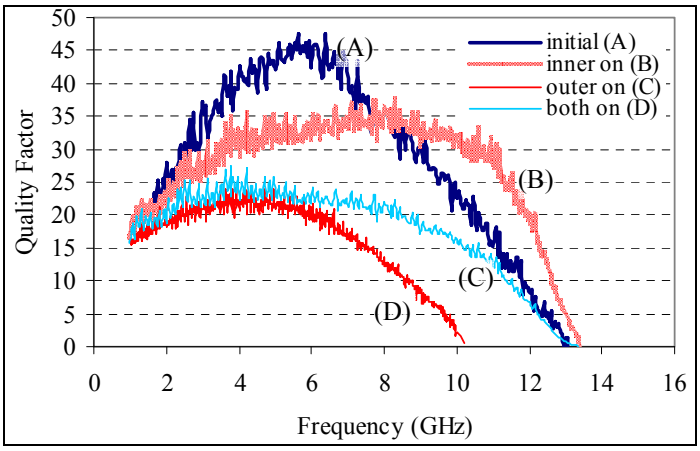


Figure 33: Measured embedded *Q*, showing the *Q* drops as the inductor is tuned.

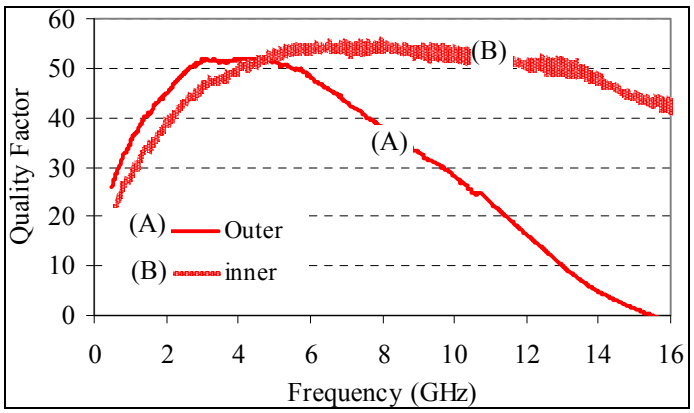
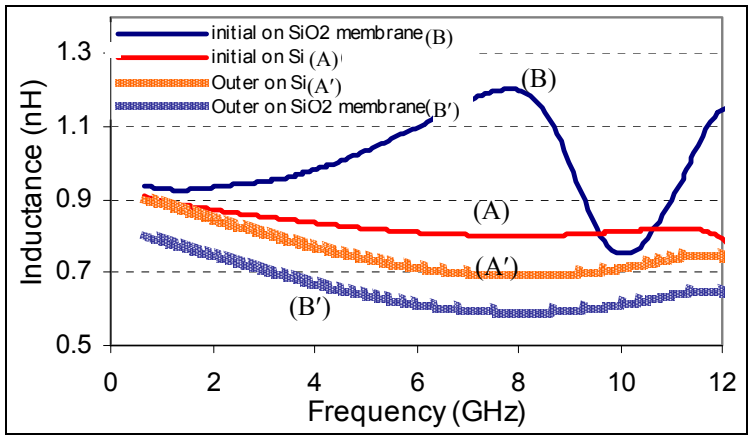


Figure 34: Measured *Q* of the inductors at Port 2 on an Avatrel membrane.

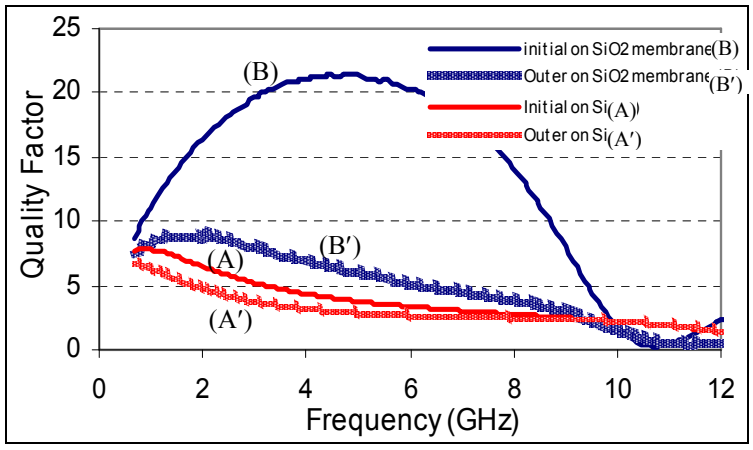
2.5.4 Effect of Q on Tuning

To demonstrate the effect of the *Q* on the tuning ratio of the switched tunable inductors, identical devices are fabricated on different substrates (Figure 35). On sample

A, inductors are fabricated on a CMOS-grade silicon substrate passivated with a 20 µm thick PECVD silicon dioxide layer. The silicon substrate is removed from the backside of inductors of sample B, leaving a 20 µm thick silicon dioxide membrane beneath the inductors. Silicon dioxide has a higher permittivity than Avatrel, which results in a higher substrate loss [26]. Therefore, the Q of inductors on a silicon dioxide membrane (sample B) is lower than the Q of inductors on an Avatrel membrane that is shown in Figure 33. Figure 35 compares the effective inductance and Q of the tunable inductors on samples A and B at two different states.



(a)



(b)

Figure 35: Measured (a) inductance and (b) embedded Q of identical tunable inductors fabricated on (A) a passivated silicon substrate and (B) a 20 µm thick silicon dioxide membrane. State A and B are the initial inductances, and states A′ and B′ are when the outer inductor is switched on.

As shown in Figure 35, the percent tuning is lower for sample A that has a lower Q. The inductance of sample B changes by 36.8% at 4.7 GHz when the outer inductor is switched on (state B′). At this frequency, the tuning that is resulted from switching on the outer inductor of sample A (state A′) is only 9.7%. Consequently, employing low-loss materials, such as Avatrel, helps improving the tuning characteristic of the switched tunable inductors.

It should be mentioned that the performance of the silver tunable inductors can be further improved. The routing metal layer of the fabricated inductors is less than three times the skin depth of silver at low frequencies, where the metal loss is the dominant Q-limiting mechanism. Therefore, the Q of the switched tunable inductors is limited by the loss of the routing layer and can be improved by increasing the thickness of this layer. As shown in Figure 14, a fixed inductor with identical dimensions to L_1 but with no routing layer exhibits a high embedded Q of greater than 150 at 6 GHz [75]. The limited thickness of the routing layer has a more pronounced effect on the Q of the switching inductors at Port 2 as the length of the routing layer is longer at Port 2 (Figure 27). The Q of a 0.88 nH inductor with identical dimensions to the inner inductor but with no routing layer is shown in Figure 36. The inner inductor without routing exhibits a high embedded Q of greater than 140 at 6 GHz. A comparison of Figure 34(A) and Figure 36 proves that the metal loss is higher for the inner inductor with the thin routing layer.

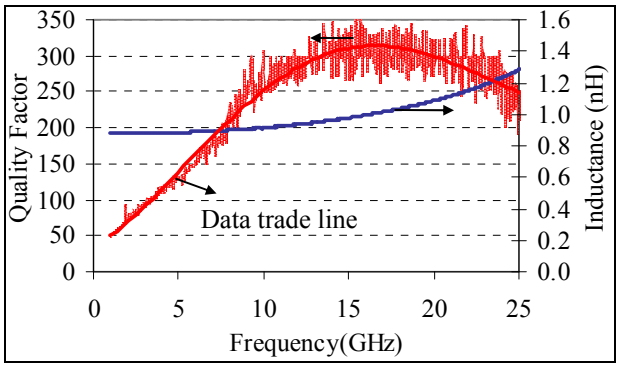


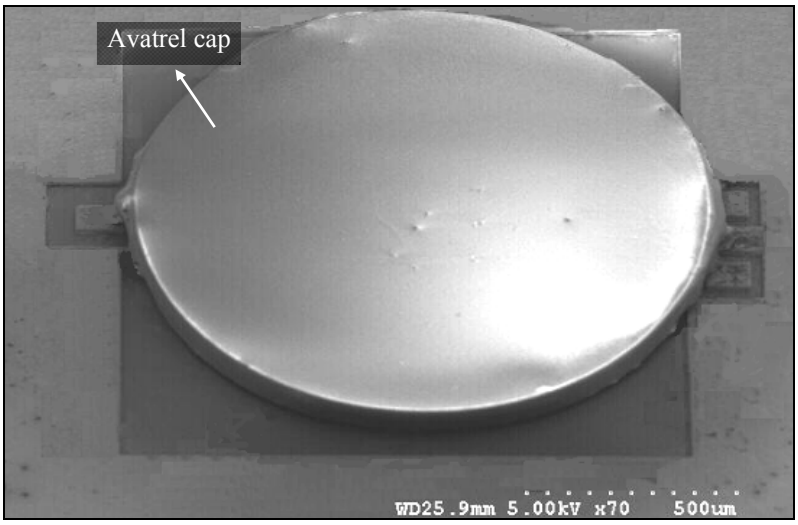
Figure 36: Measured characteristics of the inner inductor without the routing layer fabricated on an Avatrel membrane, showing Q in excess of 140 at 6 GHz.

2.5.5 Packaging Results

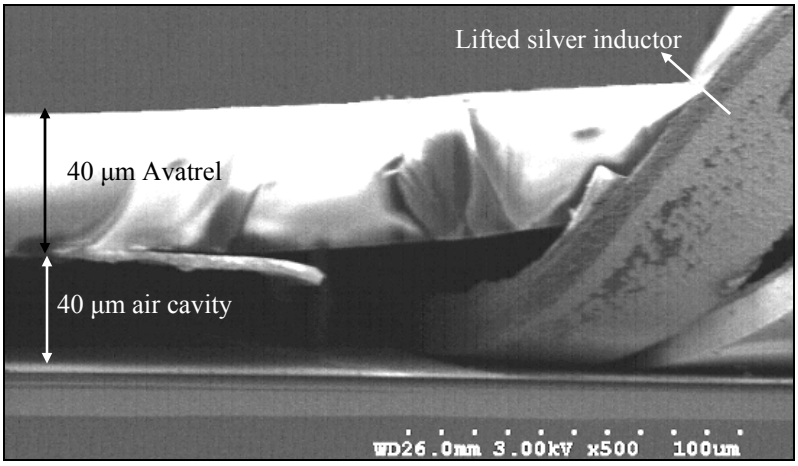
In Section 2.1, we discussed that a hermetic or semi-hermetic encapsulation of the silver microstructures increases the lifetime of the device by protecting it from the corrosive gases and by reducing the possibility of the electrochemical migration. For the tunable inductor structure presented here, the possible location of the dendrite failure is between the switch plates only when the switch is in contact. When off, there is an air gap between the switch plates, which blocks the path for the growth of dendrites.

We have encapsulated the tunable inductors using the on-wafer encapsulation technique introduced in Section 2.1. Figure 37 is a SEM view of the encapsulated switched tunable inductor and a close-up view of a broken package, showing the air cavity inside. The inductor trace is peeled during the cleaving process.

Figure 38 shows the Q of two identical inductors before the decomposition of the Unity sacrificial polymer. The two inductors, one packaged and one un-packaged, are fabricated on a silicon nitride-passivated high-resistivity (ρ = 1 kΩ.cm) silicon substrate. As expected, the un-decomposed packaged inductor has a lower Q at higher frequencies because of the dielectric loss of the Unity sacrificial polymer. When Unity is decomposed and the packaging process is completed, the two inductors are measured again. As shown in Figure 39, the switched tunable inductor shows no degradation in Q after the packaging process is completed, indicating that the Unity sacrificial polymer is fully decomposed. To demonstrate the effect of the package on preserving the Q of the silver tunable inductor, the performance of the packaged inductor is measured after 10 months and is shown in Figure 40. As shown, the performance of the packaged inductor has not changed during this time period.



(a)



(b)

Figure 37: A SEM view of the packaged switched inductor and (b) a close-up view of a broken package.

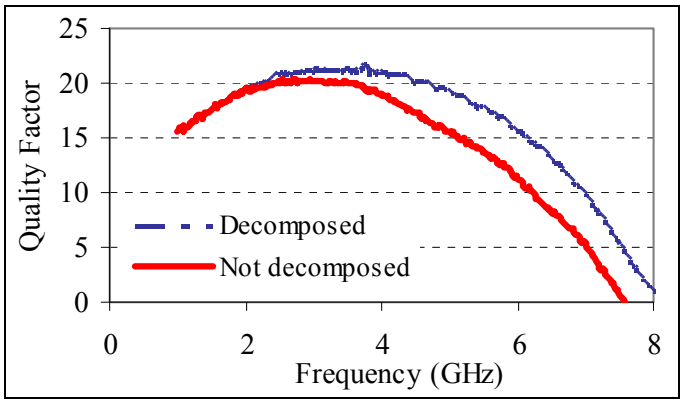


Figure 38: Measured embedded *Q* of two identical inductors, one packaged with un-decomposed Unity and one un-packaged.

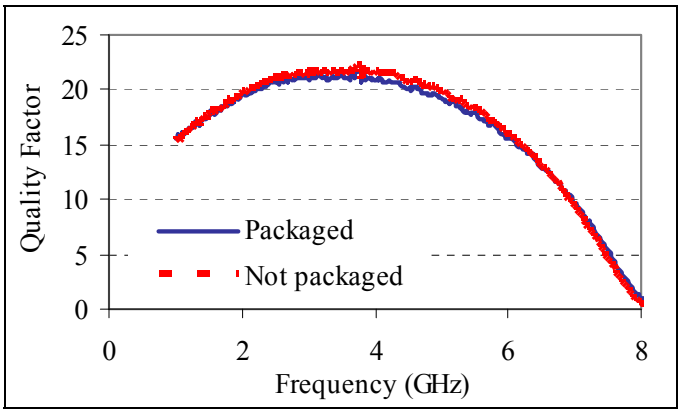


Figure 39: Measured embedded *Q* of two identical inductors when both switches are off, one packaged and one un-packaged.

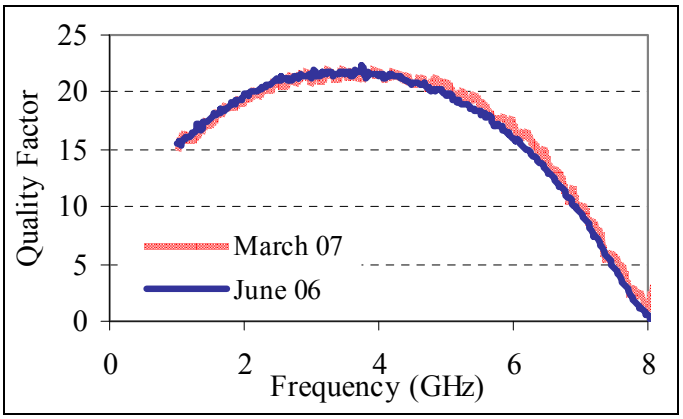


Figure 40: Measured embedded *Q* of the packaged silver tunable inductor, showing no degradation in *Q* after 10 months.

CHAPTER 3

WAFER-LEVEL PACKAGED FIXED-FREQUENCY LUMPED BANDPASS FILTERS

In Chapter 1, we discussed that the integration of high-performance lumped element filters *on the standard silicon substrate* has attracted very little effort, mainly because of the insufficient Q of the individual on-chip inductors and capacitors, causing a high insertion loss and a poor out-of band rejection for the filters. With the knowledge about the sources of loss in an on-chip lumped filter, we developed a silver micromachining technique that offers high-performance components on silicon. Using this technique, we demonstrated record high-Q fixed and tunable inductors as well as tunable capacitors, as discussed in Chapter 2. The high-Q passives enabled by this fabrication method make the implementation of low-loss narrow-band filters on silicon possible.

In this chapter, we demonstrate high-performance fixed-frequency bandpass filters in the UHF range. We identify the quality factor of the individual passive components and explain the physical and practical limits of achieving the required filter performance. We address the issue of silver fatigue and failure, such as the formation of silver dendrites, by employing the wafer-level polymer encapsulation technique introduced in Chapter 2. We also demonstrate an array of several fixed bandpass filters for the application of filtering closely-located signals. We experimentally show the effect of the termination impedance and physical layout on the performance of the lumped filters. Finally, we determine the temperature characteristics of the lumped silver filters by measuring the frequency response of the filters at elevated temperatures.

3.1 Filter Design

Typical specifications in a bandpass filter are center frequency (f_0), bandwidth, insertion loss, out-of-band rejection, roll-off, ripple, and group delay. In addition, the size of the filter is an important parameter, particularly for integrated lumped filters in the VHF and UHF range. Among different LC filter configurations, Elliptic filters require the fewest components with the most practical values to attain a specific filter Q. Therefore, using an Elliptic filter topology not only simplifies the fabrication of MEMS filters, but also minimizes the die area. A drawback to Elliptic filters is their nonlinear phase delay, which its importance has to be identified based on the filter application. For these reasons, we have chosen the Elliptic configuration for our bandpass filters. Filters are designed with the following restrictions on the component values:

1) Inductor value should be between 0.5 nH and 10 nH for the practical high-Q ($Q > 80$) implementation on chip.
2) Capacitor value should not exceed 10 pF for obtaining a high Q. The minimum value of the capacitance is defined by the parasitic capacitances to be 0.1 pF.

With the above-mentioned specifications, third-order bandpass Elliptic filters are designed in the UHF range. The general circuit diagram of an Elliptic filter showing the function of each parallel tank is illustrated in Figure 41. The identical parallel tanks at the input and output mainly define the center frequency, and the tanks connected in series between the input and output define the location of the notches of the Elliptic filter.

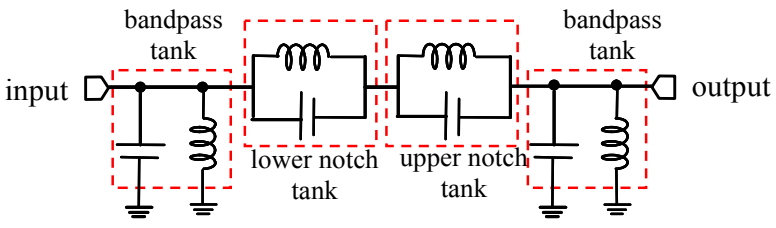
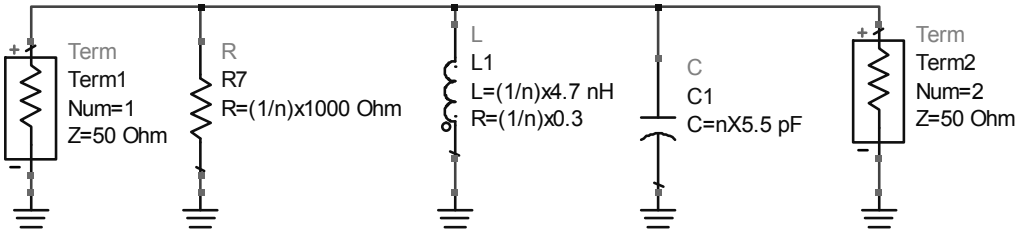


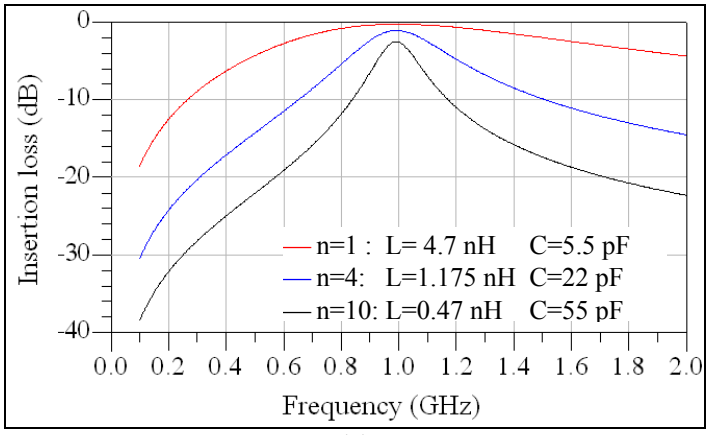
Figure 41: Schematic view of a third-order bandpass Elliptic filter.

It is worth mentioning that for a given termination impedance, the Q of a parallel LC tank increases by increasing the value of the capacitor while maintaining the $L \times C$ value constant. Figure 42 is an illustration of this fact. In Figure 42(a), the circuit diagram of a parallel LC tank circuit with 50 Ω termination impedances is illustrated. The individual components are assumed to have a specific Q. The frequency responses of three parallel tanks are shown in Figure 42(b), illustrating that as the ratio of the capacitance to inductance increases, the Q of the parallel resonator increases. Here, the resonator Q is defined as the following relation, where Δf_{-3dB} is the 3 dB-bandwidth of the resonator.

$$Q = \frac{f_0}{\Delta f_{-3dB}}. \tag{15}$$



(a)



(b)

Figure 42: (a) Circuit diagram and (b) frequency response of three parallel tank circuits, assuming a constant Q for the individual lumped components. The Q of the parallel resonator increases by increasing the C/L ratio.

However, for a specific tank Q, by increasing the termination impedance, the required capacitance value decreases and the inductance value increases (Figure 43). As shown in Figure 43, the parallel tank with 150 Ω terminations requires a smaller capacitance and a larger inductance to exhibit the same Q as the parallel tank with 50 Ω terminations offers. To obtain a high-Q parallel resonator, such as the one shown in Figure 43, the required component values for the resonator with larger terminations are more practical.

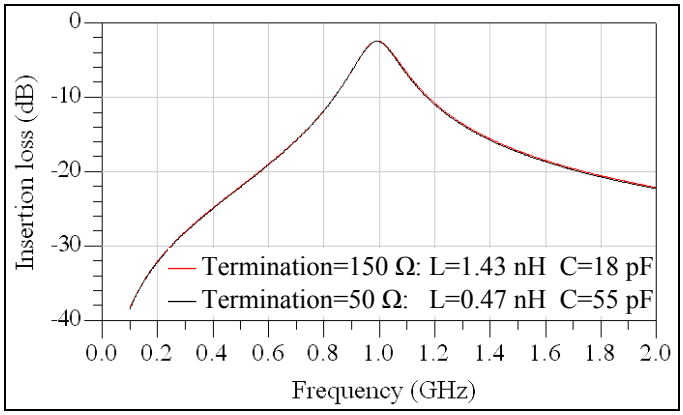


Figure 43: Frequency response of two parallel tank circuits with the same *Q* but with different termination impedances, showing that by increasing the termination impedance, the inductance value increases and the capacitance value decreases.

Consequently, in this work, we have considered the termination impedance as a design parameter that offers the alternative of changing the value of the individual lumped components without sacrificing the overall performance of the filter. For each filter presented in this thesis, we accordingly describe our rationale for selecting a particular termination impedance.

3.2 A Low-Loss Filter at 1.2 GHz

3.2.1 Electrical Circuit Design

A third-order bandpass Elliptic lumped filter is designed using the *hp*ADS simulation tool. The filter is designed at 1 GHz with a 3 dB-bandwidth of 300 MHz and

out-of-band rejection of more than 15 dB when terminated to the standard 50 Ω impedance. This filter could be used in front of acoustic filters with higher *Q*s to improve the overall out-of-band rejection of the system and to remove the spurious modes of the acoustic filters. The schematic diagram of the Elliptic filter, outlining each component value, is shown in Figure 44. The frequency response of the filter, when terminated to 50 Ω, is shown in Figure 45. In the filter simulation, the inductor and capacitor *Q*s are taken as 60 and 120, respectively. The resulted minimum insertion loss of the filter is 0.92 dB, as shown in Figure 45.

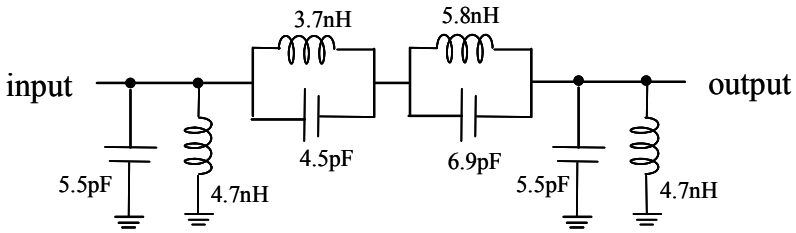


Figure 44: Schematic view of the third-order bandpass Elliptic filter at 1 GHz.

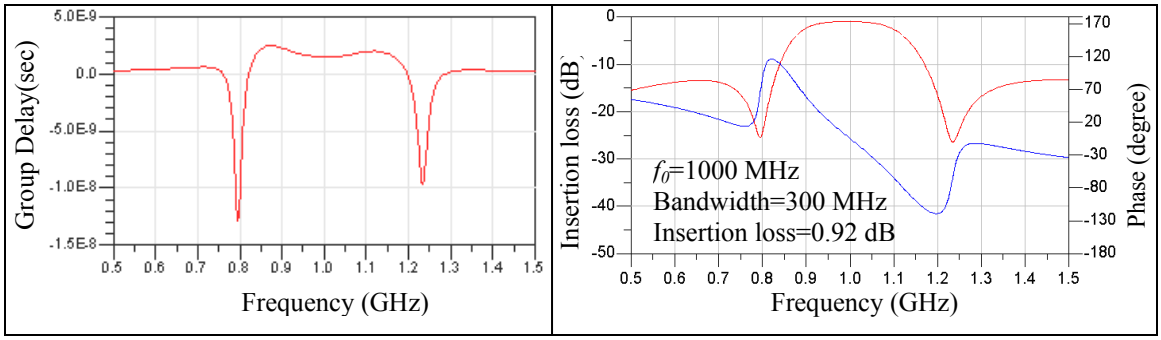


Figure 45: Simulated group delay and frequency response of the Elliptic filter.

3.2.2 Measured Results

The Elliptic filter is fabricated using the silver micromachining technique introduced in Chapter 2 with an electroplated silver thickness of 40 μm and a routing layer of 4 μm. The silicon dioxide interlayer dielectric defines the capacitive gap of the metal-insulator-metal (MIM) capacitors and is 3.5 μm in this batch. A SEM view of the

fabricated filter is shown in Figure 46. With a capacitive gap of 3.5 μm, this filter occupies 3 mm × 3 mm of die area. Reducing the capacitive gap thickness significantly reduces the size of each capacitor and consequently, the size of the filter.

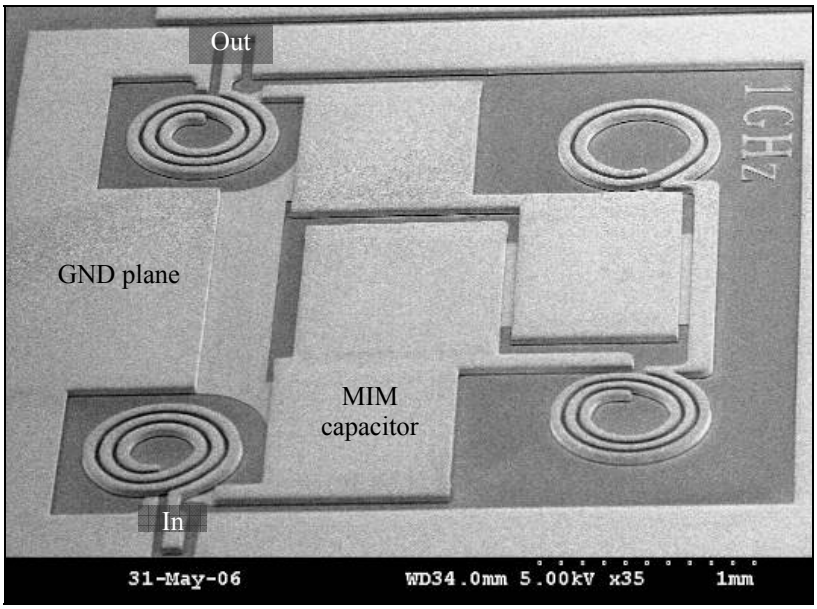


Figure 46: A SEM view of the fabricated silver Elliptic filter.

Figure 47 compares the measured S_{21} of two identical filters, one is fabricated on an Avatrel membrane (silicon is removed from the backside), and the other one is fabricated on an Avatrel-passivated CMOS-grade silicon substrate (silicon is not removed). The filter on the Avatrel membrane exhibits a very low insertion loss of 0.9 dB at 1.2 GHz with a bandwidth of 330 MHz when terminated to 50 Ω. The identical filter on passivated silicon substrate has an insertion loss of 3.6 dB and a smaller bandwidth because of the lower $Q_{substrate}$ of the components and higher loss of the interconnects on silicon.

The measured center frequency and bandwidth of the filters are deviated from the initial ADS simulations, which is in part due to the imprecise thickness of the silicon dioxide layer. To investigate this further, the layout of the filter is simulated in the Sonnet using the Sonnet thick-metal model with two sheets, and the fitted values for the silver

conductivity as well as the silicon dioxide thickness and loss tangent are obtained. The simulated and measured frequency responses are compared in Figure 48.

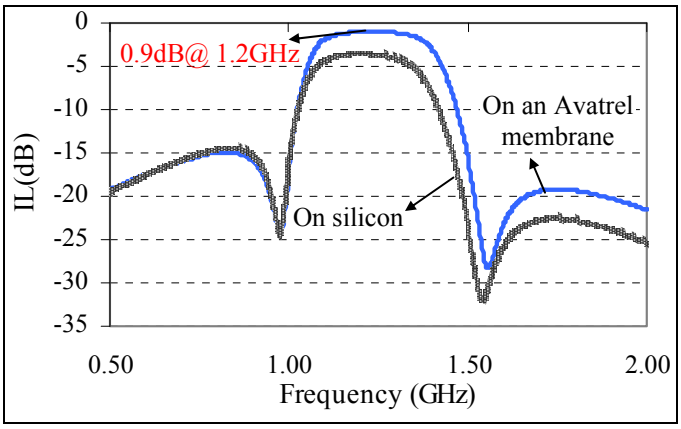


Figure 47: Comparison of the measured S_{21} of a third-order Elliptic filter fabricated on an Avatrel membrane and a passivated silicon substrate.

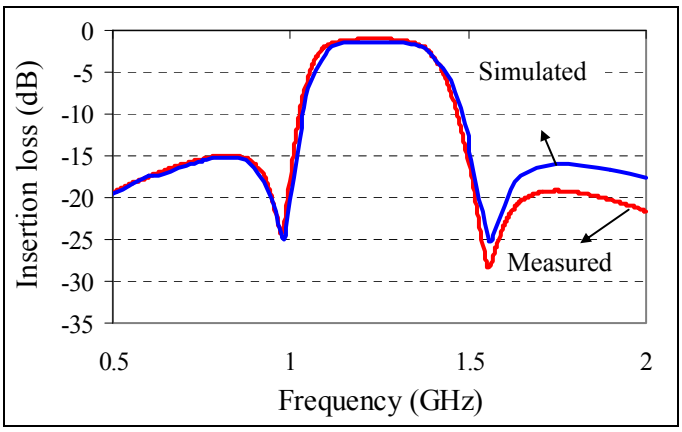


Figure 48: Measured and Sonnet simulated response of the Elliptic filter on an Avatrel membrane.

The fitted model of the filter suggests that the loss tangent and permittivity of the silicon dioxide layer is 0.001 and 3.8, respectively. In the initial calculations, the oxide permittivity was taken as 3.9. The lower permittivity of the PECVD silicon dioxide results in a lower capacitance density, which in turn increases the center frequency and bandwidth of the fabricated filter.

In addition, the thickness of the silver layer is 40 μm, which is comparable to the width of the spiral turns (Figure 46). A planar spiral inductor with thicker metal lines

exhibits a lower inductance, as suggested by the expanded Grover equation (also known as Greenhouse equation) for the inductance value noted below [81].

$$L_T = L_0 + M_+ - M_-, \qquad L_0 = \sum L_x$$
$$L_x = 2l_x\{\ln[2l_x/(w+t)] + 0.50049 + [(w+t)/3l_x]\}, \tag{16}$$

where t and w are the respective conductor thickness and width in centimeter. l_x is the length of each spiral segment in centimeter. L_x, M_+, and M_- are the inductance of each segment, the positive mutual inductance, and the negative mutual inductance in nanohenry, respectively. In (16), note that when the length of each segment is much larger than the sum of the width and thickness, the last term (i.e., $(w+t)/3l_x$) is negligible and the inductance is related to the negative sign of $(w+t)$. Therefore, thick silver inductors have a lower inductance than that predicted by the Mohan's equation [82], which was used in our preliminary calculations. In Mohan's equations, the effect of the conductor thickness is disregarded. As a result, the measured center frequency of the filter is higher than expected.

The frequency response of three filters measured on different parts of a four inch wafer is shown in Figure 49. As shown, all filters have common characteristics in the pass-band, which shows that the fabrication process has a high yield. Also noticeable from Figure 49 is an unexpected notch at 2 GHz. The same frequency behavior can be seen from the Sonnet simulation response shown in Figure 50. To identify the origin of this notch, several simulations with different layouts for the filter are performed. By comparing the Sonnet simulated response of identical filters with different layouts for the ground plane, it is verified that the high-frequency notch of the filter is resulted from the part of the ground plane that is extended between the input and output inductors, as shown in Figure 46.

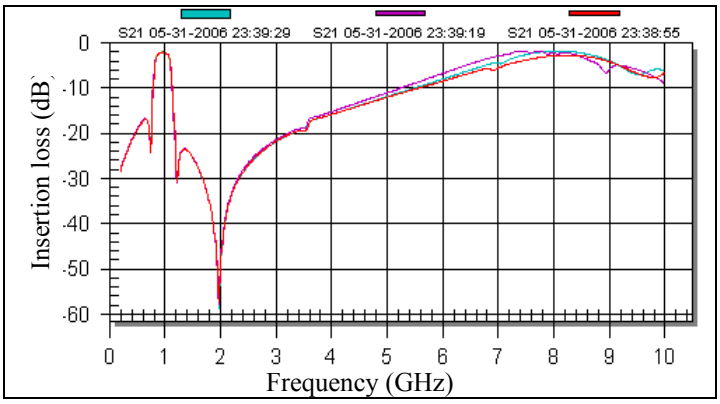


Figure 49: Measured response of three Elliptic filters on the same wafer.

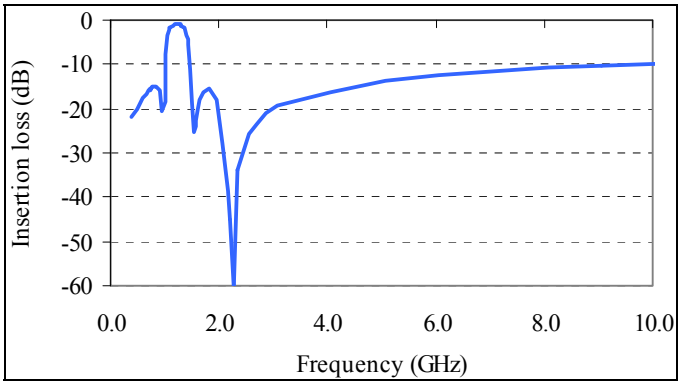


Figure 50: Sonnet simulated response of the Elliptic filter in a broad frequency range.

3.2.3 Packaging Results

Figure 51 shows the frequency response of the filter fabricated on a high-resistivity silicon substrate (ρ >1 kΩ.cm). In this case, the passivation layer is only 1 µm silicon nitride in addition to 1 µm silicon dioxide. At 1.2 GHz, the dominant source of loss is the ohmic loss of the metal layers, which is significantly reduced because of the high conductivity of silver. Therefore, despite the passivation layer being much thinner than that of the filters shown in Figure 49, the insertion loss of the filter on the passivated HRS substrate is increased by only 1.2 dB (to 2.1 dB) at 1.2 GHz. To preserve the quality of silver and to maintain the insertion loss low, we have encapsulated the filter using the wafer-level polymer encapsulation technique introduced earlier. Figure 51 shows the frequency response of two identical filters on the same wafer, which only one

of them is encapsulated. As shown in Figure 51, the performance of the encapsulated filter has not changed after packaging [75], [83].

To investigate the effectiveness of the package, the two filters are measured again after 21 months (Figure 52). As shown in Figure 52, the insertion loss of the encapsulated filter remained un-changed, while the performance of the un-packaged silver filter is deteriorated by 0.3 dB. This indicates that Avatrel, without any metal over-coating, is providing some level of hermeticity. A SEM view of the encapsulated filter is shown in Figure 53. The encapsulated filter occupies 3 mm × 3 mm of die area.

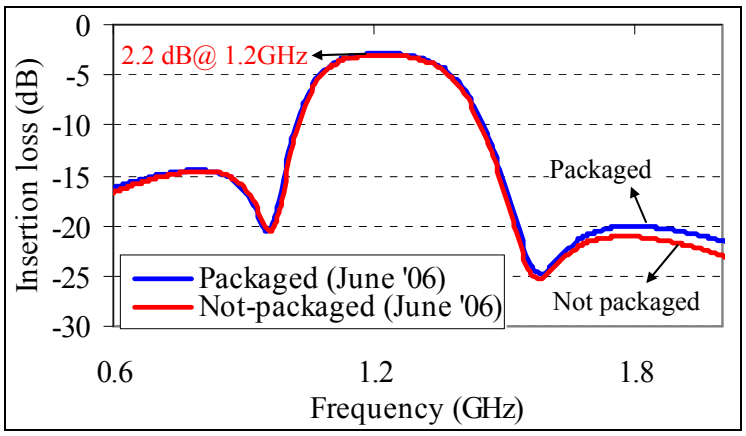


Figure 51: Measured frequency response of the Elliptic filter at 1.2 GHz fabricated on a high-resistivity silicon substrate, one is packaged and the other one is not packaged.

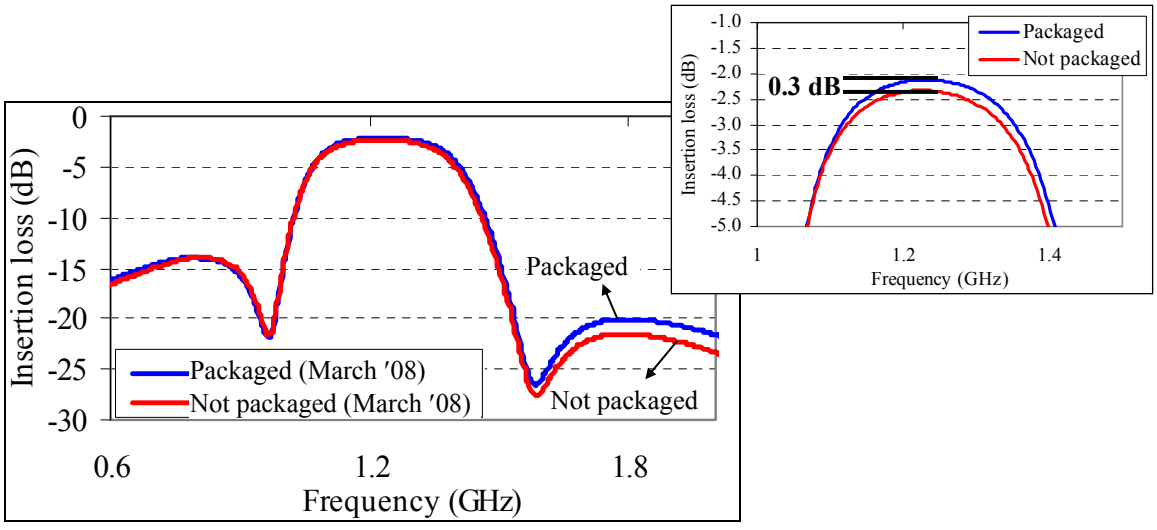


Figure 52: Measured frequency response of the Elliptic filters after 21 months. The inset is the close-up view of the response of the filter response at pass-band.

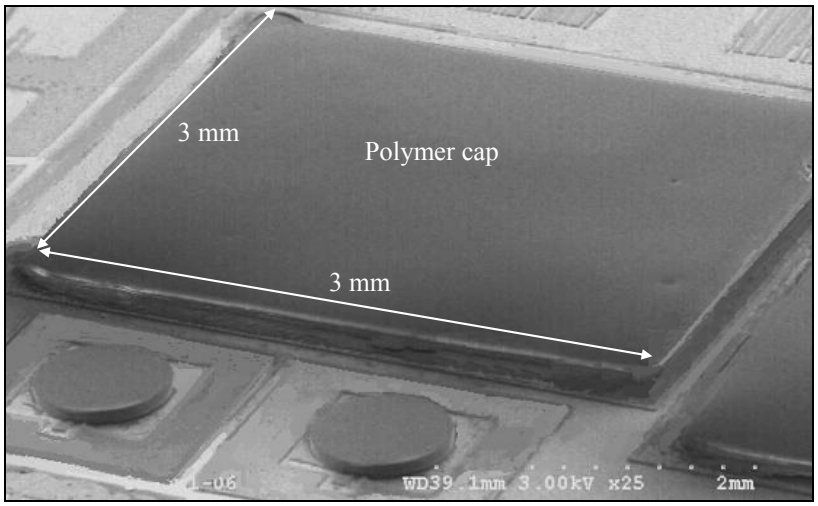
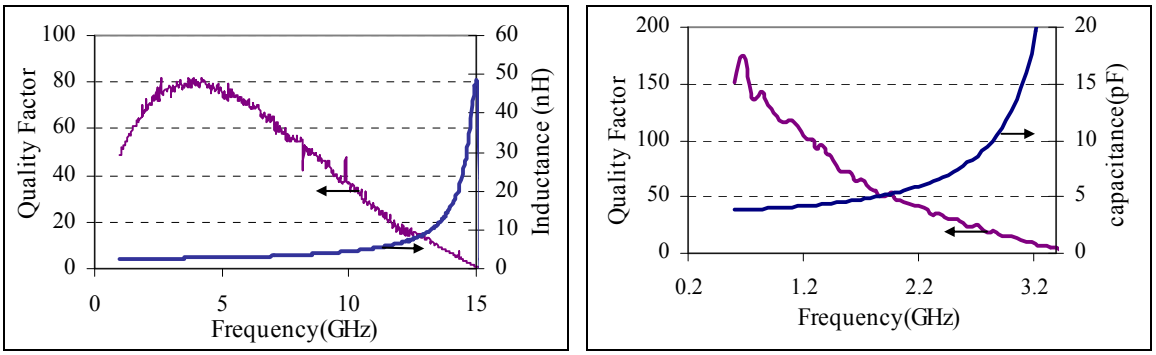


Figure 53: A SEM view of the wafer-level encapsulated filter.

3.2.4 Individual Component Q

The quality factor of the individual fixed components used in the filter is measured on test structures. The responses of the lowest-value inductor and capacitor are shown in Figure 54.



(a) **(b)**

Figure 54: Measured characteristics of the individual filter components on an Avatrel membrane; (a) a 3.2 nH inductor and (b) a 3.8 pF capacitor.

As explained in Section 3.2.2, both the measured inductance and capacitance values are lower than the designed values shown in Figure 44. A 3.2 nH inductor and a 3.8 pF capacitor exhibit *Q*s of 60 and 102 at 1.2 GHz, respectively (Figure 54). The larger inductors used in the filter have higher *Q*s at 1.2 GHz. Therefore, this is the lower bound

of the individual inductor *Q*. To further improve the performance of the bandpass filter and passive components, several issues have to be addressed. We discuss this matter in the next section.

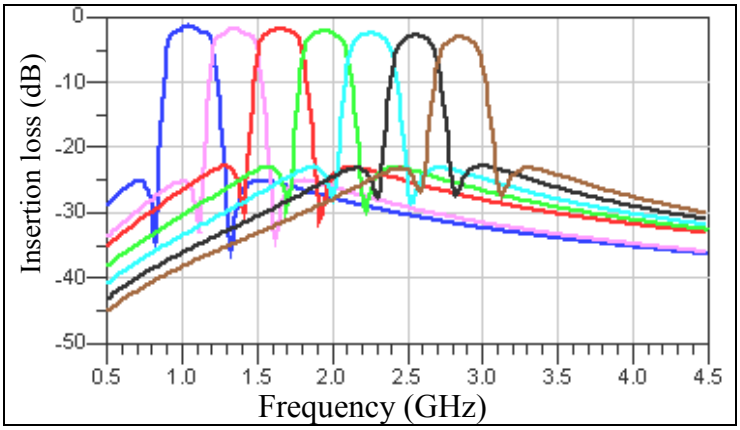
3.3 Array of Integrated Bandpass Filters

In Section 3.2, we detailed the implementation and characterization of a low-loss micromachined lumped element bandpass filters at 1.2 GHz that is terminated to the standard 50 Ω impedance. In this section, we document the design procedure of an array of such filters in the UHF range with an optimized termination impedance. The termination impedance of the filter array is optimized for a higher filter performance in a smaller area. The filter array is composed of seven non-overlapping fixed bandpass filters for the applications that require filtering closely-located signals. In this section, we show the effect of the physical layout on the performance of lumped filters and discuss a number of design strategies to improve the frequency response of the silver lumped filters in the frequency range of interest.

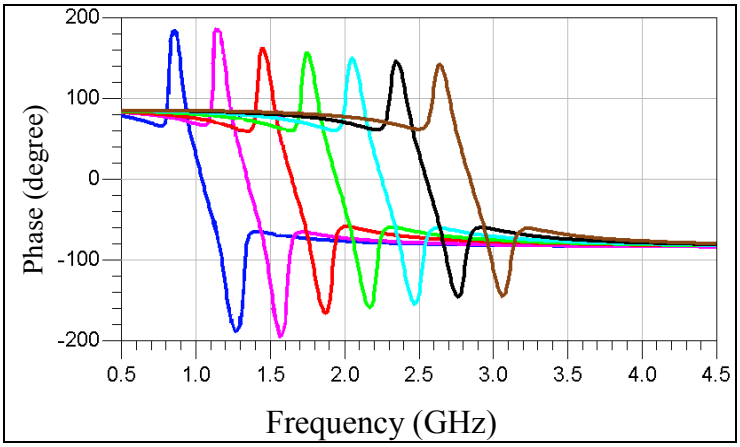
3.3.1 Electrical Circuit Design

The initial design and simulation of the filter array is performed in the Agilent *hp*ADS using lumped element models for the inductors and capacitors. The filters are designed to have a bandwidth of 300 MHz with center frequencies in the range of 1.05 GHz to 2.85 GHz and out-of-band rejection of 25 dB when terminated to 150 Ω. In Section 3.1, we verified that a parallel resonator with a larger termination impedance requires a smaller capacitor and a larger inductor than a resonator with a similar *Q* but with a lower termination impedance. Consequently, the termination impedance of the filters in the array is increased to 150 Ω so that the capacitance decreases to offer a higher *Q* and the inductance increases to reach the practical value. Besides the fact that 150 Ω offers suitable component values, it is sufficiently low to be easily matched to the antenna [84].

The simulated frequency response of all seven filters, when terminated to 150 Ω, is shown in Figure 55. In simulations, the Q of the inductors and capacitors at the center frequency of each filter is taken as 80 and 100, respectively. The insertion loss is less than 2.5 dB for the highest-Q filter (at 2.85 GHz) and is 1.3 dB for the lowest-Q filter (at 1.05 GHz).



(a)



(b)

Figure 55: ADS simulated response of an array of seven non-overlapping bandpass Elliptic filters.

Obtaining a low insertion loss for a filter at higher frequencies is more challenging as the filter Q increases and the requirements on the individual component Q become more critical. For this reason, the result of the highest-frequency filter is shown in more detail in this chapter. The simulated S-parameter of the highest-frequency filter

is shown in Figure 56. The simulated group delay of this filter at the mid-band is about 1.7 ns, and the maximum variation of the group delay in the pass-band is within 1.5 ns, as shown in Figure 57.

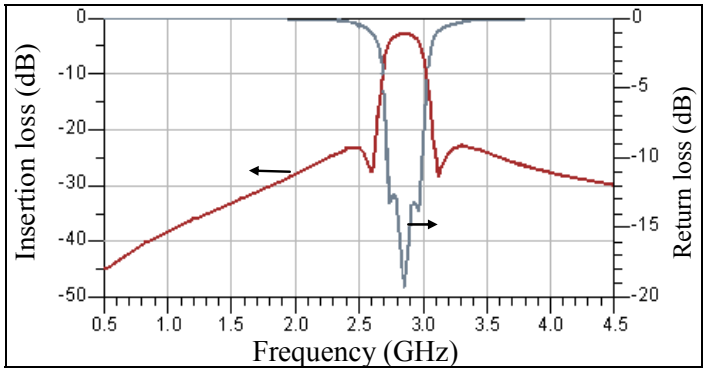


Figure 56: Simulated S-parameter of the highest-frequency filter.

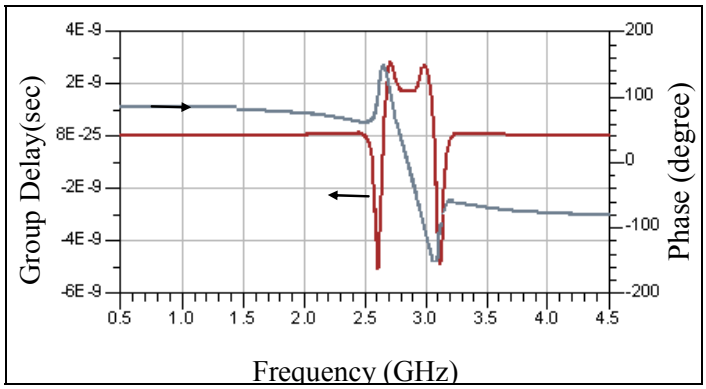


Figure 57: Simulated group delay and phase of the highest-frequency filter.

3.3.2 Electromagnetic Design

The optimization on the physical layout of the filters is performed in the Sonnet. Sonnet simulations are performed using the Sonnet thick-metal model with two sheets. Modeling the thickness of the silver layer with two sheets overestimates the loss of the filters [85]. Using more than two sheets gives a more accurate estimate of the insertion loss but is computationally intensive. Therefore, the thickness of the silver layer is simulated using two sheets in the Sonnet.

The physical layout of the bandpass filters is finalized by optimizing the layout of the incorporated passives to get the desired frequency response for each individual LC tank. The length of the lines interconnecting the tanks is maintained as short as possible to minimize the effect of the line parasitics. In addition to parasitics of the interconnects, there is another important layout constraint that has to be considered, which is the cross-talk between the spiral inductors. We show the effect of the mutual inductances in Section 3.3.8. The Sonnet simulated frequency response of the filter array is shown in Figure 58. To account for the surface roughness and impurities in the electroplated film, silver conductivity is taken as 6×10^7 S/m, which is lower than the text value for the bulk conductivity (Table 4). The optimized EM simulated insertion loss of the lowest-frequency filter and the highest-frequency filter is 1.3 dB and 2.3 dB, respectively.

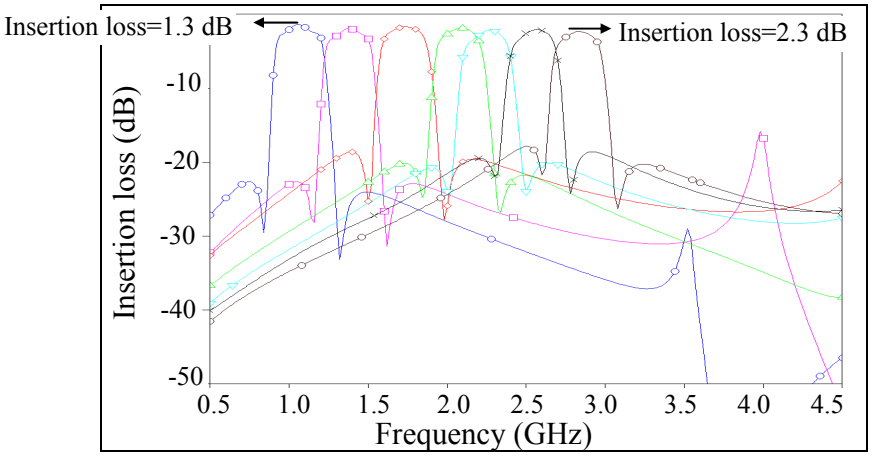


Figure 58: EM simulation response of the array of bandpass Elliptic filters using the Sonnet.

3.3.3 Fabrication Overview

Filters are fabricated on a 3 μm thick silicon dioxide membrane. Instead of Avatrel, silicon dioxide is chosen as the membrane material in this batch since it is widely available in the CMOS processes. The routing layer in this batch is 4 μm thick silver. With a capacitive gap of 1 μm, each filter in the array occupies less than 3 mm × 3

mm of die area. Figure 59 shows a picture of a fabricated four inch wafer, showing the filters and the close-up view of the filters in the array, showing the envisioned position of the antenna.

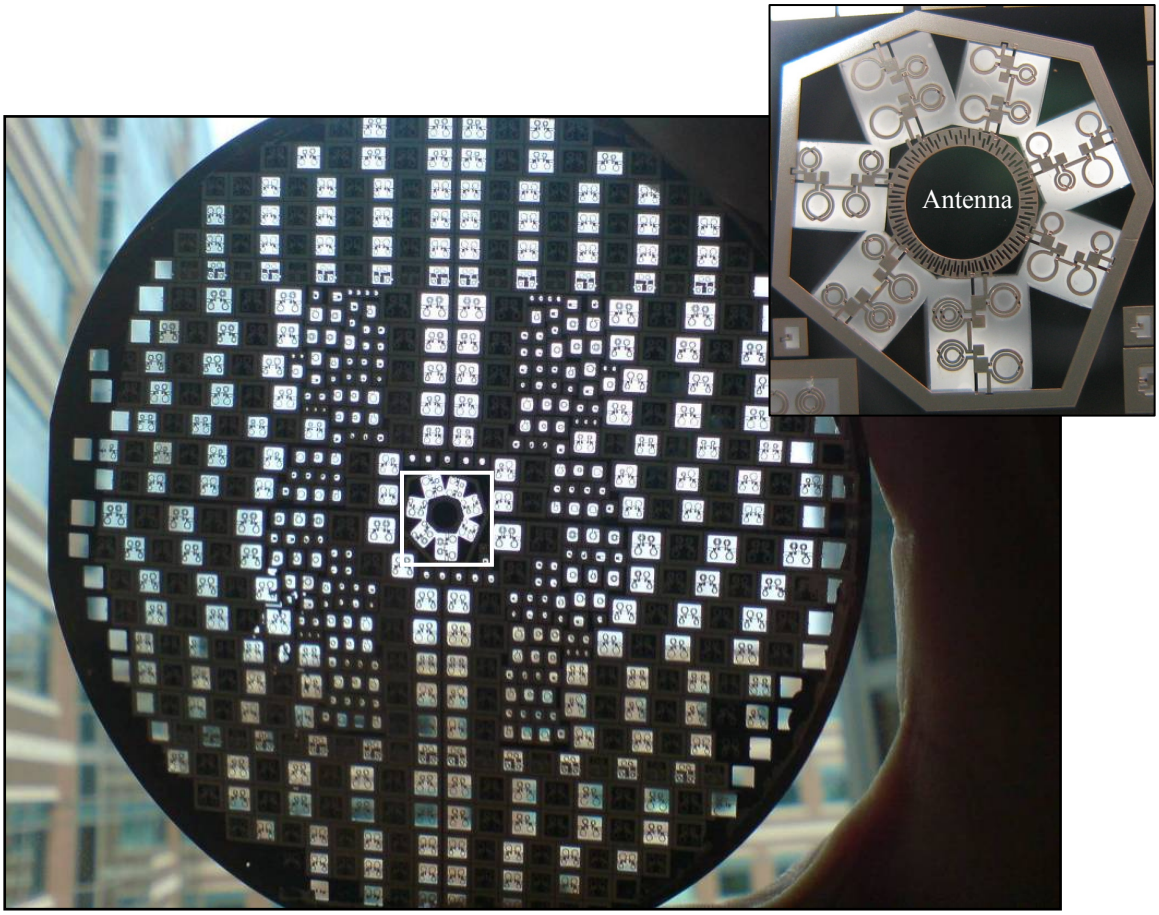


Figure 59: A picture of the four inch wafer showing the filters on a 3 µm thick silicon dioxide membrane and a close-up view of the filter array.

Figure 60 shows a SEM view of the lowest-frequency filter together with a close-up view of the filter cross-section taken from a device that is intentionally broken, showing the silicon dioxide membrane, the routing, and the electroplated silver layer. Symmetrical inductors are employed in these filters as they exhibit higher *Q*s than the conventional spiral inductors shown in Figure 46 [86]. Figure 61 shows a SEM view of the highest-frequency filter fabricated on a silicon dioxide membrane. This filter with a 500 µm wide ground plane occupies 2.1 mm × 2.4 mm of die area.

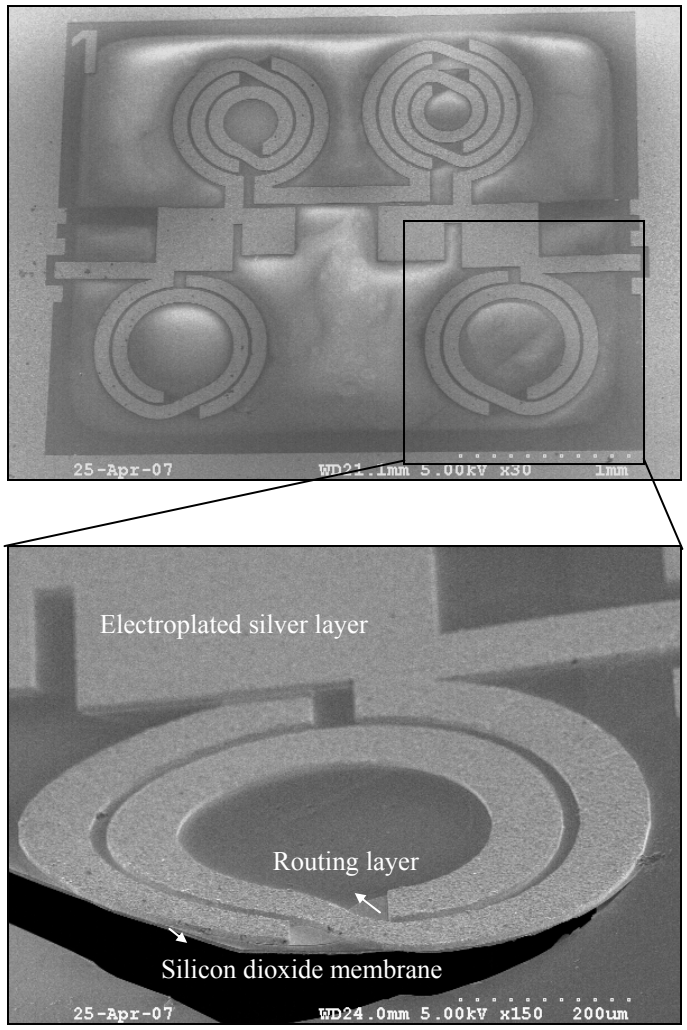


Figure 60: A SEM of the lowest-frequency filter fabricated on a 3 µm thick silicon dioxide membrane and a close-up view of the filter cross-section taken from a broken device.

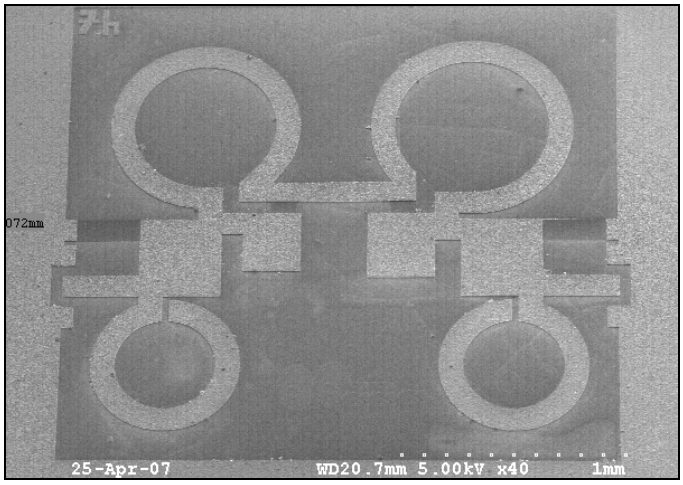
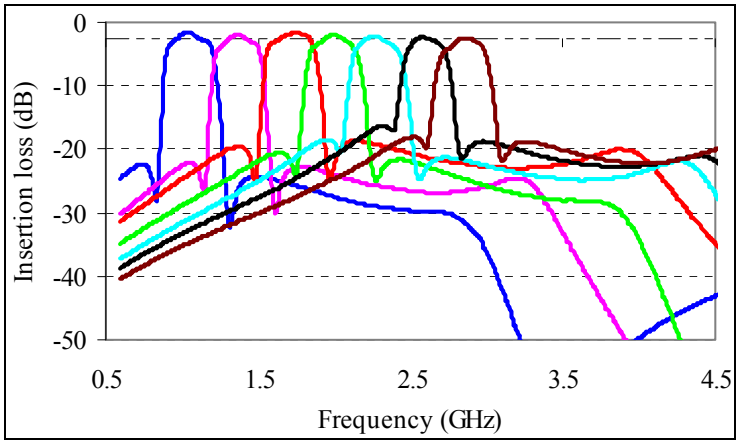


Figure 61: A SEM of the highest-frequency filter fabricated on a 3 µm thick silicon dioxide membrane, showing the filter occupies 2.1 mm × 2.4 mm of die area.

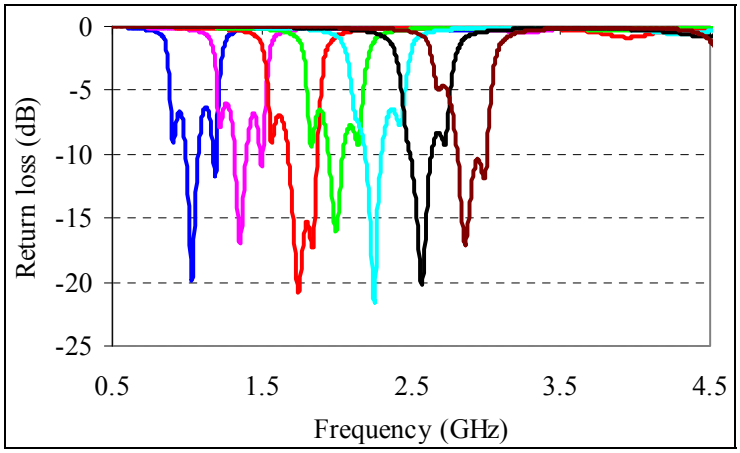
3.3.4 Measured Results of the Array

To measure the frequency response of the filter with 150 Ω terminations, first, the calibration is performed using the SOLT calibration procedure on the Cascade 50 Ω impedance standard substrate (101-190). The filter response when terminated to 150 Ω is then measured by converting the termination impedance of the VNA to 150 Ω.

Figure 62(a) and (b) show the measured frequency response of the integrated array of seven non-overlapping silver bandpass filters when terminated to 150 Ω. The measured insertion loss at the center frequency of each filter is less than 2.52 dB, which makes these integrated filters suitable candidates for wireless applications.



(a)



(b)

Figure 62: Measured response of an integrated array of seven non-overlapping silver bandpass filters fabricated on a silicon dioxide membrane when terminated to 150 Ω.

In Figure 62(a), note that the designed center frequency and bandwidth of the lowest-frequency filter is identical to the filter with 50 Ω terminations shown in Figure 49. The improved performance of the lowest-frequency filter of Figure 62(a) compared to the filter shown in Figure 49 is due to an enhanced electrical design, an extensive optimization performed on the filter layout in the Sonnet, and a larger termination impedance used in this design. As shown in Figure 60, the ground plane is not extended between the input and output inductors of the filter in the array. Therefore, the 2 GHz notch of the filter with 50 Ω design is eliminated in the new design.

The measured group delay and phase response of the highest-frequency filter is illustrated in Figure 63, showing that the variation of the group delay in the pass-band is less than 1.5 nsec. A comparison of Figure 63 and Figure 57 demonstrates that the measured phase response of the filter is in good agreement with the ADS simulation response.

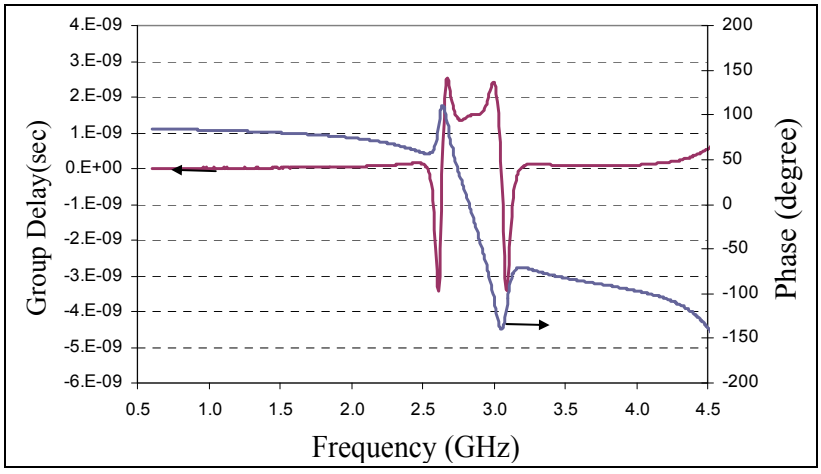


Figure 63: Measured group delay and phase of the highest-frequency filter.

3.3.5 Effect of Silicon Substrate

Since the passivation layer is only a 3 μm thick silicon dioxide layer, the *Q* of individual filter components is greatly improved by the selective removal of the silicon

substrate. Figure 64 compares the measured frequency response of the highest-frequency filter fabricated on a silicon dioxide membrane with an identical filter on a passivated silicon substrate. At this frequency range, the substrate loss is the dominant *Q*-limiting mechanism, and thus the filter response is significantly affected by the loss of the silicon substrate. As shown earlier, the substrate loss does not affect the performance of the filter at 1.2 GHz to the same extend. Therefore, removal of the silicon substrate becomes more indispensable when a narrow-band filter with a low insertion loss at higher frequencies is required.

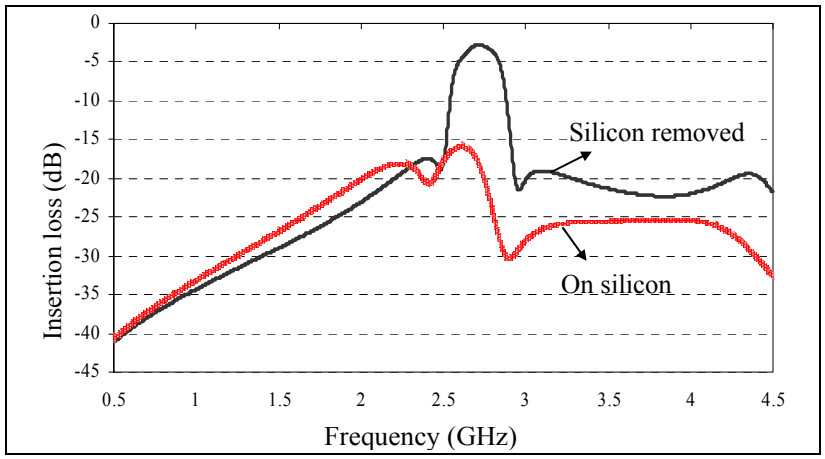


Figure 64: Measured S_{21} of the highest-frequency filter before and after removing the silicon substrate, showing an insertion loss of 2.52 dB on a silicon dioxide membrane and a distorted response on a passivated silicon substrate.

3.3.6 Measured versus Simulated

The measured frequency of all filters agrees well with the Sonnet simulation response. Figure 65 shows the measured frequency response of the highest-frequency filter together with the simulated response using the thick-metal model in the Sonnet. The measured response of the filter shows an unwanted resonance at ~ 4.67 GHz, which is due to parasitics introduced by the interconnects and the self resonance of the lumped components. In the simulated response, the frequency of this resonance is 5.34 GHz.

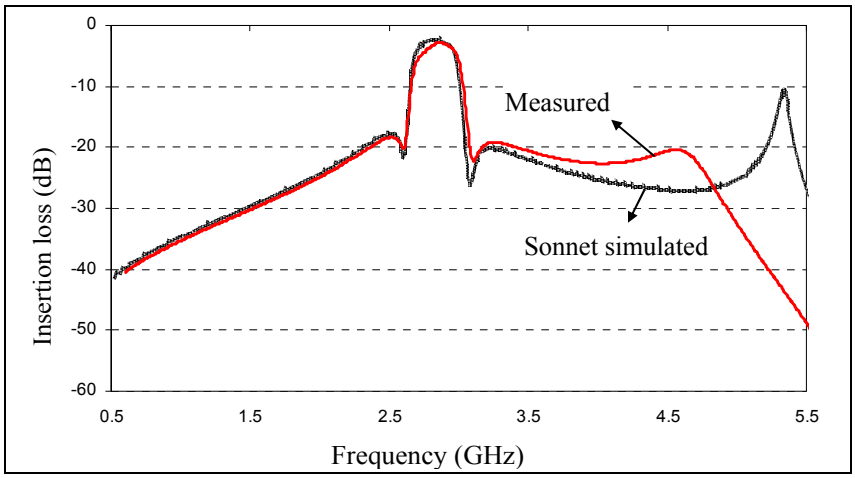


Figure 65: Measured and simulated frequency response of the highest-frequency filter using the thick-metal model in the Sonnet.

3.3.7 Measured versus Modeled

To better understand the behavior of the fabricated filters and the source of the unwanted resonance, the highest-frequency filter is modeled in the *hp*ADS. Figure 66 shows the electrical model of a bandpass Elliptic filter on a silicon dioxide membrane. The long interconnect lines shown in Figure 61 are modeled as an inductor and a small series resistor. From the modeled response, it is noticeable that the parasitic of these lines is the dominant source of the unwanted peak at 4.67 GHz. There is a small coupling inductance between the input and output inductors as well as the inductors of the tanks connected in series between the input and output, which degrades the out-of-band rejection of the filter (κ_1 and κ_2 in Figure 66). Figure 67 compares the measured response of the highest-frequency filter with the modeled response. As shown, the measured and modeled responses are in very good agreement.

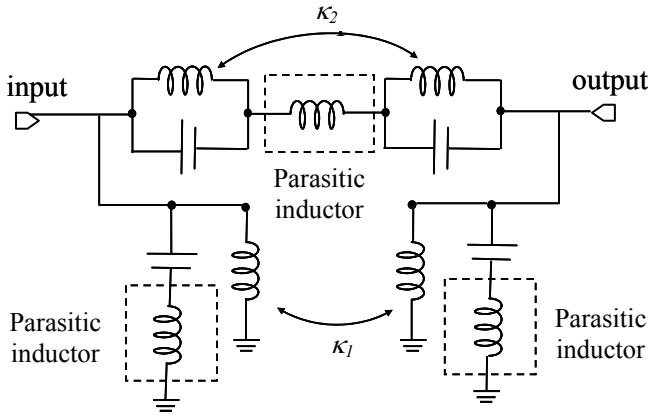


Figure 66: Electrical model of Elliptic silver filters on a silicon dioxide membrane. The parasitic of the interconnects is modeled as a low-*Q* inductor.

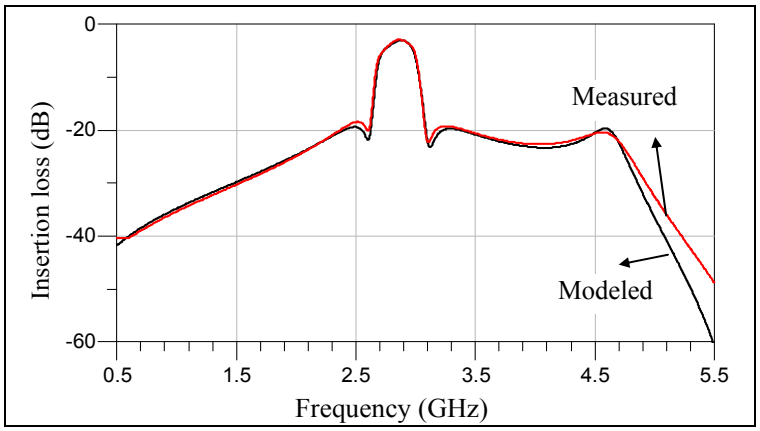


Figure 67: Measured and modeled frequency response of the highest-frequency filter using the electrical model shown in Figure 66.

3.3.8 Effect of the Parasitic Inductances

Prior to the successful fabrication of the filters and achieving the results we showed in Figure 62-Figure 67, we once fabricated the filters with a different layout and obtained a poor performance for the filters (Figure 68). As shown in Figure 68, the center frequency of the filters, particularly the higher frequency filters, is shifted down, and the out-of-band rejection of all filters is severely deteriorated.

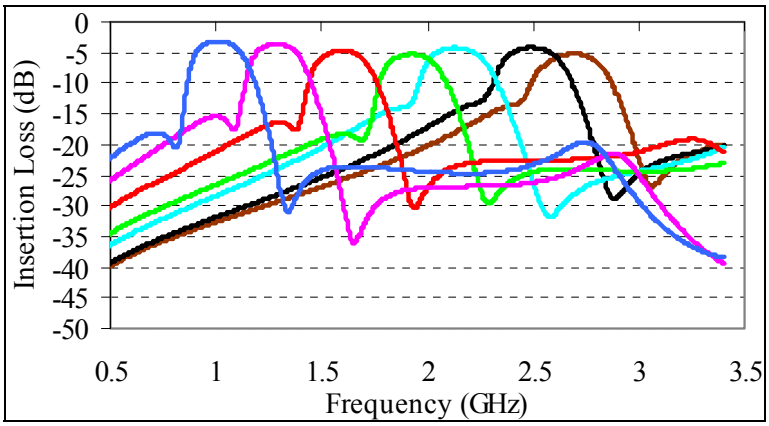
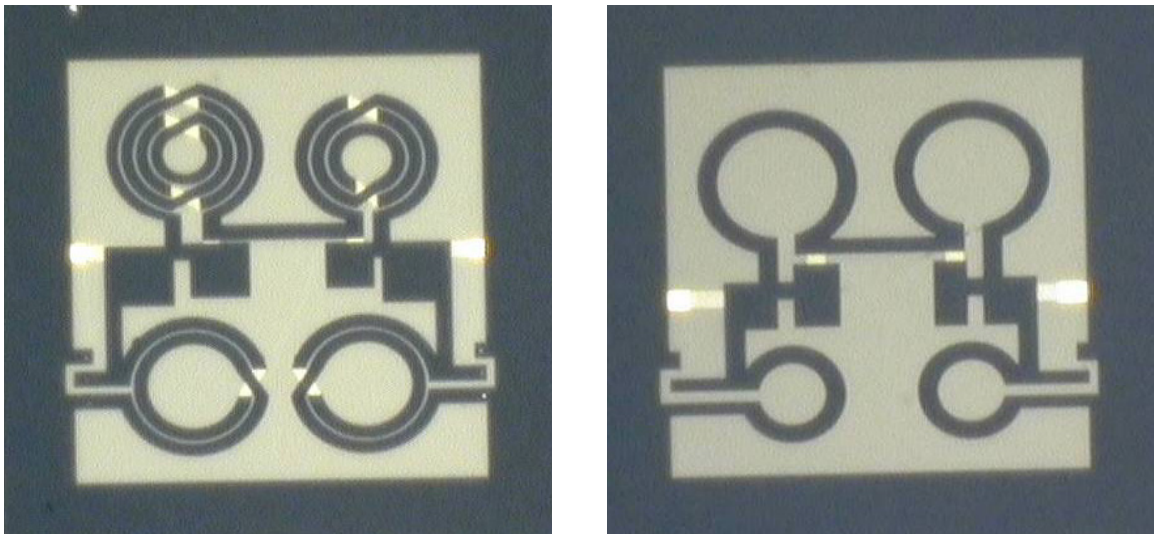


Figure 68: Measured frequency response of the array with a different layout.

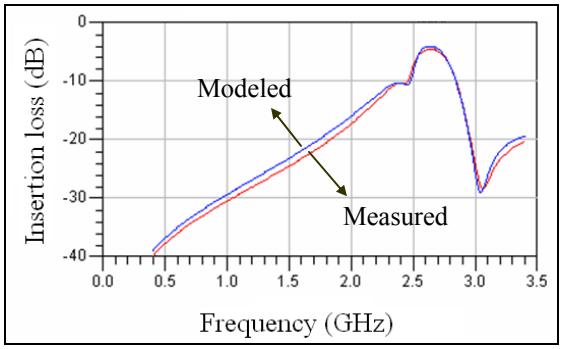
The micrograph of the lowest- and the highest-frequency filters with the poor layout are shown in Figure 69. Filters with the poor layout are modeled in the ADS using the electrical model shown in Figure 66. Figure 70 shows the modeled together with the measured response of the highest-frequency filter. From the modeled values for the individual circuit components (shown in Figure 70(c)), we identified that the strong inductance coupling between the closely-located input and output inductors is the main reason for the inferior performance of these filters. Because of the nature of the layout, the input and output inductors have a positive mutual inductance (i.e., κ_I is positive). This mutual inductance results in an increase in the effective inductance seen at the input and output terminals, which in turn lowers the center frequency and deteriorates the frequency response. At higher frequencies, the inductance coupling is stronger; therefore, its effect on the filter performance is more noticeable (Figure 68). In addition, the length of the interconnects in the poor layout is not the minimum possible. A longer interconnect has a higher parasitic inductance and is more detrimental to the performance of the filter.

In summary, at radio frequencies, obtaining a high-performance integrated lumped filter not only necessitates high-Q components, but also requires extensive optimizations of the layout using high-accuracy electromagnetic simulator. We discuss the importance of the EM simulations further in Chapter 4.

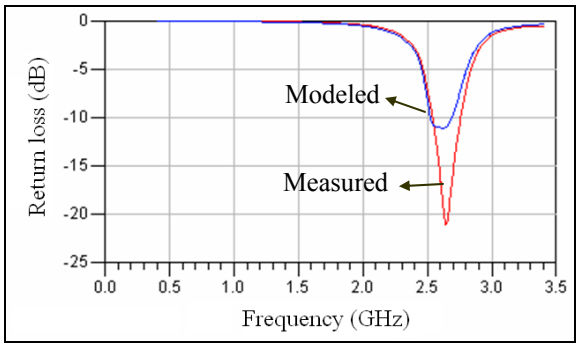


(a) (b)

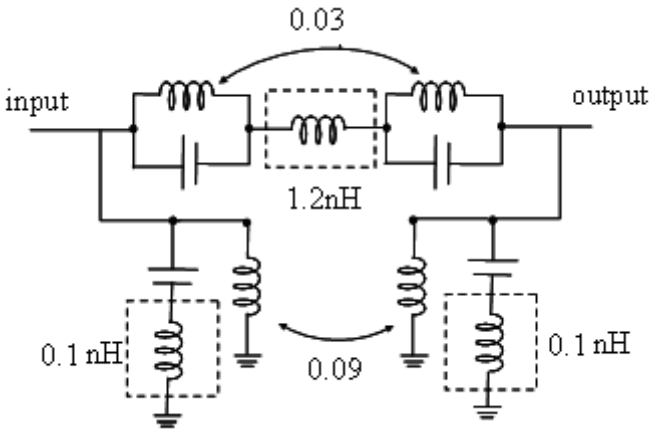
Figure 69: Micrographs of (a) the lowest-frequency and (b) the highest-frequency filter of the array with a poor layout, showing the position of the inductors.



(a)



(b)

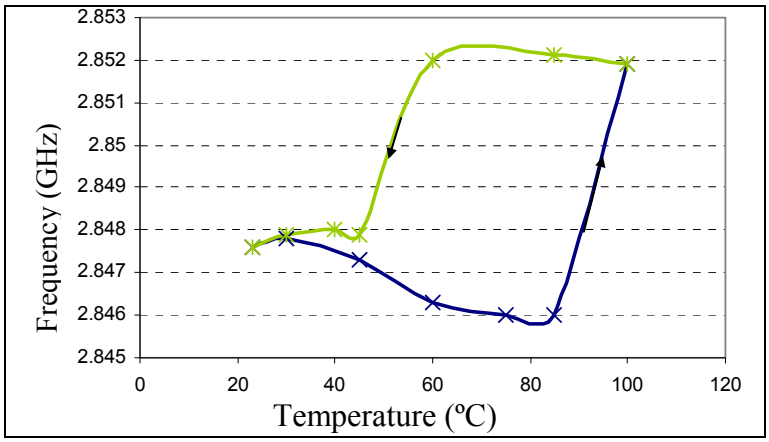


(c)

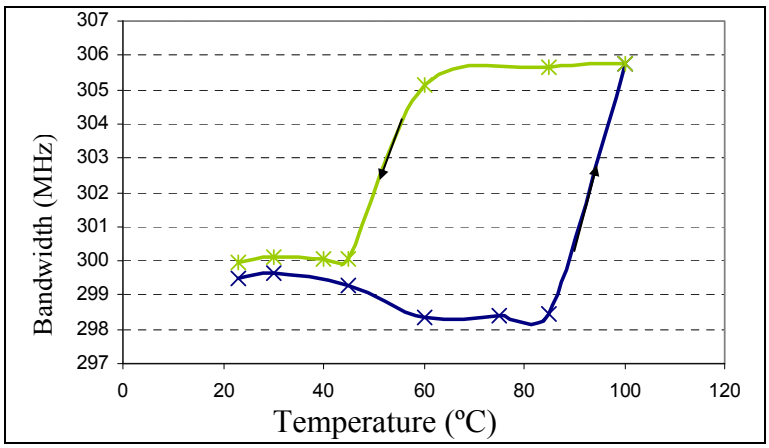
Figure 70: Measured and modeled response together with the electrical model of the highest-frequency filter with the layout shown in Figure 69.

3.3.9 Temperature Characteristic

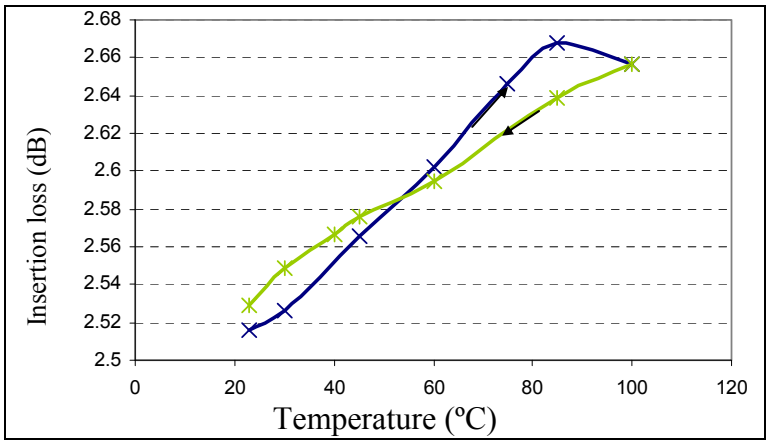
The temperature stability of the filters is tested in a temperature-controlled RF probe station from Desert Cryogenics. Over the range of 23° C to 100° C, the highest-frequency filter exhibits a temperature drift of less than 0.23% in the center frequency and less than 2.6% in the 3-dB bandwidth, as shown in Figure 71. The insertion loss of the filter is reasonably stable with temperature (Figure 71(c)). The temperature test took several hours resulting in a slight degradation in the calibration that is a contributing factor for the higher insertion loss at high temperatures. The response of the filter shows small hysteresis versus temperature.



(a)



(b)



(c)

Figure 71: (a) Frequency, (b) bandwidth, and (c) insertion loss behavior of the highest-frequency filter in the 23° C to 100° C temperature range.

CHAPTER 4

NARROW-BAND TUNABLE LUMPED FILTERS

Thus far, we have demonstrated high-Q inductors, one-port tunable capacitors, and low-loss fixed-frequency bandpass filters on CMOS-grade silicon using a low-temperature silver micromachining process. In this process, silicon dioxide is used as the sacrificial layer and is removed in a wet solution to release the movable components. In Chapter 3, we showed that for the realization of high-order Elliptic filters both one-port and two-port capacitors are needed. However, the fabrication process that we devised does not enable two-port tunable capacitors. To obtain a two-port tunable capacitor, the movable actuator port has to be electrically isolated from the movable capacitor port. For that, a second dielectric layer is needed to maintain a mechanical connection between the actuator and capacitor while ensuring an electrical isolation between them. Therefore, we have modified the silver micromachining process introduced in Chapter 2 and have developed a new process to add the possibility of realizing two-port tunable capacitors that are required in most high-order bandpass filters. In addition, in the modified process, we have employed a dry-release scheme to eliminate the stiction problem.

In this chapter, we first introduce the dry-released silver micromachining fabrication process used for the implementation of two-port tunable capacitors and tunable lumped filers. Next, we explain the design of the two-port tunable capacitors and show the measured results that we have obtained for these components. Finally, we demonstrate tunable lumped UHF filters using the dry-released silver micromachining technique. The filters presented in this chapter, to our best knowledge, are the first implementation of fully integrated tunable lumped UHF filters on CMOS-grade silicon substrates. In this chapter, we demonstrate different filter designs to achieve the lowest insertion loss and the highest quality factor for the filters. We also discuss different

aspects of each design and provide solutions for further improvement of the tunable lumped LC filters.

4.1 Dry-Released Silver Micromachining Technique

The schematic diagram of the fabrication process flow is shown in Figure 72. This process requires four lithography steps and enables the co-fabrication of high-Q inductors as well as one-port and two-port tunable capacitors.

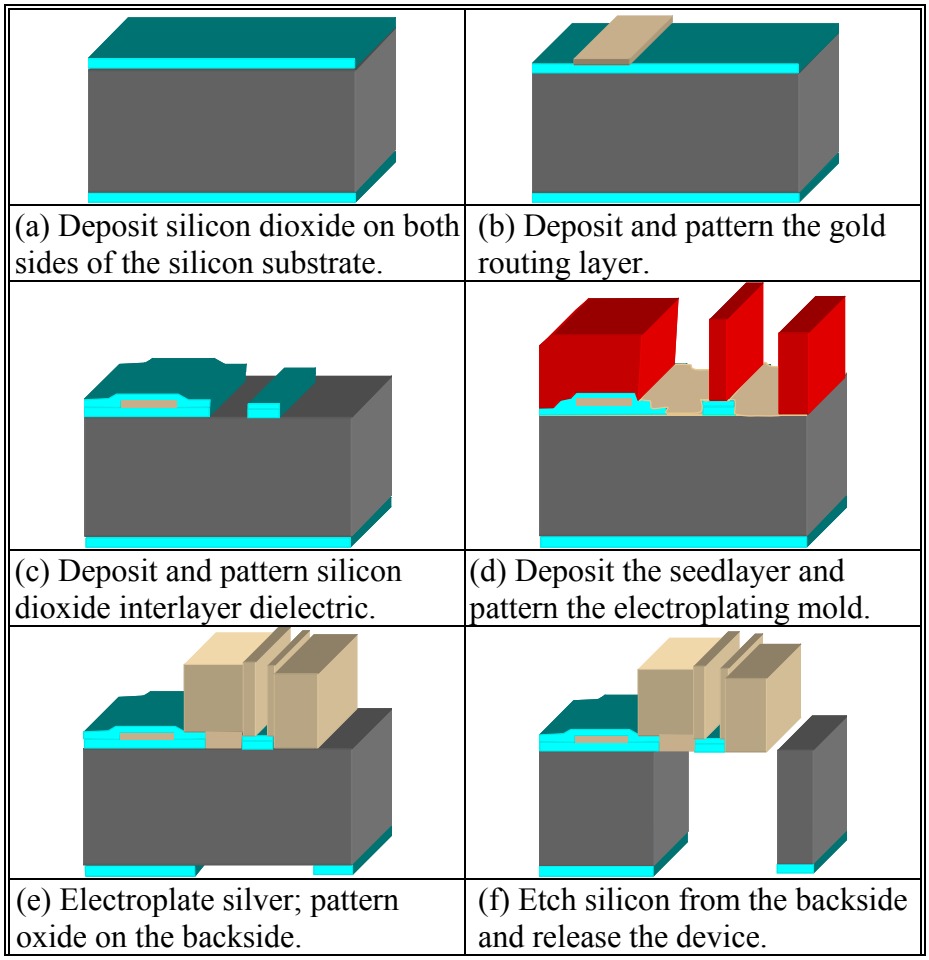


Figure 72: Fabrication process of tunable bandpass filters and high-Q passives.

First, a 3-5 μm thick PECVD silicon dioxide layer is deposited on the top and backside of the silicon substrate (Figure 72(a)). The first metal layer, which consists of a 2-4 μm gold layer, is evaporated and patterned (Figure 72(b)). A thin (300 Aº) layer of

chromium (Cr) is used to promote the adhesion of gold to the silicon dioxide layer. Next, another layer of PECVD silicon dioxide is deposited. The silicon dioxide layers are then selectively removed from the topside using an inductively-coupled plasma system (ICP) (Figure 72(c)). A seedlayer of Ti/Ag/Ti is deposited and a 20 μm thick silver layer is electroplated into a photoresist mold to define the inductors and the tunable capacitors (Figure 72(d)). The mold and seedlayer are subsequently removed using the same recipe discussed in Chapter 2. The silicon dioxide layer deposited on the back is patterned using an ICP system (Figure 72(e)). Finally, the tunable capacitors are dry-released by selective etching of the silicon substrate from the backside using a DRIE system (Figure 72(f)). The electroplated silver layer is protected from the silicon etching plasma, which contains the sulfur hexafluoride (SF_6) gas, using a thin layer of PECVD silicon dioxide. A SEM picture of a failed sample that was not protected during the backside etching step is shown in Figure 73. As shown, the silver structure is oxidized by the SF_6 gas. Therefore, protecting the plated silver layers is crucial to the successful fabrication of the silver microstructures.

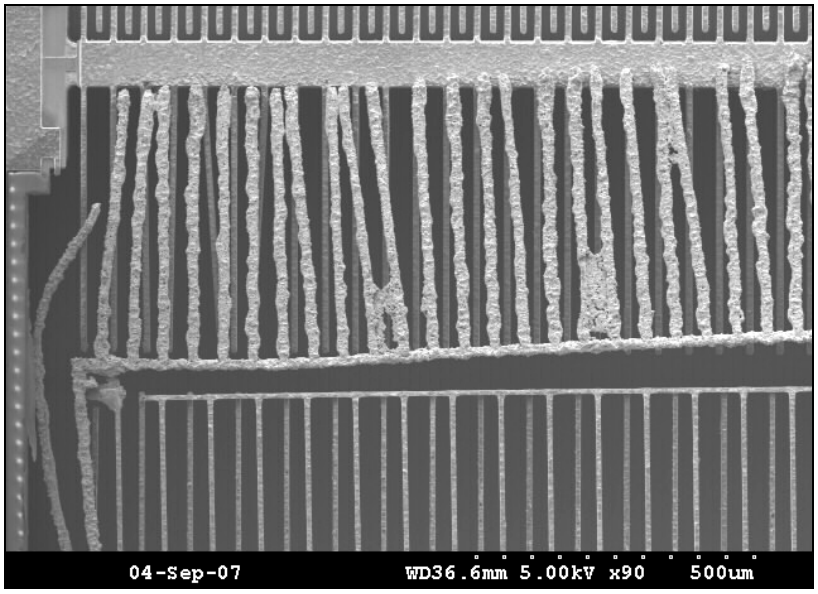


Figure 73: SEM view of a failed sample showing the unprotected silver structure is oxidized in a plasma etching process using the SF_6 gas.

4.2 Two-port Tunable Capacitors

In Section 2.4, we demonstrated several one-port tunable capacitors using dual-gap actuation scheme in which the parallel-plate actuation gap is larger than the parallel-plate sense gap to enhance the tuning range. To realize a two-port capacitor, we have modified the capacitor design to electrically isolate the actuator from the parallel-plate capacitor while coupling them mechanically using a segment of a PECVD silicon dioxide, as shown in Figure 74.

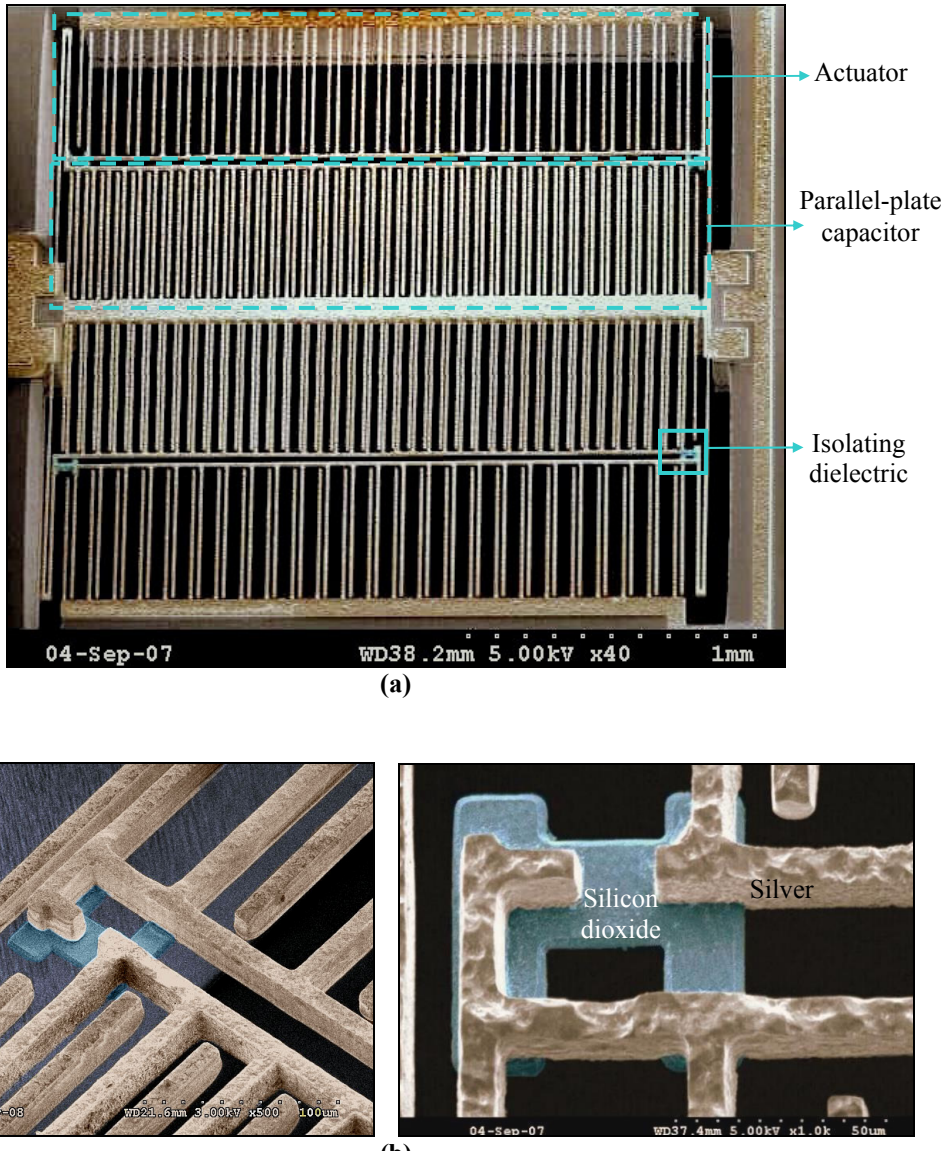


Figure 74: Colored SEM views of (a) a two-port tunable capacitor and (b) the isolating segment.

Isolating the actuator from the capacitor using a dielectric segment has been reported in the literature [87]. The advantage of this design compared to the previously reported two-port tunable capacitors is its small form-factor. As shown in Figure 74, the isolated actuator and capacitor are folded into each other to reduce the die area as well as the length of the movable shuttle. In addition, the tunable capacitor presented in this thesis is suspended in air to reduce the substrate loss and to increase the *Q*. Therefore, this design offers a higher *Q* and self-resonance frequency in a smaller size.

For tunable filters in the UHF range, two-port tunable capacitors of a few picofarads are needed. Accordingly, we have increased the length and number of the parallel-plate fingers from what presented previously and have designed a 1.3 pF tunable capacitor (Figure 74). This capacitor is designed with a thickness of 20 μm, a capacitive gap of 10 μm, and an actuation gap of 20 μm. The physical layout of the capacitor is simulated in the Sonnet using four sheets for the electroplated silver layer to get an estimation of the *Q* and capacitance value. The result is shown in Figure 75.

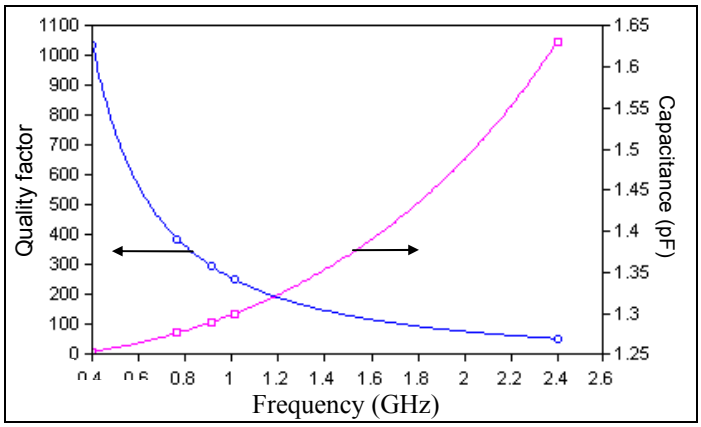


Figure 75: Sonnet simulated response of the two-port tunable capacitor.

In addition, the two-port capacitor is modeled using the Coventor, which is a 3D MEMS software [88], to study the functionality of the movable device and the mechanical deformation of the shuttle and springs. As shown in Figure 76, a maximum displacement of 7.5 μm is expected for the two-port tunable capacitor when a load of 2

kPa is applied to the springs. For the capacitor shown in Figure 76 and the following Coventor simulations, the capacitor gap is assumed to be 8 μm.

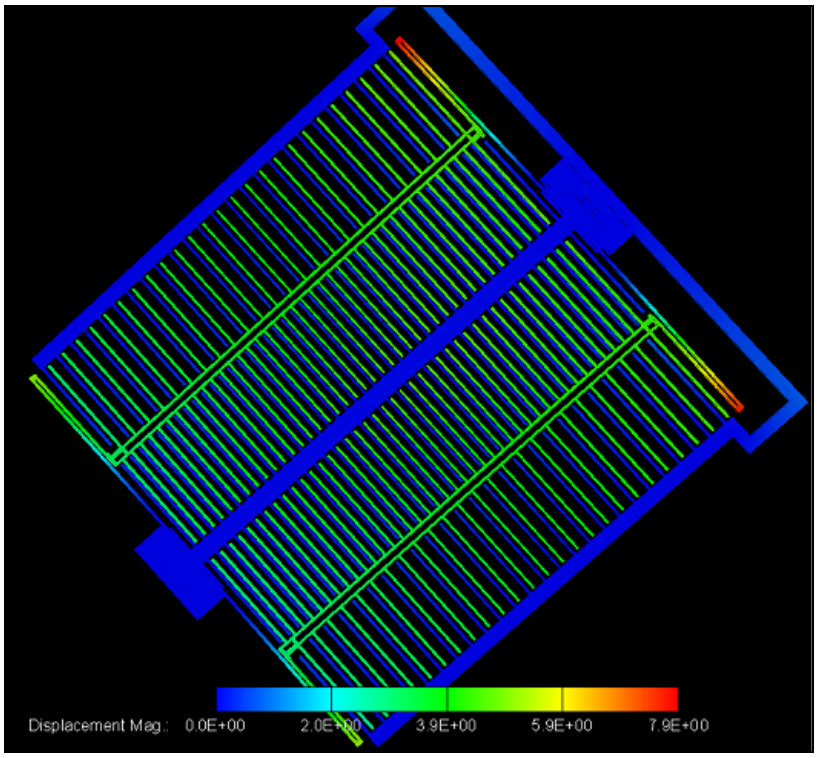


Figure 76: Coventor simulated displacement of the two-port tunable capacitor when a load of 2 kPa is applied to the springs, showing a maximum deflection of 7.9 μm.

The charge density on the capacitor, obtained using the MEMElectro module of the Coventor software, is shown in Figure 77. The capacitance value between the capacitor and ground plates, which are separated by 8 μm, is simulated to be 1.6 pF. The parasitic capacitance between the capacitor and actuator plates is only 0.03 pF, and the capacitance of the actuator to ground is 0.8 pF. Since the ground plane carries the charge produced by both the actuator and the capacitor, the density of charge is the maximum on the ground plates (fingers), as shown in Figure 77. Also noticeable from Figure 77 are a high charge density on the sharp corners and a low charge density on the wide capacitor and actuator routing silver lines.

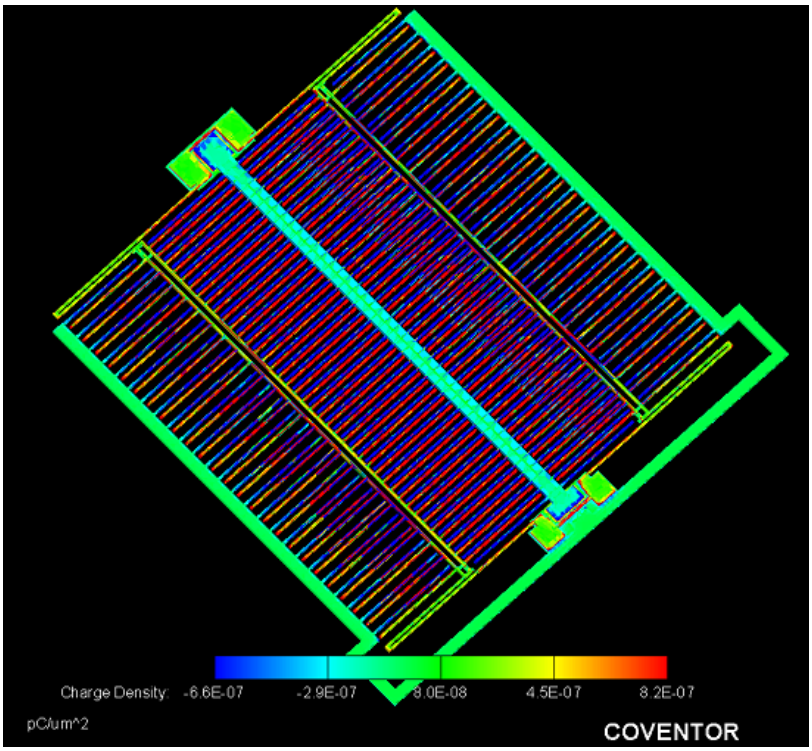


Figure 77: Simulated charge density of the two-port capacitor when the capacitor, ground, and actuator voltages are set at -1 V, 1 V, and 0 V, respectively. The density of charge is the highest on the ground plates.

For comparison, the mechanical and electrical behavior of a one-port capacitor with identical parallel-plate finger dimensions to the one showed in Figure 76 and Figure 77 is simulated using the Coventor. Figure 78 shows an exaggerated mechanical displacement of the one-port tunable capacitor. The maximum displacement of the one-port capacitor is 6.5 μm when a load of 2 kPa is applied to the springs. The lower displacement of the one-port capacitor with the same load is due to the shorter spring length. The length of the spring in the two-port configuration was extended to accommodate the silicon dioxide isolating segment.

The charge density of the one-port capacitor is shown in Figure 79. The capacitor to ground capacitance is 1.6 pF for the one-port configuration, which is similar to the one for the two-port configuration. For the one-port capacitor shown in Figure 79, the charge density is the highest on the ground fingers and is close to zero on the wide actuator routing line.

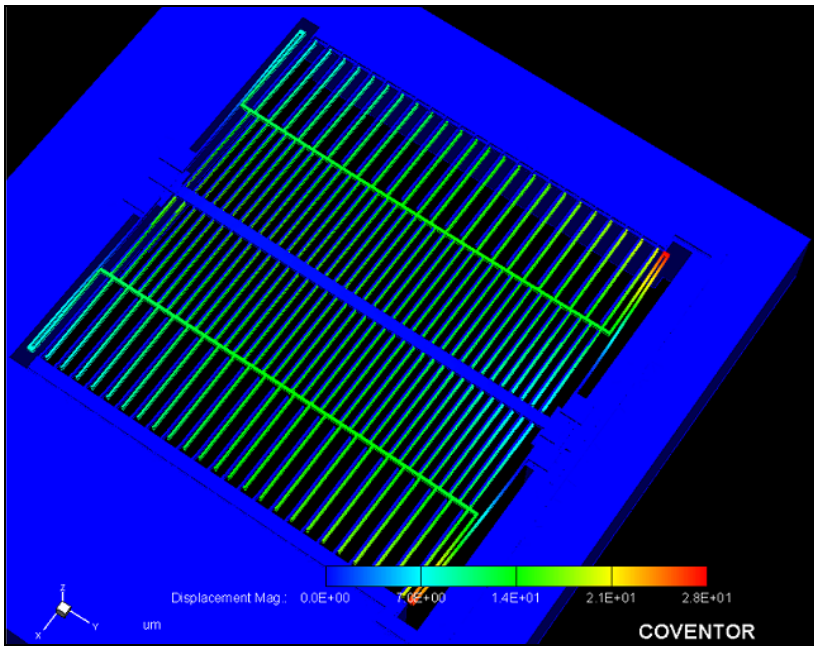


Figure 78: Exaggerated simulated displacement of the one-port tunable capacitor, showing the deformation of the spring. The maximum displacement is 6.5 µm when a load of 2 kPa is applied to the springs.

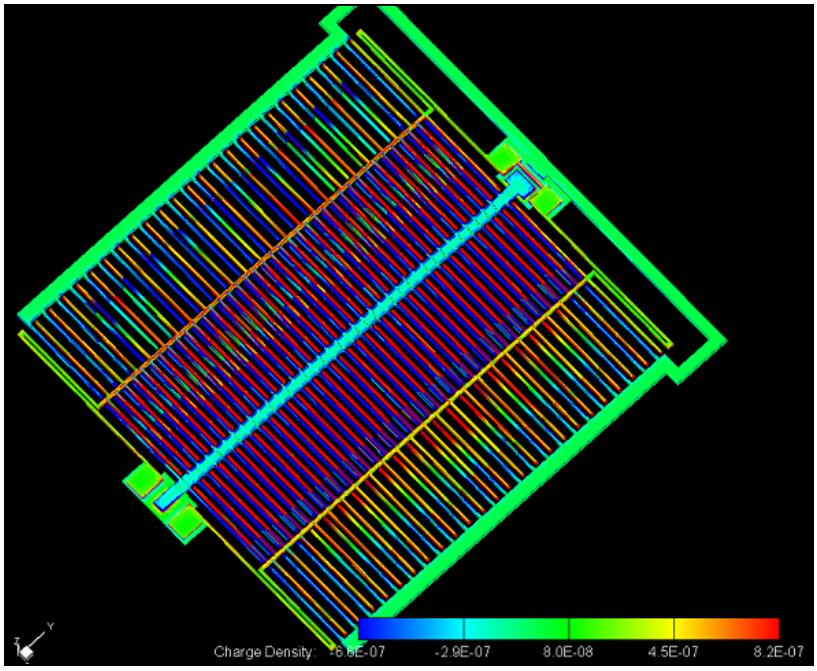


Figure 79: Simulated charge density of the one-port capacitor when the capacitor, ground, and actuator voltages are set at -1 V, 1 V, and 0 V, respectively. The density of charge is the highest on the ground plates.

Figure 80 shows the measured S_{11} of the actuator and capacitor. Because of the significant reduction of both the metal loss and the substrate loss, the two-port capacitor

shows a very high Q in excess of 500 up to 2 GHz (Marker 1 in Figure 80). However, the fixed port of the actuator is supported by the CMOS-grade silicon substrate, and thus the actuator exhibits a lower Q (Marker 2 in Figure 80).

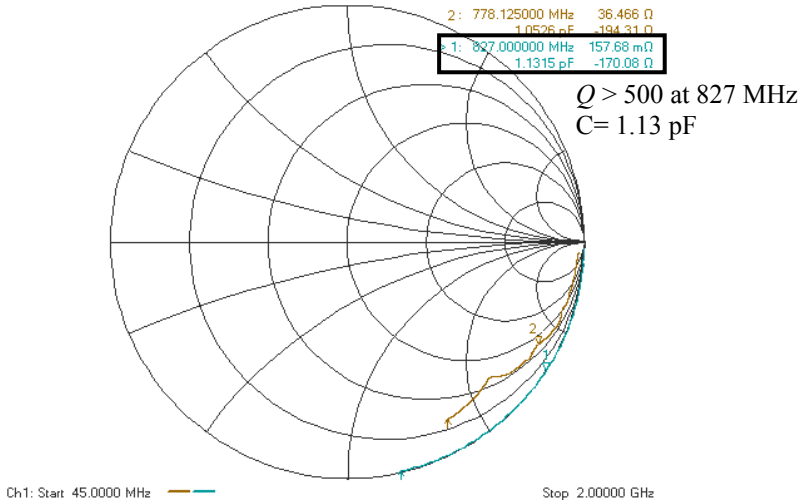


Figure 80: Measured S_{11} of the two-port capacitor (Marker 1) and the actuator (Marker 2), showing a Q in excess of 500 up to 2 GHz for the tunable capacitor.

Figure 81 shows the measured C-V tuning curve of this capacitor. The capacitor is changed by 1 pF with the application of 61 V to the isolated actuator. Lower tuning voltages can be attained by reducing the actuation gap thereby, increasing the capacitance density at the actuator side.

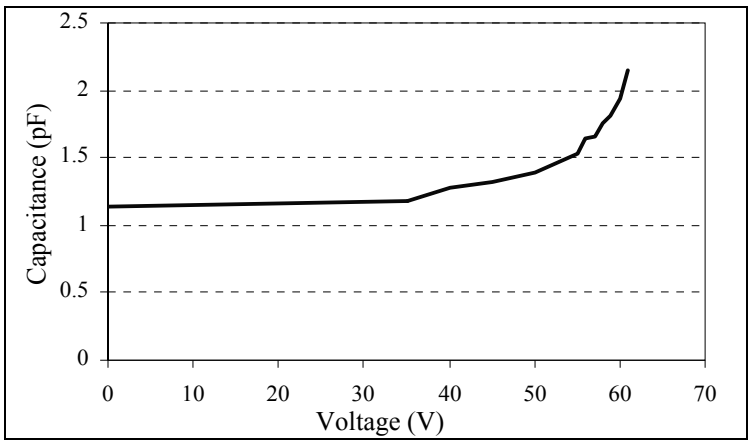


Figure 81: C-V tuning curve of the two-port tunable capacitor. The DC bias is applied to the isolated actuator.

4.3 Tunable Resonator at 1.8 GHz

Prior to designing the tunable filters, we first study the effect of changing the termination impedance and tuning the capacitance on the frequency response of tunable lumped MEMS resonators. Figure 82 shows the electrical model of a parallel lumped resonator, reflecting the limited *Q* of the components as series resistors.

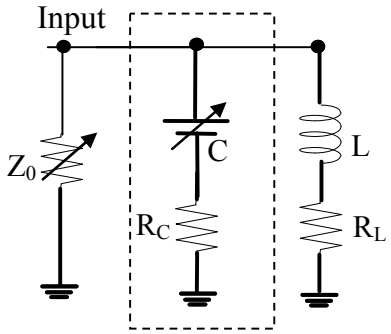


Figure 82: Electrical model of the tunable resonator, highlighting the tunable capacitor.

For the LC resonator shown in Figure 82, there exists a specific termination impedance, called the matched impedance (Z_0), which results in an infinite return loss at the input port. This impedance satisfies the matched condition and depends on the ratio of the capacitance to inductance. On the other hand, the matched condition is heavily influence by the *Q* of the lumped components. The matched impedance and the angular resonance frequency (ω_0) of the parallel LC resonator shown in Figure 82 can be calculated from the S_{11}-parameter using the following equations.

$$S_{11} = \frac{\omega[(L + R_L R_C C) - Z_0(R_C + R_L)C] + j[(LC\omega^2 R_C - R_L) + Z_0(1 - LC\omega^2)]}{\omega[(L + R_L R_C C) + Z_0(R_C + R_L)C] + j[(LC\omega^2 R_C - R_L) - Z_0(1 - LC\omega^2)]}. \quad (17)$$

Therefore,
$$S_{11} = -\infty \Rightarrow \begin{cases} \omega_0 = \dfrac{1}{\sqrt{LC}} \times \sqrt{\dfrac{L/C - R_L{}^2}{2R_L R_C + R_C{}^2 + L/C}} \\ Z_0 = \dfrac{R_C R_L + L/C}{R_C + R_L} \end{cases}. \quad (18)$$

From (18) it is clear that Z_0 decreases if the series resistances increase. In other words, lower-Q components have a lower matched impedance than the higher-Q components of the same reactance values. Therefore, if the fabricated components exhibit lower Qs than that used in the design, the resonator is no longer fully matched to the designed termination impedance, and the rejection degrades. Instead, a lower termination impedance satisfies the matched condition. The equation of matched condition also suggests that a larger termination impedance calls for a smaller capacitor and a larger inductor.

As a proof of concept, we have designed and fabricated a tunable resonator at 1800 MHz with a termination impedance of 500 Ω. We have employed the extracted parameters of the two-port tunable capacitor shown in Section 4.2 in our electrical design. Figure 83 shows a SEM view of the fabricated silver resonator. The experimental results are shown in the following two subsections.

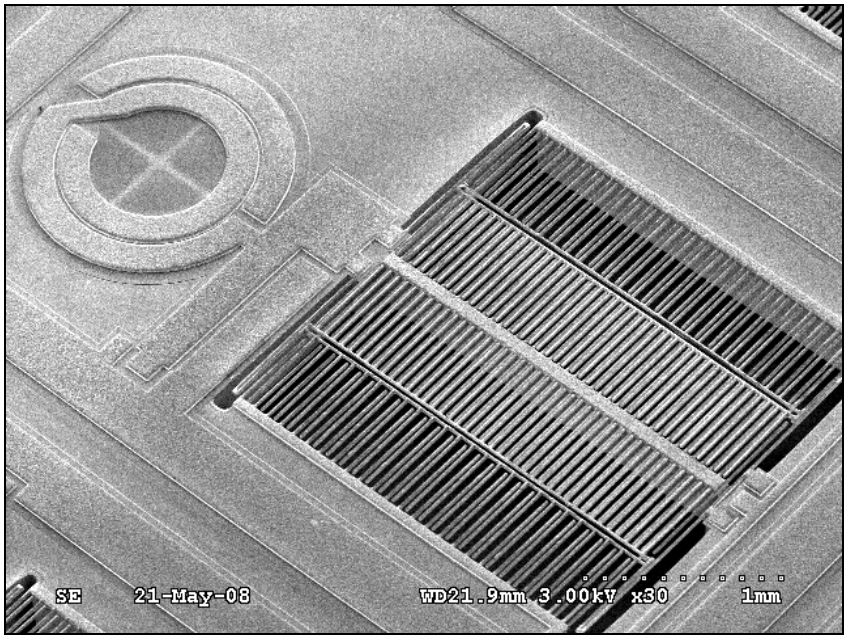


Figure 83: A SEM view of a silver tunable resonator.

4.3.1 Frequency Tuning via Capacitance Change

Figure 84 shows the measured insertion rejection of the tunable resonator with different voltages applied to the tunable capacitor. The measurements are performed with a 500 Ω termination impedance.

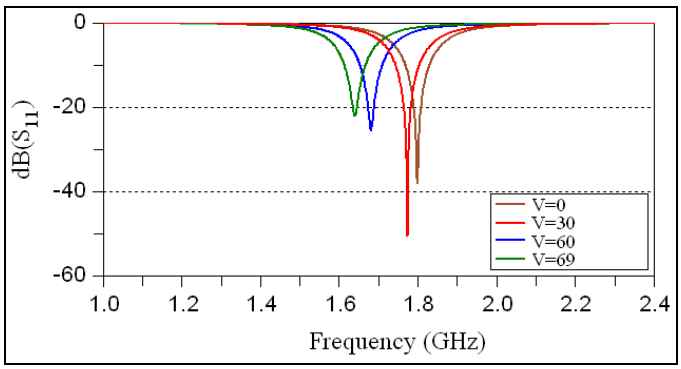


Figure 84: Measured tuning characteristic of the tunable silver resonator.

Both the *Q* and rejection of the resonator change as the resonance frequency is tuned down (Figure 84). When an actuation voltage of 30 V is applied, the change in the effective capacitance results in a matched condition, and the rejection improves to more than 50 dB (note that a more accurate measurement is needed to extract the *Q*). The increase in the rejection with a higher capacitance entails that the fabricated components exhibit a lower *Q* than that taken in the design. Further increase in the capacitance results in a deviation from the matched impedance and the rejection degrades. With the application of 69 V, the frequency is tuned to 1644 MHz while the rejection is reduced to only 20 dB.

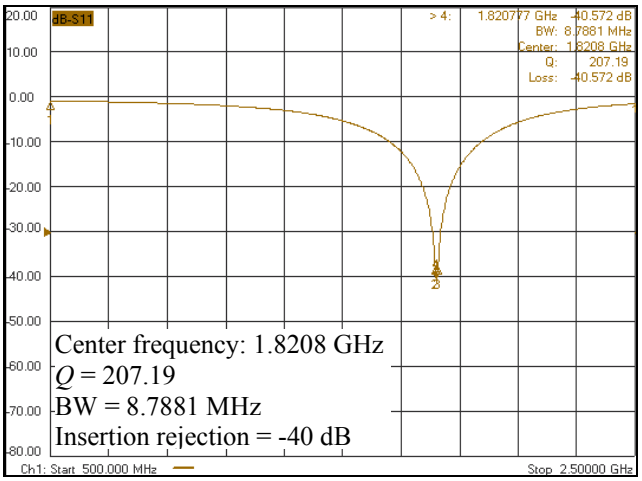
4.3.2 Bandwidth Tuning via Termination Change

From the measured results shown in Figure 84, we determined that the fabricated components exhibit lower *Q*s than that assumed in the design, decreasing the matched impedance from 500 Ω. To confirm this theory, the response of the filter with different termination impedances is measured. The results are shown in Figure 85. As shown in

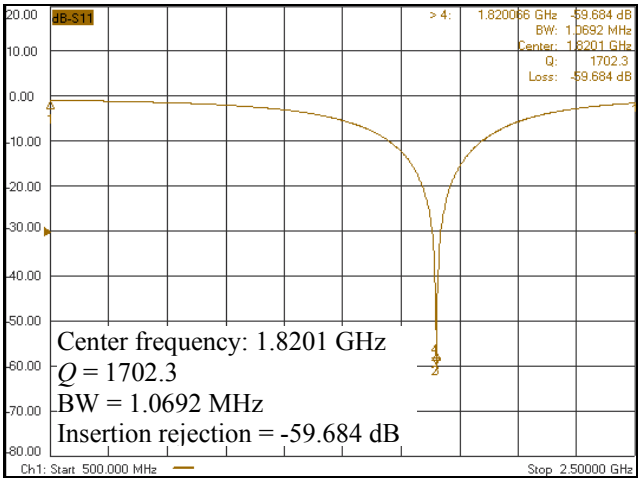
Figure 85 (a) and (b), our experimental results support the theoretical analysis, and the matched impedance is shifted down to 497 Ω. When terminated to the matched impedance, the resonator exhibits a maximum rejection of 60 dB and a high Q of 1702. If the termination impedance is further reduced to 490 Ω, the resonator is no longer matched, and both the Q and the insertion rejection degrade (Figure 85(c)).

The measured results demonstrated in this section are the proofs of the following three facts:

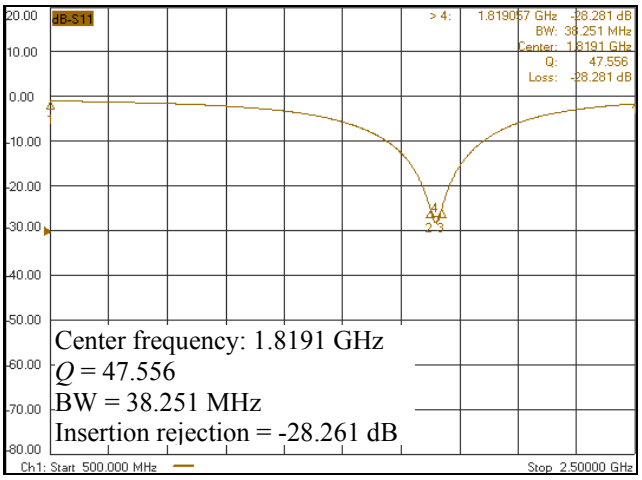
1) A large termination impedance is advantageous if a high-Q tunable parallel LC resonator was demanded as it requires smaller-value capacitors and higher-value inductors. A smaller-value tunable capacitor is preferred as it occupies a smaller area and exhibits a higher Q.
2) The Q of a parallel resonator can be adjusted by changing the termination impedance without causing a significant shift in the resonance frequency.
3) Regardless of the Q of the individual inductor and capacitor, there exists a matched impedance that results in an infinite reflection for the one-port parallel LC resonator. The Q of the components is only important in determining the pass-band loss.



(a) Termination impedance: 500 Ω



(b) Termination impedance: 497 Ω



(c) Termination impedance: 490 Ω

Figure 85: Measured S_{11} of the tunable silver resonator with different termination impedances.

4.4 Tunable Bandpass Filter

In Chapter 3, we demonstrated several low-loss (< 2.52 dB) fixed-frequency lumped filters with 3dB-bandwidth of 9%–30% in the upper UHF range. In this chapter, our goal is to study the feasibility of implementing narrow-bandwidth (5%) integrated tunable bandpass filters using the dry-released silver micromachining technique introduced in Section 4.1. In more specific terms, we aim to achieve a 3dB-bandwidth of less than 5% for a tunable filter in the 800 MHz - 1000 MHz frequency range. The maximum tolerable termination impedance is 200 Ω. Since antennas are generally designed for the standard 50 Ω termination, realizing a matching network for larger termination impedances (i.e., > 200 Ω) adds to the loss of the system. The goal is to achieve an insertion loss of less than 5 dB for a filter with the aforementioned specifications. The out-of-band rejection of the filter is not specified but is intended to be more than 30 dB.

The results of this research demonstrate the first step towards the implementation of a fully integrated high-performance UHF bandpass filter on CMOS-grade silicon. In the following sections, we discuss the results of two types of filters we designed and fabricated: a pseudo-Elliptic filter and a coupled-resonator filter. For each type, we first detail the electrical and physical design of the filter. We then present the measured results and discuss the challenges involved with the electromagnetic simulation of the thick-metal microstructures. We finally provide strategies to improve the performance of the tunable MEMS lumped filters.

4.4.1 Pseudo-Elliptic Filter

4.4.1.A Electrical Design

An 850 MHz filter is designed with a 3dB-bandwidth of 50 MHz and a termination impedance of 200 Ω in a third-order pseudo-Elliptic configuration. In pseudo-Elliptic filters, the two tanks connected in series between the input and output

ports are identical, resulting in a single notch next to the pass-band (Figure 86). In the initial filter design, the *Q* of each LC tank is taken as 75, resulting in an insertion loss of less than 3 dB for the filter. The simulated response of the filter obtained using the ADS is shown in Figure 87.

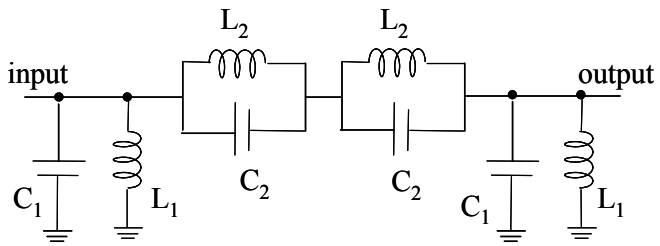


Figure 86: Schematic diagram of the pseudo-Elliptic tunable filter.

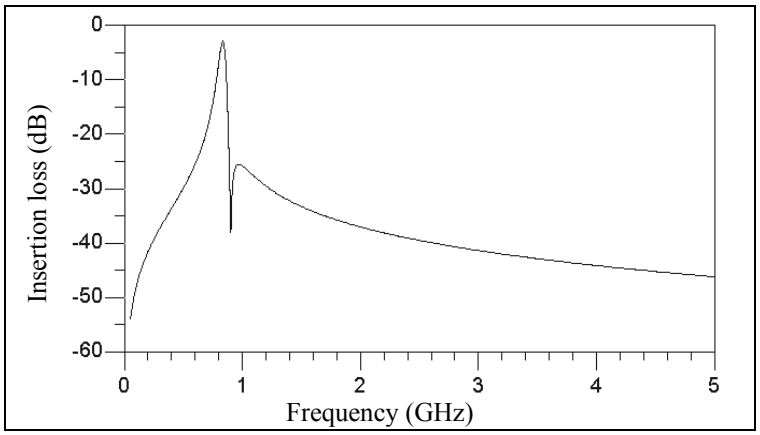


Figure 87: Frequency response of the pseudo-Elliptic tunable filter.

4.4.1.B Sonnet Simulation Response

Electromagnetic simulations of the filter response are carried out in the Sonnet. The memory requirement to run a simulation on the entire layout of the filter exceeds the maximum allowable memory using the Sonnet suite. Therefore, the EM simulations are performed on the individual tanks. The S-parameter responses of the individual tanks are then exported from the Sonnet to the ADS as data items. Finally, the estimated frequency response of the filter is obtained by interfacing the S-parameter of the tanks in the ADS.

In the Sonnet simulations, the electroplated silver layer is formed using the Sonnet thick-metal model. When using thick-metal model, the structure is approximated by two or more infinitely thin metal sheets connected in parallel. As observed from the Sonnet simulation results presented in the previous chapters, using two sheets generally provides a high-accuracy solution. However, for the lateral tunable capacitors, where the gap between the interdigitated fingers is in the order of the metal thickness, the capacitance coupling is underestimated with two sheets. In this case, more sheets are required. However, increasing the number of sheets increases the memory requirements and processing time and is computationally intensive. Therefore, the number of sheets was limited to only two layers, knowing that using two sheets results in an overestimation of the metal loss and a higher insertion loss for the filter [85].

Figure 88 shows the EM simulated frequency response of the filter obtained using the Sonnet and ADS. The simulated center frequency of the filter is 880 MHz at which the filter exhibits an insertion loss of 9.5 dB. The bandwidth of the filter is 57 MHz in simulations. With the assumption that the two-sheet model overestimates the metal loss and underestimates the capacitive coupling, a lower loss, resonance frequency, and bandwidth are expected for the fabricated filter.

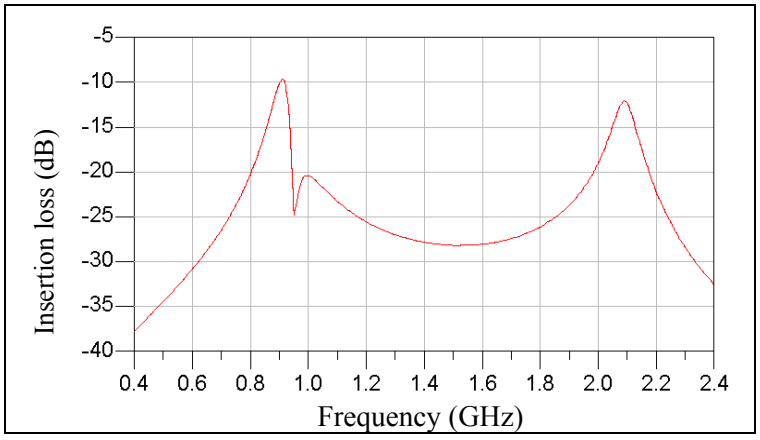


Figure 88: EM simulated frequency response of the pseudo-Elliptic tunable filter obtained using the Sonnet.

4.4.1.C Measured Frequency Response

A SEM view of the fabricated pseudo-Elliptic filter is shown in Figure 89 [89]. The silicon dioxide gap of the fixed capacitors is 4 μm in this design. The inductors are supported on 8 μm thick silicon dioxide membranes and the tunable capacitors are suspended on air cavities.

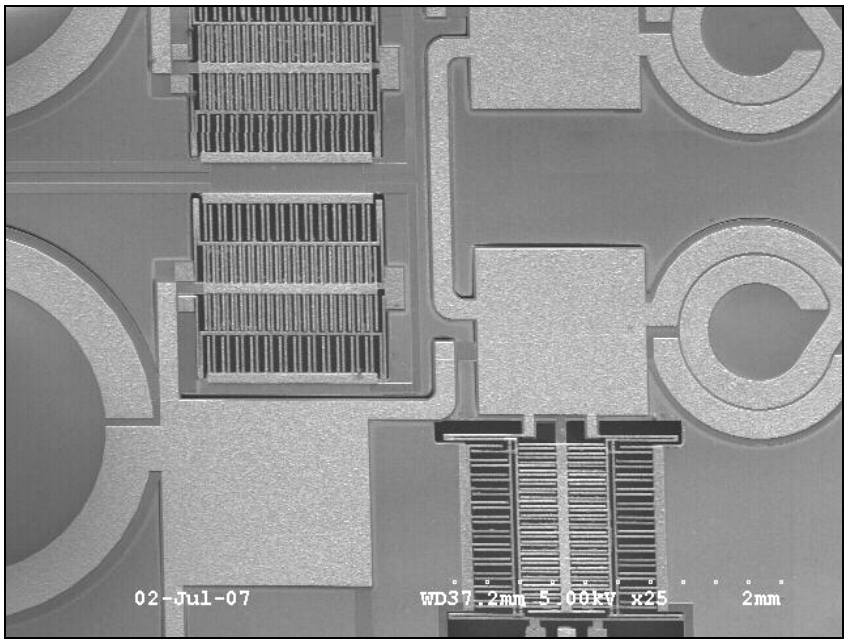


Figure 89: A SEM view of the silver tunable pseudo-Elliptic filter fabricated on a CMOS-grade silicon substrate.

Figure 90 shows the measured S-parameter of the filter when terminated to 200 Ω. The measured embedded insertion loss of the filter at 831 MHz is 4.0 dB, indicating an individual component *Q* of more than 150 and a tank *Q* close to 75 at the pass-band (as demonstrated in Figure 87). As expected, both the center frequency and insertion loss of the fabricated filter is considerably lower than that obtained using the Sonnet simulations. However, the measured bandwidth of the filter is 75 MHz, which is not consistent with what is expected from the Sonnet simulations. A comparison of the measured and simulated frequency response of the filter clearly indicates that the Sonnet tool is not suited for modeling the response of thick tunable microstructures.

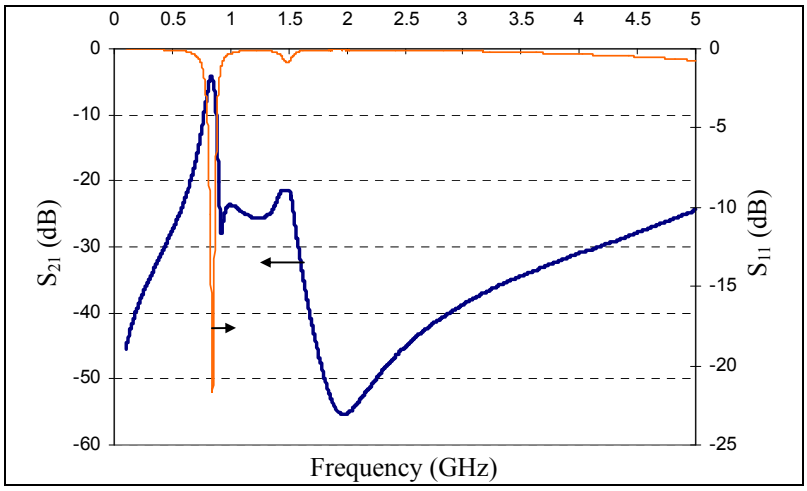


Figure 90: Measured S-parameter of the filter at 831 MHz, showing an insertion loss of 4 dB and a return loss of 20 dB when terminated to 200 Ω.

In the prototype implementation of the pseudo-Elliptic filter, tunable capacitors of 1 pF are laid in parallel with fixed MIM capacitors to obtain the desired capacitance value. Because of the large value of the fixed capacitors, the total capacitance change is not as pronounced, and hence the frequency shift obtained by electrostatic tuning of the capacitors is not more than 17 MHz (Figure 91).

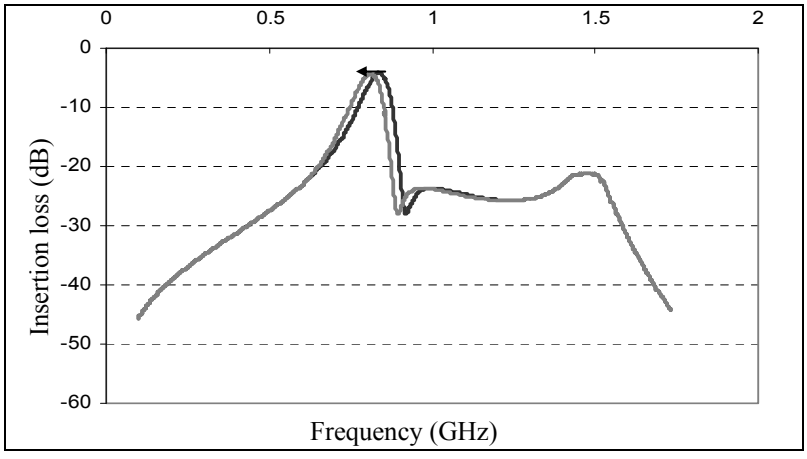


Figure 91: Measured electrostatic tuning of the filter. A DC voltage of 61V is applied to the tunable capacitors.

Figure 92 shows the measured frequency response of the filter at the initial state together with the measured response when each capacitor is doubled (by depositing a

thinner interlayer silicon dioxide dielectric), demonstrating that the filter can potentially be tuned by 150 MHz if a larger portion of the capacitors is made tunable. As shown in Figure 92, by increasing the capacitor values, the *Q* of each parallel LC tank increases, resulting in a lower bandwidth as the filter is tuned. If the tuning range is improved, this filter would be a potential candidate for the GSM 850 band. The frequency shift of 150 MHz shown in Figure 92 is more than the maximum tuning required to cover both GSM 900 and GSM 850.

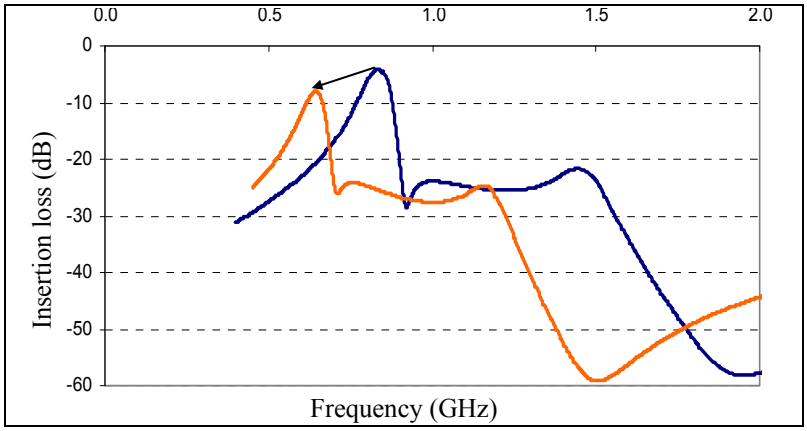


Figure 92: Measured response of the filter. Each capacitor is doubled, resulting in a 150 MHz frequency shift.

4.4.1.D Temperature Characteristic

The temperature stability of the filter is tested in the temperature-controlled RF probe station introduced in Section 3.3.9. The calibration is performed at room temperature and is not repeated for each measurement. Over the range of 23 °C to 85 °C, the filter exhibits a temperature drift of less than 0.19% in the center frequency and less than 0.5% in the 3dB-bandwidth, as shown in Figure 93. The insertion loss of the filter degrades as the temperature increases because of two reasons: the higher loss of silver layers at higher temperatures and the calibration errors. Nevertheless, the insertion loss variation remains less than 5% (Figure 94).

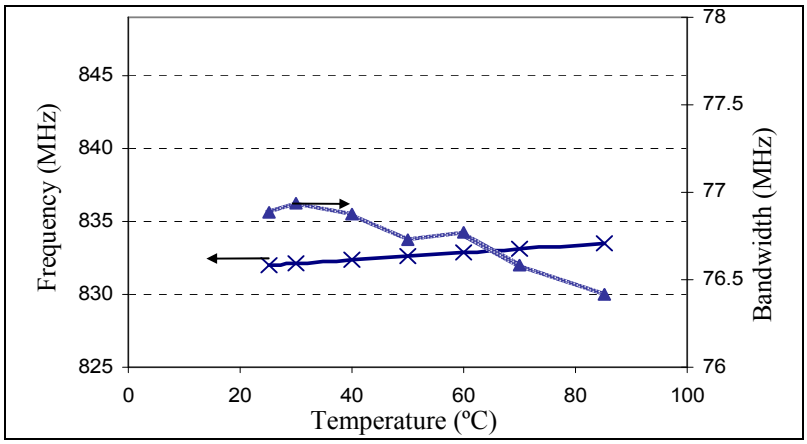


Figure 93: (Left) frequency and (right) bandwidth behavior of the filter in 23º C to 85º C temperature range.

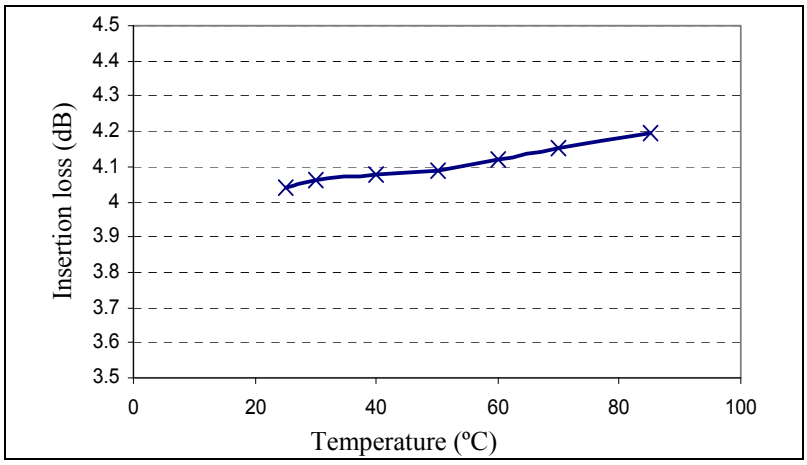


Figure 94: Insertion loss versus temperature, showing a fairly-stable performance over 23º C-85º C range.

4.4.2 Coupled-Resonator Tunable Bandpass Filters at 750 MHz

4.4.2.A Electrical Design

Although the pseudo-Elliptic filter shows promising performance for GSM applications, the bandwidth of the filter has to be further reduced to 25 MHz, which is a three-time reduction from the current performance. In addition, as shown in Figure 92, the bandwidth of the pseudo-Elliptic filter changes as the center frequency is tuned. For most applications, a constant bandwidth is required across the tuning range. For these

reason, we have investigated a coupled-resonator filter topology and have designed an integrated scheme to maintain the bandwidth constant when tuning the filter.

In designing the filter, a second-order 800 MHz tunable filter with a 3dB-bandwidth of 40 MHz is targeted. A two-pole coupled-resonator configuration is utilized, as shown in Figure 95 [90]. This configuration is an alternative realization of a chebychev filter, where the series resonators (with two-port capacitors) are converted to parallel resonators using immittance inverters [91]. The second-order filter has a fewer lumped components compared to higher-order filter topologies, resulting in a simplified tuning mechanism, lower insertion loss, and reduced die area at the expense of inferior out-of-band rejection. An all-pole filter topology is selected to minimize the in-band group delay variation. As shown in Figure 95, the filter is designed using two identical parallel resonators to reduce the number of components that have to be characterized, individually. Also, fabrication inaccuracies have an equal effect on the identical resonators, which reduces the resulting distortion in the filter frequency response. The input termination impedance of this filter is 200 Ω due to the reasons discussed earlier in this chapter.

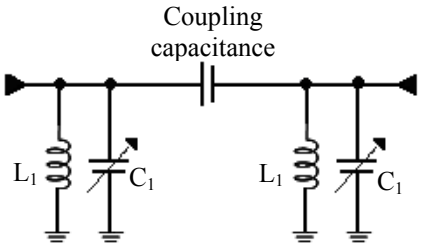


Figure 95: Schematic of the 800 MHz coupled-resonator tunable bandpass filter.

Because of the insufficient capacitance density of the tunable capacitors, each capacitor in the LC resonator is a parallel combination of a fixed MIM capacitor and a smaller lateral tunable capacitor. Frequency tuning is achieved by varying the tunable capacitors, electrostatically. When tuned, the overall capacitance increases resulting in a

higher resonator Q, which in turn reduces the bandwidth of the filter. To maintain a constant bandwidth across the tuned frequency range, one has to either tune the coupling capacitance or adjust the output termination impedance of the filter. Since in most applications the bandpass filter is interfaced with a LNA, we have chosen the latter approach and have tuned the input impedance of the amplifier, accordingly. As the input impedance of the LNA drops, the load reflection coefficient (Γ_L) decreases, which in-turn, negatively affects the reflection coefficient at the input terminal (Γ_{in}) (19). The result is a lower selectivity for the output tank and a larger bandwidth for the filter.

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad . \tag{19}$$

Generally, the low-noise amplifier (or any gain block that follows the bandpass filter) has a very high input impedance. Therefore, the filter is designed with 2000 Ω output termination to eliminate the need for an extra matching network. The equivalent input capacitance of the active component can be minimized such that it does not cause significant power reflection. Alternatively, the capacitor of the resonator at the output of the filter can be tuned to accommodate the extra capacitance seen from the input of the active circuit. The schematic view of the LNA with a tunable input impedance is shown in Figure 96. This design benefits from the high gain and high stability of the cascade stage with a noise figure performance close to that of a single common-source amplifier. As shown in Figure 96, the output load of the LNA consists of a lumped LC tank. The resonance frequency of this tank matches the center frequency of the bandpass filter, resulting in a lower overall bandwidth for the cascaded filter and LNA. With this design the overall bandwidth of the system is reduced from 40 MHz (the bandwidth of the filter) to 32 MHz, which corresponds to a 40% boost in the Q.

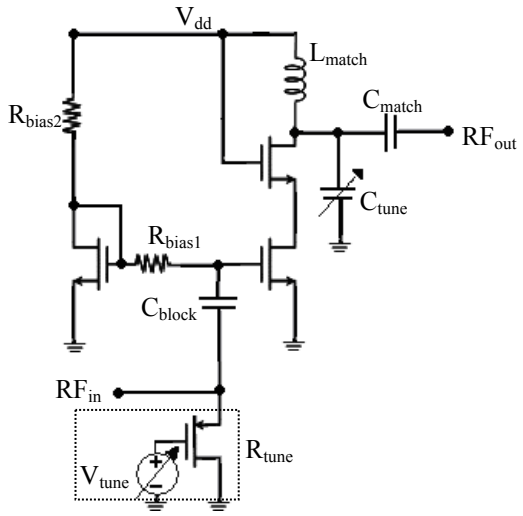


Figure 96: Schematic view of the low-noise amplifier with tunable input impedance.

4.4.2.B Sonnet Simulations

A preliminary EM simulation on the filter layout is performed in the Sonnet with two metal sheets for the electroplated silver. The silver conductivity is taken as 5.8×10^7 S/m and the loss tangent of silicon dioxide is taken as 0.001 in the simulation. Figure 97 shows the Sonnet simulated frequency response of the filter.

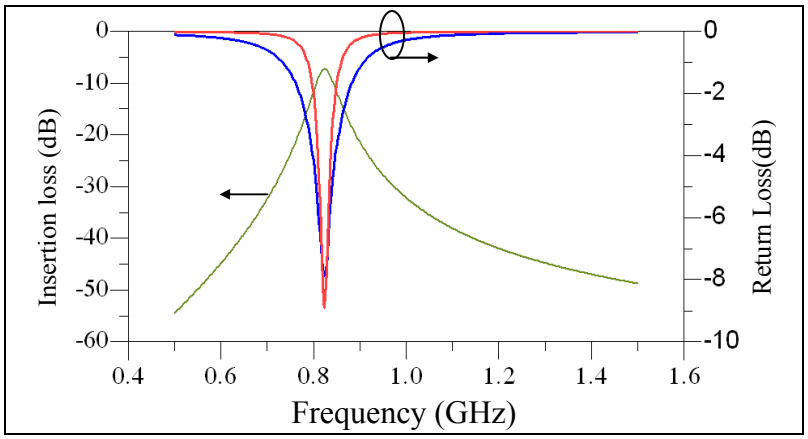


Figure 97: Simulated frequency response of the coupled-resonator bandpass filter obtained using the Sonnet EM simulation tool.

With the aforementioned values for the silver conductivity and silicon dioxide loss tangent, the electromagnetic simulated center frequency and bandwidth of the filter are 824 MHz and 41 MHz, respectively. The simulated insertion loss of the filter at 824

MHz is 6.8 dB. In Section 4.4.1.B, we discussed that the two-sheet model overestimates the metal loss, and our experimental result (shown in Figure 90) was a proof of this assumption. Therefore, a better insertion loss was expected for the fabricated filter. However, as discussed later in this chapter, this is not the case and further optimizations need to be performed to improve the performance of the filter in terms of center frequency and insertion loss.

4.4.2.C Fabrication Overview

A SEM view of the bandpass filter is shown in Figure 98. The planar spiral inductor is fabricated on a 4 μm thick silicon dioxide membrane, which is supported by two silicon bars. The gap thickness of the fixed capacitor in this design is 1 μm. Figure 99 shows the close-up SEM views of the tunable capacitor. When designing the layout of the tunable capacitor, a silicon bar is retained underneath the fixed capacitor plate to increase the mechanical integrity of the device. This silicon bar is isolated from the silver layer using a 4 μm thick silicon dioxide layer. Later in this chapter, we show that the electrical performance of the filter can be improved by removing the silicon entirely from underneath the capacitor and inductor.

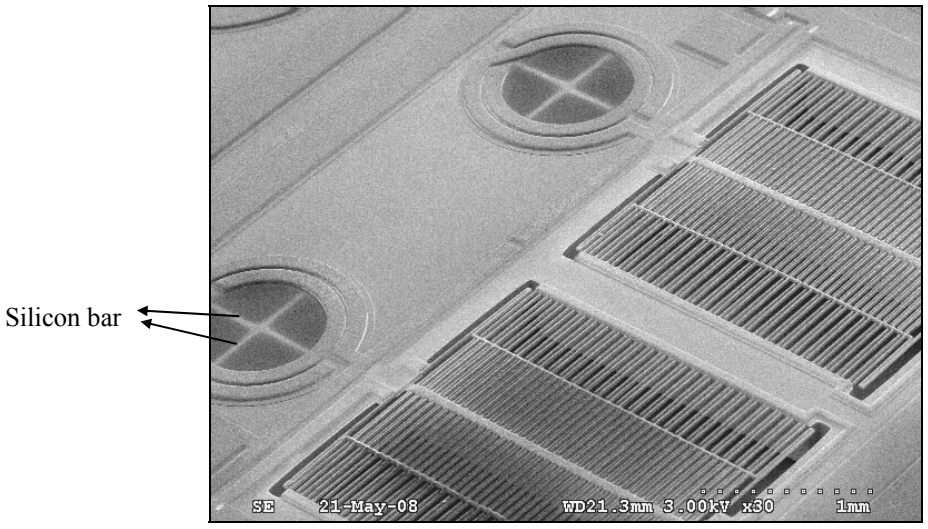


Figure 98: A SEM view of the silver tunable lumped LC resonator of the coupled-resonator filter fabricated on a 10-20 Ω.cm silicon substrate.

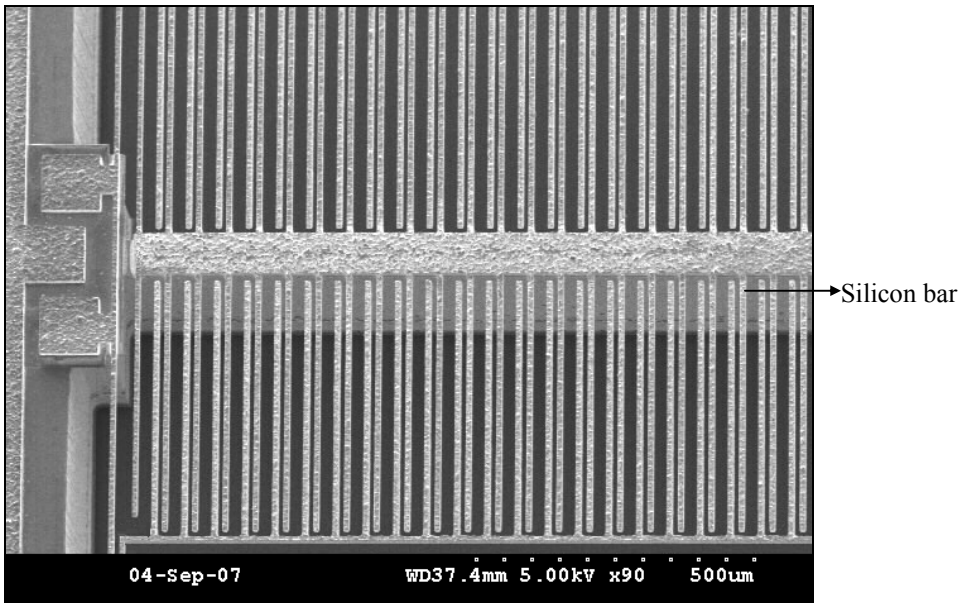


Figure 99: A close-up SEM view of the tunable silver capacitor. A silicon bar is retained to increase the mechanical integrity of the device.

The calibration is performed using the Cascade 50 Ω standard substrate (101-190). The filter response when terminated to 200 Ω at the input and 2000 Ω at the output is measured by converting the termination impedance of the network analyzer, accordingly.

4.4.2.D Measured Results

Figure 100 shows the micrograph of the coupled-resonator lumped bandpass filter fabricated on a 10-20 Ω.cm silicon substrate. As shown, this filter occupies 5.5 mm × 4.6 mm of die area, which is considered small compared to the reported tunable lumped filters operating in this frequency range [92], [93].

Figure 101 shows the measured S-parameter of the bandpass filter. The filter exhibits a 3dB-bandwidth of 42.7 MHz at 752.6 MHz with an insertion loss of 10.7 dB. As shown in Figure 101, the filter response is spurious free in a broad frequency range (45 MHz - 2 GHz). The reasons for the high insertion loss of the filter and the approaches taken to improve the filter performance are explained in the following sections.

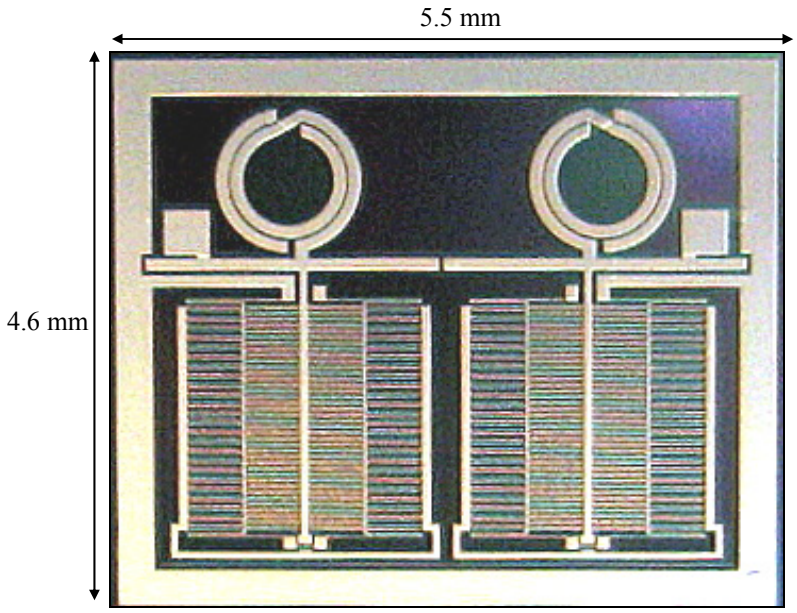


Figure 100: A micrograph of the tunable coupled-resonator bandpass filter, showing the dimensions of the filter.

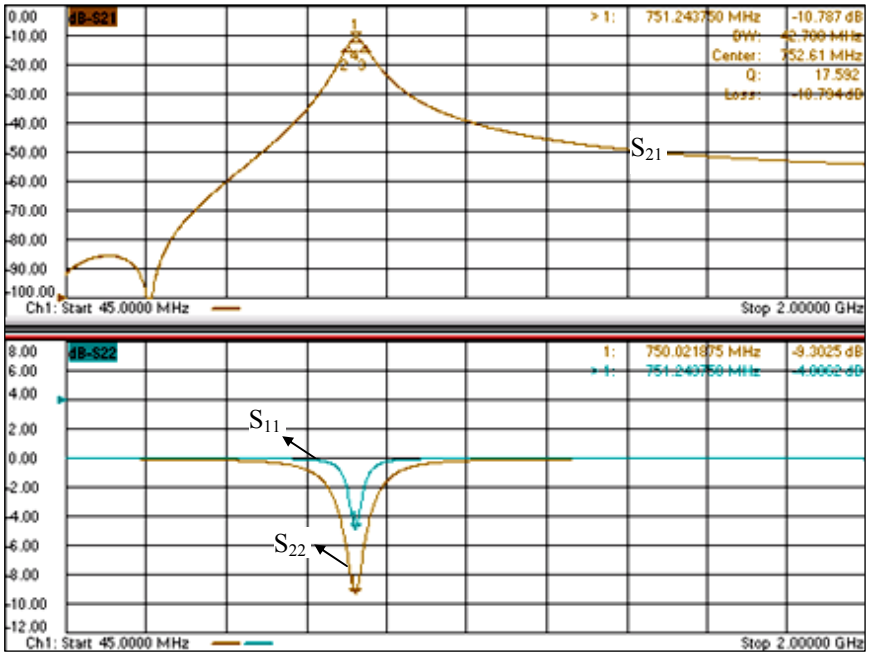


Figure 101: Measured frequency response of the coupled-resonator bandpass filter.

Figure 102 shows the measured electrostatic tuning characteristic of the coupled-resonator filter when equal DC voltages are applied to the tunable capacitors. As expected, the bandwidth of the filter (prior to interfacing with the LNA) reduces from 42

MHz to 39 MHz when tuning the center frequency of the filter from 752 MHz to 711 MHz.

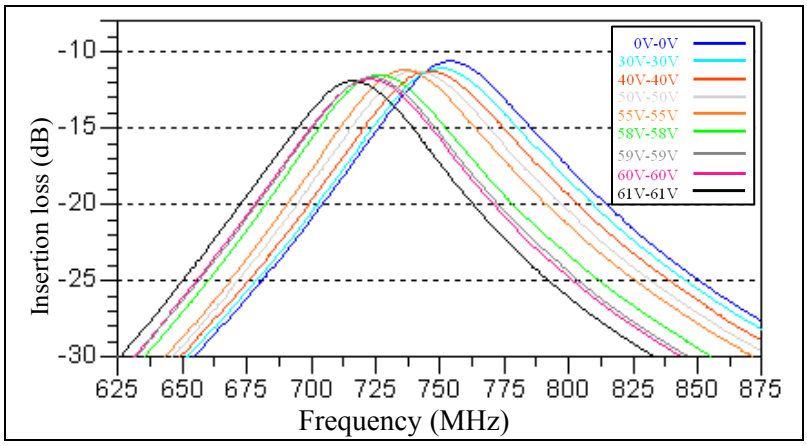


Figure 102: Measured electrostatic tuning of the filter, showing tuning range of > 40 MHz. The inset shows the DC voltages applied to each tunable capacitor.

4.4.2.E System-Level Results

The proposed LNA is interfaced with the measured S-parameters of the fabricated filter at the lower- and upper-end of the tuning range. The combined coupled-resonator filter and LNA show greater than 10 dB of gain across the pass-band (Figure 103). The LNA is designed in the 1P6M 0.18 µm CMOS process and consumes 2.7 mA out of 1.8 V supply. Given the loss of the tunable bandpass filter, the power consumption of the LNA is slightly increased.

As discussed earlier, the 3dB-bandwidth of the cascaded filter and LNA is less than that of the individual bandpass filter. At the initial state of the capacitors, the overall bandwidth is 32 MHz. As the filter is tuned, the overall bandwidth drops to 28 MHz. Therefore, a tunable impedance is realized at the input of the LNA using a shunt tunable PMOS transistor to keep the bandwidth constant. The PMOS transistor is operated in the linear region. To tune the impedance, V_{GS} of the transistor is changed. Altering V_{GS} from 1.6 V to 1.0 V results in a 2× impedance change. Since the value of this resistor is large,

its associated noise is small and therefore has minimal effect on the overall noise figure of the LNA. Tuning this impedance from 2000 Ω to 1000 Ω increases the overall bandwidth at the tuned state from 28 MHz to 32 MHz, resulting in a constant bandwidth across the tuned frequency range (Figure 103).

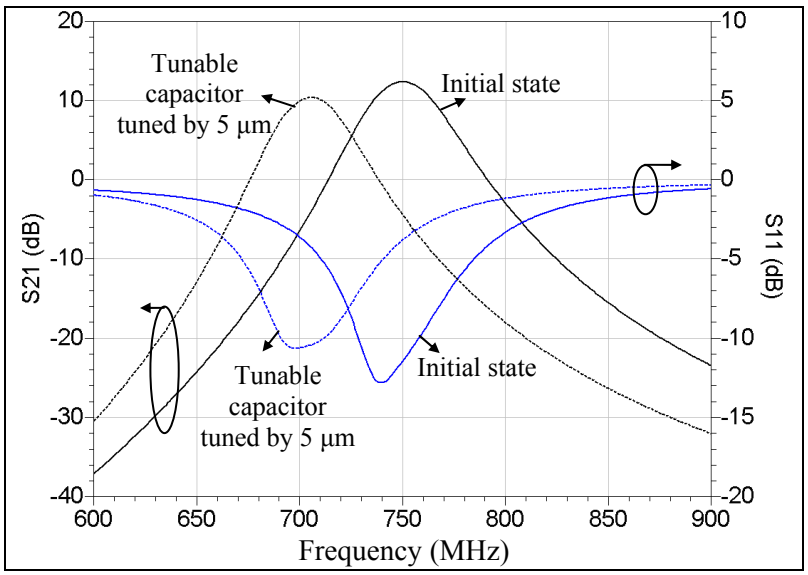


Figure 103: Frequency response of the cascaded filter and tunable-input LNA. The bandwidth of the cascaded filter and LND is 32 MHz at both ends of the tuning range.

4.4.2.F Tuning Range Improvement

The fixed capacitors form a large fraction of the total capacitance in each LC resonator and hence heavily load the overall capacitance tuning range. Consequently, while the application of 61 V results in 2× capacitance change for the tunable capacitors (Figure 81), the overall capacitance change is no more than 20 %. The tuning of the coupled-resonator filter can be significantly improved by increasing the ratio of the tunable to fixed capacitor. To increase the overall tuning of the capacitance, one can reduce the parallel-plate gap spacing or place several identical tunable capacitors in parallel at the cost of an increased area.

4.4.2.G Insertion Loss Improvement

To identify the source of the high insertion loss, the quality factor of the individual components is measured and the filter is subsequently modeled using the measured data. Figure 104 shows the measured quality factor of a stand-alone tunable silver capacitor identical to the one used in the filter (fabricated on the same substrate). As shown, this capacitor has a Q of close to 80 at the center frequency of the filter. This capacitor is identical to the capacitor shown in Figure 74 that exhibits a high Q of greater than 500, as shown in Figure 80. The lower Q of the capacitor incorporated in the filter is due to the loss that is introduced by the silicon bar retained under the fixed capacitor plate. To increase the Q of this capacitor, the silicon bar is removed in an improved layout of the filter. We discuss the result of the improved layout in the next section.

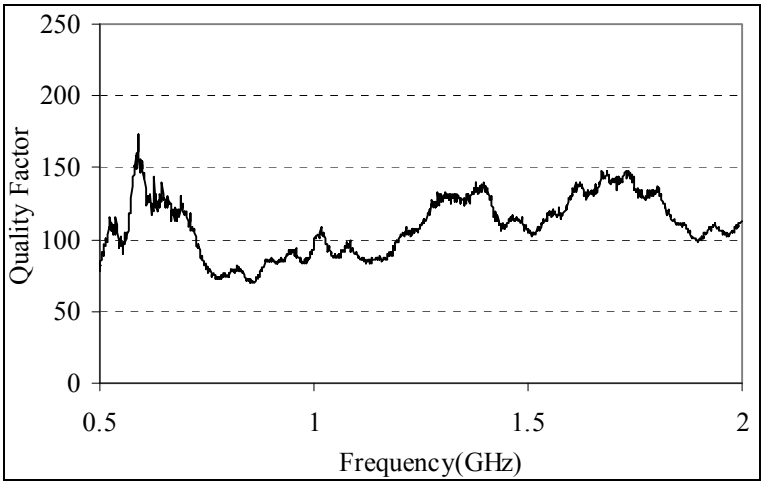


Figure 104: Extracted embedded Q of the two-port tunable capacitor shown in Figure 99. A silicon bar is retained under the fixed capacitor port, resulting in a lower Q than that shown in Figure 80

In addition, as shown in Figure 105, the fixed capacitor exhibits a low embedded Q at the frequency of interest (Q =61 at 752 MHz), which is due to the poor quality of the interlayer PECVD silicon dioxide dielectric. To improve the quality of the silicon dioxide, the deposition temperature is increased to 350º C in a new batch and the deposition process is divided into three runs to reduce the density of the pin holes, which

are the main causes for the low quality of the PECVD silicon dioxide. The result is shown in the next section.

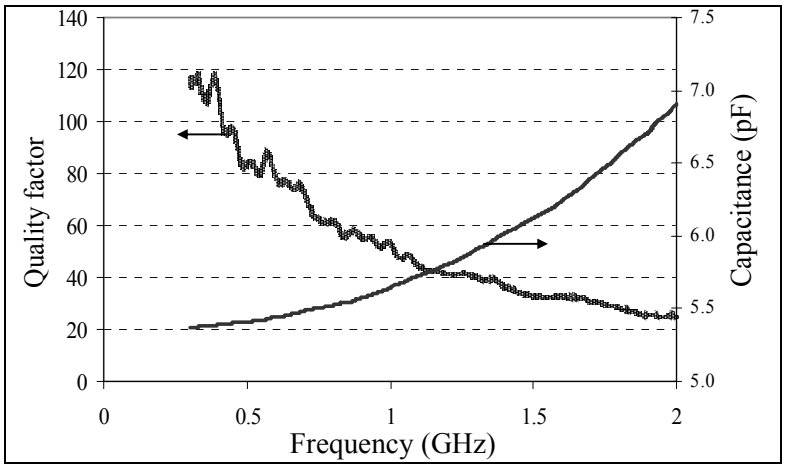


Figure 105: Measured embedded characteristic of the fixed silver capacitors.

The measured characteristic of the on-chip inductors is shown in Figure 106. Although a high *Q* of 79 is achieved for the integrated inductor at 1.54 GHz, the *Q* of the inductor at the filter pass-band (the hatched area) is not at its maximum possible value.

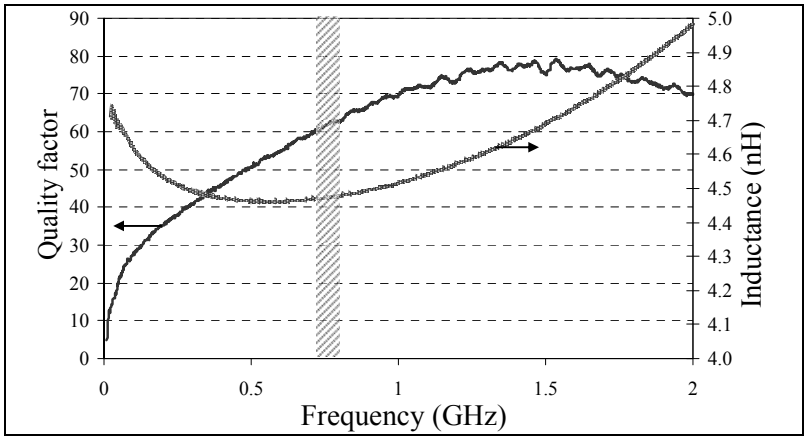


Figure 106: Measured embedded characteristic of the on-chip silver inductor.

Using the measured characteristics of individual components, the electrical model of the filter is derived (Figure 107). The long lines interconnecting the two resonators as

well as the lines connecting the tunable capacitors to the ground plane are modeled as inductors in series with small resistors. The value of these parasitic inductors and resistors are adjusted such that the modeled response fits that of the measurement. Figure 108 compares the measured and modeled frequency response of the filter, showing a good agreement between them. The electrical model of the filter suggests that the parasitic inductances of the interconnecting lines and the folded springs, significantly lower the center frequency of the filter.

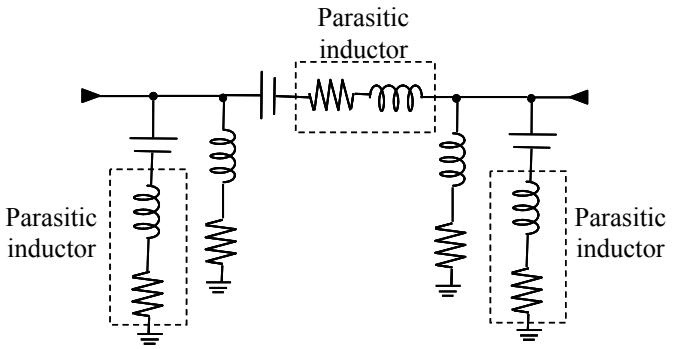


Figure 107: Equivalent electrical model of the bandpass filter using the measured characteristic of the individual lumped components.

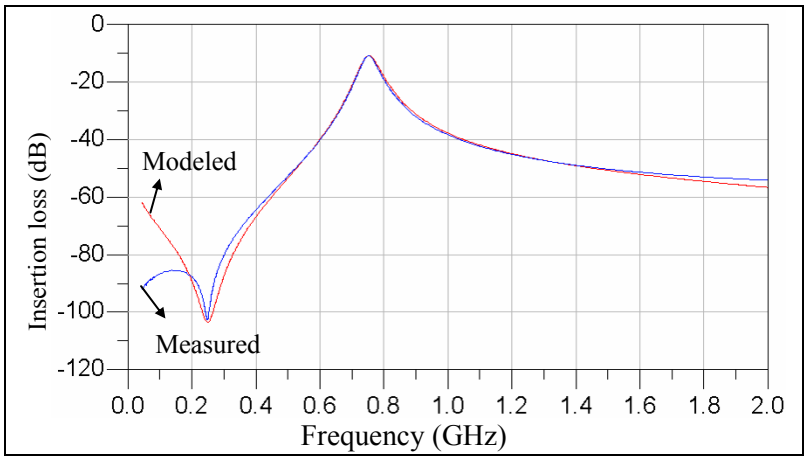


Figure 108: Comparison of the measured and modeled frequency response of the coupled-resonator filter.

On the other hand, a comparison of Figure 97 and Figure 108 clarifies that the measured frequency response is significantly deviated from the Sonnet response in terms of insertion loss and center frequency. While a lower center frequency is expected for the

fabricated filter, the high measured insertion loss cannot be justified using the Sonnet. With a better understanding of the shortcomings of our filter layout, we proceed with the simulation of the fabricated filter in a 3D modeler for a more accurate result. The Agilent HFSS 3D electromagnetic full-wave solver is used for this purpose. Figure 109 shows the 3D model of the filter.

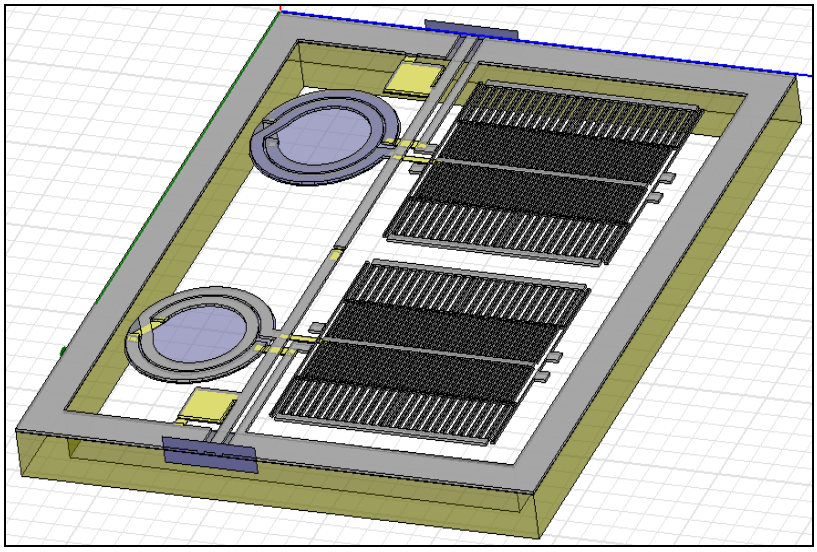


Figure 109: HFSS model of the coupled-resonator bandpass filter.

The fitted EM model for the fixed capacitor shows a high loss tangent of 0.005 for silicon dioxide, which is five times worse than that expected and used in the preliminary Sonnet simulations. On the other hand, the fitted response of the inductors shows a high conductivity of 6×10^7 for the electroplated silver layer. Using these values, the HFSS responses of the filter at the initial state together with the response when the tunable capacitors are tuned by 5 μm are shown in Figure 110. The HFSS simulation response is in excellent agreement with the measured response at both ends of the tuning range (compare Figure 102 with Figure 110).

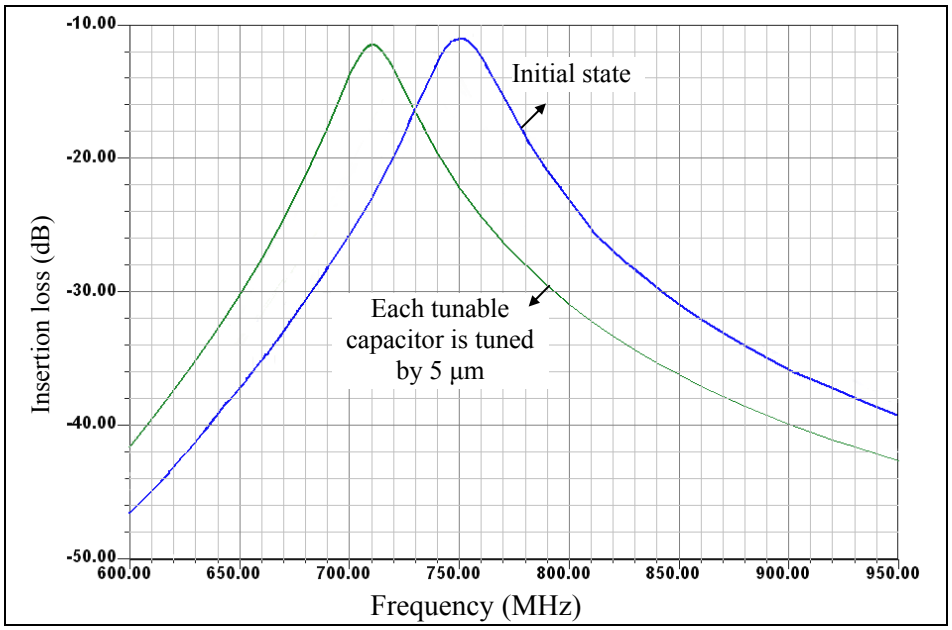


Figure 110: EM simulated frequency response of the coupled-resonator bandpass filter at both ends of the tuning range obtained using the HFSS 3D solver.

Using the fitted values for the silver conductivity and the silicon dioxide loss tangent, further optimizations are performed on the physical layout of the filter. HFSS simulation shows that by optimizing the layout of the filter, the insertion loss can be improved to less than 6 dB. In the optimized layout, the two tanks are placed physically closer to each other, as shown in Figure 111, to reduce the length of the interconnecting line and hence to improve the insertion loss further. Inverting the layout of one tank with respect to the other (as shown in Figure 111) results in a smaller coupling between the two in-plane inductors, which in turn improves the frequency response of the filter. In addition, in the optimized layout, which we call the invert layout, the silicon is entirely removed from backside of the tunable capacitors and inductors. As a result, the insertion loss of the optimized filter with the same material properties is improved to 6.0 dB while the bandwidth is reduced to 35.5 MHz (Figure 112).

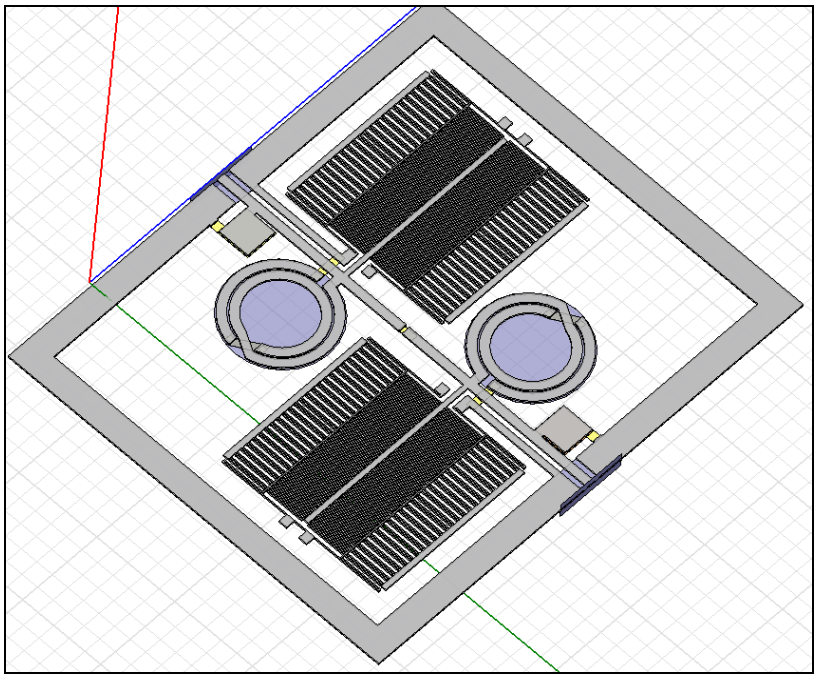


Figure 111: HFSS model of the optimized filter (the invert layout).

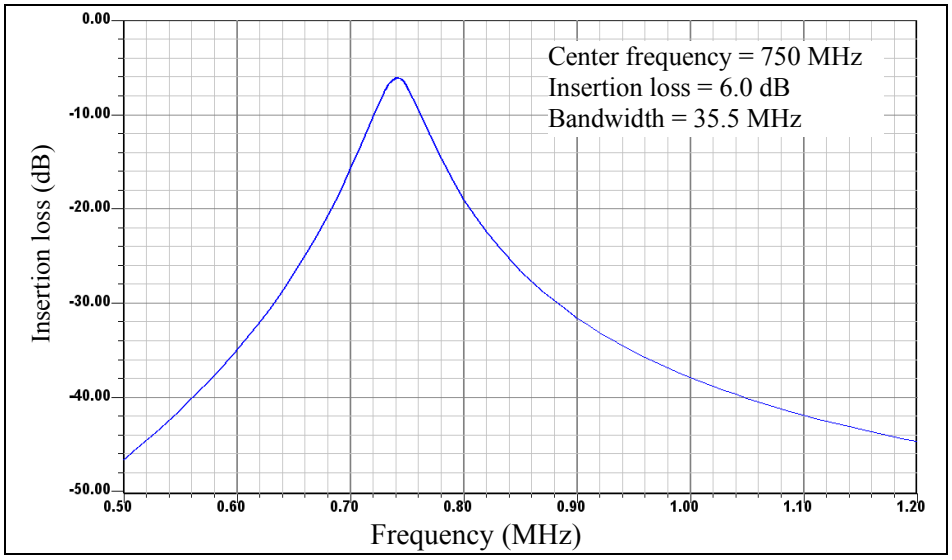


Figure 112: Optimized frequency response of the coupled-resonator filter obtained using the HFSS.

Figure 113 shows the measured S-parameter of the fabricated bandpass filter with the invert layout. As discussed earlier, the silicon dioxide deposition temperature is increased in this batch resulting in a higher Q for the fixed capacitors. This filter exhibits a 3dB-bandwidth of 38.8 MHz at 750.9 MHz (a percentage bandwidth of 5.1) with an

insertion loss of 5.9 dB. The measured center frequency and bandwidth are shifted due to a slightly larger air gap between the parallel-plate fingers of the tunable capacitor. The tuning characteristic of this filter is similar to the one shown in Figure 102. Figure 114 shows the micrograph of this filter. As shown, this filter occupies 4.8 mm × 5.7 mm of die area. To our best knowledge, this is the first implementation of an integrated tunable lumped filter in the UHF range with such a low insertion loss and small bandwidth.

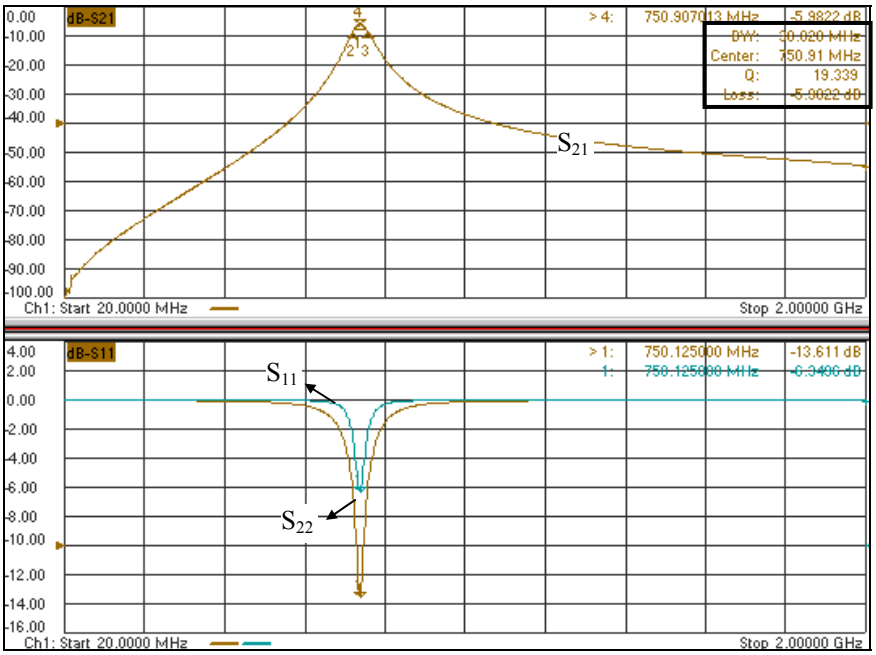


Figure 113: Measured frequency response of the filter with the optimized layout.

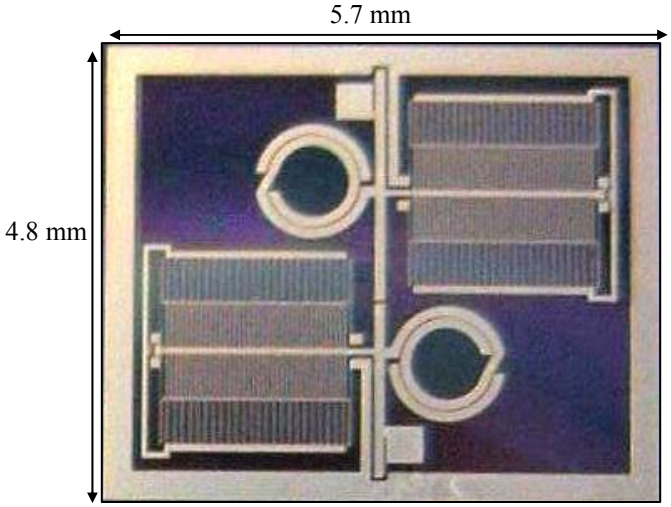


Figure 114: A micrograph of the optimized tunable bandpass filter.

Figure 115 shows a SEM view of the filter with the invert layout. As shown in Figure 115 and in the close-up view of the Figure 116, the silicon is removed from backside of the tunable capacitors, resulting in a higher Q for these devices.

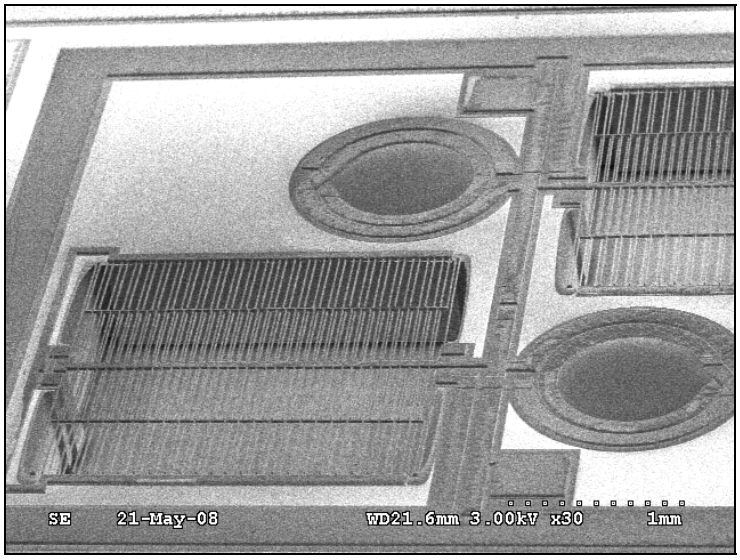


Figure 115: A SEM view of the coupled-resonator bandpass filter with the optimized layout.

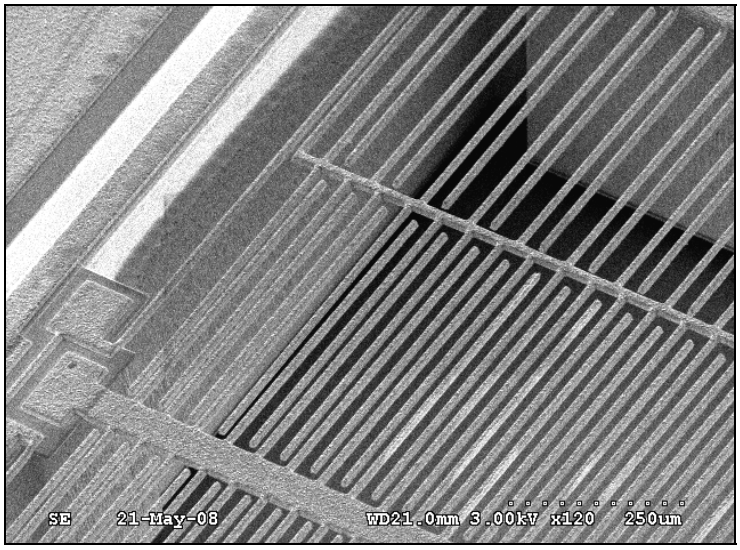


Figure 116: A close-up SEM view of the tunable capacitor, showing the silicon is removed from backside of the fixed capacitor plate.

In the new batch, the second-order coupled-resonator filter with the direct layout (shown in Figure 109) exhibits an insertion loss improvement of more than 2 dB, owing

to the better quality of the interlayer silicon dioxide and higher Q of the fully elevated tunable capacitors (Figure 117). In addition, in this batch, the tunable capacitor gap is reduced to 8 μm (from 10 μm), resulting in a smaller 3dB-bandwidth of 4.3% for this filter. A SEM view of this filter is shown in Figure 118.

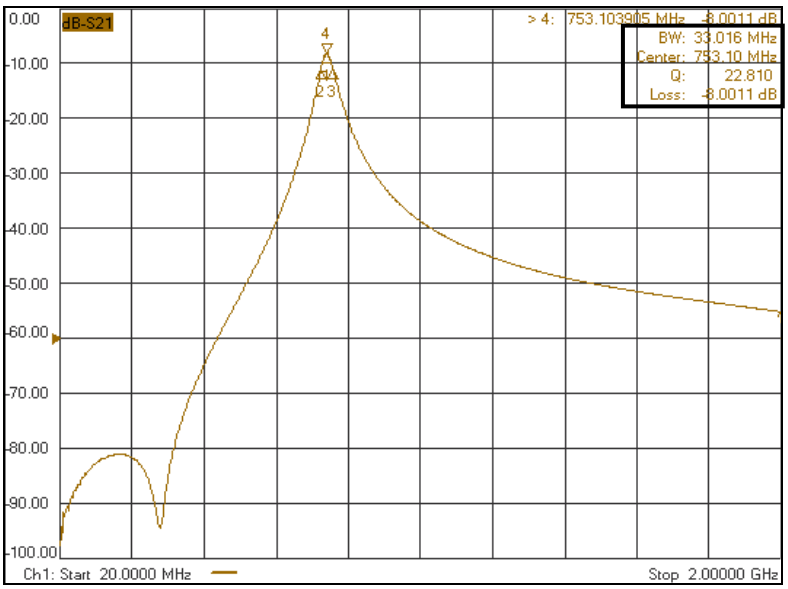


Figure 117: Measured frequency response of the coupled-resonator bandpass filter with the direct layout fabricated using higher-quality silicon dioxide and an improved layout for the tunable capacitors. The insertion loss is improved to 8 dB and the bandwidth is reduced to 33 MHz.

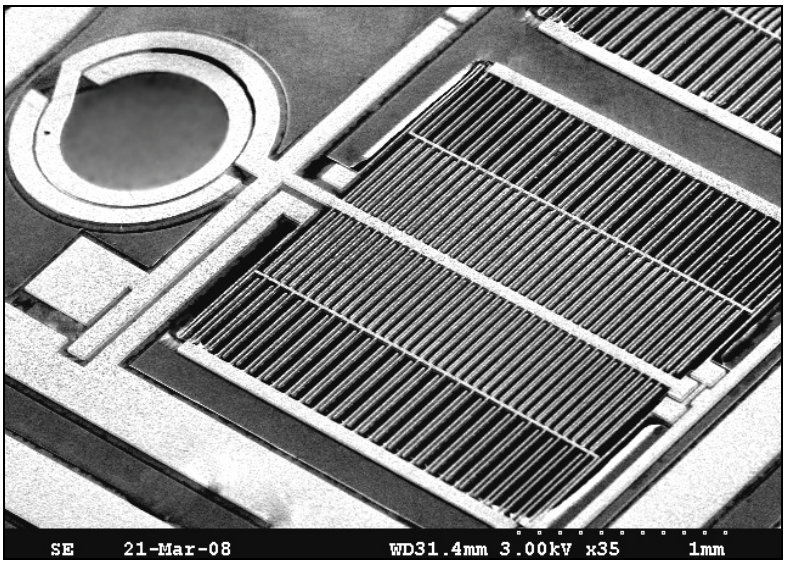


Figure 118: A SEM view of the coupled-resonator filter with the direct layout. The silicon is entirely removed from the backside of the tunable capacitor in this design.

4.4.3 Coupled-Resonator Tunable Bandpass Filters at 1 GHz

Using the fitted values obtained for the silver conductivity and silicon dioxide loss tangent, we have also designed a coupled-resonator bandpass filter at 1 GHz with a 3 dB-bandwidth of 50 MHz. The HFSS simulated response of this filter is shown in Figure 119. As shown, the expected insertion loss of the filter is 6.2 dB at 990 MHz. In this design, the thickness of oxide is 2 μm, resulting in a higher Q for the spiral inductors. The higher Q of the inductor with a thicker oxide is due to the lower parasitic capacitance between the underpass routing layer and the electroplated silver layer.

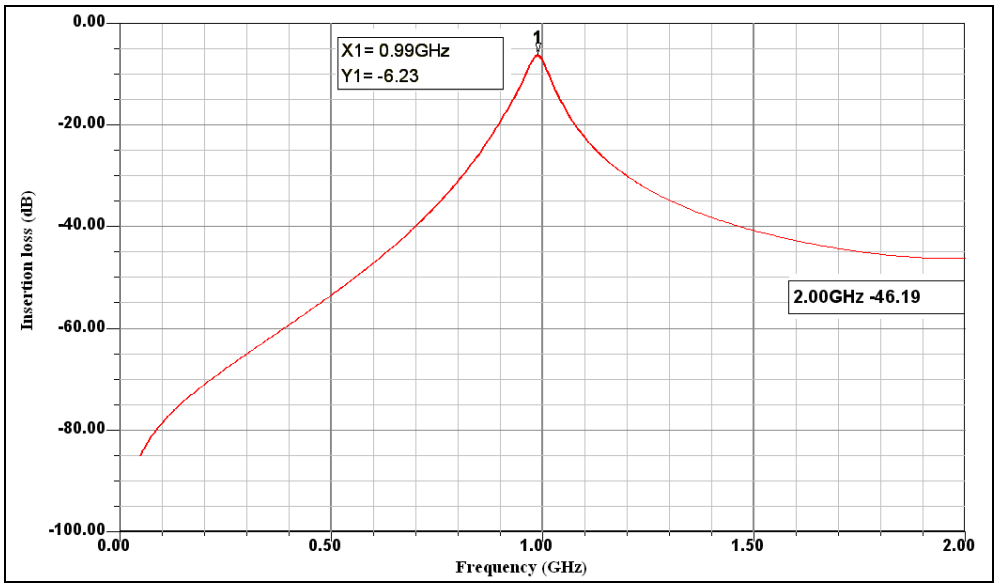


Figure 119: HFSS response of the filter at the initial state, showing an insertion loss of 6.2 dB at 0.99 GHz and bandwidth of < 50 MHz.

Figure 120 shows a SEM view of the fabricated filter. The silver layer is 17 μm thick and the gold routing layer is 3 μm thick. This device is fabricated on a high resistivity silicon substrate with a resistivity of > 1000 Ω.cm. Although silicon is removed from backside of the lumped components and the resistivity of silicon does not have a significant effect on the Q of the inductors and tunable capacitors, a higher resistivity silicon substrate introduces smaller parasitics for the ground plane and the 100 μm-wide interconnect lines, resulting in a better performance for the filter.

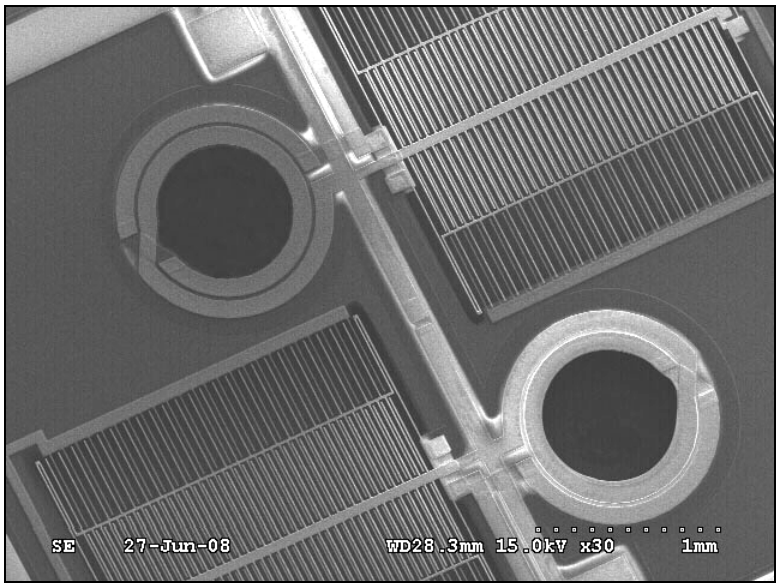


Figure 120: A SEM view of a 17 µm thick silver tunable bandpass filter at 1075 MHz.

Figure 121 shows the measured insertion loss of the filter showing an insertion loss of 6.0 dB at 1.075 GHz and a narrow bandwidth of 5.8%. The deviation of the measured bandwidth from that obtained using the HFSS simulation is due to the inaccurate spacing of the tunable capacitor interdigitated fingers, thickness of the silver layer, and permittivity of the silicon dioxide layer.

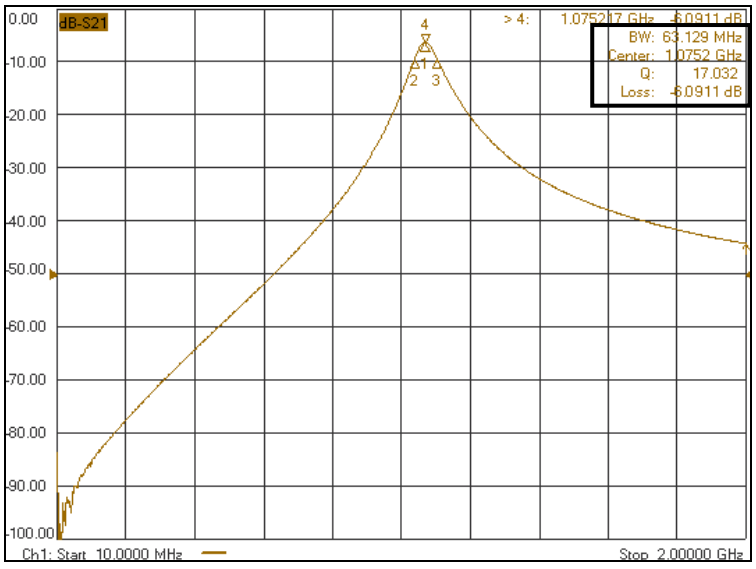


Figure 121: Measured response of the filter, showing a small bandwidth of 63.1 MHz and an insertion loss of 6.0 dB at 1.075 GHz.

The measured tuning characteristic of the filter is shown in Figure 122. The filter is tuned by more than 123 MHz with the application of 65 V to both tunable capacitors incorporated in the filter. As discussed earlier, the bandwidth of the filter decreases and the insertion loss increases by increasing the capacitance values and thereby tuning the filter. The insertion loss of the filter is at 8.4 dB at the lower end of the tuning range (952 MHz) and the bandwidth is 53.5 MHz.

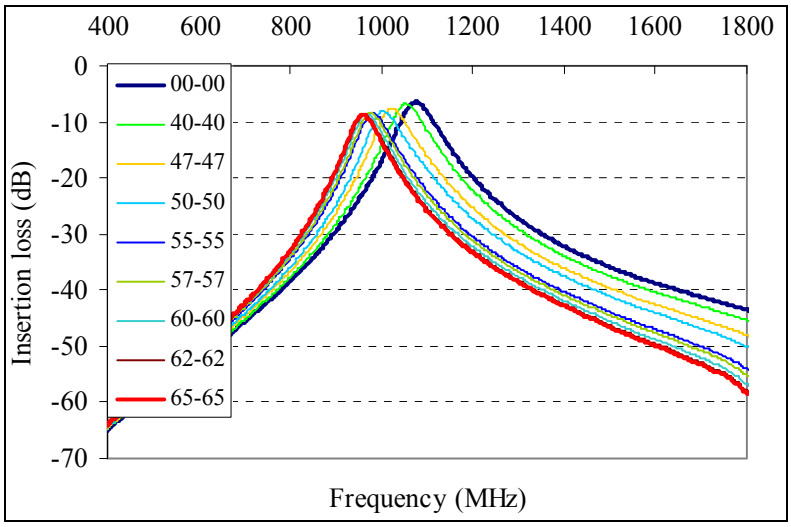


Figure 122: Measured tuning characteristic of the filter, showing a tuning of 123.5 MHz (11.5%) with the application of 65 V to the tunable silver capacitors.

To maintain the bandwidth constant, the same tunable termination concept introduced in Section 4.4.2.A can be applied. Figure 123 shows the measured response of the filter when terminated to 2000 Ω at 1075 MHz and to 750 Ω at 952 MHz. As shown, by tuning the termination impedance at the tuned state, a constant bandwidth of 63 MHz is obtained at both ends of the tuning range. In addition, the insertion loss is reduced to 7.6 dB at the tuned state, showing an improvement of 0.8 dB.

Measured characteristics of individual filter components are shown in Figure 124-Figure 126. Both the tunable and fixed capacitors exhibit a high embedded Q in excess of 200 at the center frequency of the filter. The quality factor of the inductor is 50 at 1.075 GHz, which is loading the insertion loss of the filter.

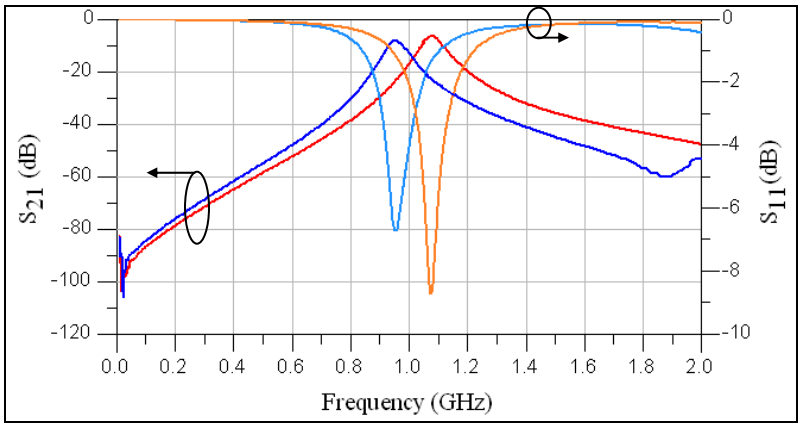


Figure 123: Measured S-parameter of the filter at the high and low end of the tuning range, showing that the bandwidth can be maintained constant by tuning the termination impedance.

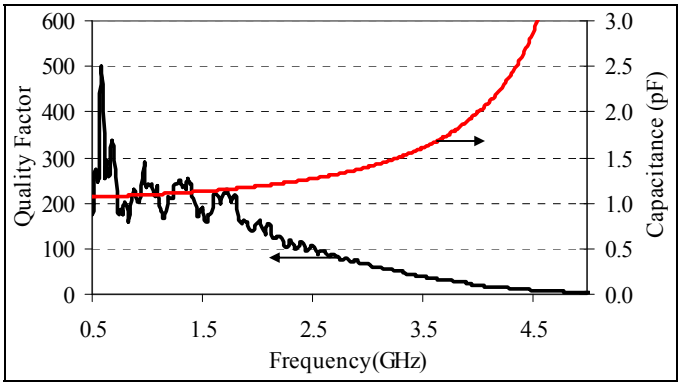


Figure 124: Measured embedded characteristic of the silver tunable capacitor, showing a *Q* of > 200 at the center frequency of filter.

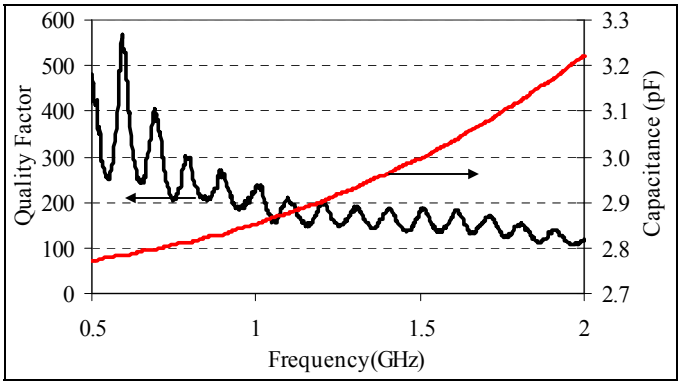


Figure 125: Measured characteristic of a 2.9 pF fixed capacitor incorporated in the filter.

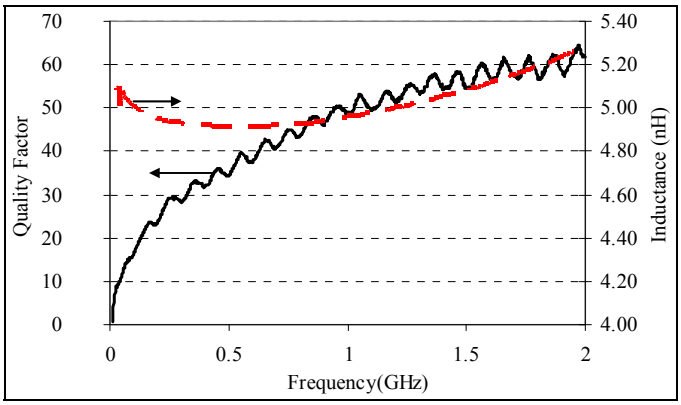


Figure 126: Measured characteristic of a 5 nH inductor incorporated in the filter.

Consequently, to achieve a high-performance tunable lumped filter the followings are the imperative requirements.

1) A competent design: when designing a MEMS tunable lumped filter, it should be remembered that the practical filter topologies are limited. This is mainly due to the restrictions posed by the realizable component values using microfabrication processes.

2) A high-accuracy electromagnetic simulation tool: here, we want to emphasize that running a simulation on the entire layout of a high-order bandpass filter even using advanced 3D modelers, such as HFSS, is not trivial. Thick and high-aspect-ratio MEMS components require a large number of meshes to be correctly modeled, resulting in an increased memory requirement. For example, the coupled-resonator filter presented in this chapter requires more than 30 GB of memory using the HFSS tool. Therefore, thoughtful trade-offs have to be made to perform the EM simulations, successfully.

3) An advanced micromachining technique: the process has to enable high-Q tunable passives components and low-loss interconnects. Therefore, the silver micromachining technique presented in this chapter is well-suited for the implementation of lumped tunable filters on chip.

CHAPTER 5

LOW-VOLTAGE LARGE-VALUE TUNABLE CAPACITORS USING SELF-ALIGNED HARPSS

Tunable filters in the low VHF region require large-value tunable capacitors to achieve a wide frequency tuning range. Large-value tunable MEMS capacitors can also find applications in energy harvesting systems [94]. Several designs of small-value micromechanical tunable capacitors have been reported in the literature, as discussed in Chapter 1. However, low-actuation voltage tunable capacitors with large values in small form-factors are yet to be shown. To achieve the highest-density capacitors, 3D interdigitated plates with narrow and high-aspect-ratio vertical gaps are needed. Monajemi et al. had previously reported on the application of the high-aspect-ratio polysilicon and single crystal silicon (HARPSS) fabrication technique [95] for the realization of high-Q low-voltage one-port capacitors on the silicon substrate [28]. In this technique, vertical gaps are defined between the polysilicon structures and silicon substrate by the deposition of a thermal oxide (sacrificial oxide) layer, and thus the gaps can be scaled to values less than 50 nm with aspect-ratios of more than 200 [96]. Hence, the HARPSS process is well-suited for the fabrication of high-value capacitors. However, the conventional HARPSS process does not offer different-size self-aligned narrow gaps between the polysilicon and single crystal silicon structures, which is a required feature for high-performance tunable capacitors. For this reason, we have developed a modified version of HARPSS, called the self-aligned HARPSS, to implement one-port and two-port tunable capacitors.

In this chapter, we first introduce the self-aligned HARPSS fabrication process, describing the details of the process parameters that need to be carefully characterized. Next, we discuss the design of one-port and two-port large-value HARPSS tunable

capacitors. We finally conclude the chapter by documenting the results that we have obtained for the fabricated devices.

5.1 Fabrication Process

Figure 127 shows the fabrication process flow of the self-aligned HARPSS process, which requires only three lithography masks [97]. In this process, the sub-micron high-aspect-ratio vertical capacitive air gap is defined by thermally growing a thin layer of sacrificial silicon dioxide. Wider vertical gaps of different sizes are defined by silicon nitride in a self-aligned manner. Silicon nitride is used as it acts as a mask during the thermal growth of silicon dioxide and is etched back from the surface at the final step to define the trenches in silicon.

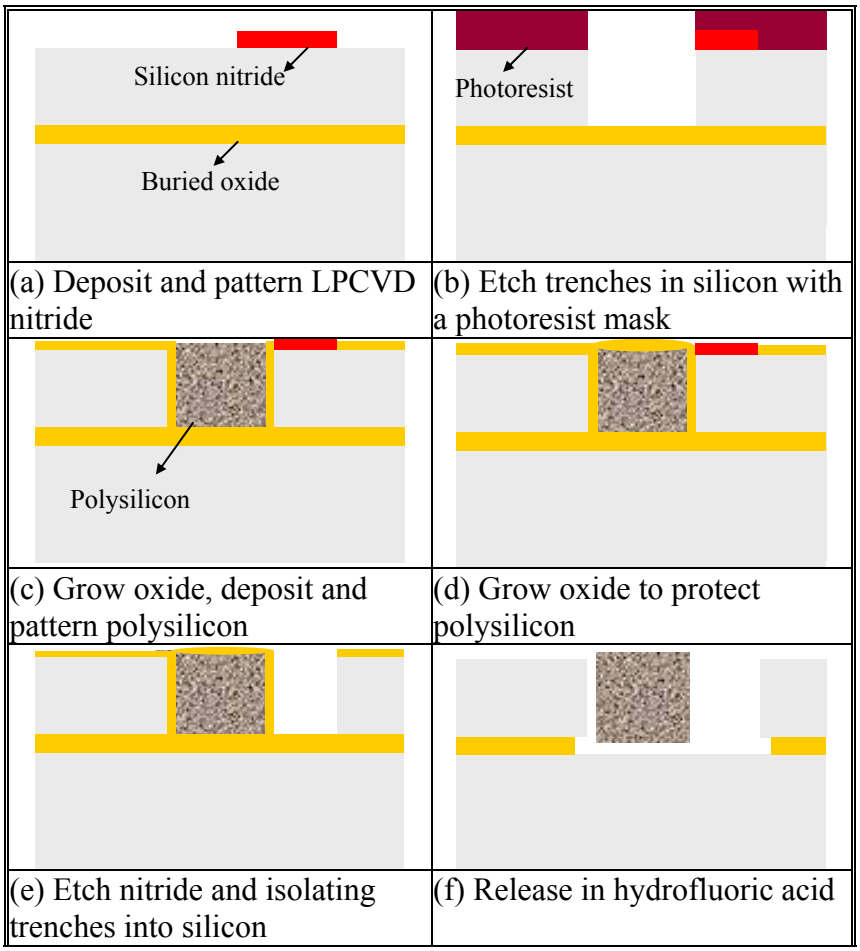


Figure 127: Fabrication process flow for the self-aligned HARPSS.

The process starts with the deposition and patterning of a 3000 A° low-pressure chemical vapor deposited (LPCVD) silicon nitride on a 60-80 μm thick SOI substrate (Figure 127 (a)). Next, deep trenches are etched into the device layer using the Bosch process and a photoresist mask (Figure 127 (b)). The photoresist is subsequently removed in a Pirhana solution. The thin layer of sacrificial silicon dioxide (< 1 μm) is then thermally grown at 950º C. The oxide growth temperature is reduced to minimize the stress. It is worth mentioning that the silicon nitride patterns introduce a significant amount of stress. Therefore, reducing the oxide growth temperature is crucial to the successful fabrication of the self-aligned HARPSS devices. Ideally, silicon nitride acts as a mask during the wet oxidation process. However, a thin layer of oxide grows underneath the edges of the nitride pattern, which is called the bird's beak effect [98]. The width of the nitride pattern defines the width of the trenches that are to be etched in the silicon device layer. The bird's beak effect results in narrowing of the trench width. If the nitride pattern width is not designed properly, this would cause difficulty when etching narrow trenches into the thick device layer. An example of the bird's beak effect is shown in Figure 128.

The trenches are then refilled with a LPCVD polysilicon layer, which is subsequently boron-doped and annealed. Annealing parameters of polysilicon heavily influence the residual stress of this film, which affects the performance of the movable structures, as discussed later in this chapter. Polysilicon is subsequently etched back from the surface and patterned using a photoresist layer as the mask (Figure 127 (c)). Over etching of polysilicon results in a disconnection between the polysilicon anchor and the beams, as shown in Figure 129.

A 1 μm thick silicon dioxide layer is grown to protect the polysilicon structures in the final silicon etching step (Figure 127 (d)). The silicon dioxide layer cannot be grown much thicker than 1 μm as it causes stress and impairs the performance of devices. Silicon nitride is then removed by reactive ion etching and the self-aligned isolating

trenches are etched into the device layer (Figure 127(e)). Since the initial thickness of the silicon nitride is chosen properly, it can be selectively removed without causing an excess reduction in the thickness of silicon dioxide. Finally, the devices are released in dilute hydrofluoric acid (Figure 127 (f)). Using this fabrication process, several one-port and two-port tunable capacitors are designed and fabricated.

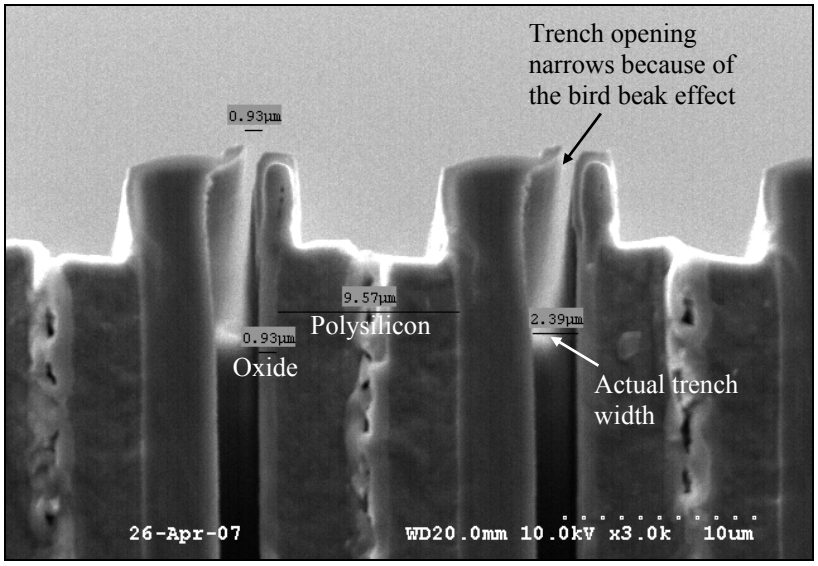


Figure 128: A SEM picture of the trench narrowing because of the bird's beak effect.

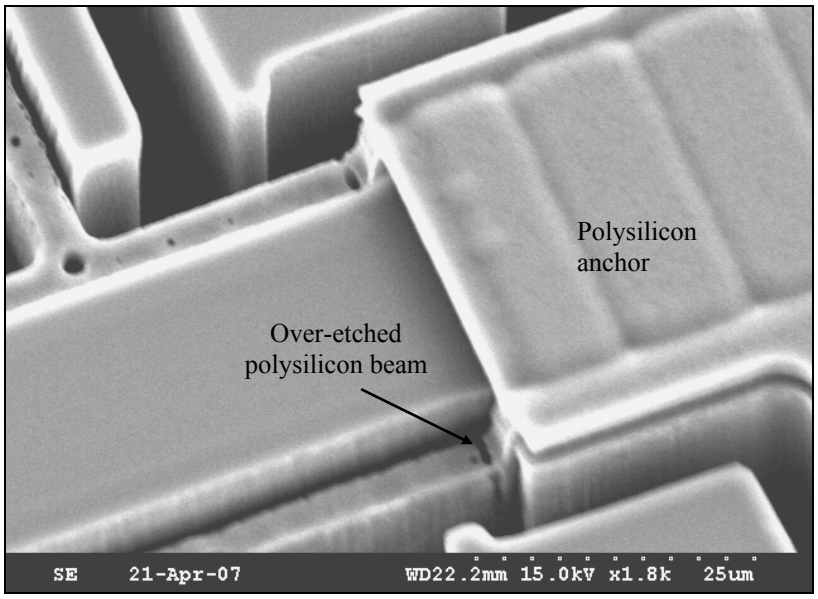


Figure 129: A SEM picture of the polysilicon beam, showing the over-etched beam has a loose connection to the anchor.

5.2 Capacitor Design

The sub-micron gap offered by the HARPSS process makes the realization of large-value capacitors as well as low-tuning voltage actuators possible. The schematic diagram of the two-port tunable capacitor is shown in Figure 130. To maximize the electrostatic tuning, the actuator is designed in a comb-drive and the capacitor is in a parallel-plate configuration. As discussed in Chapter 1, the tuning range of a comb-drive actuator is limited by the lateral snap-down of the interdigitated fingers. Yet, with a proper design, that is when the maximum travel range (x_{max}) is more than the parallel-plate capacitor gap, the tuning range is infinite.

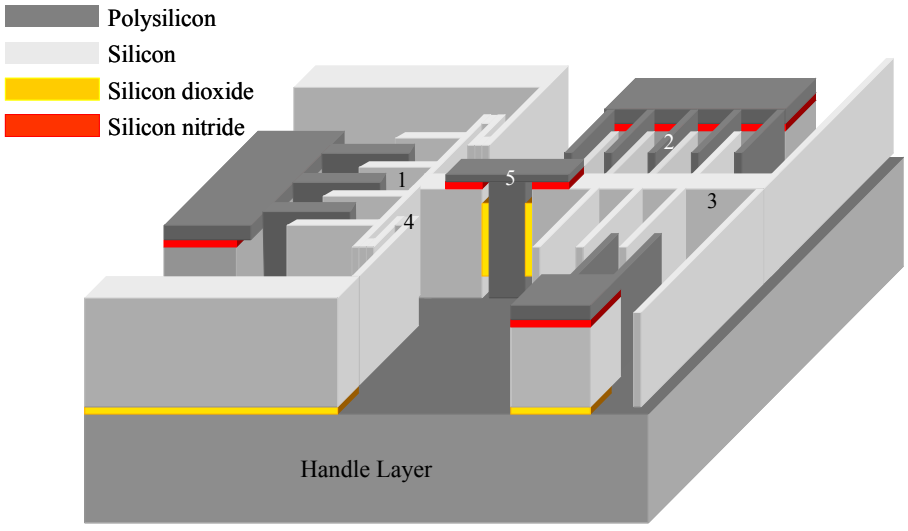


Figure 130: Schematic of the two-port tunable capacitor, showing 1: comb-drive actuator, 2: parallel-plate capacitor, 3: shuttle, 4: spring, and 5: polysilicon clamp.

The main challenge in designing a two-port HARPSS tunable capacitor is to electrically isolate the movable plates of the tunable capacitor from the actuator while maintaining a mechanical connection. This has been achieved using the self-aligned HARPSS fabrication process without any additional complexity. Such a connection is provided by a polysilicon clamp that is electrically isolated from both the capacitor and actuator using sacrificial oxide in the bulk and nitride on the surface (Figure 130). Figure

131 shows a SEM view of a two-port tunable capacitor. To minimize the sensitivity to the external acceleration, the capacitors are made symmetric about both x and y axes, as shown in Figure 131. If one-port capacitors are desired, the polysilicon clamp is not needed and a solid silicon shuttle connects the actuator to the parallel-plate capacitor, as shown in Figure 132. If otherwise stated, devices are fabricated on a 70 μm thick SOI substrate with a low resistivity of less than 0.001 Ω.

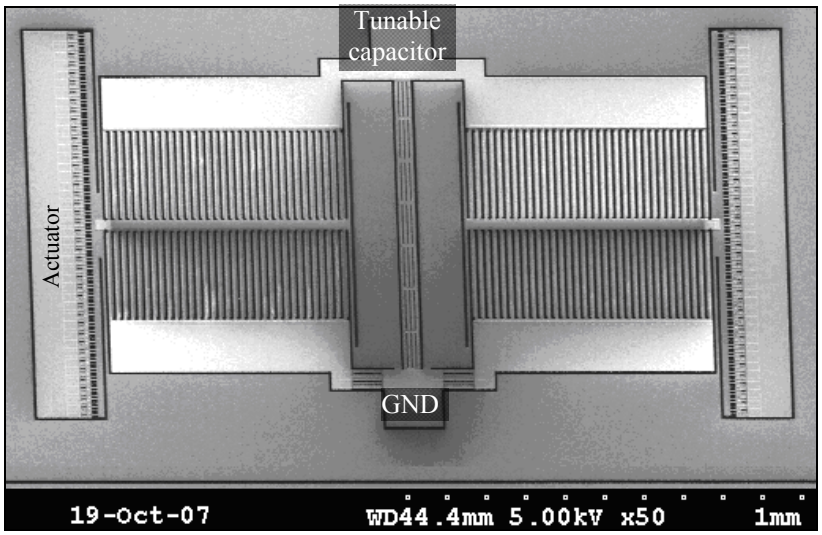


Figure 131: A SEM view of a 15 pF two-port tunable HARPSS capacitor.

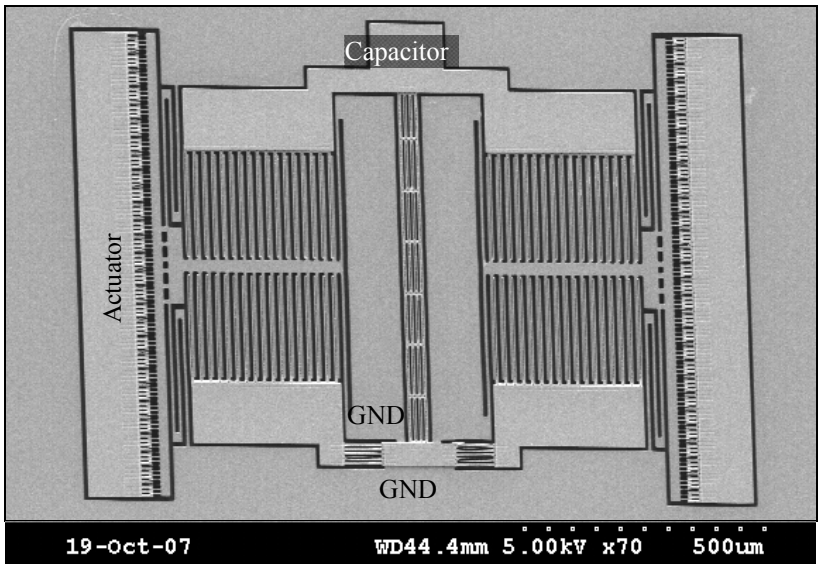
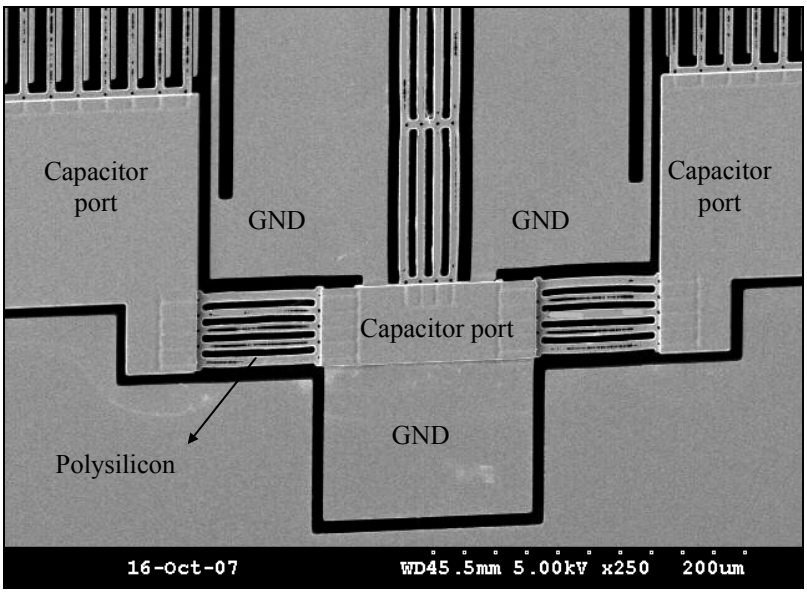
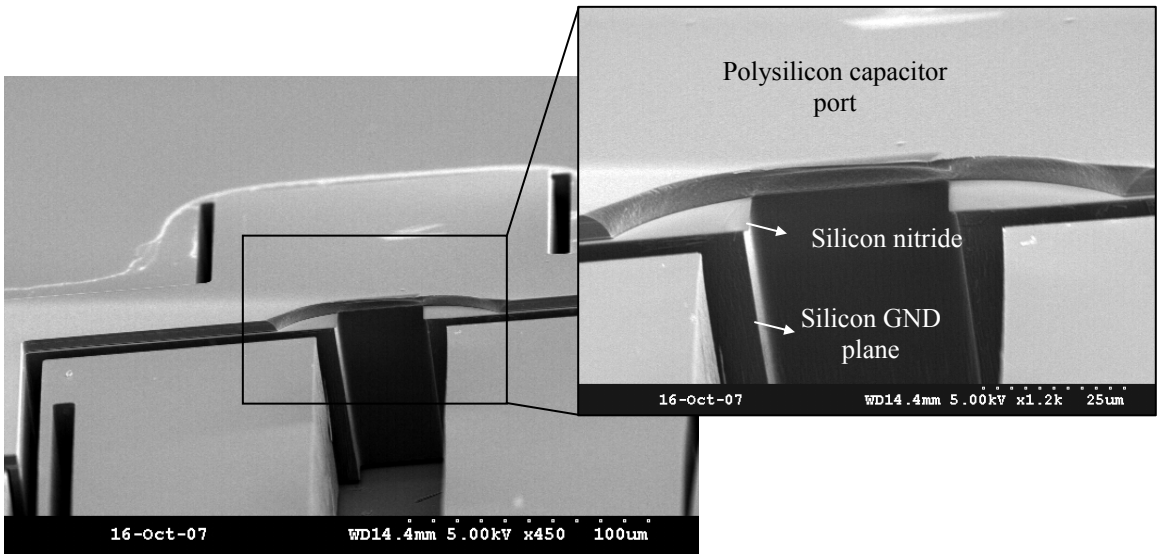


Figure 132: A SEM view of a one-port tunable HARPSS capacitor.

The top and the bottom plates of the capacitor are connected trough four polysilicon beams, while they are isolated from the silicon ground plane using the silicon nitride layer (Figure 131 and Figure 132). Close-up views of the isolation area are shown in Figure 133.



(a)



(b)

Figure 133: SEM views of the isolation area. The capacitor plates are connected using the polysilicon layer while electrically isolated from the ground using the silicon nitride layer.

It is worth mentioning that in the self-aligned HARPSS process, the polysilicon layer by no means has an electrical connection to the silicon device layer. More particularly, the polysilicon layer is either isolated from the silicon layer using thermal oxide or silicon nitride. Figure 134 and Figure 135 show the close-up views of the polysilicon clamp and the sub-micron capacitive gap, respectively.

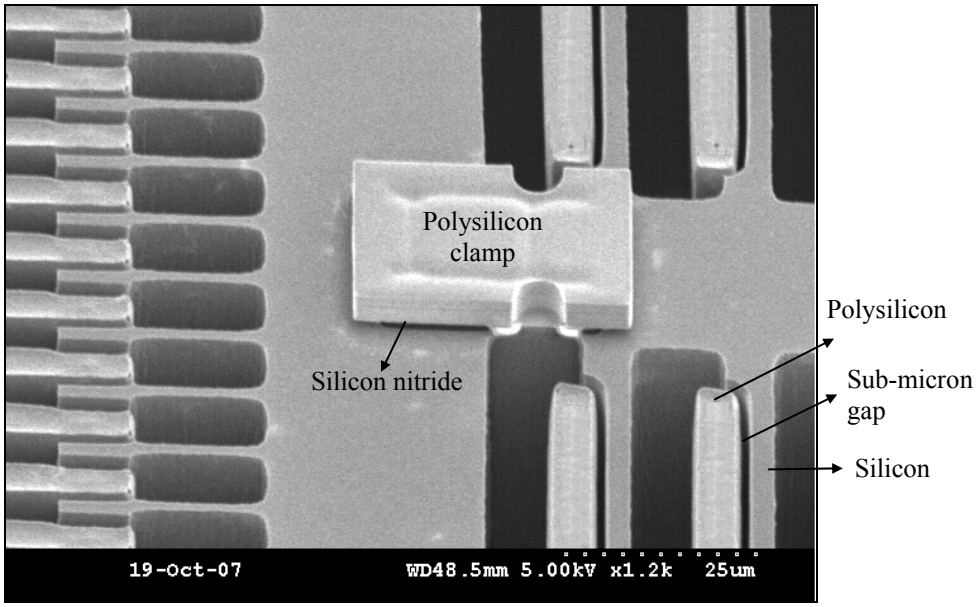


Figure 134: A SEM view of the polysilicon clamp.

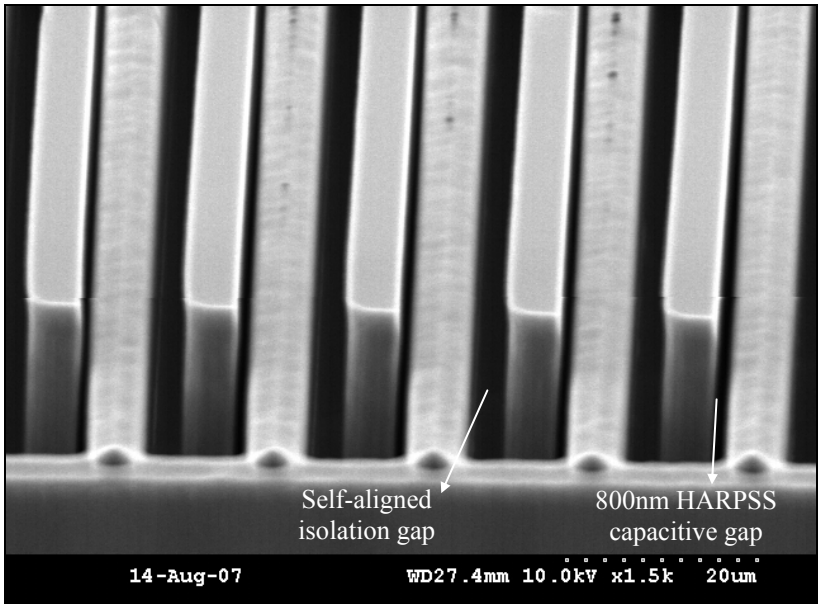


Figure 135: A close- up view of showing the 800 nm gap between the parallel-plate fingers.

The width of the polysilicon beams cannot exceed 8 μm as the thickness of the polysilicon layer that has to be deposited becomes impractical. Therefore, the polysilicon fingers and beams are designed with an aspect-ratio of less than 50:1. Here, the aspect-ratio is defined as the ratio of the length to the width of the beam. Polysilicon beams with higher aspect-ratios bend because of the residual stress. The same design constrain applies to the movable silicon shuttle. Long and narrow shuttles buckle down. In a case where the thickness of the buried oxide layer is not sufficient, the buckled silicon shuttle sticks to the handle layer, and the device fails. For these reasons, the implementation of higher value capacitors represents a challenge from a fabrication point of view.

5.3 Results and Discussion

DC tuning voltages are applied to the actuator and the capacitance values are measured at 2 MHz using an Agilent E4980A precision LCR meter. Figure 136 shows the measured C-V tuning curve of a 15 pF two-port tunable capacitor. As shown, this capacitor is continuously tuned to 51 pF with the application of 3.5 V. At higher tuning voltages, lateral snap-down of the comb-drive actuator occurs. The layout of the capacitor is simulated using the HFSS. Figure 137 shows the physical model of the capacitor along with the HFSS simulation results.

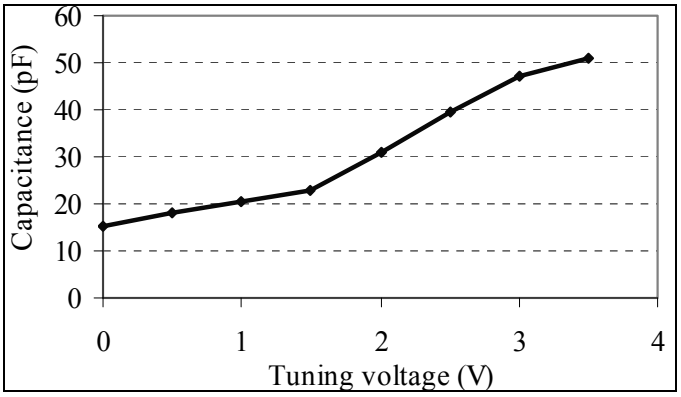
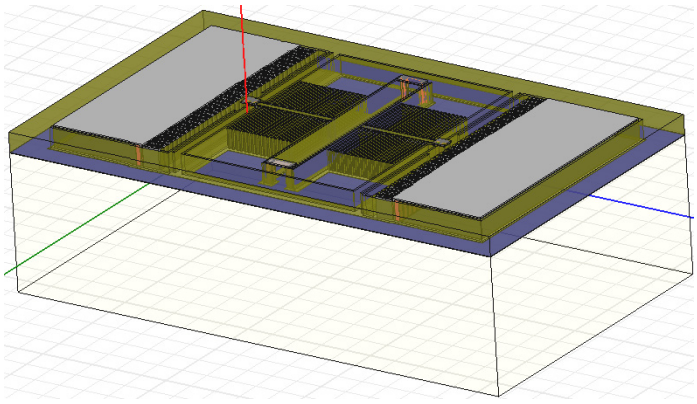
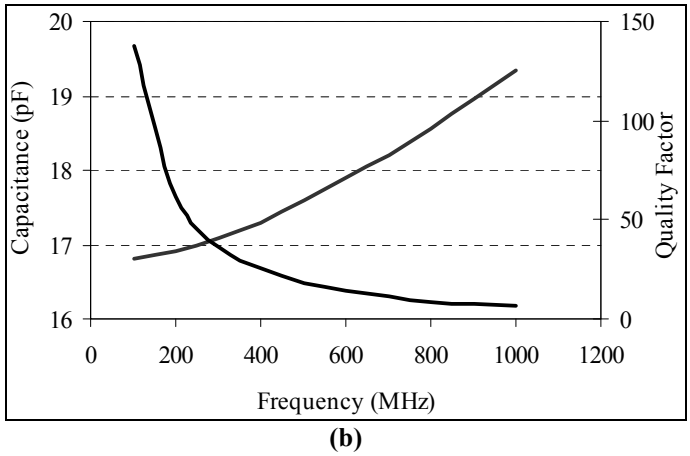


Figure 136: C-V tuning curve of a 15 pF two-port HARPSS capacitor, showing a maximum tuning of 240%.

In the simulations, the same resistivity of 0.001 Ω.cm is assumed for the polysilicon and silicon structures. The resistivity of polysilicon in the fabricated device is 0.04 Ω.cm, resulting in a lower measured *Q* than that predicted by the simulations. More accurately, the *Q* of the fabricated device is 40 times lower than expected. On the other hand, the measured capacitance value shown in Figure 136 is in good agreement with the simulated result shown in Figure 137 (b). To improve the *Q* of the HARPSS capacitors, the resistivity of the polysilicon capacitor plate needs to be reduced. This can be achieved by using a lower resistivity boron source when doping the polysilicon layer. Another approach to increase the *Q* of the HARPSS capacitors is depositing a thin metal layer after the HF release step [28].



(a)



(b)

Figure 137: (a) 3D HFSS model and (b) simulation results of the 15 pF tunable capacitor shown in Figure 131.

As discussed earlier, the implementation of larger value capacitors becomes more challenging as the movable shuttle gets longer, and the possibility of its stiction to the handle layer is higher. The residual stress in the polysilicon is also more pronounced in larger devices, leading to the bending of structures, which hampers the device performance. An example of a failed device is shown in Figure 138. As shown, the excess stress in the polysilicon resulted in bending of the parallel-plate fingers and the polysilicon spring.

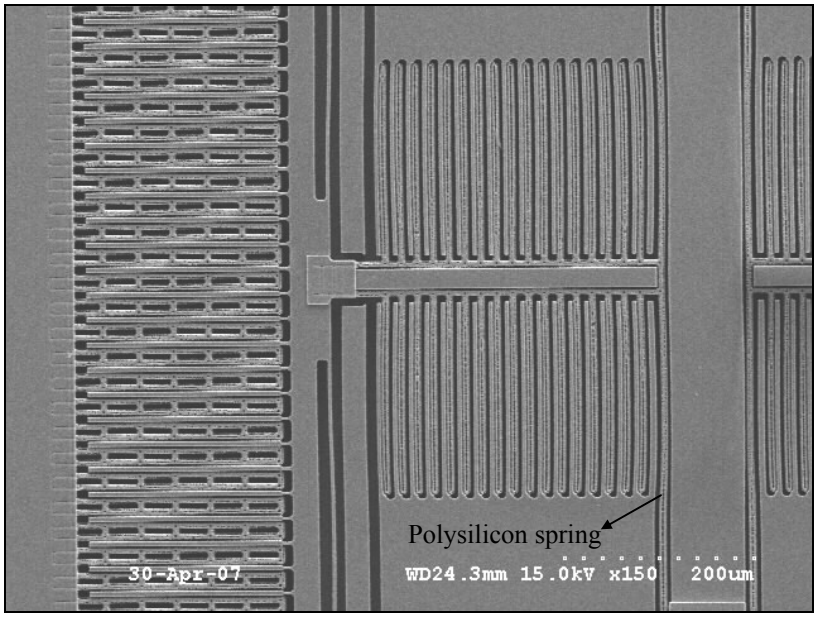


Figure 138: A SEM picture of a failed sample. The fingers and the polysilicon spring are bent due to the excessive stress of the polysilicon.

Another consequence of a high level of stress is shown in Figure 139. The deposition of the polysilicon layer in the deep high aspect-ratio trenches is not fully conformal, resulting in the formation of a void in the refilled trench [99]. In most cases, this void does not affect the performance of the device. However, if the stress in the polysilicon layer does not moderate during the annealing process, the void can open up during the HF release step, and the divided polysilicon beam sticks to the adjacent silicon structure (Figure 139). Therefore, controlling the deposition and annealing parameters

(pressure, gas flow rate, temperature, and time) of the polysilicon is crucial to the successful fabrication of large-value capacitors.

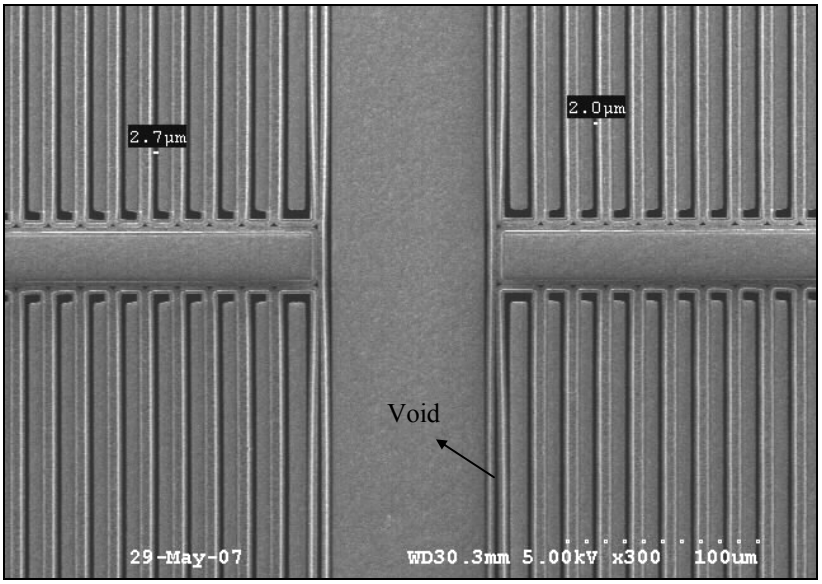


Figure 139: A SEM picture of a failed sample. The void in the beam has opened because of the excessive stress of the polysilicon.

By characterizing the process parameters, a 32 pF and a 106 pF tunable capacitor are successfully fabricated. The tuning curve of the 32 pF two-port tunable capacitor is shown in Figure 140. A maximum capacitance change of 218 % is observed for this capacitor with a tuning voltage of 6 V.

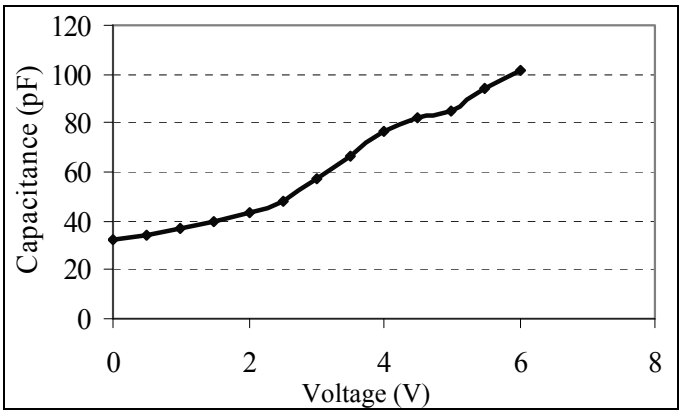


Figure 140: Tuning curve of a 32 pF two-port HARPSS capacitor, showing a maximum tuning of 218%.

Figure 141 and Figure 142 show the tuning curves of the actuation port and the parallel-plate port of a 60 μm thick 106 pF one-port tunable capacitor, respectively. As expected, the comb-drive capacitance changes linearly with the applied DC voltage. The large parallel-plate capacitor varies over 23.5 pF by the application of 0.9 V. The self-actuation (i.e., parallel-plate actuation) of the capacitor requires a five times higher voltage compared to the one required for tuning the capacitor (i.e., comb-drive actuation). This capacitor occupies 8 mm × 1 mm of die area (shown in Figure 143) and can be further reduced in size by increasing the aspect-ratio of the capacitive gap, which is feasible using the self-aligned HARPSS process.

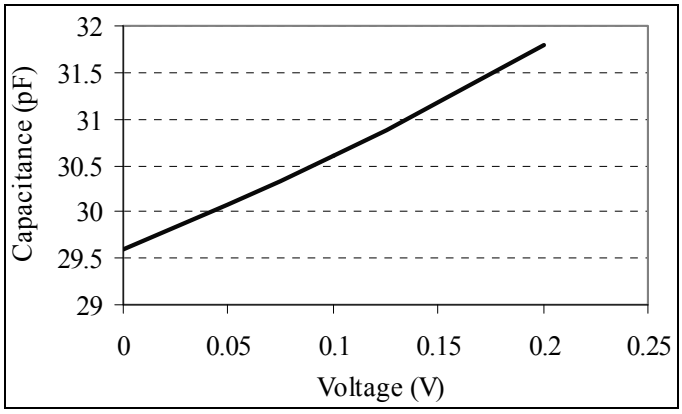


Figure 141: Tuning curves of the actuation port of a 60 μm thick 106 pF tunable capacitor.

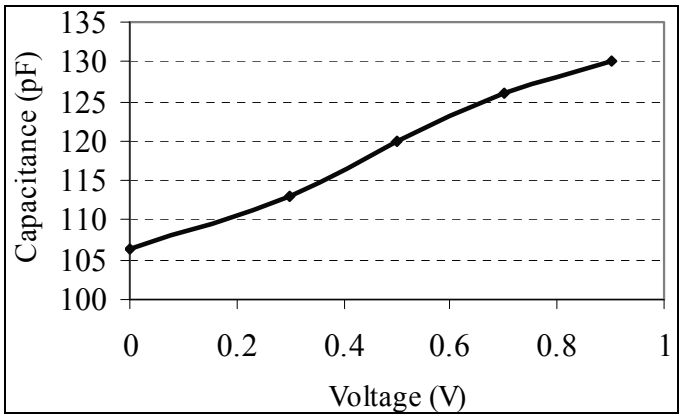


Figure 142: Tuning curves of the parallel-plate sense port (self-actuation) of a 60 μm thick tunable capacitor, showing a capacitance change of 23.5 pF.

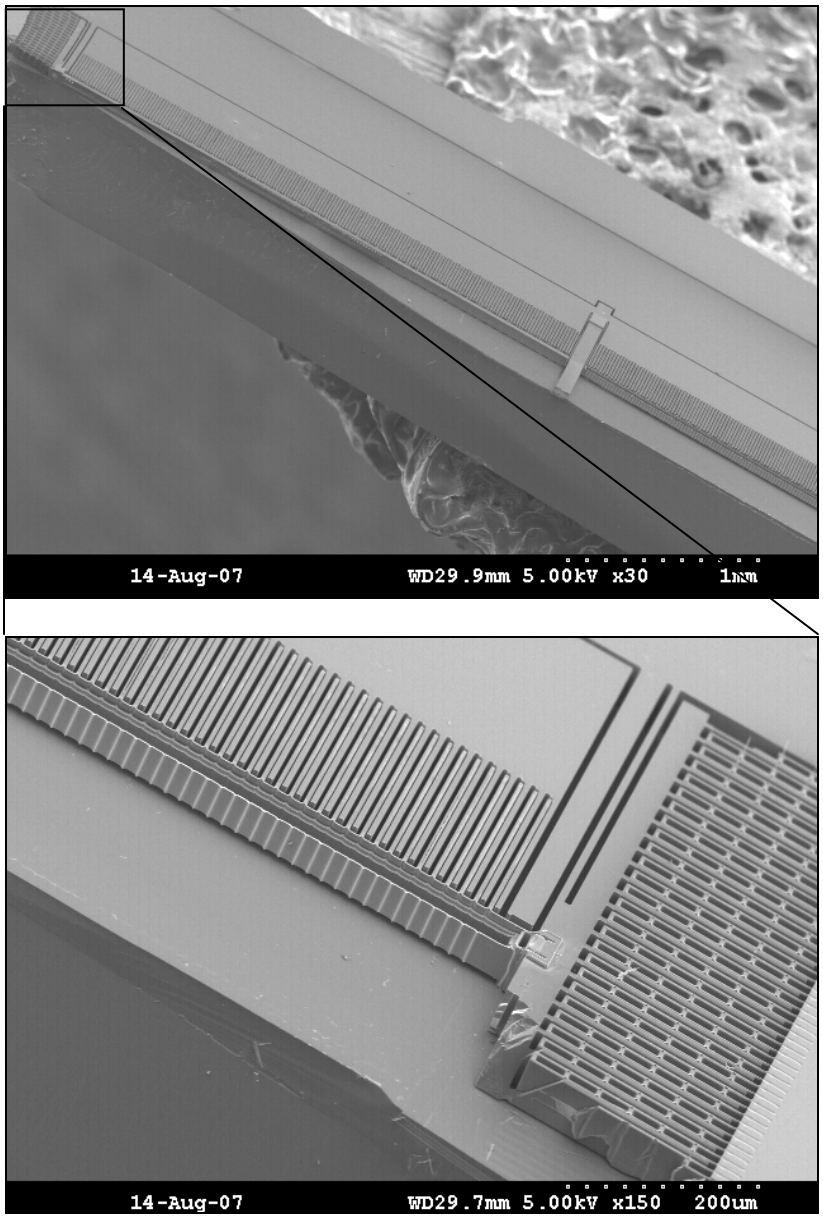


Figure 143: SEM views of a broken capacitor, showing the 60 µm thick device on a SOI substrate.

Although the polysilicon deposition and annealing parameters are characterized for minimal stress, the polysilicon fingers are not perfectly straight due to the slight residual stress in the polysilicon layer. This is the main issue that impedes an ideal tuning of the large comb-drive actuator.

To appreciate the low tuning voltage of the HARPSS actuator, a one-port capacitor is designed with a lithographically defined parallel-plate actuator (Figure 144).

In this design, the movable capacitor and actuator plates are connected to the ground plane through the springs. The close-up SEM view shown in Figure 145 compares the sub-micron HARPSS gap with the lithographically defined capacitive gaps at the actuator slide.

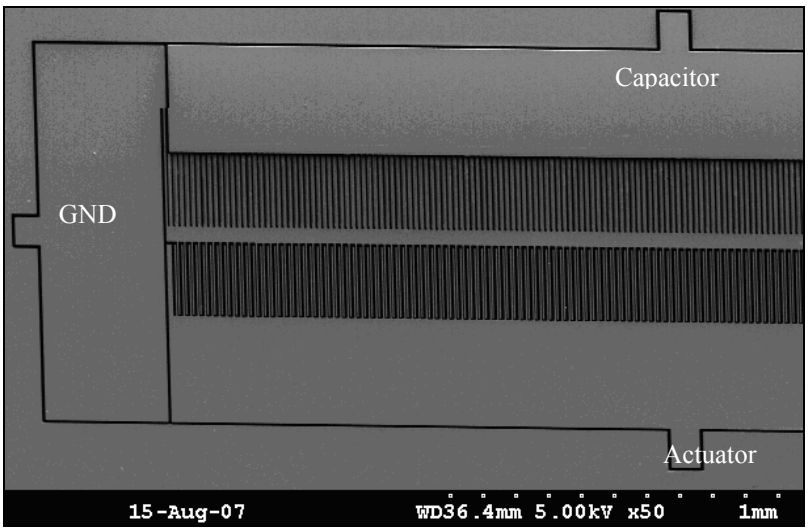


Figure 144: A SEM view of a one-port HARPSS tunable capacitor with a lithographically defined parallel-plate actuator.

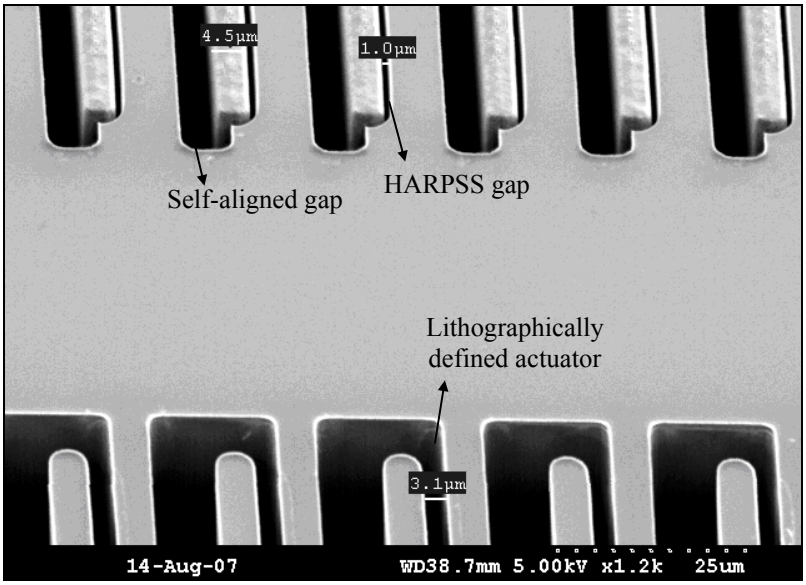


Figure 145: A close-up SEM view of the one-port HARPSS tunable capacitor with a lithographically defined parallel-plate actuator.

Figure 146 shows the tuning result obtained for the large-value capacitor of Figure 144. Compared to the low tuning voltages obtained for the parallel-plate HARPSS capacitor, the tuning voltage of the lithographically defined actuator has significantly increased to more than 25 V, which is due to a larger gap and a lesser actuator capacitance density.

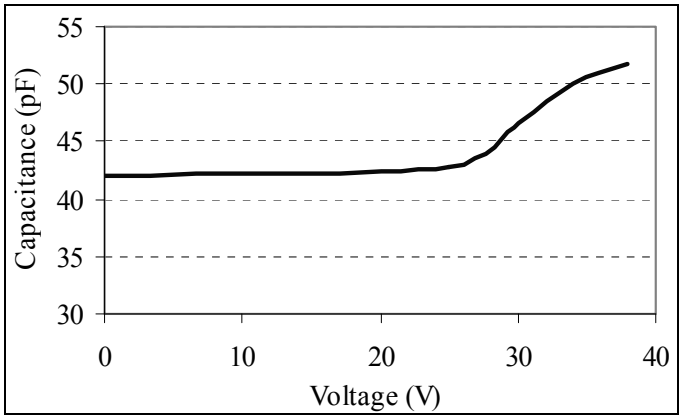


Figure 146: C-V tuning curve of a 42 pF one-port HARPSS capacitor with a lithographically defined parallel-plate actuator. The tuning voltages are high as a result of a larger actuation gap.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

The goal of this dissertation was to present high-performance tunable MEMS passives for RF integrated circuits and to address the challenges involved with the realization of a low-loss narrow-band tunable bandpass filter on CMOS-grade silicon substrate. We present conclusions of this work in Section 6.1, and in Section 6.2, we provide directions for the future research in the area of tunable lumped integrated MEMS filters.

6.1 Conclusions

In this dissertation, we addressed the lack of low-loss integrated passives and bandpass filters on CMOS-grade silicon and presented the first demonstration of an integrated narrow-band (< 5%) tunable micromachined lumped filter in the UHF range. To achieve a high-performance filter in the frequency range of 30 MHz- 3 GHz, the main issue had been the insufficient quality factor of the on-chip lumped components. Prior work had demonstrated high-Q components on low-loss substrates, such as organic substrates, high-resistivity silicon, and glass. However, the poor performance of passive components on CMOS-grade silicon had remained a challenge that had impeded the realization of a narrow-band filter with a low insertion loss, which could be monolithically integrated with the CMOS circuitry. In this work, we devised a new micromachining technique that offers record high-Q inductors and tunable capacitors by minimizing both the high-frequency loss of silicon and the ohmic loss of the metal layers. In this process, we exploited silver, which has the highest conductivity of all metals, and we selectively removed the substrate to achieve a kind of performance that had not been obtained using the reported fabrication processes.

In addition, we demonstrated that the parasitics of interconnects have a significant contribution to determining the frequency response of the filter. The parasitic issue becomes particularly important for lumped filters in the VHF and UHF range, which employ bulky lumped components. For these filters, the length of interconnects become considerable and the effect of interconnects on the filter performance becomes significant. We showed that attaining a high-performance micromachined filter not only requires high-Q components, but also necessitates a systematic layout. This can only be accomplished using high-accuracy electromagnetic simulation tools, which had not been available until recently. In spite of that, the memory requirement to perform a thorough simulation on the physical layout of a MEMS filter is immense, and such simulations are computationally intensive. As a result, the lack of an accurate electromagnetic modeling/simulation tool presented a challenge to the design of the lumped filters.

There are several other challenges involved with both the design and the fabrication of micromachined narrow-band tunable filters and high-Q lumped components. For instance, the frequency characteristic of the narrow-band filters is heavily influenced by the filter configuration. Different filter topologies offer different advantages, and one can decide on the best-suited filter topology based on the filter requirements for a particular application. However, the choices are limited when designing a MEMS lumped element filter. This is mainly due to the restrictions posed by the realizable component values using micromachining technology. Furthermore, nano-precision fabrication techniques that can offer low actuation voltage MEMS tunable capacitors and/or switches in high yield and small area need to be developed. Equally important is the thin-film packaging of the silver microstructures, which represents a significant challenge to the realization of reliable MEMS solutions. To address these challenges, the following research directions are recommended.

6.2 Future Research Directions

6.2.1 Quality Factor Improvement

6.2.1.A Fabrication

In this dissertation, we employed a silver micromachining technique to achieve high-Q integrated passives. Although we obtained record high-Q inductors and low-loss bandpass filters using this process, there is room to further improve the performance of the silver components. The multi-turn spiral inductors, tunable inductors, and MIM capacitors presented in this thesis were fabricated with a relatively-thin routing layer, which is a major contributing factor to the metal loss. The ongoing research regarding the fabrication includes the application of several thick electroplated layers to reduce the ohmic loss of the passive components and to improve the Q. It should be noted that there are several challenges involved with thick multi-level electroplating as it adds to the fabrication complexity. An issue with a thick routing layer is the uneven surface profile. If the first metal layer (routing layer) was thick, the substrate has to be planarized with a thick sacrificial layer prior to the deposition of subsequent layers. This sacrificial layer must have a proper adhesion to the electroplated silver layer as well as the subsequent layers. In addition, the sacrificial layer has to be selectively removed in the final step without causing an excess reduction in the thickness of the electroplated silver. Hence, future research involves material characterizations and new process developments.

6.2.1.B Design

In addition to the fabrication development, the physical layout of the components can be improved for a higher quality factor. Future research in this area includes the use of lower-loss structures, such as solenoids and toroids, to substitute the in-plane spiral inductors used in this work. In addition, one can employ a lower loss tangent material (e.g., a low-loss polymer) as the capacitive dielectric for the MIM capacitors to enhance

the performance of these devices. Accordingly, the electrical and mechanical properties of the new materials have to be obtained from the fitted models and the physical layout of the capacitors needs to be optimized.

6.2.2 Tuning Range Improvement

As discussed in Chapter 4, because of the low capacitance density of the silver tunable capacitors, a fixed MIM capacitor was connected in parallel to the tunable capacitor to obtain the required capacitance value. Therefore, although the tunable capacitors exhibited reasonable tuning (> 2:1), the effective tuning of the overall capacitor was insufficient, limiting the frequency tuning of the bandpass filters. In Chapter 5, we showed several high-density low-actuation voltage HARPSS tunable capacitors that can be potential candidates for tunable filters. However, the quality factor of the HARPSS capacitors in the UHF range is not sufficiently high. To enhance the tuning characteristics of the filters, both high-Q and high-aspect-ratio lateral capacitors should be developed. Therefore, another avenue for future research is combining the HARPSS process with the silver micromachining technique for the realization of a high-value integrated tunable capacitor with a low loss.

In this thesis, we used the electrostatic actuation mechanism to tune the capacitors and accordingly, the filters. Although electrostatic actuation offers several advantages, the tuning voltages obtained for the silver capacitors using the electrostatic actuation were relatively high. Future research can include the use of different actuation mechanisms for the tunable capacitors, switches, and inductors to lower the actuation voltages and to improve the tuning range of the filters.

Another research topic that we did not investigate in this thesis is the use of tunable inductors in the bandpass filters to achieve a broader frequency tuning. As discussed in Chapter 2, the silver micromachining technique presented in this work enables simultaneous fabrication of the switched tunable inductors and lateral tunable

capacitors. Therefore, one can study the design of a tunable filter that employs both the switched tunable inductors and the tunable capacitors, fabricate the filters using the silver micromachining technique, and investigate the frequency characteristics of the filter.

6.2.3 Antenna Matching

In Chapter 3, we demonstrated an array of fixed-frequency bandpass filters for the applications that require filtering closely located signals. We developed the layout of the array considering the envisioned position of the antenna, and we successfully fabricated the filters. However, it should be noted that a matching network is required before these filters can be connected to the same node and to the antenna. This matching network has to be optimized such that each filter has a minimal effect on any other filter and yet, be properly matched to the antenna. The design and implementation of the matching network is another research topic that is initiated from the work presented in this thesis.

6.2.4 Encapsulation Technique

In this dissertation, we employed a wafer-level encapsulation technique to protect the silver microstructures from fatigue and dendrite failure. We showed that the insertion loss performance of the fixed-frequency filters and the quality factor of the inductors did not change after the encapsulation process was completed.

The reliability of wafer-level encapsulated tunable MEMS capacitors and switches is a topic that we did not study in this work. Packaging and reliability issues have been major bottlenecks in successful commercialization of micromechanical devices. Thus, an imperative future research is to further investigate the effect of the encapsulation scheme used in this work, to study the reliability of the silver tunable filters, and to develop aging models that are not currently available for these devices.

In summery, in this thesis we addressed some of the challenges involved with the integration of high-performance tunable filters on silicon. We also described the

challenges that are yet to be overcome before tunable MEMS filters become viable solutions to RF microsystems.

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