Design and Fabrication Considerations in Developing High-Q MEMS Capacitors and Inductors

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***Abstract* — Despite great advancement in micromachining techniques, design and fabrication of high-Q tunable capacitors and inductors remain to be a challenging task. This paper discusses the design and fabrication considerations in developing high-Q fixed and tunable micro-electromechanical capacitors and inductors. Electrostatic actuation mechanism is employed for tuning the value of passives. The measurement results of several high-Q capacitors and inductors fabricated on silicon substrate are presented, and a number of research directions to improve the performance of tunable passives are proposed.**

***Index Terms* — Passives, quality factor, tunable capacitor, tunable inductors**

I. Introduction

Continuously tunable micro-electromechanical systems (MEMS) and micro-machined passives (i.e., inductors and capacitors) are critical elements for miniaturized low-power cognitive radios. Based on their actuation type, tunable passives can be classified as: electrostatic, thermal, piezoelectric, or magnetic. Among them, electrostatic actuation can offer the highest actuation speed and the lowest DC power consumption. In addition, the biasing network of electrostatic actuators is relatively straightforward. As such, there has been extensive research on developing electrostatically tunable passives and particularly capacitors and several devices with wide tuning range have been reported in the literature [1] – [3]. However, for successful insertion of these devices into RF systems, several other performance aspects of the device are equally important and need to be addressed; some or none of which is considered for most reported tunable capacitors. These include quality factor (Q), self-resonance frequency (SRF), temperature stability, travel range, power handling, tuning speed, and tuning linearity. Development of a continuously tunable inductor that satisfies all of the above mentioned criteria has been even more challenging. Therefore, most reports are focused on discrete tuning mechanisms for altering the inductance value [4]. This paper presents the design and fabrication considerations in developing high-performance continuously tunable capacitors as well as tunable inductors with emphasis on the electrostatic actuation scheme.

On the other hand, the size and the low-Q of fixed inductors have been the major barriers in increasing the performance and reducing the size of RF integrated circuits (RF ICs) such as filters, voltage controlled oscillators (VCOs), and power amplifiers (PAs). Several researchers proposed inductor-less approaches to reduce the size of these modules at the cost of increased power consumption and reduced dynamic range and linearity. This paper presents a detailed analysis of the loss mechanisms that limit the quality factor of lumped passives on silicon. The measurement results of a number of high-performance fixed inductors are also presented in this paper.

II. Quality Factor

Three major loss mechanisms limit the Q of passives, the resistive loss of the conductor lines, the substrate loss, and where applicable the loss of the inter-layer dielectrics. Therefore, the Q can be defined as

$$\frac{1}{Q} = \frac{1}{Q_{metal}} + \frac{1}{Q_{substrate}} + \frac{1}{Q_{dielectric}}. \quad (1)$$

The dielectric loss is the result of dissipations associated with damping of the vibrating dipole moments [5]. Such dissipations are usually formulated using loss tangent ($tan\delta$), which is equal to

$$tan\,\delta = \frac{\omega\varepsilon'' + \sigma}{\omega\varepsilon'}, \quad (2)$$

where ω is the angular frequency; ε' is the real part of the dielectric constant most commonly referred to as the dielectric permittivity; ε'' is the imaginary part of the dielectric constant and is a measure of dipole loss. Using a dielectric with small loss tangent, such as aluminum oxide, parylene, or thermally grown silicon dioxide, the dielectric loss is small and can be neglected.

The substrate loss is the limiting loss mechanism at high frequencies. At these frequencies, induced currents in the substrate limit the $Q_{substrate}$ by converting the electromagnetic energy into heat [6]. In dielectrics and high-resistivity semiconductors, the dipole loss is the determining loss mechanism. In low-resistivity substrates such as CMOS-grade silicon, the electrically-induced current dominates over the dipole loss. In case of inductors, creation of a magnetically induced eddy current at high frequencies in low resistivity substrates further reduces the $Q_{substrate}$. The substrate loss can be substantially reduced by removing the substrate and

leaving the device suspended on an air cavity. Perhaps, implementation of suspended passives has been the major motivation behind using micromachining techniques for RF MEMS devices. Other approaches to reduce the substrate loss mainly involves reducing the loss tangent of the substrate through employment of a thick passivation layer, partial removal of the substrate [6], or use of lower-loss substrates such glass. It is worth mentioning that for the substrate, a low permittivity material is preferred to reduce the capacitive parasitics to the ground.

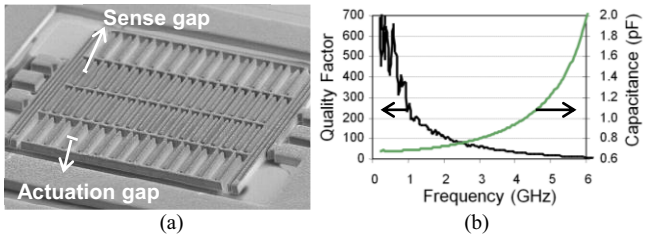
Reducing the conductor loss is more challenging as all materials have a limited electrical conductivity resulting in a limited Q for lumped passives at low frequencies. At high frequencies, skin and proximity effects further increase the resistance by reducing the effective area in which the current can flow [5]. In addition, for conductor lines with closely located ground plane (microstrip type lines), the current recedes to the bottom surface of the conductor making it ineffective to increase the thickness of the line beyond twice of the skin depth for reduced resistive loss. A uniform distribution of current can be achieved across the height of the conductor by properly engineering the position of the conductor relative to ground [6]. Therefore, it is possible to achieve very small resistances by employing high conductivity metals (such as silver, copper and gold) and scaling the conductor thickness into the third dimension. This calls for a fabrication technique which offers thick high-conductivity metal structures. Electroplating is commonly used to create thick metallic structures as it offers a fast deposition rate compared to sputtering or evaporation and results in a smaller residual stress in the metal layer. A fabrication process that includes thick metal electroplating steps together with bulk micromachining of the silicon substrate can enable the implementation of high-Q passives as well as low-loss interconnects providing the ultimate solution to the performance issues associated with the limited Q of lumped passives in RF ICs.

The fabrication technique considered herein is a thick silver micromachining technique first introduced in [7]. In this process, silver is employed as the structural material as it possesses the highest electrical conductivity of all metals and has a relatively low Young's modulus (for reduced bias voltage). Silicon is removed from the backside. The passivated silicon layer is retained beneath the anchors to provide a firm mechanical support. In this process, thick silver electroplating is the last metallization step. Two other metal layers are available for routing and creating fixed or vertically movable tunable capacitors as well as switches. As will be shown, high-performance tunable capacitors as well as tunable inductors can be simultaneously realized using this process.

III. Tunable Capacitors

Continuously tuned capacitors can reduce the size of multi-band radios by eliminating many of the redundant components, resulting in a drastically smaller form factor and reducing the bill-of-materials. Compared to switched tunable capacitors with two capacitance states, the design of continuously tunable capacitor is more challenging as it is more difficult to precisely control the gap or the area between the capacitor plates. In addition, the power handling of continuously tuned capacitor depends on the capacitance state and is much lower than switched tunable capacitors. The significant advantage of continuously tuned capacitor is that the capacitor value can be adjusted to account for fabrication inaccuracies. In addition, any given capacitance value can be achieved within the capacitor tuning range. This becomes important when employing the capacitor in a tunable filter that needs to select or reject a signal whose frequency is not known in advance.

Compared to area tuning capacitors, gap tuning capacitors can be realized in a smaller chip area. To avoid the pull-in effect in gap tuning capacitors, dual-gap actuation scheme can be employed [1], [7]. The capacitors discussed in this paper are all continuously tunable and are designed in dual-gap configuration. Fig. 1(a) shows a SEM view of a laterally movable parallel-plate capacitor. The actuation gap of this capacitor is three times the sense gap. A larger ratio of actuation to parallel-plate sense gap yields higher tuning linearity but requires larger tuning biases for the same capacitance value [1]. The capacitor exhibits a tuning of 3.3:1 with the application of 100 V. The frequency characteristic of the capacitor is shown in Fig. 1(b). With minor design modifications, the capacitor can be implemented in a two-port configuration, as shown in Fig. 2(a). In this configuration, the actuator and RF ports are electrically isolated while mechanically coupled using a small piece of silicon dioxide [8]. The C–V tuning curve of the two-port capacitor is shown in Fig. 2(b).

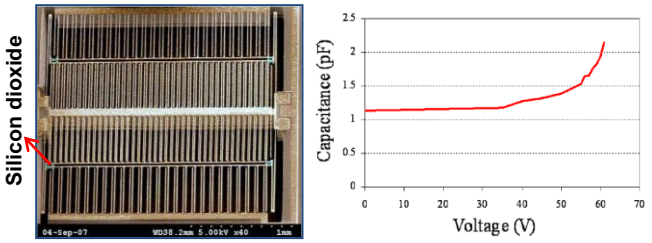


(a) (b)

Fig. 1. (a) A SEM view and (b) measured characteristics of a 40 μm thick one-port silver tunable capacitor designed in dual-gap configuration.

Thick silver micromachining technique can provide high-value and high-Q tunable capacitors. However, the tuning speed of these capacitors is low (less than 1 kHz) because of the large mass of the device. Using smaller

gaps and thinner (or higher aspect ratio) metal layers, the tuning speed can be significantly improved.



(a) (b)

Fig. 2. (a) A SEM view and (b) measured tuning curve of a laterally movable two-port silver tunable capacitor designed in dual-gap configuration. Silicon dioxide (in blue) is used to isolate the actuator.

Fig. 3 shows a SEM view of a vertically tunable dual-gap capacitor that is designed for fast tuning stabilization (< 50 µsec) using a dual-gap configuration with gap ratio of 4:1 (RF capacitor gap=0.5µm; actuation gap =2µm). The mechanical design of the membrane and springs is optimized to overcome the warping issue due to residual stress and temperature variation, while maintaining a pull-in voltage below 30V. Using this design, a wide tuning range of 5:1, high Q exceeding 100 (at 1GHz) at each tuned state, and SRF of more than 13.5 GHz is achieved. The temperature stability of capacitance is better than 7%. Detail design of the capacitor is given in [9].

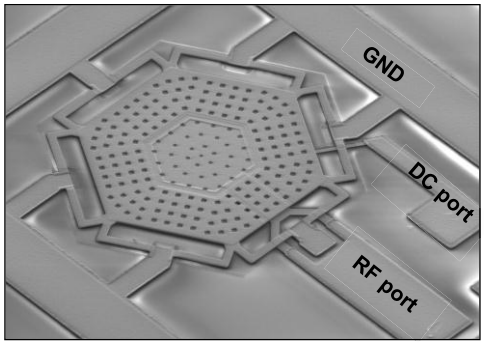


Fig. 3. A SEM view of a vertically tunable dual-gap capacitor.

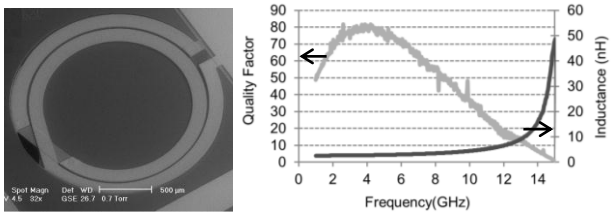
IV. Fixed Inductors

Fixed inductors can be designed in in-plane (spiral) or out-of-plane (toroid, helical) configuration. Out-of-plane inductors can potentially exhibit higher Qs as their magnetic field is parallel to the substrate. However, the fabrication and packaging process of out-of-plane inductors is significantly more complex. Conversely, the magnetic field of spiral inductors penetrates directly through the substrate resulting in increased substrate loss but their fabrication process is straight forward. The inductors presented in this work are designed in symmetrical spiral configuration [8] as they can be co-fabricated with the presented tunable capacitors. As mentioned earlier, to efficiently reduce the substrate loss, silicon is selectively removed from the backside but the passivation layer is retained beneath the inductors to provide a firm mechanical support.

Given a specific inductance value, the design of the inductor is optimized for the highest Q at the frequency range of interest. The dependency of the Q, SRF, and inductance value on geometric parameters is as following:

1. With increasing the conductor line width, the Q increases, the inductance slightly reduces and the SRF shifts to the lower frequencies because of the increased capacitive parasitics to the substrate.
2. With increasing the thickness, the low frequency Q increases and the inductance value reduces.
3. By increasing the area of the inductor (using fewer turns), the low-frequency Q increases and high frequency Q drops. SRF shifts to lower frequencies.

Fig. 4 shows a SEM view together with the measured response of a 2 nH inductor that is optimized for high Q at frequencies between 2– 6 GHz. The response of a similar value inductor optimized to work at higher frequencies is shown in Fig. 5. This inductor has narrower line width and is smaller in size.



(a) (b)

Fig. 4. A SEM view (a) together with the measured Q and inductance of a two-turn 2nH inductor (b). Q is optimized at 2–10 GHz.

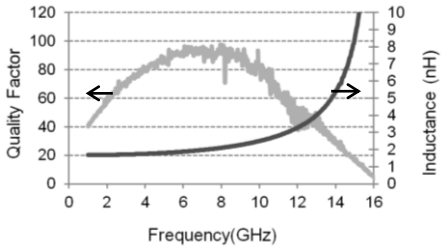


Fig. 5. Measured Q and inductance of a two-turn 1.8 nH inductor optimized for maximum at 4–10 GHz range. Compared to the inductor shown in Fig. 4, this inductor has narrower conductor lines.

V. Tunable Inductors

While tunable capacitors are most commonly used to achieve frequency tuning, co-fabrication of tunable inductors can become critical when optimum tuning or impedance matching in a broad frequency range is desired. Both discrete and continuous tuning methods of lumped

inductors have been reported in the literature using micromachining techniques. Wide continuous tuning of inductors has been achieved using movable structures with large traveling range [10]. Although significant tuning has been reported using this method, the fabrication technique is complex, making the on-chip implementation and packaging process of the inductors difficult. Alternatively, discrete tuning of inductors is achieved by changing the length or configuration of a transmission line using micromachined switches. While by using a switching mechanism the tuning speed can be improved, the incorporation of switches in the body of the tunable inductor increases the resistive loss and, hence, reduces the Q. To achieve a fast tuning speed, a high Q and a high SRF, the transformer action can be used [4]. In this approach, the tunable inductor is placed in proximity of a number of secondary inductor each of which is connected to a micromechanical switch that is normally off (see Fig. 6). Inductors at port two are different in size and, thus, have different mutual inductance effect on port one when activated. The effective inductance of port one can have $1+n(n+1)/2$ different states, where n is the number of inductors at port two. Using this approach, the design of the tunable inductor (primary inductor) can be optimized for high-Q and high SRF, independently. On the other hand, the tuning speed, and tuning bias can be designed by properly engineering the micromechanical switch. MEMS switches can offer high linearity and small loss and when properly designed can be operated for several billions of cycles. A detailed guideline for designing MEMS switches with high performance is given in [11].

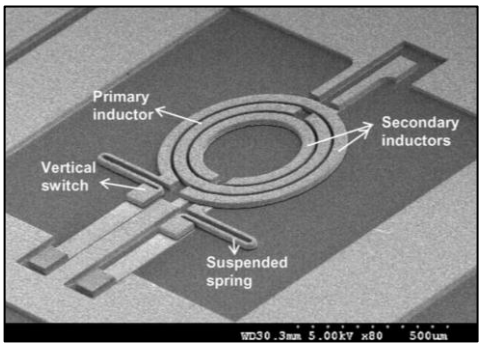
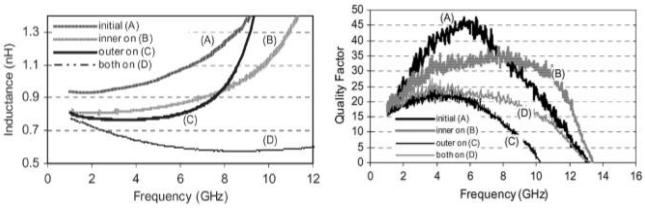


Fig. 6. SEM view of a silver switched tunable inductor, showing the position of the tunable inductor (primary inductor) with respect to the secondary switching inductors.

Fig. 7 shows the measured result of a tunable inductor implemented using the switching transformer method. As shown, a 1.1 nH silver tunable inductor is switched to four discrete values and shows a maximum tuning of 47% at 6 GHz [4]. Furthermore, the switched tunable inductor is packaged to increase the reliability of the switch and to protect silver from oxidation. No degradation in Q was observed after packaging [4]. This switched tunable inductor outperforms the reported tunable inductors with respect to its high embedded Q at gigahertz frequencies. When integrated with the tunable capacitors presented in this paper, these tunable inductors can enable wide tuning range and low-loss tunable filters at high frequencies.



(a) (b)

Fig. 7. Measured (a) inductance and (b) Q of the switched tunable inductor shown in Fig.6. Maximum tuning is 47.5%.

VI. Conclusion

The design considerations for developing high-performance passives were presented. For applications in which the tuning speed is not the major concern but high Q values are needed, thick and high aspect ratio laterally tunable capacitors can be employed. On the other hand, dual-gap vertically tunable capacitors can be employed for applications concerning fast tuning speed and low DC biases. In addition, the fabrication and characterization of high-Q fixed as well as switched tunable inductors have been discussed. These inductors can be directly integrated with the tunable capacitors to implement continuously tunable filters for reconfigurable radio applications.

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References

[1] T.G.S.M Rijks et al, *IEEE MEMS*, Jan. 2004, pp. 777– 780.
[2] G.V. Ionis, A. Dec, and K. Suyama, *Microelectromechanical Systems Conference,* pp.vii+116, 2001.
[3] J. Zou, C. Liu, and J. Schutt-Aine, *Int. J. RF Microwave*, vol. 11, pp. 322–329. Aug. 2001.
[4] M. Rais-Zadeh, P. A. Kohl, and F. Ayazi, "MEMS switched tunable inductor," *IEEE JMEMS*, pp. 78-84, Feb. 2008.
[5] D. Pozar, *Microwave Engineering*, John Wiley & Sons, Inc.
[6] M. Raieszadeh et al., "High-Q integrated inductors on trenched Si islands," *IEEE MEMS conf.*, 2005, pp. 199-202.
[7] M. Rais-Zadeh et al., "High-Q micromachined silver passives and filters," *IEEE IEDM*, Dec. 2006, pp. 727-730.
[8] M. Rais-Zadeh and F. Ayazi, *IEEE MEMS*, Tuscan, Arizona, Jan. 2008, pp. 1032-1035.
[9] Y. Shim, Z. Wu, and M. Rais-Zadeh, "A high-performance temperature-stable continuously tuned MEMS capacitor," *IEEE MEMS*, Cancun, Mexico, Jan. 2011.
[10] I. Zine-El-Abidin et al., "RF MEMS tunable inductor," *IEEE Microw., Radar Wireless Conf.*, 2004, pp. 817–819.
[11] G. M. Rebeiz, *RF MEMS: Theory, Design and Technology*, John Wiley & Sons, Inc.