RF MEMS Passives on High-Resistivity Silicon Substrates

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***Abstract*—Diverse RF passive devices and microelectro- mechanical systems (MEMS) can be monolithically integrated on a high-resistivity silicon (HR-Si) substrate. However, parasitic surface conduction (PSC) at the interface of HR-Si and a silicon dioxide ($\mathrm{SiO_2}$) passivation layer reduces the effective substrate resistivity, which in turn results in deterioration of the device quality factor (Q) and non-linearity. Trap-rich HR-Si has been proposed as a low substrate loss alternative, eliminating the problems associated with PSC. However, the full potential of trap-rich HR-Si as a common platform for implementing MEMS passives is not fully explored. In this letter, we evaluate the effectiveness of the trap-rich layer by comparing the frequency response of a number of RF passive devices fabricated on standard and trap-rich HR-Si substrates. In addition, we suggest an electromagnetic (EM) simulation setup that can be used to efficiently and accurately simulate the device performance.**

***Index Terms*—Electromagnetic simulation, parasitic surface conduction, RF MEMS passives, trap-rich HR-Si substrate.**

I. Introduction

RESISTIVITY and dielectric loss are the most critical substrate parameters that need to be considered when designing high-performance RF devices. Commonly, quartz [1] or borosilicate glass [2] substrates have been used for fabrication of RF devices because of their small dielectric loss and high resistivity. However, compared to silicon, these materials have lower thermal conductivity resulting in heating issues, are harder to bulk micromachine, and are not applicable as a common platform for implementing diverse MEMS. Therefore, micromachined CMOS-grade Si [3], HR-Si [4], or silicon-on-insulator (SOI) [5] substrates have been used when monolithic integration is necessary. Commonly, $\mathrm{SiO_2}$ is used as the passivation layer of silicon-based substrates. The effective resistivity of passivated HR-Si, especially that of the top few micrometers, is lower than the bulk resistivity value by several orders of magnitude because of the accumulation of charges at the interface between silicon and the silicon dioxide passivation layer [6]. As a result, the Q and harmonic distortion of RF passives on HR-Si substrate are exacerbated [6]. In order to improve such losses in HR-Si, additional trap-rich layer such as poly-silicon (Psi) or amorphous silicon (α-Si) can be deposited prior to the silicon dioxide deposition step [7], [8]. The trap-rich layer captures the free electrons attracted to the positive fixed charges, thus reduces PSC effect and increases the effective substrate resistivity.

In this letter, first, EM simulation setup is proposed which can predict the performance of integrated passive components on both standard HR-Si and trap-rich HR-Si substrates. The effectiveness of the trap-rich layer to reduce PSC effect is verified using diverse RF passives. Measurement results demonstrate that the trap-rich HR-Si substrate can be a common platform for implementing RF passives in a wide frequency range and for various applications.

II. Electromagnetic Simulation

Due to formation of a PSC layer, simply applying the nominal bulk substrate properties in EM simulations does not provide a good estimate of passive device performance on a passivated HR-Si. However, EM tool is still very effective in modeling the metal loss and interconnects and can be an accurate simulation option if the effect of PSC and trap-rich layers is well reflected. Here, we investigate an effective setup to simulate the RF response of passives on HR-Si, without requiring heavy computation resources.

To estimate the effective substrate resistivity, first, the carrier distribution is extracted using semiconductor physics tool, ATLAS TCAD Silvaco software [9]. This is a more convenient and easier way to extract the carrier distribution than solving the typical Poisson equations [10]. The carrier concentration (p and n) is simulated with the assigned parameters such as the substrate bulk resistivity (ρ_0), oxide thickness (t_{ox}), and oxide charge density (Q_{ox}). The simplified one-dimensional resistivity distribution ($\rho(\mathrm{x})$) can then be derived. Fig. 1 shows the extracted resistivity distribution under different conditions of ρ_0 and Q_{ox}. The typical range of Q_{ox} is 1×10^{10} to 1×10^{12} $\#/\mathrm{cm}^2$. HR-Si is highly affected when $Q_{ox} > 10^{10}$ $\#/\mathrm{cm}^2$ [Fig. 1(b)]. It is also observed that higher resistivity substrates are more sensitive to Q_{ox} as the PSC layer affects a deeper thickness of the substrate [Fig. 1(a)]. Also, increasing the thickness of the oxide (within a reasonable range) does not have a substantial effect on the substrate effective resistivity.

To imitate the effect of PSC in EM simulations, in the HR-Si substrate model with no trap-rich layer, we add another layer be-

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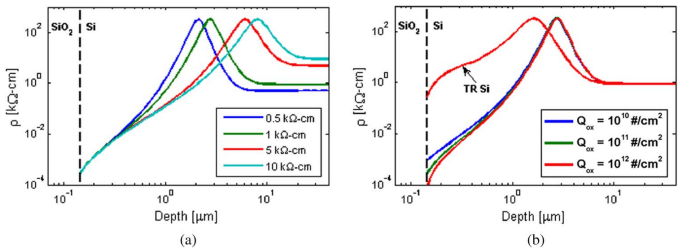

Fig. 1. Simulated resistivity versus substrate depth; (a) with $\rho_0 = 0.5$, 1, 5, 10 $\mathrm{k\Omega \cdot cm}$ and $Q_{ox} = 1 \times 10^{11}$ $\#/\mathrm{cm}^2$; (b) with $\rho_0 = 1$ $\mathrm{k\Omega \cdot cm}$ and $Q_{ox} = 1$, 10, 100×10^{10} $\#/\mathrm{cm}^2$; the effect of 300 nm trap-rich layer with 10^{21} $\mathrm{cm}^3/\mathrm{eV}$ of defect density on a substrate with $\rho_0 = 1$ $\mathrm{k\Omega \cdot cm}$ and $Q_{ox} = 1 \times 10^{12}$ $\#/\mathrm{cm}^2$ is also included.

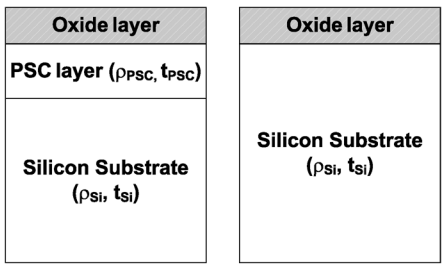

Fig. 2. HR-Si substrate stack used for RF simulation; (a) model of the HR-Si with a PSC layer; (b) model of a substrate with the trap-rich layer.

tween silicon dioxide and the substrate with a thickness of t_{PSC} and an effective resistivity of ρ_{PSC} (Fig. 2(a)). The thickness of this layer, t_{PSC}, can be calculated as the depth at which $\rho(\mathrm{x})$ becomes equal to ρ_0. The effective resistivity of this PSC-dominant layer (ρ_{PSC}) can be derived as

$$\rho_{PSC} = \frac{1}{t_{PSC}} \cdot \int_0^{t_{PSC}} \rho(x)dx. \qquad (1)$$

We set the resistivity of the remaining silicon substrate at its bulk nominal value (ρ_{Si}). On the other hand, the effect of surface charges is negligible with the inclusion of a proper trap-rich layer [7], [8]. We analytically verified that more than 300 nm of a trap-rich layer with an intermediate defect density of 10^{21} $\mathrm{cm}^3/\mathrm{eV}$ can effectively suppress the PSC effect [Fig. 1(b)]. Therefore, the properties of HR-Si with a trap-rich layer are taken as the bulk nominal values and the single layer shown in Fig. 2(b) is used for trap-rich HR substrates.

To verify the accuracy of EM simulations using the substrate setup in Fig. 2, SONNET [11] EM simulation results are compared with the measurement results of fabricated devices, as will be shown later in this letter. Using this setup, more accurate EM simulations can be performed for HR-Si with or without the trap-rich layer.

III. Fabrication Process

The detailed specifications of each substrate are outlined in Table I. Trap-rich layer was deposited by LPCVD on a 10 $\mathrm{k\Omega \cdot cm}$ Si substrate (TR-10k) at 625°C (PSi) and on a 4 $\mathrm{k\Omega \cdot cm}$ Si substrate (TR-4k) at 525°C (α-Si). The α-Si layer was then crystallized using rapid thermal annealing with duration of 120 s at 900°C. On all wafers, a 150 nm-thick capping thermal oxide was grown at 950°C partially consuming the PSi trap-rich layer. The resulting trap-rich layer thickness is of 330 and 360 nm for

TABLE I
Specifications of the HR-SI Substrates

Substrate	ρ_{Si} (Ω·cm)	SiO_2 (nm)	Intermediate trap-rich layer
HR-4k	> 4k	150	-----
HR-10k	> 10k	150	-----
TR-4k	> 4k	170	α-Si (360 nm)
TR-10k	> 10k	150	PSi (330 nm)

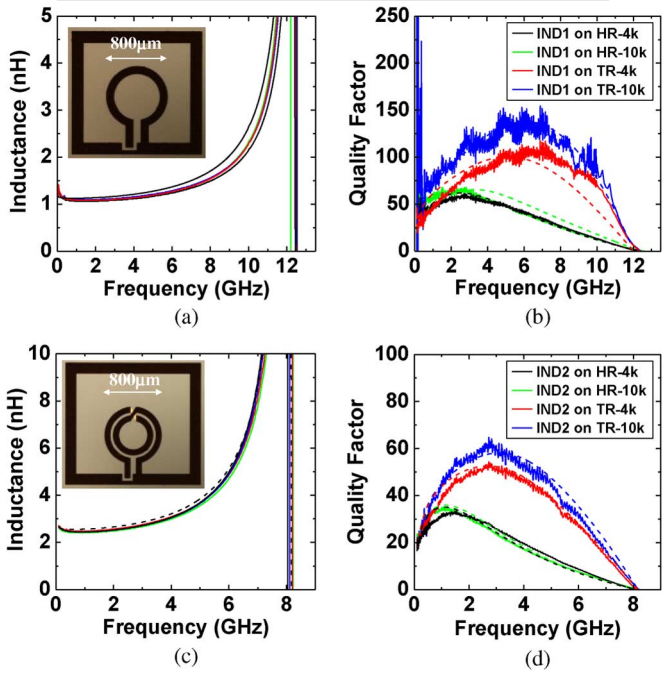

Fig. 3. Measurement results of inductors on four different substrates listed in Table I; (a) inductance of $IND1$ (inset: microscope image of $IND1$); (b) Q of $IND1$; (c) inductance of $IND2$ (inset: microscope image of $IND2$); (d) Q of $IND2$; The dashed lines show the EM simulation results.

TR-10k and TR-4k, respectively. Passive devices are designed and fabricated on these four different substrates using the fabrication process described in [12].

IV. Measurement Results

A. Inductors

Two inductors ($IND1$, $IND2$) are fabricated using two electroplated metals, (5 μm gold (Au) and 35 μm copper (Cu), as the structural and underpass layers. Thick electroplated metals are used to obtain sufficiently low ohmic resistance required to observe the effect of the trap-rich layer.

Fig. 3 shows the measurement results of the inductors compared with the EM simulation results. As predicted using the SONNET EM tool, trap-rich HR-Si provides a much higher Q than the standard HR-Si. The maximum Q of a single-turn circular inductor, $IND1$ on 10 $\mathrm{k\Omega \cdot cm}$ trap-rich HR-Si is more than 130 at 6.0 GHz, while the corresponding value on standard HR-Si is only around 66.6 at 2.57 GHz. As expected, the difference in the substrate resistivity (10 $\mathrm{k\Omega \cdot cm}$ versus 4 $\mathrm{k\Omega \cdot cm}$) does not make as prominent difference as does the inclusion of the trap-rich layer. Due to substantial reduction of losses, $IND1$ on trap-rich HR-Si exhibits Q values similar in range to the inductors fabricated on other low-loss substrates or patterned silicon substrates [3], [13]. $IND2$, a two-turn circular inductor

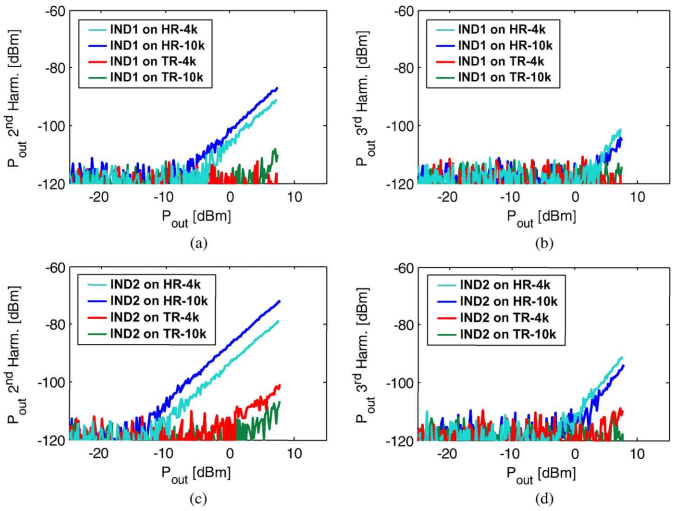

Fig. 4. Measured nonlinear response of inductors vs. output power at the fundamental frequency, 4 GHz; (a) the second harmonic distortion in $IND1$; (b) the third harmonic distortion of $IND1$; (c) the second harmonic distortion in $IND2$; (d) the third harmonic distortion of $IND2$.

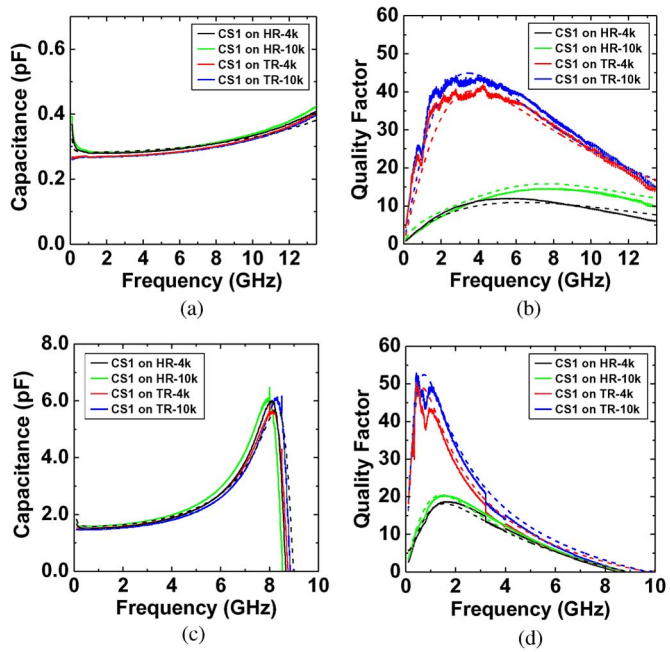

Fig. 5. Measurement results of a capacitive switch on the four different substrates listed in Table I. (a) capacitance at initial state; (b) Q at initial state; (c) capacitance at touch-down state; (d) Q at touch-down state; The dashed lines show the EM simulation results.

(Fig. 3(c) inset), also shows a similar trend. For both inductors, the measured and simulated responses are in good agreement.

The effect of the trap-rich layer in improving the linearity of the components is also studied by measuring the output power at the second and third harmonic frequency upon application of a single tone signal at 4 GHz. As shown in Fig. 4, the second harmonic is suppressed by >30 dB in both $IND1$ and $IND2$ on the trap-rich HR-Si substrates. Similarly, the third harmonic is well suppressed for the inductors on the trap-rich HR-Si wafers.

B. Capacitive Switch

In order to verify the effectiveness of the trap-rich layer and the applicability of our simulation platform to predict the response of capacitive components, the capacitive switch was fabricated on the substrates listed in Table I. Detailed design and operation principle of this type of switch can be found in [12]. The extracted capacitance and Q are shown in Fig. 5 and compared with SONNET EM simulation (dashed lines), using the same substrate setup used for inductor simulation. As shown, the Q is improved by more than 200% using the trap-rich layer. The peak Qs of the capacitors on trap-rich HR-Si substrates are similar and independent of the initial resistance of the substrate.

V. Conclusion

The performance of various RF components such as inductors and capacitive switches are compared using trap-rich HR-Si and standard HR-Si as the substrate. A substrate setup for EM simulations is proposed and its accuracy was verified by comparing the simulation results with measurement values. In both analysis and measurements, all passive devices on the trap-rich HR-Si substrate show superior characteristics such as higher Qs and higher harmonic suppression than those implemented on standard HR-Si substrates. Trapping ability is known to be more effective in crystallized α-Si than poly-Si because of smaller grains and more number of traps [14]. However, we observed similar trends for Q and harmonic suppression using either crystallized α-Si or poly-Si trap-rich layers. The presented RF passive technology using trap-rich HR-Si and thick electroplated metals is an ideal platform for implementing high-performance RF devices with predictable performances.

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