High Performance Inductors on CMOS-Grade Trenched Silicon Substrate

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***Abstract*—This paper reports on a new implementation of high-quality factor copper inductors on CMOS-grade silicon substrates (ρ = 10-20 $\Omega \cdot$ cm) using a CMOS-compatible process. A low-temperature fabrication sequence (<300 °C) is used to reduce the loss in silicon at RF frequencies by trenching the silicon substrate. The high aspect-ratio (30:1) trenches are subsequently bridged over or refilled with a low-loss dielectric to close the open areas and create a rigid low-loss island, referred to as Trenched Si Island. This method does not require air suspension of the inductors, resulting in mechanically-robust structures that are compatible with any packaging technology. A one-turn 0.8 nH inductor fabricated on a Trenched Silicon Island exhibits a very high peak quality factor of 71 at 8.75 GHz with a self-resonant frequency larger than 15 GHz.**

***Index Terms*—CMOS compatible, high-Q inductors, low-loss substrate, micromachining.**

I. Introduction

HIGH-quality factor (Q) integrated inductors can improve the performance and integration-level of RFICs while reducing their power consumption and cost. Inductors are vastly used in voltage controlled oscillators, low noise amplifiers, power amplifiers, mixers, filters, and matching networks. However, on-chip inductors in commercially available CMOS processes exhibit poor Qs (< 30) due to the high-frequency loss in standard silicon (Si) substrate and ohmic loss of thin metal layers [1]. While metal loss can be reduced by using thick high-conductivity metals, the loss in substrate has remained the major barrier in reaching Qs comparable to that of off-chip inductors on Si. Common techniques employed to reduce the metal loss in inductors include the use of high-conductivity metal layers [2], in particular, electroplating thick copper (Cu) layer [3], [4] and utilizing multi-level metal interconnects to increase the effective thickness of inductor [5], [6]. Nevertheless, the most effective way of reducing the metal loss is through electroplating a thick Cu layer.

Micromachining techniques have been utilized to reduce the substrate loss and increase the Q [7]. Previously reported techniques include the use of thick isolating silicon dioxide (SiO_2) layer [8], [9], use of porous silicon to increase the substrate resistance [10], suspension of the inductors [11]–[13], use of 3-D structures such as toroids and self assembled solenoids [14]–[16], and use of low-K dielectrics with thickness of less than 20 μm [17], [18]. Suspension may cause susceptibility to shock and vibrations and can complicate die packaging. Quality factor of 3-D and suspended inductors may also drop due to the encapsulating material used in packaging [19]. The use of thin ($\leq$ 20 μm) low-K dielectric materials alone is not sufficient to effectively reduce the substrate loss.

This paper investigates the effect of trenching the Si on the Q of inductors. The trenched area is covered or filled with a low-loss dielectric to provide a solid low-loss support for the inductors. Therefore, Q of inductors on this micromachined substrate is less affected by the packaging material compared to the suspended inductors. Also, the capacitive loss of the pads is simultaneously reduced, resulting in high de-embedded Q for inductors on Trenched Si Islands (TSI). The height and width of the trenches as well as the trenched area are characterized by fabricating several spiral type inductors on TSI. Quality factor of the inductors on TSI is compared to the Qs of identical inductors on other types of micromachined substrates including Oxide Islands (OI). Comparison shows the remarkable effect of trenching the Si in improving the performance of inductors at radio frequencies.

II. Sources of Loss

Any mechanism that converts the electromagnetic energy into heat is considered as loss. For inductors, the only desirable source of energy storage is magnetic field and hence any source of electric energy storage is considered as parasitic. As a result, the Q of an inductor can be expressed as follows [20]:

$$Q = 2\pi \frac{\text{peak magnetic energy} - \text{peak electric energy}}{\text{Energy dissipated per cycle of oscillation}}. \quad (1)$$

Two independent loss mechanisms are present in inductors: the metal loss and the substrate loss. Therefore, the unloaded Q of an inductor can be expressed by [21]

$$\frac{1}{Q} = \frac{1}{Q_{\text{substrate}}} + \frac{1}{Q_{\text{metal}}} \quad (2)$$

where $Q_{\text{substrate}}$ and Q_{metal} represent the substrate loss and the ohmic loss of metal strips, respectively.

At very low frequencies, the dc series resistance of the metal layers is the dominant Q-limiting mechanism. At higher frequencies, where the skin depth is less than half the thickness of the conductor, skin and proximity effects reduce the effective area of current flow and thus further limit the Q. At even higher frequencies, loss mechanisms present in the substrate sets the lower limit on the Q. Fig. 1 shows the contribution of each loss mechanism on the Q of a 0.8 nH inductor on standard Si

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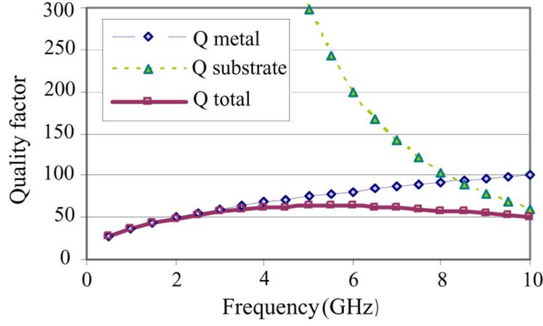


Fig. 1. Q versus frequency for a one-turn 0.8 nH inductor (inductor I) ($d_{\mathrm{out}} = 500\ \mu$m, $w = 50\ \mu$m, $t_{\mathrm{metal}} = 20\ \mu$m, $t_{\mathrm{ox}} = 60\ \mu$m, and $\rho = 10\ \Omega\cdot$cm).

substrate with 60 μm insulating SiO_2 obtained through Sonnet electromagnetic simulations. This inductor with its specific dimensions is referred to as inductor (I) throughout this paper. As shown in Fig. 1, the metal loss is dominant at low frequencies, while the substrate loss sets the lower limit on the Q at higher frequencies.

To obtain high-Q inductors, the effect of both substrate and metal loss has been effectively suppressed in this work.

A. *Effect of Trenching the Si on Substrate Loss*

At RF frequencies, induced currents in the Si substrate limit $Q_{\mathrm{substrate}}$ by converting the electromagnetic energy into heat. The ac current flowing in the inductor produces a magnetic field H. If a static potential difference of V exists between the inductor and the ground plane, the Maxwell equations can be written as follows [22]:

$$\nabla \times H = j\omega\varepsilon E + \sigma E, \quad \mu H = \nabla \times A \tag{3}$$

$$\nabla \times E = -j\omega\mu H, \quad E = -\nabla V - j\omega A \tag{4}$$

where A is the vector potential, σ and ε represent the substrate conductivity and permittivity, respectively; ω is the angular frequency and μ is the substrate permeability. Substituting (4) into (3) gives

$$\nabla \times H = -j\omega\varepsilon\nabla V - \sigma\nabla V + \omega^2\varepsilon A - j\sigma\omega A. \tag{5}$$

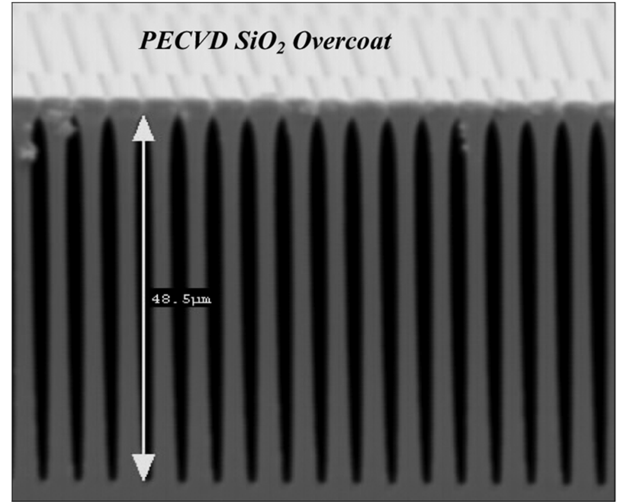
If we call $-j\omega A$ the magnetically-induced electric field E' penetrating into the substrate, the overall current density in the substrate can be found from

$$J = j\omega\varepsilon'(-\nabla V + E') + \sigma(-\nabla V + E') + \omega\varepsilon''(-\nabla V + E') \tag{6}$$

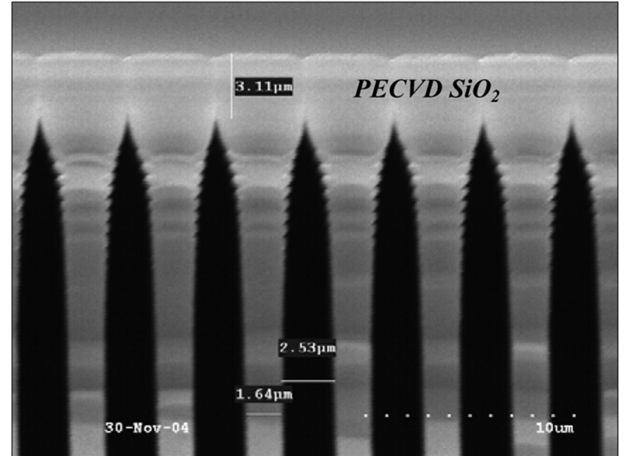
where ε' and ε'' are the real and imaginary parts of substrate permittivity, respectively, (loss tangent $= \tan\delta = \varepsilon''/\varepsilon'$).

The first term of right hand side represents the capacitive loss of the substrate. The second term corresponds to the conduction loss $(-\sigma\nabla V)$ and the eddy current loss $(\sigma E')$. The last term $(\omega\varepsilon''(-\nabla V + E'))$ denotes the electrically- and magnetically-induced dipole loss, which becomes dominant at high frequencies.

For low-resistivity substrates such as CMOS-grade Si, the electrically-induced current density $(-\sigma\nabla V)$ and losses associated with the eddy current $(\sigma E')$ dominates over the dipole loss. However, for high-resistivity substrates the dipole loss is the determining loss mechanism.



(a)



(b)

Fig. 2. Cross-section SEM view of (a) 50-μm-deep TSI with (b) close-up view of the smooth surface (surface roughness $< 0.3\ \mu$m).

Therefore, disrupting the path of dissipating currents by vertically-slicing the substrate with deep high-aspect-ratio trenches reduces the conduction and eddy current losses as well as the capacitive and dipole losses, which in turn increases the Q. Two low-temperature processing approaches can be taken to create a rigid and smooth surface on the trenched areas for subsequent inductor fabrication. These approaches include bridging-over the trenches with a plasma enhanced chemical vapor deposited (PECVD) dielectric layer (e.g., SiO_2), and filling the trenches with a low-loss material (e.g., Avatrel polymer).

1) Silicon Dioxide Bridge-Over: The main approach in this work is bridging over the open areas through deposition of a thin PECVD SiO_2 layer. The required film thickness to bridge over the open areas in a Trenched Si Island and create a smooth surface is in the order of trench width. Fig. 2 shows cross-section SEM view of a 50-μm-deep TSI together with a close-up view of the smooth surface (surface-roughness $< 0.3\ \mu$m). The width of the openings should be optimized for low substrate loss and reasonable bridge-over SiO_2 thickness. For a TSI with repeated trench width of 2 μm and Si width of 2 μm, the required PECVD SiO_2 thickness is $\sim 3\ \mu$m.

TABLE I
COMPARISON OF ELECTRICAL PROPERTIES OF AVATREL WITH BCB AND POLYIMIDE [23]–[25]

	Avatrel	Polyimide	BCB
tan δ@ 1GHz	0.009	0.01-0.015	0.015
Permittivity (ε_r)	2.50	3.1- 4.1	2.7
Moisture uptake	<0.1%	0.5-3%	0.23%

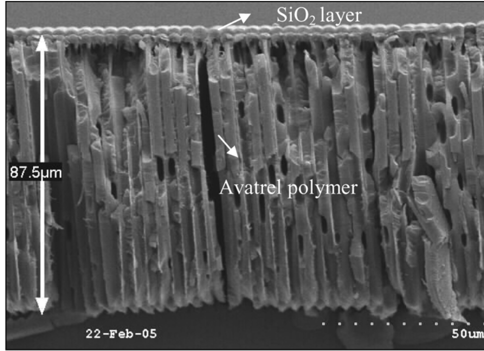


Fig. 3. SEM picture of Trenched Si area refilled with Avatrel.

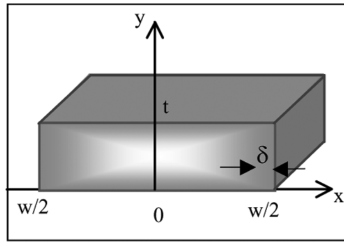


Fig. 4. Effective area of the current flow for isolated strips.

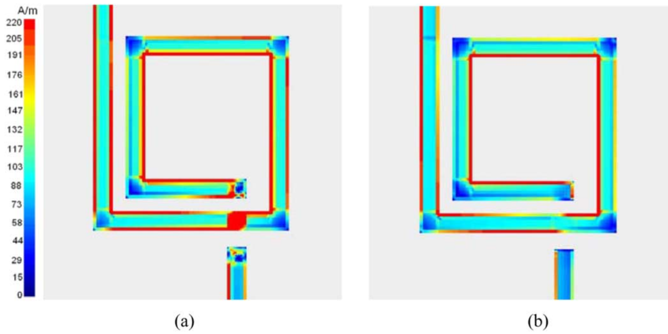


Fig. 5. Current density of a 1.5-turn inductor at 10 GHz (a) at the bottom surface of metal, and (b) at the top surface of metal.

2) Avatrel Polymer Trench Refill: As an alternative way, trenches can be refilled with a low-K dielectric to create a rigid substrate. Avatrel 2000P polymer from Promerous Inc. has been selected for this purpose since it has a low dielectric permittivity compared to other dielectric materials [23]. Table I compares the electrical properties of Avatrel with two other low-K dielectrics commonly used as insulating layers, showing the small relative permittivity and loss-tangent of this material.

Fig. 3 shows the cross section of 90-μm-deep trenched Si area refilled by spin-coating of Avatrel. The refilled trenches are successively coated with a thin PECVD SiO_2 layer ($\sim 1\ \mu$m) in order to promote the adhesion of consecutive layers to the substrate.

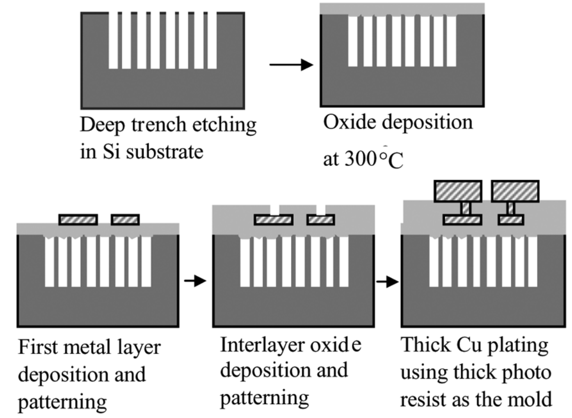


Fig. 6. Inductor fabrication process flow on TSI.

B. Effect of Copper Thickness on Metal Loss

Micromachined planar inductors have rectangular strip metallization on the substrate with a distant ground, usually implemented on the same plane as that of the inductor, or at the back of a thick substrate. Therefore, the series resistance of the metal strip can be approximated by the isolated strip conductor formula [26]. According to this formula, current does not recede on the bottom surface of the conductor, as opposed to microstrip lines with close ground. Fig. 4 shows the effective area of the current flow for an isolated strip line at high frequencies, where the skin depth is less than half the thickness of the conductor. Thus, the series resistance of the conductor can be approximated by

$$R_{ac} = \frac{kl}{2\sigma\delta(w+t-2\delta)}$$
$$\text{where } \delta = \sqrt{\frac{1}{\pi f \sigma \mu}} \quad (7)$$

conductor width, total length and thickness are represented by w, l, and t, respectively. σ is the electrical conductivity of the metal and δ is the skin depth (e.g., $\delta_{\mathrm{Cu}} = 1.3\ \mu$m at 2.4 GHz). k is a correction factor, which depends on w and t. In contrary to microstrip lines, Q_{metal} of thick strip conductors increases with metal thickness in excess of 5× skin depth. Simulation results confirm that for coplanar inductors, current also flows on the top surface of the metal conductor. The verification of this fact is shown in Fig. 5 (black color shows the highest current density).

As shown in Fig. 5, the current is pushed to the inner side of the inner turn of the conductor. This is due to the proximity effect, which takes place when a conductor is under the influence of a time-varying field produced by a nearby conductor carrying a time-varying current. In the inductors, the skin-effect eddy current and the proximity-effect eddy current superimpose to form the total eddy current distribution, resulting in the increase of the ac resistance.

In this work, metal loss is reduced by electroplating thick Cu ($\sim 20\ \mu$m) layer and reducing the effect of ground plane by increasing the signal to ground distance in the inductor layout.

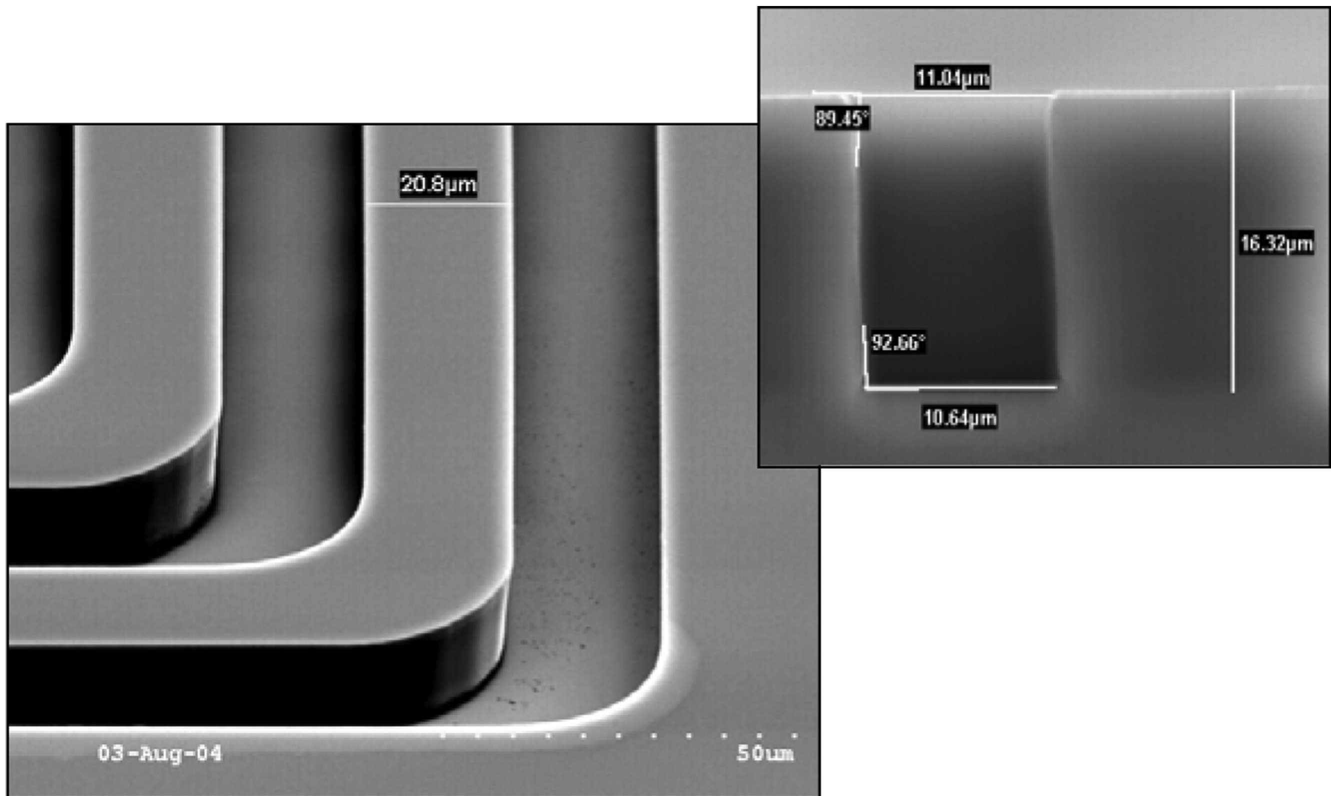


Fig. 7. SEM pictures of (left) a 17-μm–thick NR4-8000P used as the electroplating mold, and (right) close-up view of the straight photoresist side walls.

III. Inductor Fabrication

Fig. 6 shows the fabrication process flow for the Cu inductors on TSI. First, deep high-aspect-ratio (30:1) trenches are etched into the Si substrate using the deep reactive ion etching (DRIE) Bosch process. A 2–3-μm-thick PECVD SiO_2 layer is then deposited at 300 °C to cover the openings and lower the substrate parasitic capacitances. The first metal layer is subsequently formed by evaporation and patterning of a 1.5-μm-thick Chrome (Cr)–Cu–Cr layer. To isolate the two metal layers, a 2-μm-thick PECVD SiO_2 is deposited at 300 °C and vias are opened. A 1000 Å seed layer of Cr–Cu is then sputter deposited, followed by spin-coating and patterning of the electroplating mold. Thick NR4-8000P negative-tone photoresist has been used for this purpose, which produces high-aspect-ratio (4.5:1) and straight-sidewall columns as shown in Fig. 7. Finally, thick layer of Cu is electroplated and the photoresist and seed layer are removed. Fig. 8 shows SEM pictures of a one-turn inductor on TSI.

As was mentioned earlier, trenches are alternatively refilled by spin-coating of Avatrel polymer. The polymer is then cured and a 1-μm-thick SiO_2 is deposited on the refilled trenched Si area at 160 °C. The deposition temperature is reduced to avoid bubbling of Avatrel. Subsequent processing steps are as shown in Fig. 6.

It is worth mentioning that increasing the undercut of Si in RIE (during the trench etching step), further reduces the substrate loss by decreasing the equivalent substrate relative permittivity and conductivity. Fig. 9 shows a 0.8 nH inductor (*Inductor I*) on 70-μm-deep TSI. As shown in Fig. 9, the trench width in the bulk of trenched region is reduced to 1 μm, while the opening width is kept at 2 μm (to avoid deposition of thicker bridge-over SiO_2 to cover the trenches).

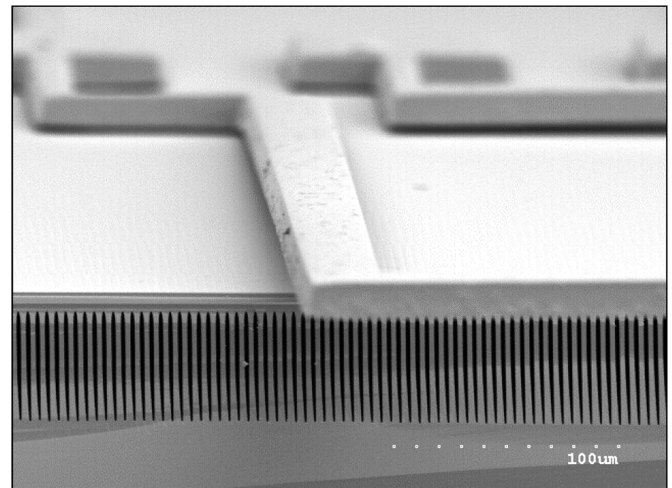


Fig. 8. SEM picture of a one-turn inductor on top of TSI ($w = 40\ \mu$m, $d_{\rm out} = 860\ \mu$m, $t_{\rm metal} = 26\ \mu$m, and $Q = 45$).

IV. Characterization Results

Rectangular and circular type inductors of various dimensions are fabricated and tested on trenched Si substrates. On-wafer S-parameter measurements are carried out using an HP8517B vector network analyzer and ground-signal-ground Cascade micro-probes. The pad-only characteristics are measured on the open pad dummy structures fabricated on the same substrate as the corresponding inductor. The parasitics

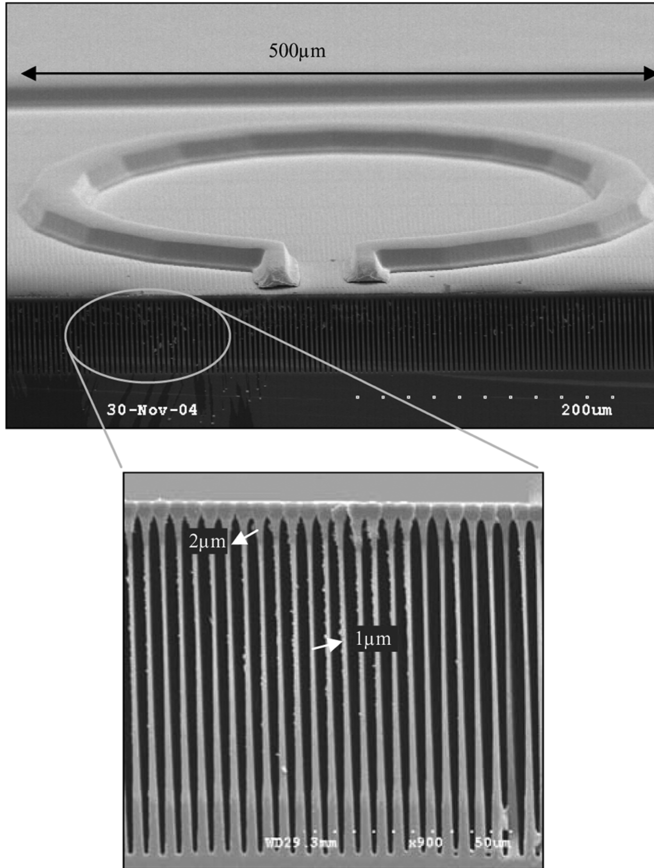


Fig. 9. SEM picture of inductor (I) on top of TSI with a close-up view of the high-aspect ratio trenches ($w = 50\,\mu$m, $d_{\rm out} = 500\,\mu$m, $t_{\rm metal} = 20\,\mu$m, and Q =71).

associated with the pads-only (not the access lines connecting the pads to the inductors) are then de-embedded from the overall inductor characteristic by subtracting the Y-parameters of the pads from the Y-parameters of the embedded inductors [27]. Inductance and Q are calculated from

$$L = \frac{\mathrm{Im}\left(\frac{1}{Y_{11}}\right)}{2 \times \pi \times f} \quad Q = \frac{\mathrm{Im}\left(\frac{1}{Y_{11}}\right)}{\mathrm{Re}\left(\frac{1}{Y_{11}}\right)}. \tag{8}$$

A. Q on Trenched Si Islands

Fig. 10 shows the embedded and de-embedded Q and inductance of inductor (I) fabricated on 70-μm-deep TSI with Si resistivity of 10 Ω·cm (SEM picture is shown in Fig. 9). The quality factor is over 50 in the 5–10 GHz range with a maximum of 70.6 at 8.75 GHz. The self resonant frequency of this inductor is much higher than 15 GHz.

The significant effect of trenching the Si in improving the Q is revealed by comparing the loss of TSI with loss of standard Si substrate coated with thick dielectrics. Fig. 11 shows the measured Q of inductor (I) on 10 Ω·cm Si substrate coated with (a) 20-μm-thick PECVD SiO_2 (deposited at 300 °C), and (b) 20-μm-thick Avatrel. Similar performance is observed at low frequency regime, where Q is limited to $Q_{\rm metal}$. At high frequencies, however, Q of inductor (I) on TSI is 2× higher than the Q of identical inductors on standard Si substrate passivated with 20-μm-thick dielectrics, showing the remarkable effect of disrupting the path of current on the Q.

It is notable that inductors fabricated on TSI have high embedded Q in contrast to the suspended inductors reported in literature [Fig. 10(a)] [12]. This is because the parasitic capacitances of pads are reduced simultaneously by reduction of the substrate loss underneath the pads.

B. Q on Avatrel Refilled Trenched Substrate

Fig. 12 shows the Q of a 0.9 nH inductor on Avatrel refilled 90-μm-deep trenched Si substrate, showing a maximum Q of 60 at 1.75 GHz. The performance is compared to an identical inductor fabricated on 50-μm-thick embedded Oxide Island (OI). The thick OI is realized by oxidizing the Si left in between the trenches at 1000 °C [8]. As it can be seen in this figure, $Q_{\rm substrate}$ in the two cases are almost equal, resulting in similar Q values at high frequencies ($f \geq$3 GHz).

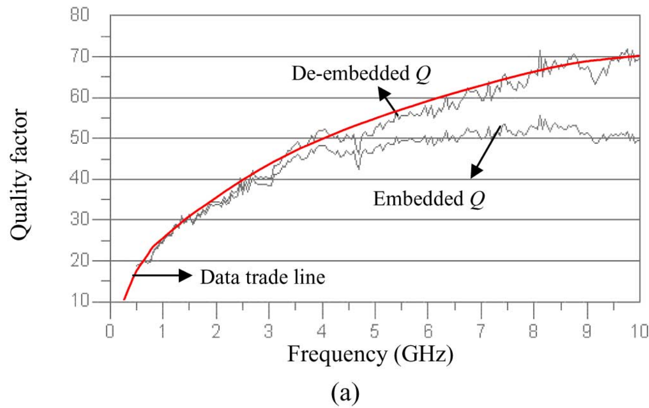
Fig. 13 compares the effect of trench depth on the Q when the substrate is coated with a thick layer of Avatrel. Inductor (A) is fabricated on 90-μm-deep Avatrel refilled trenched Si substrate. The thickness of the Avatrel on the surface of the refilled substrate is negligible (as shown in Fig. 3). Inductor (B) is fabricated on a 50-μm-deep trenched refilled Si island. The thickness of the Avatrel layer covering the refilled trenches is about 20 μm, as shown in Fig. 14. The peak Q is higher for the inductor (A), which is fabricated on 90-μm-deep trenched Si without extra Avatrel coating, demonstrating that the substrate loss cannot be effectively reduced by merely coating it with a thin ($<$ 20 μm) low-K dielectric layer.

C. Efficiency of Trenched Si Island

To evaluate the effectiveness of trenching the substrate in the inductor performance, identical 1 nH inductors are fabricated on 70-μm-deep SiO_2 bridge-over TSI, 20-μm-thick PECVD SiO_2 coated Si, and Avatrel refilled trenched Si substrate. Comparing the measured Q of inductors on different type of micromachined substrates reveals that TSI (without refilling) exhibits the lowest loss compared to other low-temperature micromachined Si substrates (Fig. 15). As shown, Q of the inductor on 70-μm-deep TSI is 2.5× higher than the Q of the identical inductor on 20-μm-thick SiO_2 coated standard Si substrate at high frequencies (f >4 GHz), where the substrate loss is the dominant loss mechanism.

The performance of inductors fabricated on TSI was also compared to the performance of identical inductors fabricated on thick OI. Fig. 16(a) shows the de-embedded Q of the fabricated inductors. As shown in Fig. 16(b) the embedded S_{11}-parameter of the inductor fabricated on 50-μm-deep TSI (low-temperature processing) is very close to the one fabricated on 50-μm -thick solid OI (high-temperature processing), and the inductor has significant higher Q compared to when it is fabricated on a 4-μm-thick SiO_2-covered standard Si substrate.

Fig. 17 shows the simulated characteristics of the inductors shown in Fig. 16. The thick copper inductor is modeled using Sonnet thick metal model. The simulated performance of the inductors on OI and 4-μm-thick SiO_2 is in perfect agreement with the measurement. The accurate modeling of the inductors on TSI is computationally intensive. Therefore, the TSI is modeled as a solid substrate with an effective permittivity, loss tangent



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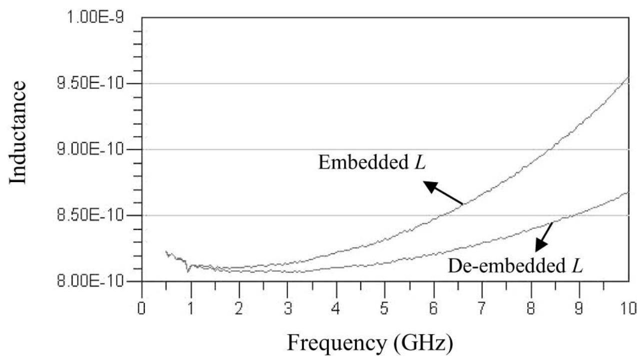
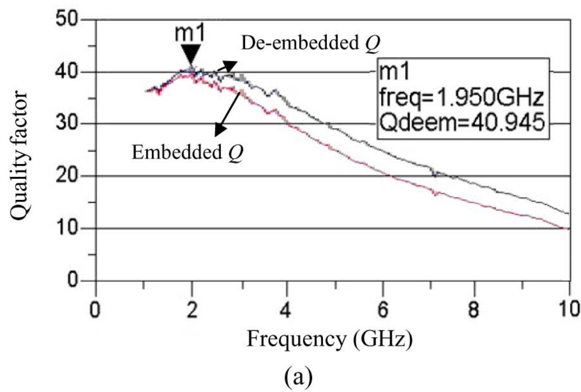
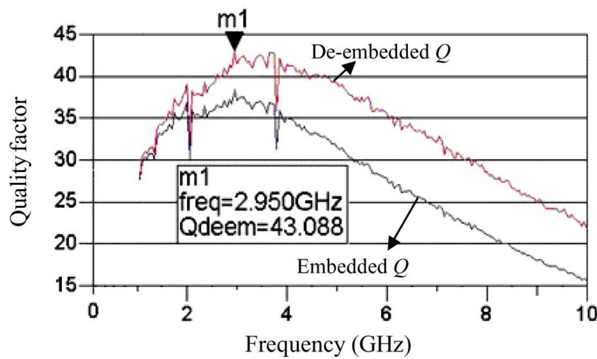


(b)

Fig. 10. Measured (a) Q, and (b) inductance of a one-turn 0.8 nH inductor (inductor (I)) on 70-μm-deep TSI ($t_{\rm metal} = 20\ \mu$m, $w = 50\ \mu$m, $d_{\rm out} = 500\ \mu$m).



(a)



(b)

Fig. 11. Measured Q, of inductor (I) on (a) 20-μm-thick SiO_2, and (b) 20-μm -thick Avatrel coated standard Si substrate.

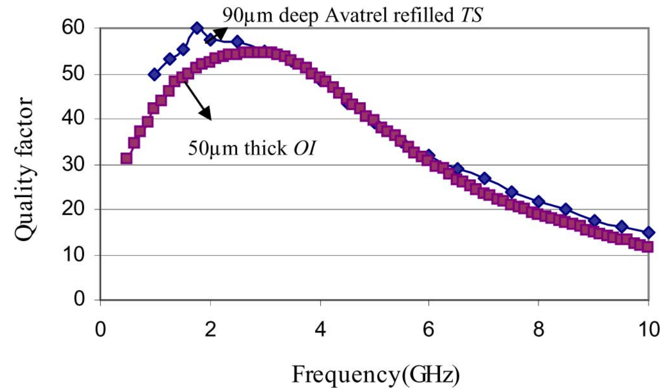


Fig. 12. Comparison between measured Q of a 0.9 nH inductor fabricated on OI and Avatrel refilled TSI.

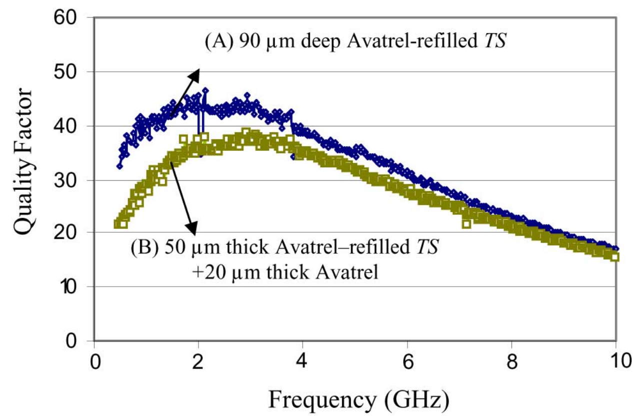


Fig. 13. Comparison between measured Q of a 0.8 nH inductor fabricated on (A) 90-μm-thick Avatrel refilled trenched Si, and (B) 20-μm-thick Avatrel coated 50-μm-deep trenched Si substrate.

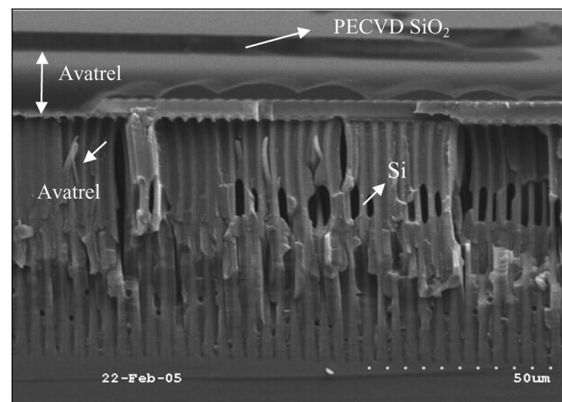


Fig. 14. Cross section SEM view of a TS filled with Avatrel, and coated with a 20-μm-thick Avatrel layer and 4-μm-thick SiO_2 layer.

and conductivity. As shown in Fig. 17, the simulated quality factor of the inductor on modeled TSI is in good agreement with the measurement.

The equivalent circuit model for spiral inductors is shown in Fig. 18(a) [28]. For one-turn inductors C_s is negligible. Therefore, the simplified modeled shown in Fig. 18(b) is used to extract the electrical parameters of the inductors on TSI and OI. Table II summarizes the modeled parameter of the simulated and measured inductors fabricated on TSI and OI, showing lower

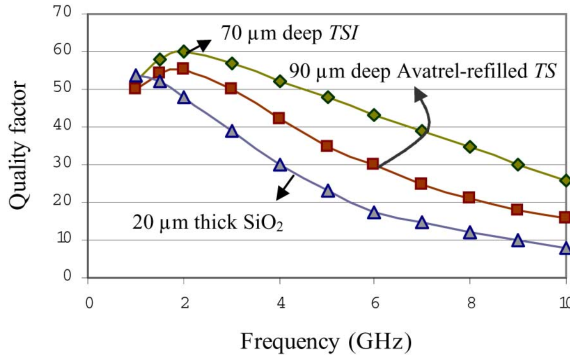
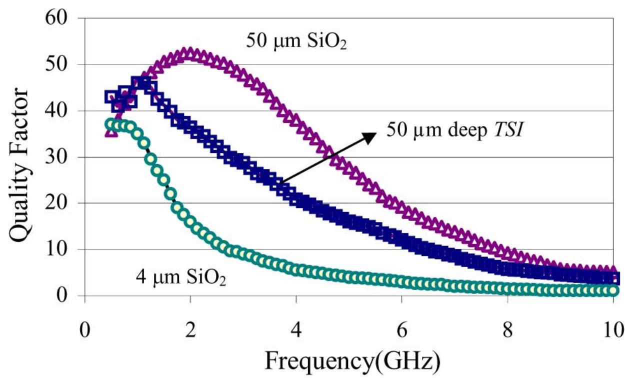
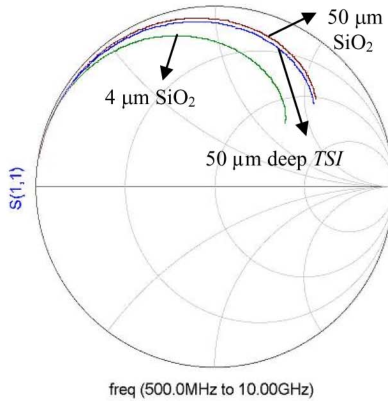


Fig. 15. Measured Q of a 1 nH inductor on 70-μm-deep TSI, 20-μm-thick PECVD SiO_2 coated Si, and 90-μm-deep Avatrel refilled trenched Si substrate.



(a)



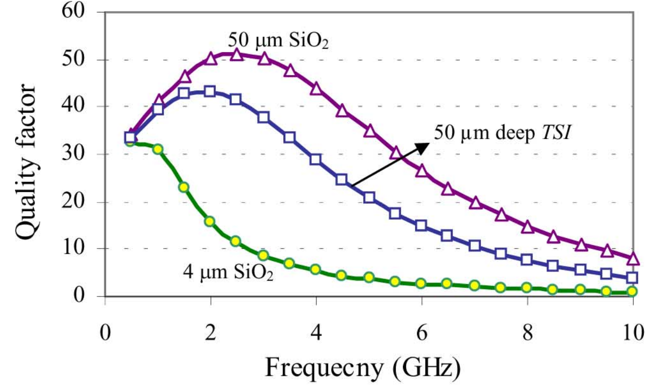
(b)

Fig. 16. Comparison of (a) measured Q (b) S-parameter of a 1.0 nH inductor on OI, TSI and 4-μm oxide-covered Si substrate. ($t_{\rm metal}$ = 25-30 μm, w = 60 μm, and $d_{\rm out}$ = 825 μm).

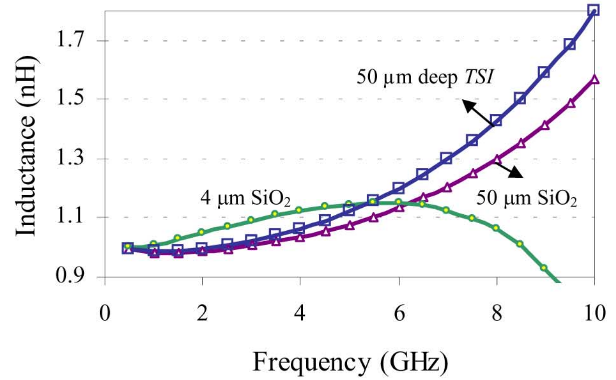
substrate parasitic (R_{si} and C_{si}) for the inductor on OI. To reach higher Q on TSI, trench depth must be increased.

D. Effect of Trenched Area

Another interesting result extracted from measurement is the dependency of Q on the trenched island area. As shown in Fig. 19(b) a negligible difference in Q has been observed when the trenched area is extended beyond 50 μm from the edge of the Cu tracks [$X > 50$ μm in Fig. 19(a)], alleviating the need for trenching the entire area beneath the inductor.

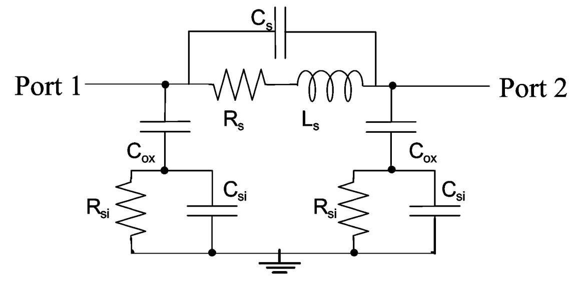


(a)

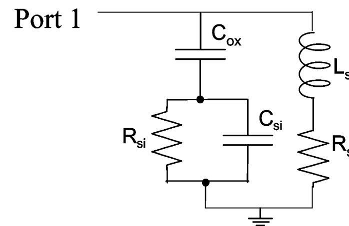


(b)

Fig. 17. Simulated (a) Q and (b) inductance of the inductor shown in Fig. 16 using Sonnet. The TSI is modeled as a solid substrate with effective permittivity of 5.95, effective loss tangent of 0.002, and effective conductivity of 0.1 S/m.



(a)



(b)

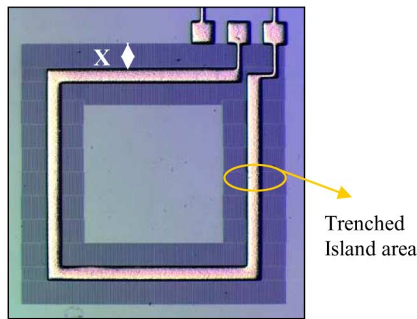
Fig. 18. (a) Equivalent electrical model of a planar spiral inductor for two-port configuration and (b) simplified model for one-port one-turn inductors.

E. Effect of Metal Thickness

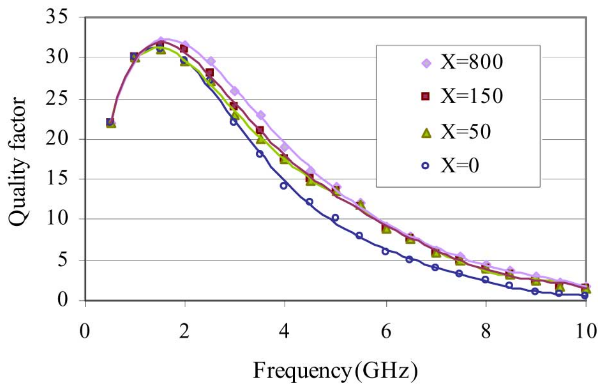
The Q versus frequency plots for a one-turn Cu inductor with two different metal thicknesses is shown in Fig. 20, confirming improvement in coplanar inductor Q for metal thicknesses in

TABLE II
MODELED PARAMETERS OF IDENTICAL INDUCTORS ON OI AND TSI

Type	R_s (mΩ)	R_{si} (Ω)	C_{si}(pF)	L (nH)
OI (measured)	96.8	598	0.000	1.00
TSI (measured)	96.1	558	0.006	1.05
OI (simulated)	92.2	624	0.000	1.003
TSI (simulated)	91.9	570	0.002	1.004



(a)



(b)

Fig. 19. (a) Microscope picture of the inductor showing the definition of X, and (b) measured Q versus frequency for a one-turn inductor on TSI with various trenched island area. ($t_{\rm metal}$ = 30 μm, $w_{\rm metal}$ = 100 μm, $d_{\rm out}$ = 1200 μm).

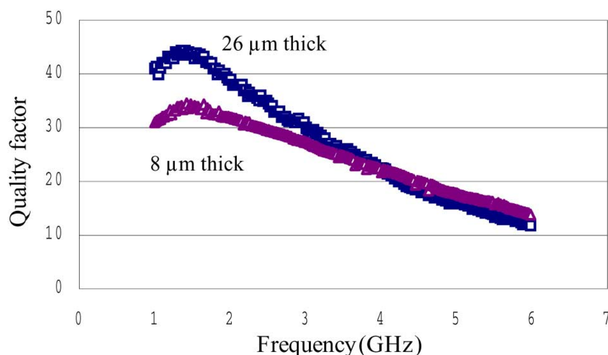


Fig. 20. Measured Q of a 1 nH inductor on TSI with different metal thicknesses.

excess of 5× skin depth at lower frequencies where metal loss is the dominant Q-limiting mechanism.

V. CONCLUSION

A new implementation of high-Q integrated Cu inductors on CMOS-grade Si substrates using a fully CMOS-compatible process was introduced. A new fabrication sequence has been used to reduce the loss of Si substrate at RF frequencies by trenching the Si. Two approaches were taken to cover the trenches and make a smooth surface: 1) high aspect ratio (30:1) trenches were bridged-over by depositing a thin layer (∼ 3 μm) of SiO_2 at 300 °C and 2) trenches were refilled by spin-coating of Avatrel Polymer. Metal loss of inductors was reduced by electroplating thick (20 μm) Cu layer. For comparison, the inductors were also fabricated on thick embedded oxide islands, thick Avatrel and thick PECVD SiO_2 coated Si.

Comparing the measured Q of identical inductors on different type of micromachined substrates revealed that the TSI (without refilling) exhibits the lowest-loss compared to other low-temperature micromachined Si substrates. Measurement results indicate a significant improvement in the Q for inductors on TSI compared to the inductors fabricated on conventional low-resistivity Si substrates.

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