

LOW-VOLTAGE LARGE-VALUE TUNABLE CAPACITORS USING SELF-ALIGNED HARPSS

M. Rais-Zadeh, A. K. Samaroo, P. Monajemi, and F. Ayazi
Georgia Institute of Technology, Atlanta, Georgia, USA

ABSTRACT

This paper presents a silicon microfabrication technique for the implementation of large-value one-port and two-port tunable capacitors with very small tuning voltages. The proposed process offers very high aspect-ratio narrow vertical gaps of different sizes in a self-aligned manner, allowing the realization of in-plane tunable capacitors in a small area. A continuous tuning of 240% is achieved for a 15 pF two-port capacitor with the application of 3.5 V. A 106 pF one-port capacitor occupies an area of 8 mm² and is tuned to 130 pF with a tuning voltage of 0.9 V.

1. INTRODUCTION

Large-value tunable and/or variable capacitors are needed in a variety of applications, including low-frequency tunable filters and electrostatic energy harvesting devices. Although several designs of small-value micromechanical tunable capacitors have been reported in the literature [1, 2], low actuation voltage tunable capacitors with large values in small form-factor are yet to be shown. To achieve the highest density capacitors, 3D interdigitated plates with narrow and high aspect-ratio vertical gaps are needed. Our group has previously shown the application of the high aspect-ratio polysilicon and single crystal silicon (HARPSS) fabrication technique [3] for the realization of high quality factor (Q) low-voltage one-port capacitors on silicon substrate [4]. In this technique, vertical gaps are defined between polysilicon structures and silicon substrate by the deposition of thermal oxide (sacrificial oxide) and thus can be scaled to values less than 50 nm and aspect-ratio of more than 200 [5]. Hence, this process is well-suited for the fabrication of high-value capacitors. However, the conventional HARPSS process does not offer different-size self-aligned narrow gaps between polysilicon and single crystal silicon structures, which is a required feature for high-performance tunable capacitors. For this reason, we have developed a modified version of HARPSS, called the self-aligned HARPSS to implement one-port and two-port tunable capacitors. Using this novel fabrication technique, tunable capacitors of different values are implemented in the bulk of a 70 μm thick silicon on insulator (SOI) substrate and are tuned by 240 % with a tuning voltage as low as 3.5 V.

2. FABRICATION

Figure 1 shows the fabrication process flow of the self-aligned HARPSS, requiring only three lithography masks. In this process, the sub-micron high aspect-ratio vertical capacitive air gap is defined by thermally growing a thin layer of sacrificial silicon dioxide. Wider vertical

gaps of different sizes are defined by silicon nitride in a self-aligned manner. Silicon nitride is used as it acts as a mask during the thermal growth of silicon dioxide and is etched back from the surface at the final step to define the trenches in silicon.

The process starts with the deposition and patterning of a 3000 Å LPCVD silicon nitride on a SOI substrate (Fig. 1(a)). Next, trenches are etched into the device layer using photoresist as the mask (Fig. 1(b)). The thin layer of sacrificial silicon dioxide (<1 μm) is then thermally grown at 950 °C. The oxide growth temperature is reduced to minimize the stress. The trenches are then filled with LPCVD poly silicon, boron-doped and annealed. Annealing parameters of polysilicon heavily influence the residual stress of this film, which affects the performance of the movable structures, as will be discussed later in the paper. Polysilicon is subsequently patterned using photoresist as the mask (Fig. 1(c)). A layer of silicon dioxide is grown to protect the polysilicon structures in the final silicon etching step (Fig. 1(d)). Silicon nitride is then removed by reactive ion etching and the self-aligned isolating trenches are etched into the device layer (Fig. 1(e)). Finally, the devices are released in hydrofluoric acid (Fig. 1(f)). Using this fabrication process, we have designed and fabricated two-port tunable capacitors.

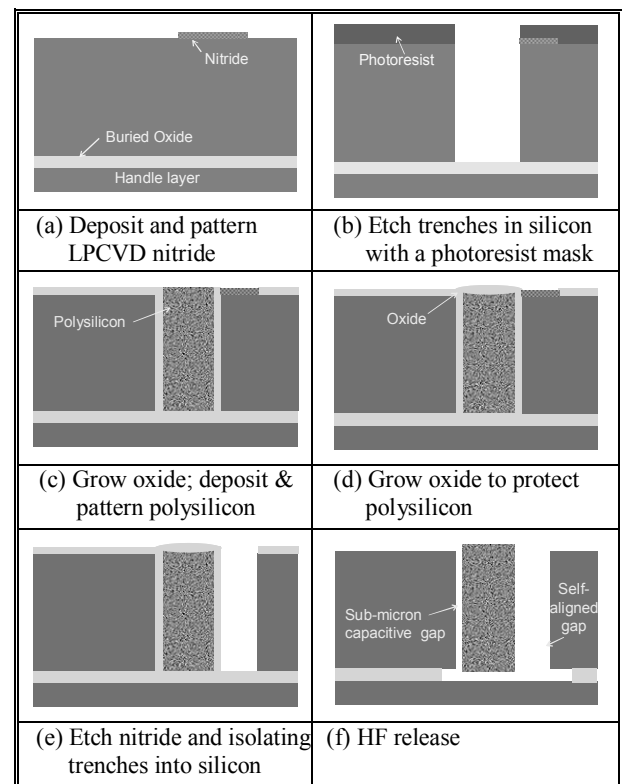


Figure 1: Fabrication process flow for the self-aligned HARPSS process.

3. DESIGN

The schematic diagram of the two-port tunable capacitor is shown in Figure 2. To maximize the electrostatic tuning, the actuator is designed with a comb-drive configuration and the capacitor is a parallel-plate. The sub-micron gap offered by HARPSS makes the realization of large-value capacitors as well as low tuning voltage actuators possible.

The main challenge in designing a two-port tunable capacitor is to electrically isolate the movable plates of the tunable capacitor from the actuator while maintaining a mechanical connection [1]. This has also been achieved with the proposed fabrication process without additional complexity. Such a connection is provided by a polysilicon clamp that is electrically isolated from the capacitor and the actuator using sacrificial oxide in the bulk and nitride on the surface. If one-port capacitors are desired, the clamp is not needed and the silicon shuttle connects the actuator to the parallel-plate capacitor. Figure 3 shows the SEM view of a two-port tunable capacitor. Figure 4 shows close-up views of the polysilicon clamp and the sub-micron capacitive gap. The device is realized on a 70 μm thick SOI substrate with a low resistivity of $< 0.001 \Omega$. To minimize the sensitivity to external acceleration, the two-port capacitor is made symmetric about both x and y axes, as shown in Figure 3.

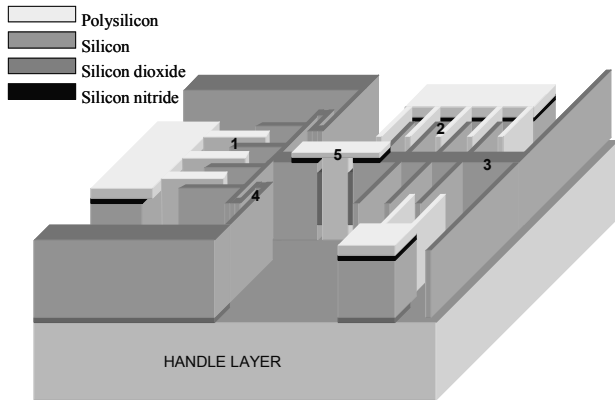


Figure 2: Schematic of the two-port tunable capacitor, showing 1: Comb-drive actuator, 2: Parallel-plate capacitor, 3: Shuttle, 4: Spring, and 5: Polysilicon clamp.

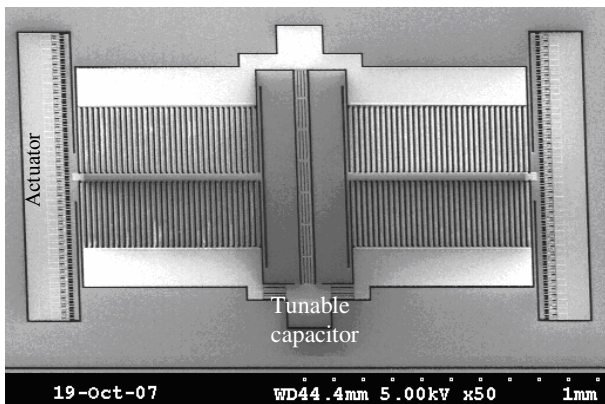
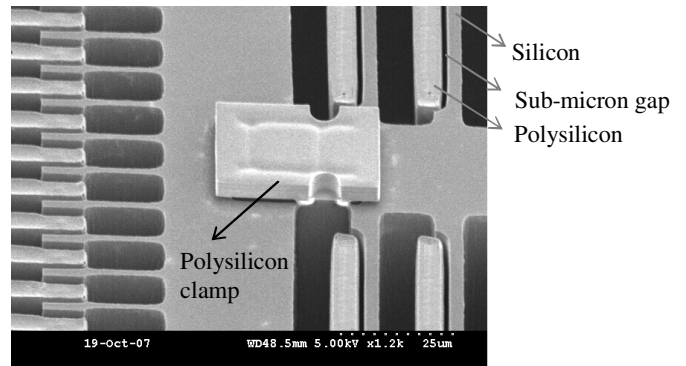
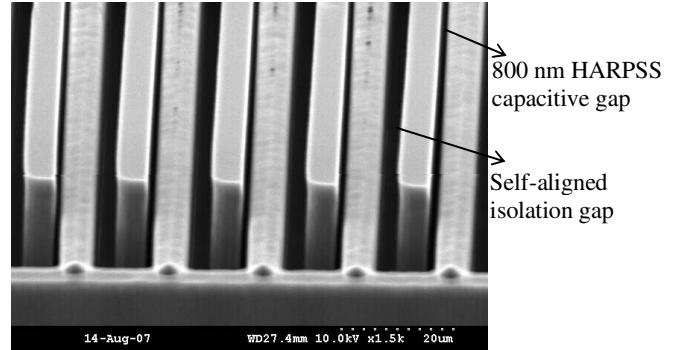


Figure 3: SEM view of a 15 pF two-port tunable HARPSS capacitor fabricated on a 70 μm thick SOI substrate.



(a)



(b)

Figure 4: (a) SEM view of the polysilicon clamp and (b) close-up view of the 800 nm gap between the parallel-plate.

Figure 5 shows a SEM view of a broken 106 pF capacitor. This capacitor is fabricated on 60 μm thick SOI substrate.

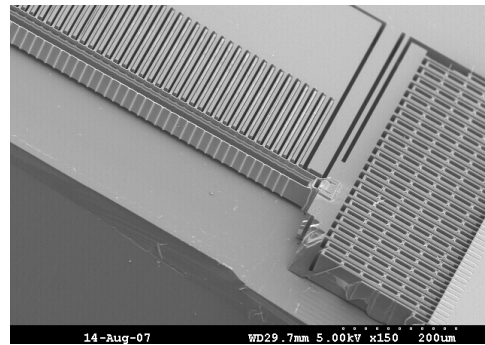


Figure 5: SEM view of a broken capacitor, showing the 60 μm thick device on SOI substrate.

4. RESULTS

DC tuning voltages are applied to the actuator and the capacitance values are measured at 2 MHz using an Agilent E4980A precision LCR meter. Figure 6 shows the measured C-V tuning curve of a 15 pF two-port tunable capacitor. As shown, this capacitor is continuously tuned to 51 pF with the application of 3.5 V. The capacitor was simulated using Ansoft HFSS full-wave EM solver. Figure 7 shows the model and the results of the simulation. The resistivity of the polysilicon is assumed to be the same as the silicon substrate, which is 0.001 $\Omega\cdot\text{cm}$. The resistivity of polysilicon in the fabricated device is 0.04 $\Omega\cdot\text{cm}$, resulting in a lower measured quality factor than that predicted by the simulations. The simulated capacitance value, on the other hand, is in good

agreement with the measured result.

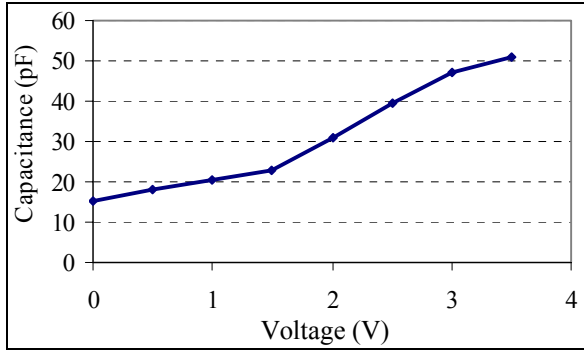
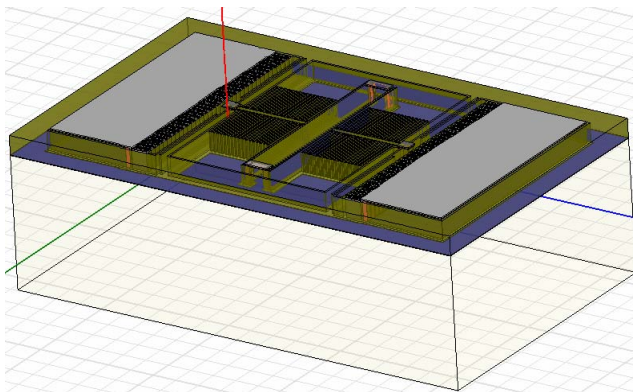
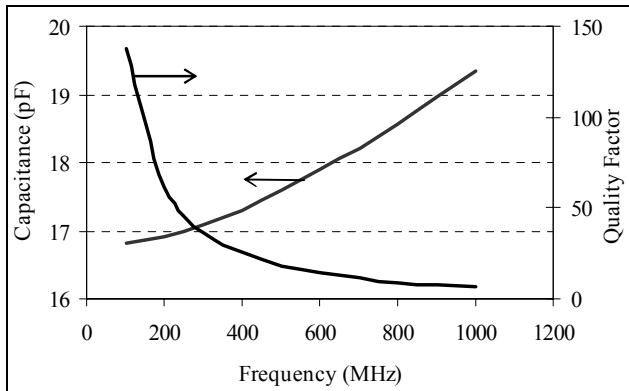


Figure 6: C-V tuning curve of a 15 pF two-port HARPSS capacitor, showing a maximum tuning of 240%.



(a)



(b)

Figure 7: (a) HFSS 3D model and (b) simulation results of the 15 pF tunable capacitor shown in Figure 6.

The implementation of larger value capacitors becomes more challenging as the movable shuttle gets longer, hence increasing the possibility of stiction to the handle layer. This can be taken care of by using a thicker buried oxide layer. The residual stress in the polysilicon is also more pronounced in larger devices, leading to bending of structures that hampers the device performance. Therefore, controlling the deposition and annealing parameters (pressure, gas flow rate, temperature, and time) of the polysilicon are crucial to the successful fabrication of large-value capacitors. By characterizing the process parameters, a 32 pF and a 106 pF tunable capacitor were successfully fabricated. The

tuning curve of the 32 pF two-port tunable capacitor is shown in Figure 8. A maximum capacitance change of 218 % is observed for this capacitor with a tuning voltage of 6 V.

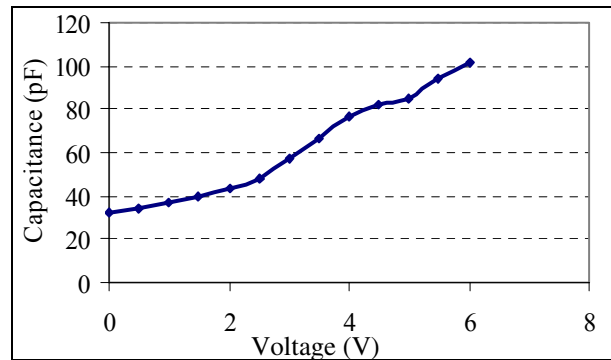
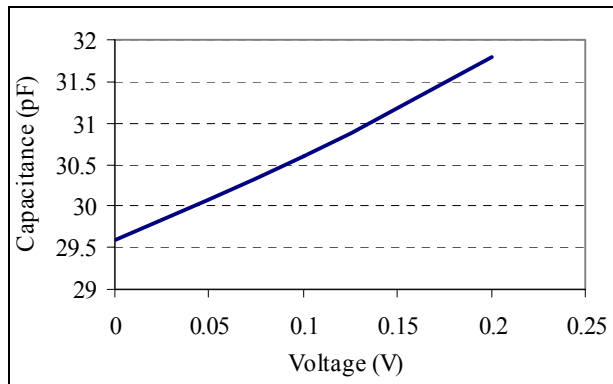
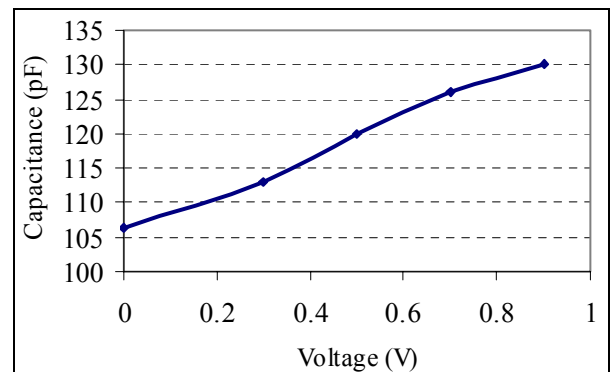


Figure 8: C-V tuning curve of a 32 pF two-port HARPSS capacitor, showing a maximum tuning of 218 %.

Figures 9 (a) and (b) show the tuning curves of the actuation and the parallel plate ports of a 60 μm thick 106 pF one-port tunable capacitor, respectively. As expected, the comb-drive capacitance changes linearly with the applied DC voltage. The large parallel-plate capacitor with an air gap aspect-ratio of 60 varies over 23.5 pF by the application of only 0.9 V. This capacitor occupies 8 mm \times 1 mm of die area and can be further reduced in size by increasing the aspect-ratio of the capacitive gap, which is feasible using the proposed self-aligned HARPSS process.



(a)



(b)

Figure 9: Tuning curves of (a) the actuation and (b) the parallel-plate sense port of a 60 μm thick tunable capacitor, showing a capacitance change of 23.5 pF with only 0.9 V.

Ideally, the design provides infinite tuning as the parallel-plate gap can be reduced to very small values with actuation travel range of $< 1\mu\text{m}$. The main issue that impedes an ideal tuning is that the comb-drive fingers are not straight due to the non-ideal trench profile and residual stress in the polysilicon, which leads to the lateral snapping of the comb-drive fingers.

To appreciate the low tuning voltage of the HARPSS actuator, a one-port capacitor is designed with lithographically-defined parallel-plate actuator (Figure 10). The close-up SEM view shown in Figure 11 compares the sub-micron HARPSS gap with the lithographically defined capacitive gaps at the actuator.

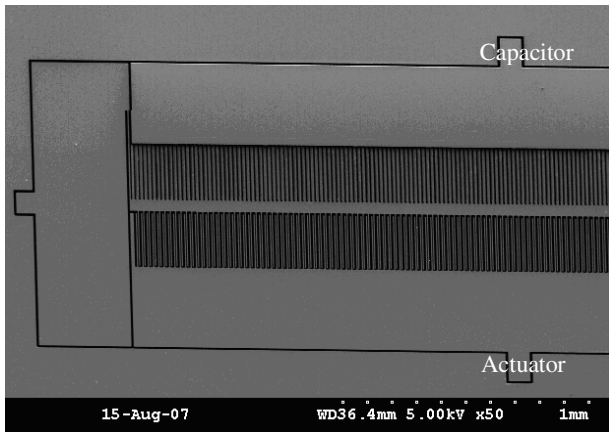


Figure 10: SEM view of a one-port HARPSS tunable capacitor with lithographically defined parallel-plate actuator.

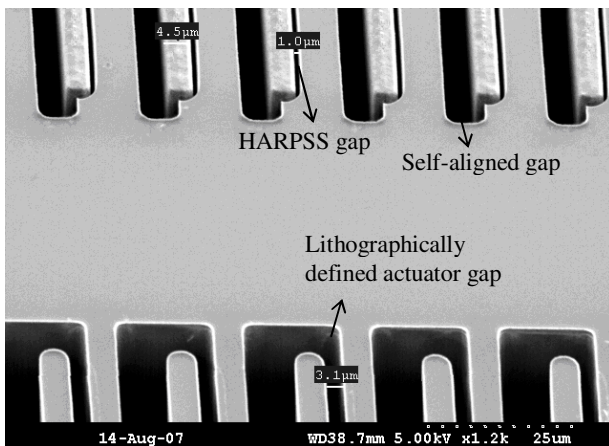


Figure 11: Close-up SEM view of the one-port HARPSS tunable capacitor with lithographically defined parallel-plate actuator.

Figure 12 shows the tuning result obtained for the large-value capacitor of Figure 10. Compared to tuning voltages obtained for parallel-plate HARPSS (shown in Figure 9), the actuation voltage has increased to more than 25 V as a result of a larger gap and lesser actuator capacitance density.

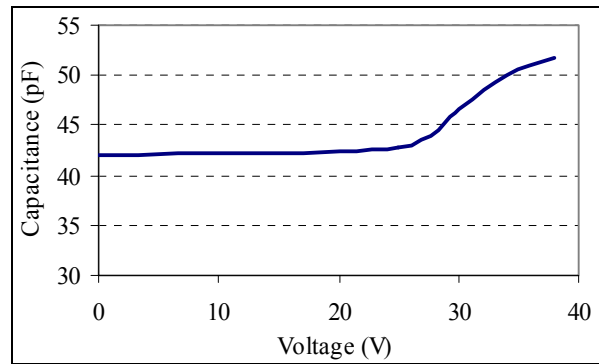


Figure 12: C-V tuning curve of a 42 pF one-port HARPSS capacitor with lithographically-defined parallel-plate actuator. The tuning voltages are high as a result of larger actuation gaps.

5. CONCLUSION

The self-aligned HARPSS fabrication process was presented. This process offers the possibility of having the sub-micron capacitive HARPSS gap together with several self-aligned gaps, which were not available using the conventional HARPSS. Using this new fabrication process, several large-value low-voltage two-port tunable capacitors are reported. With a capacitive gap of 800 nm and an aspect-ratio of 87, a maximum tuning of 240 % was observed for a 15 pF two-port tunable capacitor fabricated on a 70 μm thick SOI substrate. Using the proposed fabrication process, the aspect-ratio of such devices can easily be extended to more than 200, yielding much larger-value capacitors in the same die area.

6. ACKNOWLEDGEMENTS

This project was funded by DARPA under the Analog Spectral Processors (ASP) program. Authors would like to thank the staff at the Georgia Tech Microelectronics Research Center (MiRC) for their assistance.

REFERENCES

- [1] C. Tsai, et al., "An isolated tunable capacitor with linear capacitance-voltage behaviour," *Transducers 2003*, Boston, MA, June 2003, pp. 833 - 836.
- [2] D. McCormick, et al., "Ultra-wide tuning range silicon MEMS capacitors on glass with tera-ohm isolation and low parasitics," *Transducers 2005*, Seoul, Korea, June 2005, pp. 1075- 1079.
- [3] F. Ayazi and K. Najafi, "High aspect-ratio combined poly and single-crystal silicon (HARPSS) MEMS technology," *IEEE Journal of Microelectromechanical Systems*, Vol. 9, pp. 288-294, Sept. 2000.
- [4] P. Monajemi and F. Ayazi, "A high-Q low-voltage HARPSS tunable capacitor," *IEEE IMS '05*, Long Beach, CA, June 2005, pp. 749-752.
- [5] S. Pourkamali, et al., "High-Q single crystal silicon HARPSS capacitive beam resonators with sub-micron transduction gaps," *IEEE Journal of Microelectromechanical Systems*, Vol. 12, No. 4, pp. 487-496, August 2003.