RF SWITCHES USING PHASE CHANGE MATERIALS

Yonghyun Shim[1], Gwendolyn Hummel[1,2], and Mina Rais-Zadeh[1,3]
[1]Electrical Engineering Department, University of Michigan, Ann Arbor, MI 48109, USA
[2]Illinois Institute of Technology, Chicago, IL 60647, USA
[3]Mechanical Engineering Department, University of Michigan, Ann Arbor, MI 48109, USA

ABSTRACT

Phase change materials are attractive candidates for use in ohmic switches as they can be thermally transitioned between amorphous and crystalline states, showing several orders of magnitude change in resistivity. Phase change switches are fast, small form factor, and can be readily integrated with MEMS and CMOS electronics. As such, they have a great potential for implementing next-generation high-speed reconfigurable RF modules. In this paper, we report on the RF properties of germanium tellurium, a PC material, and its use in RF switching applications. Intrinsic resistance and capacitance at the ON (crystalline) and OFF (amorphous) states of a directly heated switch are compared and characterized. Other properties such as phase transition conditions, insertion loss, return loss, and power handling capability of the switch are also measured and analyzed.

INTRODUCTION

Recent advances in solid-state devices have led to high-performance RF switches operating at frequencies up to a few GHz [1]. RF microelectromechanical system (MEMS) switches have been investigated vigorously for higher frequencies, as they offer several advantages, including higher linearity and lower power consumption, compared to their solid-state counter parts [2], [3]. During the past few decades, several companies have started the production of MEMS switches for tunable RF solutions [4]-[7]. Very recently, resistance change or phase change (PC) materials have been investigated for RF switching applications [8]. PC materials exhibit a low resistance at the crystalline state and a high resistance at the amorphous state. When sandwiched between two metal layers (in a via configuration), the PC material can be used as an ohmic switch. Switched OFF (change from the crystalline to the disordered high-resistance phase) can be achieved by fast heating to a high temperature and fast cooling. The switch can be turned back ON by heating the PC layer to the crystallization temperature and by slowly removing the heat. The transition temperature can be reached by employing hot probes in contact with the PC material [8], using lasers [9], or passing current either through the PC material itself (direct heating) [10], or through a separate heater layer adjacent to the PC layer (indirect heating) [11].

PC materials from $Ge_xSb_yTe_z$ (GST) alloys have been used in memories due to their fast switching time, small size, and CMOS compatibility. $Ge_{50}Te_{50}$ (or GeTe), one of stoichiometric compositions of GST, is most suited for use in RF switches because of its low crystalline resistivity and high resistance change ratio of up to 10^6 [12]. Compared to MEMS switches, noticeable advantages of PC switches are lower ON resistance (for a similar size switch), easier integration with CMOS, and lower gate voltages [8]. Also, PC switches do not have special packaging requirements. However, there are still several unknowns about RF properties of GeTe and a lot of room for improvement of the PC switch performance [8]. In this paper, we report on complete RF characterizations of directly heated GeTe ohmic switches. Intrinsic properties of several GeTe switches (vias) are characterized at both crystalline and amorphous states. Joule heating simulations are performed to estimate the optimal heating condition for the phase transition. A directly heated GeTe switch is demonstrated with an insertion loss of < 1 dB and isolation of > 18 dB up to 25 GHz. The modeled response of the switch is in good agreement with the measured response. Important RF properties of the switch, including third order intercept point (IIP_3) and 1dB compression point (P1dB), are measured and analyzed. To the best of our knowledge, this is the lowest loss PC switch reported to date.

DEVICE ARCHITECTURE

Switches are fabricated on a passivated silicon substrate. The cross-section view of a directly heated GeTe switch is shown in Fig. 1 (a). The PC switch stack consists of gold top and bottom electrodes, and thin chrome diffusion barrier layers connecting the electrodes to the GeTe layer through openings in silicon dioxide insulation layers. All metal layers are lift-off patterned. GeTe is sputter deposited using a Mitsubishi Materials [13] $Ge_{50}Te_{50}$ target of 99% of purity. The silicon dioxide layer is PECVD deposited at 200 °C, the highest temperature reached during the fabrication process. RF properties of GeTe are extracted from the two GeTe switch configurations shown in Fig. 1(b), (c). For all switches, crystallization and amorphization are achieved using the direct heating scheme, where the required DC bias for phase transition is applied through the same electrodes as the RF signals.

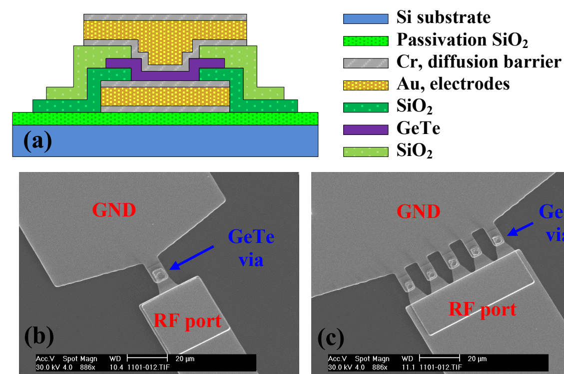

Figure 1: (a) A schematic diagram showing the cross-section of a PC switch. SEM views of (b) a single 3×3μm² via (Design 1) and (c) five parallel-connected 2×2μm² vias (Design 2).

Intrinsic RF Properties

The equivalent lumped-element model of a two-port GeTe switch is shown in Fig. 2. At both states of the switch, R_I is the intrinsic resistance of GeTe, which experiences a large change between amorphous (OFF state) and crystalline (ON state) phases. C_I models the parasitic capacitance of the GeTe layer. GeTe is known to have a relatively high permittivity (ε_r >15). Therefore, reduction of the switch size is important to achieve good isolation at high frequencies. As GeTe has a small intrinsic ON resistivity compared to other stoichiometric composition of GST, the dimension of the via can be reduced for a better isolation without sacrificing the insertion loss. The model at the OFF state is shown in Fig. 2 (c); here, R_{NI} and C_{NI} models the resistance and capacitance of the GeTe grains with incomplete phase transition. C_P is the parasitic capacitance of the substrate, and L_S and R_S model the routing layer that connects the switch to the probe pads. From Fig. 2, the input impedance Z_{11} can be expressed as,

$$Z_{11} = [(Z_S \parallel Z_P) + Z_I] \parallel Z_P + Z_S \,. \qquad (1)$$

where $Z_S = R_S + j\omega L_S$, $Z_P = 1/j\omega C_P$, and Z_I is the intrinsic impedance of GeTe via. From Equation (1), parasitic impedance Z_S and Z_P can be de-embedded from Z_I , using open calibration fixture $Z_{11,O}$ and short calibration fixture $Z_{11,S}$ fabricated on the same substrate. At the ON state, intrinsic resistance R_I of GeTe via can be extracted as

$$R_I \approx re[1/(Y_{11} - Y_{11,O}) - 1/(Y_{11,S} - Y_{11,O})]. \qquad (2)$$

At the OFF state, the two most dominant lumped elements, R_{NI} and C_I, can be extracted as

$$R_{NI} \approx re[Y_{11} - Y_{11,O}]/(im[Y_{11} - Y_{11,O}])^2 \,. \qquad (3)$$

$$C_I \approx im[Y_{11} - Y_{11,O}]/\omega \,. \qquad (4)$$

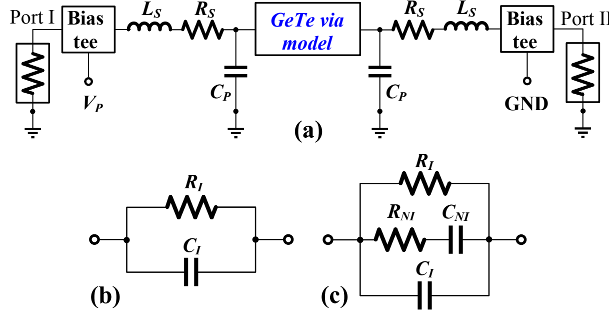

Figure 2: Equivalent electrical model of a GeTe switch; (a) the entire model including electrodes and bias control; (b) GeTe via model at crystalline state; (c) GeTe via model at amorphous state.

Two different configurations of GeTe switches in Fig. 1 are fabricated and measured to extract these intrinsic properties. Design 1 is built as a single one-port GeTe via (3×3 μm^2) while Design 2 is implemented as multiple GeTe vias with a smaller individual via size (2×2 μm^2). On-wafer measurements are performed using the Cascade ACP GSG probes, an Agilent E5061B ENA for low frequency measurement (< 3 GHz), and an Agilent N5242A PNA-X for high frequency (10 MHz–25 GHz) measurements. R_I, R_{NI}, and C_I are measured and extracted using Equations (2), (3) and (4), as shown in Figs. 3 and 4. As expected, Design 2 shows better ON resistance than Design 1, but also has a higher parasitic capacitance. An advantage of Design 2 is that phase transition could be more reliable, as smaller vias can be more uniformly heated and the state of the via is better controlled using the Joule heating method. At the OFF state, R_I is in the MΩ range; thus, R_{NI}, which models the resistance of areas that are not completely amorphized, becomes more dominant at higher frequencies, reducing the effective resistance (Fig. 3 (b)). Figure 5 shows the measured S_{11} of Design 1 and Design 2, compared with the modeled response using the equivalent circuit in Fig. 2. The measured and modeled responses are in excellent agreement.

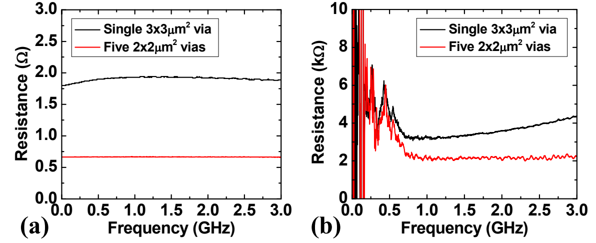

Figure 3: Measured resistance of a single 3×3μm² via (Design 1) and five 2×2μm² parallel vias (Design 2); (a) R_I at the crystalline state; (b) R_{NI} at the amorphous state.

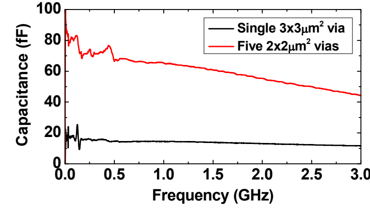

Figure 4: Measured intrinsic capacitance (C_I) of the single 3×3μm² via and five 2×2μm² vias at the amorphous state.

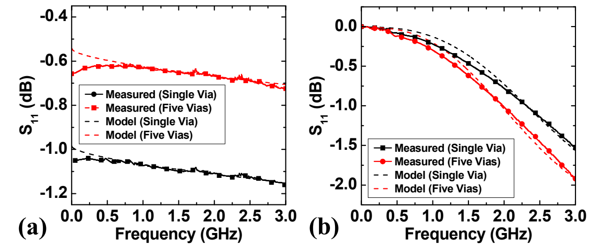

Figure 5: Measured S_{11} compared with simulation result using equivalent lumped element models; (a) crystalline state; (b) amorphous state.

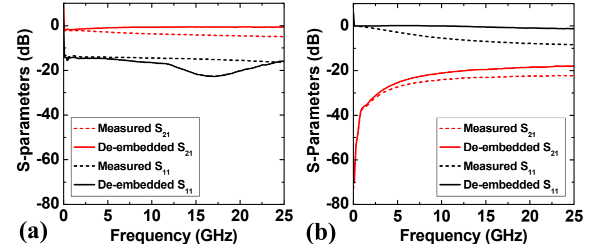

Figure 6: Measured and de-embedded S-parameters (a) at the crystalline state and (b) at the amorphous state.

Figures 6 (a) and (b) show the measured and de-embedded *S*-parameters of a two-port 3×3 μm^2 switch. To extract intrinsic S-parameters of GeTe via, the contact resistance and pad parasitics are de-embedded using test fixtures fabricated on the same wafer. The de-embedded insertion loss is less than 1 dB while isolation is better than 18 dB up to 25 GHz. This switch exhibits comparable performance to that of MEMS- and solid-state-based switches (see Table 1). Other characteristics of GeTe switches such as switching speed, IIP_3, and P1dB are measured using this switch.

Switching Speed

The setup used for measuring the switching speed is similar to that described in [14]. Crystallization requires moderate level of heating and gradual trailing of the heater bias [10], [11]. Figure 7 shows the crystallization timing diagram. The crystallization time including the stabilization time is less than 20 μs. As shown in Fig. 8, the required pulse width for amorphization is less than 500 ns. The total switching speed of the GeTe via is thus limited by the crystallization time. With sizing the via and a better choice of electrodes and diffusion barriers, heat transfer to GeTe via can be made more efficient and the switching speed can be further improved.

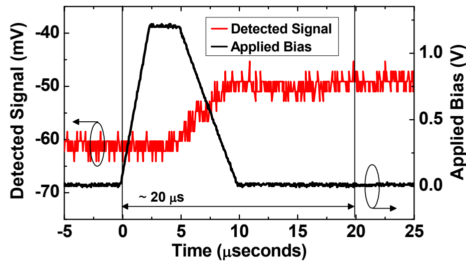

Figure 7: Timing diagram when a 1.2 V pulsed bias with duration of 5 μs and falling time of 5 μs is applied to the switch for crystallization; the total switching time including stabilization is around 20 μs.

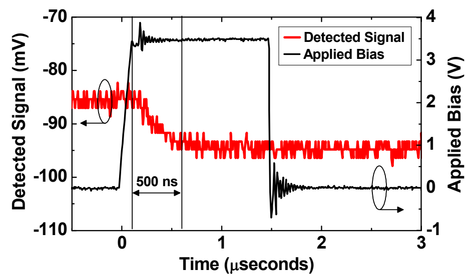

Figure 8: Timing diagram when 3.5 V bias with duration of 1.5 μs is applied to the switch for amorphization.

IIP_3 Measurement

IIP_3 of the GeTe switch is measured using two RF sources, isolators, a power combiner, and a spectrum analyzer. Since the amorphous state has a larger temperature coefficient of electrical resistance [12], IIP_3 of the amorphous state is expected to be worse than the crystalline state. This is consistent with the measurement result in Fig. 9 (a) and (b); IIP_3 at the crystalline state is extracted to be 37 dBm while the IIP_3 at the amorphous state is around 33 dBm. Also as expected, the switch linearity is worse at lower frequencies (Fig. 9 (c) and (d)). At the amorphous state, IIP_3 at 500 MHz is limited to 27 dBm while IIP_3 at 2 GHz is around 32 dBm. At all states and frequencies, the measured IIP_3 of the GeTe switch is better than CMOS switches and comparable to high-performance MEMS switches (Table 1).

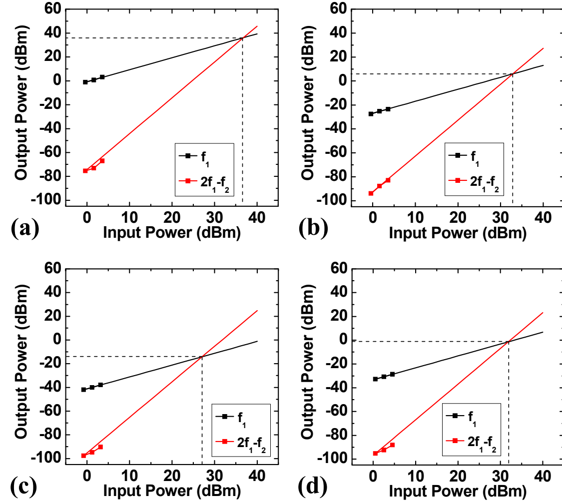

Figure 9: Measured IIP_3 of a directly heated 3×3 μm^2 PC via; (a) crystalline state with 50 kHz of frequency offset at 3.9 GHz; (b) amorphous state with 50 kHz of frequency offset at 3.9 GHz; (c) amorphous state with 50 kHz of frequency offset at 500 MHz; (d) amorphous state with 50 kHz of frequency offset at 2 GHz.

1dB Compression Point

Due to thermal transition mechanism of GeTe, the power handling capability can be a concern for phase change switches. As shown in Fig. 10, P1dB of GeTe switch is above 20 dBm at both crystalline and amorphous states. Although P1dB could not be accurately extracted due to tool limitations and P1dB may be higher than 20 dBm, GeTe switch is proved to handle sufficiently high input power, suitable for use in reconfigurable RF front-ends. P1dB could be potentially improved by optimal choice of electrodes and diffusion barriers.

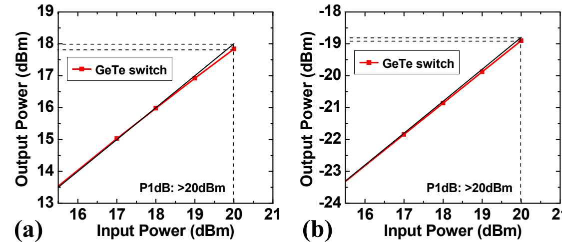

Figure 10: Measured P1dB of a directly heated 3×3 μm^2 PC via; (a) crystalline and (b) amorphous states at 1GHz.

HEAT SIMULATION

Joule heating simulations are performed using COMSOL finite element tool [15]. In these simulations, the structure of the GeTe switch in Fig. 1 (b) is simulated reflecting the material properties extracted from the

high-frequency measurements. Figure 11 shows the simulated heat distribution across the switch stack, indicating the bias conditions needed to reach crystallization or amorphization. As shown in Fig. 11 (a), amorphization (switch OFF) can be reached by applying a 3.5V DC pulse of 300 ns, reaching the melting point of GeTe (~480 K). As expected and consistent with the measured response shown earlier, crystallization (switch ON) needs a longer duration pulse (~ 30 μs) (Fig. 11 (b)).

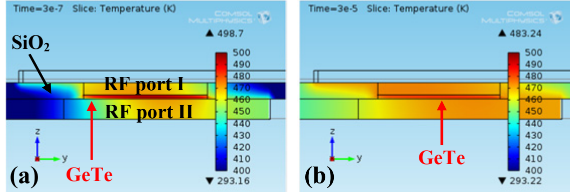

Figure 11: Simulated temperature distribution across a directly heated 3×3 μm^2 PC via; (a) when 3.5 V is applied for 300 ns to amorphize the switch; (b) when 2 V is applied for 30 μs to crystallize the switch.

CONCLUSIONS

Fundamental RF properties of phase change switches using GeTe are characterized and analyzed. The resistance ratio between the crystalline and amorphous states reaches 10^5, which is close to the bulk material property and sufficient for most switching applications. Overall, RF switches using GeTe can provide better switching speed and higher integration density than conventional MEMS switches. When monolithically integrated with MEMS passive components, such as high-*Q* inductors and varactors, this switch technology can be used to implement reconfigurable RF modules. To become a viable solution, the switch reliability should be further improved. GeTe switch reliability is a topic of future research.

ACKNOWLEDGEMENTS

This project was funded by Harris Corporation and by National Science Foundation (Award #1055308 and 1247565). Authors would like to thank Dr. Amir Mortazawi and Mr. Seungku Lee for their help with IIP_3 measurements. Devices were fabricated at the Michigan Nanofabrication Facility (LNF).

REFERENCES

[1] G. Rebeiz, et al, "Tuning in to RF MEMS," *IEEE Microwave Magazine*, pp. 55-72, Oct. 2009.
[2] Infineon, *RF CMOS SPDT Switches BGS12xx for Applications up to 3GHz*, Application Note No. 175, Rev. 1.1, Feb. 2009.
[3] V. Kaper, et al, "Monolithic AlGaN/GaN HEMT SPDT switch," *12th GAAS Symp.*, Amsterdam, 2004.
[4] K. Entesari and G. M. Rebeiz, "RF MEMS, BST and GaAs varactors system-level response in complex modulation systems," *Int. J. RF Microwave Comput. Aided Eng.*, vol. 18, pp. 86–98, Jan. 2008.
[5] www.radantmems.com/
[6] www.rfmd.com/
[7] www.wispry.com/
[8] H. Lo, "Probe reconfigurable phase change material switches," Ph.D. Thesis, Carnegie Mellon University.
[9] W. J. Wang, et al, "Nonvolatile phase change memory nanocell fabrication by femtosecond laser writing assisted with near-field optical microscopy," *J. Appl. Phys.*, vol. 98, 124313, 2005.
[10] C.-Y. Wen, et al, "A phase-change via-reconfigurable on-chip inductor," *IEEE Int. Electron Device Meeting*, pp. 237-240, Dec. 2010.
[11] K. N. Chen, et al, "Programmable via using indirectly heated phase-change switch for reconfigurable logic applications," *IEEE Electron Device Letters*, Vol. 29, No. 1, Jan. 2008.
[12] S. Raoux, et al, "Crystallization characteristics of Ge-Sb and Ge-Te phase change materials," *EPCOS*, pp. 91-98, Sep. 2009.
[13] www.mmc.co.jp/
[14] Y. Shim, et al, "A high-performance continuously tunable MEMS bandpass filter at 1 GHz," *IEEE Trans. on Microwave Theory and Techniques*, vol. 60, no. 8, pp.2439-2747, Aug. 2012.
[15] www.comsol.com/
[16] R. Chan, et al, "Low-actuation voltage RF MEMS shunt switch with cold switching lifetime of seven billion cycles," *Journal of Microelectromechanical Systems*, vol. 12, no. 5, pp. 713-719, Dec. 2003.
[17] C. D. Patel, et al, "A high power (>5 W) temperature stable RF MEMS metal-contact switch with orthogonal anchors and force-enhancing stoppers," *IEEE IMS*, pp. 1-4, June 2011.
[18] M. C. Yeh, et al, "Design and analysis for a miniature CMOS SPDT switch using body-floating technique to improve power performance," *IEEE Trans. on Microwave Theory and Techniques,* vol. 54, no. 1, pp. 31-39, Jan. 2006.

CONTACT

*Yonghyun Shim, yhshim@umich.edu

Table 1: Performance comparison of ohmic switches using different technologies.

	Chan '03 [16]	Patel '11 [17]	Yeh '06 [18]	Wen '10 [10]	*This work*
Loss (ON)	0.05 dB @ 10 GHz 0.03 dB @ 20 GHz	0.20 dB @ 10 GHz 0.30 dB @ 20 GHz	1.1 dB @ 5.8 GHz 2.0 dB @ 10 GHz	Not reported R_{ON} = 1.1 Ω	0.66 dB @ 10 GHz 0.63 dB @ 25 GHz
Isolation (OFF)	26 dB @ 10 GHz 25 dB @ 20 GHz	16 dB @ 10 GHz 11 dB @ 20 GHz	27 dB @5.8 GHz 22 dB @ 10 GHz	Not reported R_{OFF} = 33 kΩ	21 dB @ 10 GHz 18 dB @ 25 GHz
Tuning bias	15 V	80-90 V	1.8 V	1-10 V	1-4 V
Tuning speed	< 25 μs	< 5 μs	< 1 μs	> 1000 μs	0.5-20 μs
Power handling capability	N/A	> 37 dBm	P1dB = 18 dBm	N/A	P1dB > 20 dBm IIP_3 > 27 dBm
Technology	MEMS	MEMS	CMOS	Phase change	Phase change
Size	<150 × 200 μm^2	<155 × 130 μm^2	<170 × 170 μm^2	<1 × 1 μm^2	< 3 × 3 μm^2