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COURSE ANNOUNCEMENT: Fall 2002

EECS 579: Digital System Testing

3 Credits, Tue and Thu 9:00-10:30 a.m., EWRI 156

Instructor: Prof. P. Mazumder, EECS Department

Contents: Introduction to fault-tolerant computing and digital testing. Fault classification, characterization of physical defects, fault modeling, hierarchy of fault models, and testing terminologies. Test generation algorithms. Combinational circuit testing: D-algorithm, PODEM, FAN, etc. for stuck-at faults; Bridging faults testing; Delay faults testing. Functional testing of arithmetic and regular arrays. Synchronous and asynchronous sequential circuit testing. Memory (RAM, ROM and CAM), register file, and FIFO buffer testing. IDDQ testing and current monitoring. Functional testing of microprocessors and microcontrollers. Design for testability. Testability measures. Boundary scan and partial scan design. Test data and response compression. Built-in self-testing. Self-testing of RAMs, ROMs and PLAs. Pseudo-random testing. Estimation of test coverage by random test vectors: memories and logic blocks. System-on-chip (SOC) testing. Intellectual Property (IP) and embedded core testing. Modern issues in digital testing.

Prerequisite: EECS 478 or Instructor's Consent

Goal: This course examines in depth theories and techniques for testing multimillion transistor VLSI chips. As the VLSI technology is inching towards nanoelectronic dimensions, on one hand, chips are assuming gargantuan complexities of near 100 million transistors, and, on the other, deep submicron (DSM) process technologies are inducing process- and layout-related obfuscating and new failure mechanisms. The faults which are often sensitive to patterns stored in the neighborhood of a faulty component are difficult to sensitize through limited pin accessibility. The most elusive faults pose great difficulty in testing a VLSI chip comprehensively before it is shipped out to customers. Commercial VLSI chips such as Intel's *Pentium* and *Merced* as well as memory chips like 256-Mbit DRAM and 64-Mbit SRAM chips now contain several million transistors, and, by the turn of this century, the chip integration is expected to reach several billion transistors. This spectacular growth of VLSI technology is only economically viable, if high-quality Automatic Test Equipment (ATE) and accompanying CAD tools are commercially available for testing VLSI chips in reasonable time and at moderate cost.

The objective of this course is to understand the failure mechanisms in VLSI chips and characterization of failures at various levels of circuit hierarchy and finally to develop appropriate testing strategies. Test generation algorithms are segregated into different classes based on the circuits they are intended to test: combinational circuit testing, synchronous and asynchronous sequential logic testing in the presence of flip-flops, and testing of large storage arrays such as RAM's, ROM's and FIFO's. Further, how much one needs to test also depends on the composition of circuit blocks: a simple logical fault describing a signal line is shorted to ground or to power supply can suffice for random and glue logic scattered all over a chip, while for extremely fine-grained array of memory cells, occupying a large chunk of chip real estate, may require more complex fault model that will account for anomalies in masking, process parameters and chip layout.

Embedded circuit blocks like memories and PLAs cannot be fully tested by ATE because of poor controllability and observability posed by limited I/O pins. Built-in self-testing of these circuit elements must be accomplished in conjunction with other circuit blocks so that the overall chip is fully tested. It is not sufficient to know a disparate set of testing techniques, it will be imperative that a good test engineer must know how to coordinate different testing tasks (combinational testing, sequential testing, memory testing, scan testing, BIST, etc.) so that a chip is tested as a whole entity.

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Now with the advent of System-on-Chip (SOC) design concept, more and more ASIC vendors are increasingly using pre-designed embedded cores, frequently known as Intellectual Property (IP) cores. Such IP cores pose immense challenges to VLSI test engineers since they are often oblivious of internal structures of these cores supplied by third-party VLSI cell library vendors. The goal of this course will be to understand these testing issues and to develop appropriate strategies to tackle these problems.

Students majoring in VLSI kernel and CSE hardware are encouraged to take this course.

Text Book: Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits by M. L. Bushnell and V.D. Agarwal, *Kluwer Academic Press*, Boston 2000.

Supplementary Text Book: Testing and Testable Design of Random-Access Memories by P. Mazumder and K. Chakraborty, *Kluwer Academic Publishers*, New York, 1996, 430 pages.

Digital System Testing and Testable Design by M. Abramovici, M. A. Breuer, and A.D. Friedman, *IEEE Press*, New York, 1990, 652 pages (an early version of the same book was published by *Computer Science Press*).

Built-in Test for VLSI: Pseudorandom Techniques by P. H. Bardell, W.H. McAnney, and J. Savir, *John Wiley and Sons*, Somerset, New Jersey, 1987.

Evaluation: Homework (30%), Project (30%), Midterms (20%) and Final Exam (20%)

In order to attend the course, you must formally register. Unless the class size is more than 25 students, visiting will be discouraged and may not be approved.

For further queries, speak to the instructor at 763-2107, or send e-mail at mazum@eecs, or see him personally at Room No. EECS 2215.

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Text Book: *Essentials of Electronic Testing* by Bushnell and Agrawal, *Kluwer Academic Publisher* (2000)

Date	Book Chapters		References	Topic	HW/Exam
3-Sep-02	**Ch 1:** 1.1-1.5	pp. 1-15		Introduction to Testing	
5-Sep-02	**Ch 2:** 2.1-2.4	pp. 17-34		Testing Process and Test Equipment	
10-Sep-02	**Ch 3:** 3.1-3.4	pp. 35-53		Test Economics and Test Quality	
12-Sep-02	**Ch 4:** 4.1-4.5	pp. 57-78	Ref 1: pp. 96-117	Fault Modeling	
17-Sep-02	**Ch 4:** 4.1-4.5	pp. 57-78	Ref 1: pp. 96-117	Fault Modeling	
19-Sep-02	**Ch 7:** 7.1-7.4	pp. 155-176	Ref 1: pp. 117-128	Testing of Gates	
24-Sep-02	**Ch 7:** 7.1-7.4	pp. 155-176	Ref 1: 117-121	Testing of Simple Gated Networks	HW 1 (Due)
26-Sep-02	**Ch 7:** 7.4-7.8	pp. 176-210	Ref 1: 181-281	Combinational Circuit Testing	
1-Oct-02	**Ch 7:** 7.4-7.8	pp. 176-210	Ref 1: 181-281	Combinational Circuit Testing	Proposal
3-Oct-02	**Ch 7:** 7.4-7.8	pp. 176-210	Ref 1: 181-281	Combinational Circuit Testing	HW 2 (Due)
8-Oct-02	**Ch 7:** 7.4-7.8	pp. 176-210	Ref 1: 181-281	Combinational Circuit Testing	
10-Oct-02	**Ch 7:** 7.4-7.8	pp. 176-210	Ref 1: 181-281	Combinational Circuit Testing	Midterm 1
15-Oct-02	**Ch 5:** 5.1-5.7	pp. 81-125	Ref 1: 131-174	Fault Simulation	
17-Oct-02	**Ch 5:** 5.1-5.7	pp. 81-125	Ref 1: 131-174	Fault Simulation	HW 3 (Due)
22-Oct-02	**Ch 6:** 6.1-6.3	pp. 129-150		Testability Measures	Progress-1
24-Oct-02	**Ch 8:** 8.1-8.3	pp. 211-240		Sequential Circuit Test Generation	
29-Oct-02	**Ch 13:** 13.1-13.7	pp. 439-460		IDDQ Test	
31-Oct-02	**Ch 10:** 10.1-10.5	pp. 309-364		Analog and Mixed Signal Test	HW 4 (Due)
5-Nov-02	**Ch 10:** 10.1-10.5	pp. 309-364		Analog and Mixed Signal Test	
7-Nov-02	**Ch 11:** 11.1-11.6	pp. 385-413		Analog and Mixed Signal Test	Progress-2
12-Nov-02	**Ch 9:** 9.1-9.5	pp. 253-262	Ref 2: 45-70	Memory Test	
13-Nov-02	**Ch 9:** 9.1-9.5	pp. 253-262	Ref 2: 76-150	Memory Test	HW 5 (Due)
19-Nov-02	**Ch 9:** 9.1-9.5	pp. 253-262	Ref 2: 76-150	Memory Test	
21-Nov-02	**Ch 14:** 14.1-14.5	pp. 465-485	Ref 3: Chap 3	Design for Test	Midterm 2

26-Nov-02	**Ch 14: 14.1-14.5**	**pp. 465-485**	**Ref 3: Chap 4**	**Design for Test**	**HW 6 (Due)**
28-Nov-02	**Thanks Giving**			**No Class**	
2-Dec-02	**Ch 14: 14.1-14.5**	**pp. 465-485**	**Ref 3: Chap 4**	**Design for Test**	Progress-3
4-Dec-02	**Ch 15: 15.1-15.5**	**pp. 489-540**	**Ref 3: Chap 5**	**Built-in Self-Test**	
9-Dec-02	**Ch 15: 15.1-15.5**	**pp. 489-540**	**Ref 2: 221-322**	**Built-in Self-Test**	
11-Dec-02	**Ch 16: 16.1-16.2**	**pp. 549-569**		**Boundary Scan standard**	**Final Project**
13-Dec-02	**Ch 18: 18.1-17.2**	**pp. 595-608**		**SOC Testing**	
22-Dec-02					**Final Exam**

Ref 1: Digital Testing by Abaramovici, Breuer and Friedman
Ref 2: Testing and Testable Design of RAMs by Mazumder and Chakraborty
Ref 3: Built-in Self-Testing by Bardell, McAnney and Savir