PUBLICATIONS OF PINAKI MAZUMDER

Books and Book Chapters

Books

1. P. Mazumder and K. Chakraborty, "Testing and Testable Design of Random-Access Memories", ***Kluwer Academic Publishers***, 1996 (428 pages).

2. P. Mazumder and E. Rudnick, "Genetic Algorithms for VLSI Layout and Test Automation", ***Prentice Hall***, 1999 (460 pages).

3. K. Chakraborty and P. Mazumder, "Fault Tolerance and Reliability Aspects of Random-Access Memories," ***Prentice Hall***, 2002. (440 pages).

4. P. Mazumder, "Introduction to Digital Systems", Video Book on DVD, produced at MGM Studio (Orlando, Florida), ***Laureate Education, Inc.,*** 2005.

5. P. Mazumder, "Models and Techniques for VLSI Routing", ***Springer Verlag***, (under preparation)

6. R. Rajasuman (Editor) and P. Mazumder (Editor), "Semiconductor Memories: Testing and Reliability", ***Computer Science Press***, May 1998.

7. R. J. Lomax (Editor) and P. Mazumder (Editor), "Great Lakes Symposium on VLSI, 1999", ***Computer Science Press***, March 1999.

8. P. Mazumder and K. Shahookar, "MathGuru Tutorial" for K-12 Education Software.

Book Chapters

9. K. Shahookar and P. Mazumder, "Standard Cell Placement and the Genetic Algorithm", Book chapter in "Advances in Computer-Aided Engineering Design, Vol. II", I. N. Hajj (editor), ***Jai Press***, Greenwich, Connecticut, 1990, pp. 159-234.

10. W. K. Fuchs, M. F. Chang, S. Y. Kuo, P. Mazumder and C. B. Stunkel, "The Impact of Parallel Architecture Granularity on Yield", Book chapter in "Designing for Yield," Moore, Strowjas and Maly (editors), ***Adam Hilger Publisher***, 1988.

11. P. Mazumder and J. H. Patel, "Parallel Testing of Parametric Faults in DRAM", in "Advanced Research in VLSI: Design and Applications of Very Large Scale Systems", Leighton and Allen (editors**),** ***MIT Press***, 1988. (Presented at the 5-th Massachusetts Institute of Technology Conference on VLSI).

12. P. Mazumder, "Design of a Fault-Tolerant DRAM with New On-Chip ECC", Book Chapter in "Defects and Fault Tolerance in VLSI Systems", I. Koren (editor), ***Plenum Press***, 1989.

13. H. Chan and P. Mazumder, "A Systolic Architecture for High-Speed Hyper-graph Partitioning Using a Genetic Algorithm", Book Chapter in "Progress in Evolutionary Computation", Vol. 956**,** ***Springer- Verlag***, Heildelberg, 1995, pp. 109-126.

Reviewed Journal Publications

Cataloging of Journal Publications

1. ***Semiconductor Memory Systems*** - Papers: 14, 15, 16, 17, 18, 19, 20, 21, 22, 28, 30, 36, 44, 81, 96
2. ***Quantum Tunneling Circuits and CAD Tools*** - Papers: 33, 35, 36, 37, 38, 39, 47, 48, 49, 53, 70, 97, 99, 100, 101
3. ***VLSI Circuit Optimization Techniques*** - Papers: 74, 79, 80, 84
4. ***Bio-Inspired Computing*** - Papers: 57, 62, 64, 65, 69, 92, 93
5. ***Reliable VLSI Systems Design*** - Papers: 23, 24, 25, 26, 27, 28, 31, 34, 75, 77, 78
6. ***Plasmonics and THz Bio-Sensing*** - 86, 88, 89, 90, 91, 98
7. ***Quantum Physics and VLSI Synergies*** - Papers: 40, 41, 42, 45, 50, 51, 76, 84, 85, 87, 92, 93, 94, 95, 100, 101
8. ***EM Theory and VLSI Synergies*** - Papers: 71, 72, 73, 82, 83, 91, 98
9. ***Innovative VLSI Chip and System Design*** - Papers: 29, 32, 46, 52, 54, 55, 56, 58, 59, 67, 97
10. ***VLSI Complexity Issues*** - Papers: 43, 60, 61, 63, 66, 68

14. P. Mazumder, J. H. Patel and W. K. Fuchs, "Methodologies for Testing Embedded Content-Addressable Memories", ***IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems***, Jan. 1988, pp. 11-20.

15. P. Mazumder, "Parallel Testing of Parametric Faults in a Three-Dimensional Dynamic Random-Access Memory", ***IEEE Journal of Solid-State Circuits***, Vol. 23, No. 4, Aug. 1988, pp. 933-942.

16. P. Mazumder and J. H. Patel, "Parallel Testing of Pattern-Sensitive Faults in Random-Access Memory", ***IEEE Transactions on Computers,*** Vol. 38, No 3, Mar. 1989, pp. 394-404.

17. P. Mazumder and J. H. Patel, "An Efficient Built-In Self-Testing Algorithm for Random-Access Memory", ***IEEE Transactions on Industrial Electronics*** (Special Issue on Testing) Vol. 36, No. 3, May 1989, pp. 394-407.

18. J. S. Yih and P. Mazumder, "Circuit Behavior Modeling and Compact Testing Performance Evaluation", ***IEEE Journal of Solid-State Circuits***, Vol. 26, No. 1, Jan. 1991, pp. 62-65.

19. P. Mazumder and J. H. Patel, "A Comprehensive Study of Random Testing for Embedded RAM's Using Markov Chains", ***Journal of Electronic Testing: Theory and Applications***, Vol. 3 No. 4, Nov. 1992, 235-250.

20. S. Mohan and P. Mazumder, "Analytical and Simulation Studies of Failure Modes in SRAM's Using High-Electron Mobility Transistors", ***IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems***, Vol. 12, No. 12, Dec. 1993, pp. 1885-1896.

21. P. Mazumder and J. P. Hayes, "Testing and Improving the Testability of Multi-megabit Memories", ***IEEE Design and Test of Computers***, Mar. 1993, pp. 6-7.

22. K. Chakraborty and P. Mazumder, "Technology and Layout Related Testing in Static Random-Access Memories", ***Journal of Electronic Testing: Theory and Applications***, Aug. 1994.

23. P. Mazumder, J. H. Patel and J. A. Abraham, "A Reconfigurable Parallel Signature Analyzer for Concurrent Error Correction in Dynamic Random-Access Memory", ***IEEE Journal of Solid-State Circuits***, Vol. 25, No. 3, Jun. 1990, pp. 866-870.

24. P. Mazumder and J. Yih, "Restructuring of Square Processor Arrays by Built-in Self-Repair Circuit," ***IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,*** Vol. 12, No. 9, Sept. 1993, pp. 1255-1265.

25. P. Mazumder, "A New On-Chip ECC Circuit for Correcting Soft Errors in DRAM's with Trench Capacitors," ***IEEE Journal of Solid-State Circuits***, Vol. 27, No. 11, Nov. 1992, pp. 1623-1633.

26. R. Venkateswaran, P. Mazumder and K. G. Shin, "On Restructuring of Hexagonal Arrays," ***IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems***, Vol. 11, No. 12, Dec. 1992, pp. 1574-1585.

27. P. Mazumder and J. Yih, "A New Built-in Self-Repair Approach to VLSI Memory Yield Enhancement by Using Neural-Type Circuits," ***IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,*** Vol. 12, No. 1, Jan. 1993, pp. 124-136.

28. P. Mazumder, "Design of a Fault-Tolerant Three-Dimensional Dynamic Random-Access Memory with On-Chip Error-Correcting Circuit," ***IEEE Transactions on Computers***, Vol. 42, No. 12, Dec. 1993, pp. 1453-1468.

29. M.D. Smith and P. Mazumder, "Analysis and Design of Hopfield-type Network for Built-in Self-Repair of Memories," ***IEEE Transactions on Computers***, Vol. 45, No. 1, Jan. 1996, pp. 109-115.

30. K. Chakraborty and P. Mazumder, "New March Tests for Multi-port RAM Devices," ***JETTA: Journal on Electronic Testing: Theory and Applications***, Vol. 16, No. 4, Aug. 2000, pp. 389-396.

31. P. Mazumder, "Built-In Self-Repair for WSI Hexagonal Processor Arrays," ***IEEE Transactions on VLSI Systems***.

32. A. F. Gonzalez, M. Bhattacharya, S. Kulkarni, and P. Mazumder, "CMOS Implementation of a Multiple-Valued Logic Signed-Digit Adder Based on Negative Differential-Resistance Devices," ***IEEE Journal of Solid-State Circuits***, Vol. 36, No. 6, June 2001, pp. 924-932.

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35. A. Seabaugh and P. Mazumder, "Quantum Devices and Their Applications," ***Proceedings of the IEEE***, Vol. 7, No. 4, April 1999.

36. T. Ueymura and P. Mazumder, "Design and Analysis of Resonant-Tunneling-Diode (RTD) Based High Performance Memory System," ***IEICE Transactions on Electronics*** (Special Issue on Integrated Electronics and New System Paradigms), Vol. E82-C, No. 9, Sept. 1999.

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39. P. Mazumder, S. Kulkarni, G. I. Haddad, and J. P. Sun, "Digital Applications of Quantum Tunneling Devices," ***Proceedings of the IEEE,*** Apr. 1998, pp. 664-688, (**Invited paper**).

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47. S. Mohan, P. Mazumder, G. I. Haddad, R. Mains, and S. Sung, "Logic Design Based on Negative Differential Resistance Characteristics of Quantum Electronic Devices," ***IEE Proceedings-G: Electronic Devices***, Vol. 140, No. 6, Dec. 1993, pp. 383-391.

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94. P. Mazumder, S. Kang, and R. Waser, "Device, Model, and Applications of the Fourth circuit element," ***Proceedings of the IEEE***, 2012. (to appear)

95. W. H. Lee and P. Mazumder, "Color Image Processing Using Multi-Peak RTD's", ***ACM Journal of Emerging Technologies***. (to appear)

96. I. Ebong and P. Mazumder, "Self-Controlled Writing and Erasing in a Memristor Crossbar Memory," ***IEEE Transactions on Nanotechnology,*** Vol. 10, No. 6, Nov. 2011, pp. 1454-1463.

97. Y. Yilmaz and P. Mazumder, "Non-Volatile Nanopipelining Logic using Multiferroic Single-Domain Nanomagnets***," IEEE Transactions on Very Large Scale Integration Systems***. (to appear)

98. X. Zhao, K. Song and P. Mazumder, "Analysis of Doubly Corrugated Spoof Surface Plasmon Polariton (DC-SSPP) THz Waveguiding Structure with Narrow-band Transmission," ***IEEE Transactions on Terahertz Science and Technology*** (to appear)

Journal Papers under Review

99. S. Duan, X. Hu, L. Wang, and P. Mazumder, " Memristor-Based RRAM with Applications", ***IEEE Transactions on Nanotechnology.***

100. S. Duan, X. Hu, L. Wang, and P. Mazumder, "Memristive Cellular Neural/Nonlinear Network with Applications", ***IEEE Transactions on Very Large Scale Integration (VLSI) Systems***.

101. M. Rajagopal and P. Mazumder, "A Model for Steady-State, Ballistic Charge Transport through Quantum Dot Layer Super-lattices" (37 pages).

Rigorously Reviewed Conference Publications

(Generally these conferences have acceptance ratio between 15% and 35% and they require rigorous review of full paper before the decision on a paper is made. The following papers are mostly 4 or more published pages in the proceedings).

102. P. Mazumder, J. H. Patel and W. K. Fuchs, "Design and Algorithms for Parallel Testing of Random-Access and Content-Addressable Memory," ***Proceedings ACM/IEEE 24th Design Automation Conference,*** Florida, Jun. 1987, pp. 688-694 (nominated for the Best Paper Award).

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114. R. Venkateswaran and P. Mazumder, "Hexagonal Array Machine for Multi-Layer Wire Routing," ***Proceedings IEEE International Conference on Computer-Aided Design***, Nov. 1989.

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116. R. B. Panwar and P. Mazumder, "A Parallel Karmarkar Algorithm Implemented on Orthogonal Tree Networks," ***Proceedings International Parallel Processing Conference***, Aug. 1990, Vol. 3., pp. 270-273.

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272. P. Mazumder, "Plasmonics based VLSI Interconnect Design" ***Air Force Office of Scientific Research Review Meeting on Nanoelectronics,*** June 2008, Dayton.

273. P. Mazumder, "Quantum Dot Based Cellular Image Processing: Theory and design," ***IEEE Workshop on Cellular Nonlinear Networks***, July, Budapest, Hungary (**Invited**).

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288. W. Wang, J. P. Sun, N. Gu, and P. Mazumder, "Gate Current Simulation of High-k Stack Nanoscale MOSFETs," ***IEEE Computer Society Annual Symposium on VLSI,*** Brazil, 2007.

Technical Reports

289. P. Mazumder and J. H. Patel, "Parallel Testing of Pattern-Sensitive Faults in Random-Access Memory," *Technical Report CSG-56, Coordinated Science Laboratory,* Aug. 1986.

290. P. Mazumder, "Networks and Embedding Aspects of Hyper-cellular Structures for On-Chip Parallel Processing," *M. Sc. Thesis, Department of Computer Science, University of Alberta,* 1985.

291. P. Mazumder and J. H. Patel, "Testable RAM Design," *SRC Corporate Research,* 1986 Annual Report.

292. P. Mazumder, "Testing and Fault-Tolerant Aspects of High-Density VLSI Memory," *Ph.D. Thesis, Coordinated Science Laboratory,* Aug. 1987.

293. P. Mazumder "On-Chip Double-Error-Correction Coding Circuit for Three-Dimensional DRAM's," *CRL-TR-05-88, Technical Report, Department of Electrical Engineering and Computer Science, University of Michigan,* Ann Arbor, Apr. 1988.

294. A. Chakravarthy and P. Mazumder, "Gate Matrix Layout Techniques," *CSE-TR-12-90, Technical Report, Department of Electrical Engineering and Computer Science, University of Michigan,* Ann Arbor, 1990.

295. R. Venkateswaran and P. Mazumder, "Hexagonal Array Machine for Multi-Layer Wire Routing," *CSE-TR-52-90, Technical Report, Department of Electrical Engineering and Computer Science, University of Michigan,* Ann Arbor, 1990.

296. R. Venkateswaran and P. Mazumder, "On Restructuring of Hexagonal Arrays," *CSE-TR-72-90, Technical Report, Department of Electrical Engineering and Computer Science, University of Michigan,* Ann Arbor, 1990.

297. K. Shahookar and P. Mazumder, "VLSI Cell Placement Techniques," *CRL-TR-07-88, Technical Report, Department of Electrical Engineering and Computer Science, University of Michigan,* Ann Arbor, Aug. 1988.

298. P. Mazumder, "CPLA - A Software Tool That Automatically Generates "C"-Model for PLA's," *Bell Laboratories Technical Memorandum, 55612-1A-262,* Aug. 1985.

299. P. Mazumder, "Placement Algorithms for CONES," *Bell Laboratories Technical Memorandum, 55612-1F-210,* Aug. 1986.

300. P. Mazumder, "Automatic Integrated Circuit Synthesizer: Generates PLA Layout from Behavioral Description Written in C Language," *Bell Laboratories Technical Memorandum, 55612-1A-262,* Aug. 1985.

Publications in Industry (during 1976-1982)

Mixed Signal Analog and Digital VLSI Chip Design

Published over ***fifteen*** technical papers and application ideas while working at the Bharat Electronics Ltd. Topics included

- An Integrated Circuit Design for the Raster-Scan Vertical Deflection System.
- An Integrated Circuit Design for the Sync Processing Circuit
- Integrated Chip Set for Laser Range Finder in Military Applications
- An Integrated Circuit Design for High-Gain Pre-Amplifier with Automatic Level Controller
- A Integrated Circuit Design for Hearing-Aid Amplifier
- An Integrated Circuit Design for Quadrant Detection and Amplification of Frequency-Multiplexed Voice Signal
- A Large-Scale Integrated Circuit Design for Stepper-Motor-Driven Analog Clock Chip
- Study of Failure Modes in CMOS ICs During Handling
- Leakage-Current-Based Fault Characterization in a Non-planar Gas Discharge Display
- IC Design Considerations in Fabrication of Large Planar Plasma Display
- Application Notes on Analog and Digital Circuits

All these articles were published in ***BEL Application Notes*** and ***BEL Technical Report***.

Book Reviews

1. J.V. Oldfield, J.P. Gray, T.A. Kean, and R.C. Dorf, "Field-Programmable Gate Arrays for Implementation and Rapid Prototyping of Digital Systems", ***John Wiley and Sons, Inc***., New York.
2. J. Beetam, "Computer Architectures", ***Aksen Associates Inc. Publishers,*** California.
3. "The Science and Technology of Microelectronic Processing", ***Saunders College Publishing***, Pennsylvania.
4. D. Pradhan, "Fault-Tolerant System Design", ***Prentice Hall***, New Jersey.
5. Price, "Introduction to VLSI Design", ***Prentice Hall,*** New Jersey.
6. C.P. Ravi Kumar, "Computer-Aided Design for VLSI Systems", ***Kluwer Academic Publishers,*** Massachusetts.
7. Fu, "Neural Networks in Computer Intelligence", ***Prentice Hall,*** New Jersey.
8. P. Banerjee, "Parallel Algorithms for VLSI Computer-Aided Design Applications", ***Prentice Hall,*** New Jersey.
9. R. Karri, "Automatic Synthesis of Fault-tolerant VLSI Systems", ***Kluwer Academic Publishers,*** Massachusetts.
10. A. S. Sedra and K. C. Smith, "SPICE Simulation: Microelectronics Circuits", ***Prentice Hall.***
11. A. B. Marcovitz, "Introduction to Logic Design," ***McGraw Hill.***
12. N. Jha and S. Gupta, "Testing of Digital Systems," ***Cambridge Press.***

Technical Presentations (excluding conferences and workshops)

At Industries and National Laboratories

Formal Talks

1. Quantum electronic circuit design at ***Intel Corporation***, Santa Clara, California.
2. Quantum electronic circuit design at ***Samsung,*** Korea
3. Quantum electronic circuit design at ***Nippon Telegraph and Telephone***, Atsugi-shi, Japan.
4. Quantum electronic circuit design at ***Silicon Value***, Jerusalem, Israel.
5. Quantum electronic circuit design ***at Fraunhofer Institute***, Freiburg, Germany.
6. Quantum electronic circuit design at ***A-STAR Research Laboratories,*** Singapore
7. Quantum electronic circuit design at ***Hitachi Central Research Laboratories***, Kokubunji, Japan.
8. Quantum electronic circuit design at ***NEC Corporation***, Tsukuba, Ibaraki, Japan.
9. Quantum electronic circuit design at ***Fujitsu***, Morinosato-Wakamiya, Japan.
10. Quantum electronic circuit design at ***Texas Instruments***, Dallas, Texas.
11. Quantum electronic circuit design at ***Hughes Research Laboratories***, Los Angeles, California.
12. Memory testing at ***Nippon Telegraph and Telephone***, Atsugi-shi, Japan.
13. Memory testing at ***Digital Equipment Corporation***, Hudson, Massachusetts
14. Memory testing at ***Fujitsu***, Morinosato-Wakamiya, Japan.
15. Memory testing at ***Intel***, Santa Clara, California
16. Memory testing at ***Hitachi Central Research Laboratories***, Kokubunji, Japan.
17. Memory testing at ***AT&T Bell Laboratories***, Murray Hill, New Jersey.
18. Memory testing at ***Bell Northern Research Laboratories***, Ottawa, Canada
19. Embedded memory compilation at ***Synopsys,*** Palo Alto, California.
20. Embedded memory compilation at ***Neo-Magic Corporation***, Santa Clara, California.

21. Embedded memory compilation at ***Ambit Design Systems***, Santa Clara, California.
22. Memory testing at ***Micron Technology***, Boise, Idaho.
23. Memory testing at ***MCC***, Austin, Texas
24. Memory testing at ***Texas Instruments***, Bangalore, India.
25. Memory testing at ***AT&T Bell Laboratories***, Holmdel, New Jersey.
26. VLSI chip testing at ***ERIM Research Laboratory***, Ann Arbor, Michigan.
27. VLSI layout techniques at ***Nippon Telegraph and Telephone***, Atsugi-shi, Japan.
28. VLSI layout techniques at ***General Motors Research***, Warren, Michigan.
29. VLSI layout techniques at ***Bell Northern Research Laboratories***, Ann Arbor, Michigan.
30. VLSI layout techniques at ***Cypress Semiconductor***, Santa Clara, California
31. VLSI layout techniques at ***National Semiconductor***, Santa Clara, California
32. Built-in self-repairable IC design at ***Nippon Electric Company***, Princeton, New Jersey.
33. Built-in self-repairable IC design at ***Bell Communications Research***, Morris Town, New Jersey.
34. Built-in self-repairable IC design at ***Ford Motors Company***, Dearborn, Michigan.
35. Built-in self-repairable IC design at ***Nippon Telegraph and Telephone***, Atsugi-shi, Japan.
36. Research activities on circuit design at ***IBM Watson Research Center***, New York.
37. Research activities on circuit design at ***Hitachi Development Laboratories***, Mobarra, Japan.
38. Research activities on circuit design at ***David Sarnoff Research Center***, Princeton, New Jersey.
39. Research activities on circuit design at ***NEC Central Research*** Laboratories, Kanagawa, Japan.
40. Quantum electronic circuit design at ***Sun Microsystems,*** Sunnyvale, California
41. Dynamic noise analysis methodology for VLSI design at ***Sun Microsystems***, Mountainview, California
42. Dynamic noise analysis methodology for VLSI design at ***Sequent Design Automation***, San Jose, California
43. Quantum electronic circuit design at ***AMD,*** Sunnyvale, California
44. Memory testing at ***Texas Instruments***, Houston, Texas.
45. Embedded memory testing at ***Logic Vision***, San Jose, California.
46. VLSI layout techniques at ***Avant!,*** Fremont, California.
47. VLSI layout techniques at ***International Business Machine***, Fishkill, New York.
48. Memory testing at ***LSI Logic***, Milpitas, California.
49. VLSI chip layouts at ***Xilinx***, Inc., San Jose, California.
50. Built-in self-repairable design at ***Phillips Laboratories***, Kirtland, New Mexico.
51. Built-in self-repairable design at ***Altera Corporation,*** San Jose, California.

Formal Talks at Universities

52. Multilayer VLSI routing techniques at ***University of California***, Berkeley, California.
53. Memory testing at ***Stanford University***, Palo Alto, California.
54. Beyond CMOS technologies and evolutionary architectures at ***California Institute of Technology***, Pasadena.
55. Beyond CMOS technologies and evolutionary architectures at ***Columbia University***, New York.
56. Quantum electronic circuit design at ***University of Illinois***, Urbana-Champaign, Illinois.
57. Quantum electronic circuit design at ***University of California***, Berkeley, California.
58. Quantum electronic circuit design at ***Seoul National University***, Seoul, Korea.
59. Quantum electronic circuit design at ***Beijing University***, Beijing, China.
60. Quantum electronic circuit design at ***Gerhard-Mercater University***, Duisburg, Germany.

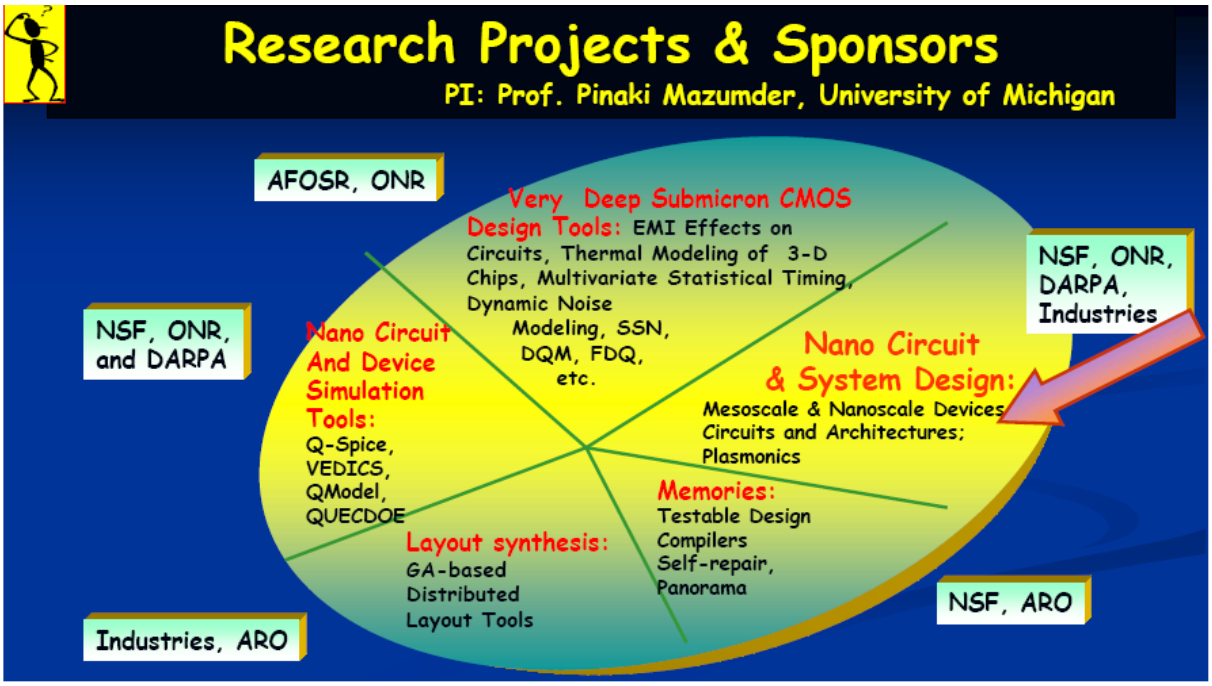
61. Quantum electronic circuit design at ***University of Santiago***, Spain
62. VLSI layout design at ***Princeton University***, Princeton, New Jersey.
63. Memory testing at ***Purdue University***, West Lafayette, Indiana.
64. Memory testing at ***University of Southern California***, Los Angeles, California.
65. Built-in self-repairable IC design at ***University of Iowa***, Iowa City, Iowa.
66. Memory testing at ***King Fahd University***, Saudi Arabia.
67. Quantum electronic circuit design at ***Nanjing University,*** Nanjing, China
68. Memory testing at ***Johns Hopkins University***, Baltimore, Maryland.
69. Quantum electronic circuit design at ***Ohio State University***, Columbus, Ohio
70. Memory testing at ***University of Minnesota***, Minneapolis, Minnesota.
71. Quantum electronic circuit design at ***University of Tokyo***, Tokyo, Japan.
72. Quantum electronic circuit design at ***Delft Technological University***, Delft, Netherlands.
73. Quantum electronic circuit design at ***King Fahd University***, Saudi Arabia.
74. Quantum electronic circuit design at ***Universidad de Las Palmas de Gran Canaries***, Spain.
75. Quantum electronic circuit design at ***South East University,*** Nanjing, China
76. Memory testing and repair algorithms at ***Indian Institute of Technology***, New Delhi, India.
77. Memory testing at ***Texas A&M University***, College Station, Texas.
78. Quantum electronic circuit design at ***Northwestern University***, Evanston, Illinois
79. Built-in self-repairable IC design at ***Wayne State University***, Detroit, Michigan.
80. VLSI layout design at ***Indian Institute of Science***, Bangalore, India.
81. Quantum electronic circuit design at ***Indian Statistical Institute,*** Calcutta (Kolkata), India.
82. Quantum electronic circuit design at ***Indian Institute of Technology***, Khragpore, India
83. Beyond Moore's Law CMOS Technology and Revolutionary Architectures, ***Asian Institute of Technology,*** Bangkok
84. IEEE Distinguished Lecture Beyond Moore's Law CMOS Technology and Revolutionary Architectures at ***Indian Institute of Technology***, Madras (Chennai), India.
85. IEEE Distinguished Lecture Beyond Moore's Law CMOS Technology and Revolutionary Architectures at ***University of Illinois***, Chicago.
86. IEEE Distinguished Lecture on Beyond Moore's Law CMOS Technology and Revolutionary Architectures ***at Indian Institute of Science,*** Bangalore, India.
87. IEEE Distinguished Lecture Beyond Moore's Law CMOS Technology and Revolutionary Architectures at ***Dhaka University***, Dhaka, Bangladesh.
88. IEEE Distinguished Lecture Beyond Moore's Law CMOS Technology and Revolutionary Architectures at ***Tata Institute of Fundamental Research***, Mumbai, India.
89. IEEE Distinguished Lecture Beyond Moore's Law CMOS Technology and Revolutionary Architectures at ***Indian Institute of Technology***, Bombay (Mumbai), India.
90. IEEE Distinguished Lecture Beyond Moore's Law CMOS Technology and Revolutionary Architectures at ***Jadavpur University***, Calcutta (Kolkata), India.
91. Quantum electronic circuit design at ***Nanyang Technological University***, Singapore

Formal Visits to University Laboratories

92. VLSI Design and Education Center, ***University of Tokyo***, Tokyo, Japan.
93. Nanoscale Science and Engineering Center, ***Harvard University***, Harvard, Massachusetts
94. Computer Engineering Research Center, ***University of Texas***, Austin, Texas.
95. Nanoelectronics Laboratory, ***University of Texas***, Dallas, Texas.
96. Testing Laboratory, ***Technical University of Budapest***, Budapest, Hungary.
97. ***Rice University***, Houston, Texas.
98. ***University of North Carolina***, Chapel Hill.
99. ***Virginia Commonwealth University***, Richmond, Virginia.
100. ***Duke University***, Durham, North Carolina

101. ***Oxford University***, Oxford, England.
102. ***Zheng Zhou Light Industry University,*** Zheng Zhou, China
103. ***Syracuse University,*** New York
104. ***University of Virginia,*** Charlottesville, Virginia
105. ***University of California Supercomputing Center, San Diego,*** California.

Summary of Research Activities



Nano-scale CMOS Design Issues
Prof. P. Mazumder, NDR Group

EM Effects on VLSI Circuits	Thermal Modeling of a 3-D Chips	Device and Interconnect Modeling	Statistical Timing Analysis	Dynamic Noise Analysis
Chebyshev's Approx & Pade Approx. for Distributed Noise Sources Finite Difference Quadrature Method	Green's Function based full-chip thermal analysis Direct Cosine Transform and IDCT for Fast Computation Hankel Transformation for Fast Computation	Envelope Function based quantum tunnel modeling of Nanoscale CMOS FET Differential Quadrature Method (DQM) for Interconnect Delay Modeling	Multivariate Normal Distributions for multi-input Domino gates Min/Max Correlation Analysis through Recursive Moment computation	Dynamic Noise Margins and Algorithms for Noise Analysis Simultaneous Switching Noise Estimation Coupling Noise Modeling for Automatic Routers

Quantum/Nano Systems Research Overview
Prof. P. Mazumder, NDR Group

Challenges: From Quantum Physics to Circuit Theory and Software Tools

CAD Tools	Circuits	Theory	Fabrication
Q-Spice * QMOS * HEMT/HBT **QModel** * RTD * Quantum Dots & Wires **QUECDOE** * 3-D Opt **VEDICS** * FD-TLM * Full Chip	▪ New Logic Families ▪ MVL Circuits ▪ Memories ▪ Nanopipelining ▪ Correlator, DDFS ▪ Turbocode Decoder ▪ Cellular Nonlinear Networks (CNN) ▪ Quantum Dot Image and Video Processors ▪ Plasmon Nanowire	▪ PDE and ODE based Nonlinear Circuit Analysis ▪ Quantum Physics based RTD & QD Modeling ▪ FD-TLM Ckt. Simulation	▪ SiO_2/Si-Ge based QMOS NRL, OSU ▪ InP based RTD+HEMT Raytheon ▪ InP based RTD+HBT KAIST, HRL ▪ GaSb Based RTD+HEMT HRL, ND

RAM Research Overview

Circuit Techniques	Test Algorithms	Error Correction	Self Repair	Compiler
• DFT for DRAM *TC-89* • DFT for CAM *TCAD-88* • DFT for random test *JETTA-92* • BIST for RAM *TIE-89* • ASIC for memory testing *JSSC-91*	• Parallel PSF *DAC-87, ITC-87* • Parallel parametric tests *JSSC-89* • Parallel stress tests *JETTA-94* • Tests for device-related faults *TCAD-93* • Board-level test *JETTA-2000*	• Double-bit ECC *JSSC-92* • Parallel signature analyzer based ECC *JSSC-93* • Projective geometric code *TC-93* • Radiation study • Reliability analysis	• Pseudo-analog adaptive circuits for self-repair *TCAD-96* • Digital adaptive circuits for self-repair *TCAD-93* • Generalized adaptive self-repair circuit techniques *TCAD-92,93*	• RAM compiler - Self-testing - Self-repair *EDAC-99* • ROM compiler - Self-testing - Self-repair *ICCD-99 VLSIJ-99*

- Books written by P. Mazumder
  - Testing and Testable Design of High-Density RAM, 1996
  - Fault Tolerance of RAM, 2000
  - Circuit Techniques for DRAMs (under preparation)

Layout Research Overview

Layout Algorithms	Parallel Multilayer Routing	New Data Structures For Layout	Layout Algorithms for On-Chip Parallel Processing
• Distributed genetic Algorithm *TCAD-93* • Genetic-Algorithm-Based: - multiway partitioning *PH-99* - standard-cell placement *VLSIJ-91* - gate matrix *IEE Proc.-94*	• Hexagonal Array for Concurrent 3-D Maze Routing • Multilayer Routing Models on Polymorphic Arrays *TCAD-90, TVLSI-93* • Switchbox Routing *IEE Proc.-95* • Channel Routing • Maze Routing • Area Routing • Chord Routing	• Quad Tree Data Structure and Planar Tessellations *CVGIP-87* • Oct Tree Data Structures and 3-D Tessellations	• Asymptotic Modeling of VLSI *ICPP-87* • Interconnect Network Evaluation *TC-87* -topological mapping -evaluation criteria -evaluation technique • Cellular Embedding Techniques *IEE Proc.-92* -Yield-related layout techniques