Technical Presentations (excluding conferences and workshops)

At Industries and National Laboratories

Formal Talks

1. Quantum electronic circuit design at Intel Corporation, Santa Clara, California.
2. Quantum electronic circuit design at Nippon Telegraph and Telephone, Atsugi-shi, Japan.
3. Quantum electronic circuit design at Silicon Value, Jerusalem, Israel.
4. Quantum electronic circuit design at Fraunhofer Institute, Freiburg, Germany.
5. Quantum electronic circuit design at Hitachi Central Research Laboratories, Kokubunji, Japan.
6. Quantum electronic circuit design at NEC Corporation, Tsukuba, Ibaraki, Japan.
7. Quantum electronic circuit design at Fujitsu, Morinosato-Wakamiya, Japan.
8. Quantum electronic circuit design at Texas Instruments, Dallas, Texas.
9. Quantum electronic circuit design at Hughes Research Laboratories, Los Angeles, California.
10. Memory testing at Nippon Telegraph and Telephone, Atsugi-shi, Japan.
11. Memory testing at Digital Equipment Corporation, Hudson, Massachusetts
12. Memory testing at Fujitsu, Morinosato-Wakamiya, Japan.
13. Memory testing at Intel, Santa Clara, California
14. Memory testing at Hitachi Central Research Laboratories, Kokubunji, Japan.
15. Memory testing at AT&T Bell Laboratories, Murray Hill, New Jersey
16. Memory testing at Bell Northern Research Laboratories, Ottawa, Canada
17. Embedded memory compilation at Synopsys, Palo Alto, California.
18. Embedded memory compilation at Neo-Magic Corporation, Santa Clara, California.
20. Memory testing at Micron Technology, Boise, Idaho.
21. Memory testing at MCC, Austin, Texas
22. Memory testing at Texas Instruments, Bangalore, India.
23. Memory testing at AT&T Bell Laboratories, Holmdel, New Jersey.
24. VLSI chip testing at ERIM Research Laboratory, Ann Arbor, Michigan.
25. VLSI layout techniques at Nippon Telegraph and Telephone, Atsugi-shi, Japan.
27. VLSI layout techniques at Bell Northern Research Laboratories, Ann Arbor, Michigan.
28. VLSI layout techniques at Cypress Semiconductor, Santa Clara, California
29. VLSI layout techniques at National Semiconductor, Santa Clara, California
31. Built-in self-repairable IC design at Bell Communications Research, Morris Town, New Jersey.
34. Research activities on circuit design at IBM Watson Research Center, New York.
35. Research activities on circuit design at Hitachi Development Laboratories, Mobarra, Japan.
36. Research activities on circuit design at David Sarnoff Research Center, Princeton, New Jersey.
37. Research activities on circuit design at NEC Central Research Laboratories, Kanagawa, Japan.
38. Quantum electronic circuit design at Sun Microsystems, Sunnyvale, California
39. Dynamic noise analysis methodology for VLSI design at Sun Microsystems, Mountainview, California
40. Dynamic noise analysis methodology for VLSI design at Sequent design Automation, San Jose, California
41. Quantum electronic circuit design at AMD, Sunnyvale, California

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1 Fellow of IEEE, Member of Sigma Xi, and Member of Phi Kappa Phi
Informal Presentations

42. Memory testing at Texas Instruments, Houston, Texas.
43. Embedded memory testing at Logic Vision, San Jose, California.
44. VLSI layout techniques at Avant!, Fremont, California.
46. Memory testing at LSI Logic, Milpitas, California.
47. VLSI chip layouts at Xilinx, Inc., San Jose, California.
49. Built-in self-repairable design at Altera Corporation, San Jose, California.

Formal Talks at Universities

50. Multilayer VLSI routing techniques at University of California, Berkeley, California.
51. Memory testing at Stanford University, Palo Alto, California.
52. Quantum electronic circuit design at University of Illinois, Urbana-Champaign, Illinois.
53. Quantum electronic circuit design at University of California, Berkeley, California.
54. Quantum electronic circuit design at Gerhard-Mercater University, Duisburg, Germany.
55. VLSI layout design at Princeton University, Princeton, New Jersey.
56. Memory testing at Purdue University, West Lafayette, Indiana.
57. Memory testing at University of Southern California, Los Angeles, California.
58. Built-in self-repairable IC design at University of Iowa, Iowa City, Iowa.
59. Memory testing at King Fahd University, Saudi Arabia.
60. Quantum electronic circuit design at Nanjing University, Nanjing, China.
61. Memory testing at Johns Hopkins University, Baltimore, Maryland.
62. Quantum electronic circuit design at Ohio State University, Columbus, Ohio.
63. Memory testing at University of Minnesota, Minneapolis, Minnesota.
64. Quantum electronic circuit design at University of Tokyo, Tokyo, Japan.
65. Quantum electronic circuit design at Delft Technological University, Delft, Netherlands.
66. Quantum electronic circuit design at King Fahd University, Saudi Arabia.
67. Quantum electronic circuit design at Universidad de Las Palmas de Gran Canarias, Spain.
68. Quantum electronic circuit design at South East University, Nanjing, China.
69. Memory testing and repair algorithms at Indian Institute of Technology, New Delhi, India.
70. Memory testing at Texas A&M University, College Station, Texas.
71. Quantum electronic circuit design at Northwestern University, Evanston, Illinois.
72. Built-in self-repairable IC design at Wayne State University, Detroit, Michigan.
73. VLSI layout design at Indian Institute of Science, Bangalore, India.

Formal Visits to University Laboratories

75. VLSI Design and Education Center, University of Tokyo, Tokyo, Japan.
76. Computer Engineering Research Center, University of Texas, Austin, Texas.
77. Nanoelectronics Laboratory, University of Texas, Dallas, Texas.
78. Testing Laboratory, Technical University of Budapest, Budapest, Hungary.
79. Rice University, Houston, Texas.
80. University of North Carolina, Chapel Hill.
82. Virginia Commonwealth University, Richmond, Virginia.