EECS 270: Introduction to Digital Logic **Fall 2000**
Homework Assignment No. 3 **Instructors: Jenkins/Mazumder**
Due Date: Oct. 2, 2000

Problem 1.

Design an Error Detector for 6-3-1-1 BCD digits. The output, F, is to be 1 iff the four inputs (A,B,C,D) represent an invalid code combination. Implement F in SOP form using 4 different styles of 2-level logic gates. Also implement F in POS form using 4 other styles of 2-level logic gates.

Problem 2.

A small corporation has 100 shares of stock, and each share entitles its owner to one vote at a stockholder's meeting. Mr. Akins owns 10 shares, Ms. Barnes owns 20 shares, Mr. Clay owns 30 shares, and Ms. Drake owns 40 shares. A two-thirds majority is required in order to pass a measure at a stockholder's meeting. Each of the four stockholders has a switch which he or she closes to vote yes for all of his or her shares and opens to vote no. A switching circuit is to be designed to turn on a light if the measure passes.

(a) Derive a truth table for the output function (Z). (Z = 1 for light on.)

(b) Write the minimum expansion for Z and simplify algebraically to a minimum sum-of-products form.

(c) Write the maxterm expansion for Z and simplify algebraically to a minimum product-of-sums form.

(d) Check with algebra to see that your answer to (c) is equivalent to the answer to (b).

(e) Design a minimum network of switches and a minimum AND-OR gate network to realize Z. For the second case, NOT may be used to invert inputs as necessary.

Problem 3.

Find the minimum SOP expressions for each function. Also identify all prime implicants and essential prime implicants.

(a) $f(a,b,c,d) = \Pi M(3,4,8,9,12)\ \Pi D(2,6)$

(b) $f(a,b,c,d) = \Sigma m(2,3,5,8,11,12) + \Sigma d(9,14)$

Problem 4.

F(a,b,c,d,e) = Σm(0,1,3,4,9,11,15,16,23,25,27,30,31) + Σd(2,12,28,29).

Find the essential prime implicants and all prime implicants by using a Karnaugh map. Write the minimum SOP expression for F. Use don't cares to best advantage.

Problem 5.

Find the minimum SOP and POS expression for the following functions and implement them in eight different 2-level logic styles. (4 for SOP and 4 for POS of each function.)

a. $f(x, y, z) = \sum m(1,2,4,7)$

b. $f(x, y, z) = \prod M(3,5,6,7)$

Design Problem

Problem 6.

(Binary-to-Excess-3 BCD Converter) Write the truth table of a binary to Excess-3 BCD code converter. Using K-map minimization technique, write the output variables as functions of input variables in minimized SOP form. Note that the output variables are don't cares (X's) for all invalid input patterns. Show the SOP in NAND-NAND form and then implement the above converter using ONLY the minimum number of 2-input NAND gates. How many 74LS00 chips are required to implement the converter?

Problem 7. Textbook problem 4.72

ALL HOMEWORK MUST BE TURNED IN DURING LECTURE TIME, OTHERWISE IT WILL NOT BE GRADED.