PINAKI MAZUMDER[1]

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Immigration Status: US Citizen (1995); Permanent Resident (1989-1995).

I. Educational Qualification

Ph.D. in Computer Engineering	University of Illinois, Urbana-Champaign	1988
M. Sc. in Computer Science	University of Alberta, Edmonton, Canada	1985
B.S. in Electrical Engineering	Indian Institute of Science, Bangalore, India	1976

I also received a degree in B.Sc. Physics Honors securing the first rank in Guwahati University, India amongst estimated 100,000 students in all disciplines of liberal arts and basic sciences.

II. Work Experience

US Government (National Science Foundation):

2007-2008	Program Director for Emerging Models and Technologies Program (funding areas: Nanoelectronics, Quantum Computing, and Biologically Inspired Computing with an annual budget of $18 Million) in the Directorate for Computer and Information and Science and Engineering, National Science Foundation, Arlington, Virginia.
2009	Program Director in Electrical, Communications and Cyber Systems Division (funding areas: Quantum, Molecular and High Performance Computing, Adaptive Intelligent Systems, Electronic and Photonic Devices, and Major Research Instrumentation) of the Engineering Directorate at National Science Foundation.

Academic Teaching and Research:

1998- to date	Tenured Professor, Division of Computer Science and Engineering, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, USA.
1996-1997	Research Fellow, Division of Electrical and Computer Engineering, Department of Electrical Engineering and Computer Science, University of California, Berkeley, USA.
1996-1997	Visiting Associate Professor, Department of Computer Science and Engineering, Stanford University, Palo Alto, California, USA.
1997	Visiting Professor, NTT Basic Research Laboratories, Atsugi-shi, Japan.
1992-1998	Tenured Associate Professor, Division of Computer Science and Engineering, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, USA.
1987-1992	Assistant Professor, Division of Computer Science and Engineering, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, USA.
1985-1987	Research Assistant, University of Illinois at Urbana-Champaign, USA.
1982-1984	Teaching Assistant at University of Alberta, Edmonton, Canada.
1974-1975	Research Assistant at Indian Institute of Science, Bangalore, India.

[1] Fellow of AAAS, Fellow of IEEE, Member of Sigma Xi, and Member of Phi Kappa Phi

Industrial Research and Development:

1985, 1986	Member of Technical Staff, AT&T Bell Laboratories, Indian Hill, Chicago
1976-1982	Senior R&D Engineer, Bharat Electronics Ltd., Bangalore, India

III. Major Fields of Research

1) VLSI design, testing and layout automation; 2) Nanoelectronics and nanomagnetics: multiscale modeling, simulation tools, circuits and architectures; 3) Terahertz technology and applications in signal processing, computing and communications.

IV. Awards and Recognitions

- Fellow of American Association for the Advancement in Science (AAAS), 2007 for "distinguished contributions to the field of very large scale integrated (VLSI) systems". The honor of being elected a Fellow of AAAS is given to those whose "efforts on behalf of the advancement of science or its applications are scientifically or socially distinguished."
- Fellow of IEEE, 1999 for "contributions to the field of VLSI Design."
- IEEE Distinguished Lecturer
- Digital Equipment Corporation Faculty Award: Excellence in Research
- Departmental Research Excellence Award (1995), The University of Michigan
- BF Goodrich National Collegiate Invention Award
- DARPA Research Excellence Award for the work in Quantum MOS Project
- Best Undergraduate Student Medal
- IETE Best Student Paper Award, and IETE Best Paper Presentation Award
- NSF Research Initiation Award
- Bell Northern Research Laboratory Faculty Development Grant
- Commendation Letter from the Dean of College of Engineering, University of Michigan, for Excellence in Teaching
- Member, Sigma Xi
- Member, Phi Kappa Phi

V. Research Funding

1. National Science Foundation (RIA): $69,948; 1988 – 1991 (Single PI)
2. Bell Northern Research Laboratory: $20,900; 1988 – 1989 (Single PI)
3. National Science Foundation: $90,620; 1989 – 1990 (Single PI)
4. Digital Equipment Corporation: $180,000; 1989 – 1992 (Single PI)
5. Office of Naval Research: $420,000; 1988 - 1991, (Co-PI)
6. National Science Foundation: $125,000; 1991 – 1993 (Single PI)
7. Rackham Faculty Research Grant: $9,980; 1991 – 1993 (Single PI)
8. U.R.I. Program (US Army): $6,000,000 (total); $250,000 (my portion); 1988 - 1992
9. General Motors: $20,000; 1992 – 1992 (Single PI)
10. International Business Machines: $45,000 (student fellowship); 1990 – 1993
11. National Science Foundation: $47,000; 1992 – 1993 (Single PI)
12. Hewlett Packard: $81,400; 1993 – 1995 (Single PI)
13. Office of Vice President Research: $52,300; 1995 - 1996
14. Defense Advanced Research Projects Agency (DARPA): $825,000; 1993 -1997 (Co-PI)
15. National Science Foundation: $182,400; 1994 – 1998 (Single PI)
16. U.R.I. Program (US Army): $5,000,000; $200,000; 1993 - 1997
17. State of Michigan Display Technology Center: $2,000,000; My portion: $200,000; 1995 - 1998
18. Texas Instruments (subcontract of a DARPA project): $304,000; 1995 – 1998 (Single PI)
19. Army Research Office's MURI-95 (Co-PI with 7 others): $4,000,000; 1995-2000 + 1 year.
20. Army Research Office's MURI-96 (Co-PI with 13 others): $5,000,000; 1996-2001 + 1 year.

21. Defense Advanced Research Projects Agency: $750,000; June 1997- May 2000 (PI)
22. National Science Foundation: $300,000; 1998 – 2002 (Single PI)
23. Nippon Electric Company, Japan: $40,000; 1998 (Single PI)
24. National Science Foundation: $195,000; 1998 – 2002 (Single PI)
25. Office of Naval Research; $270,000; 1998-2001 (Single PI)
26. NanoLogic Inc. $10,000; 1999-2000 (Single PI)
27. Air Force Office of Scientific Research: $5,000,000: 2001-2006 (Co-PI with 9 other investigators)
28. Office of Naval Research: $303,000: 2001-2002; (Single PI)
29. National Science Foundation: $210,000: 2001-2004 (Single PI)
30. Korean Government Nanoelectronics Research: $200,000: 2001-2002 (PI: Prof. G.I. Haddad).
31. Office of Naval Research: $820,000: 2002-2005 (PI)
32. Tera-Level Nanoelectronics Project, Korean Government: $170,000: 2003-2006; (Single PI)
33. National Science Foundation: $120,000: 2004-2007 (Single PI)
34. Air Force Office of Scientific Research, $480,000: 2006-2009 (Single PI)
35. National Science Foundation IPA Assignment Grant: $620,000; 2007-2009 (Single PI)
36. DARPA SyNAPSE Program on Brain Plasticity: $807,812; Co-PI: Hughes Research Laboratory
37. National Science Foundation, NIRT: $1,000,000: 2006-2012 (Co-PI).
38. SRC NRI Center (MIND): ~$200,000: 2008-2011 (Single PI)
39. National Science Foundation: EAGER Grant, $200,000; 2009-2012. (Single PI)
40. National Science Foundation: $400,281; 2010-2014. (Single PI)
41. Army Research Office: $580,000; 2010-2013. (Single PI)
42. National Science Foundation: $149,111; 2011-2012. (Single PI)
43. Army Research Office, MURI: $6,500,000; 2010-2015. (Co-PI)
44. National Science Foundation: $400,415; 2011-2014. (Single PI)
45. National Science Foundation: $1,750,000; 2011-2015. (Co-PI)
46. Defense Advanced Research Projects Agency (DARPA): $150,000; 2011-2013 (Single PI)
47. Air Force Office of Scientific Research: $449,772; 2012-2015 (Single PI)
48. National Science Foundation: $480,000; 2012-2015 (Co-PI)
49. National Science Foundation: $400,000; 2014-2017 (PI)
50. National Science Foundation: $900,000; 2015-2018 (PI).
51. Air Force Office of Scientific Research: $150,000; 2016-2017 (Single PI)
52. National Science Foundation: $330,000; 2017-2020 (Single PI)
53. National Science Foundation: $620,000; 2017-2020 (PI)
54. Air Force Office of Scientific Research: $501,000; 2018-2021 (Single PI)

Pending Proposals:

1. Engineering Research Center (ERC): Foundation for Integrative Research on Short-range Terahertz in Wireless Communication and Signal Processing, National Science Foundation, $18,000,000 for 5 years (Mazumder, PI; University of Michigan, Massachusetts Institute of Technology, University of California at Los Angeles, New Jersey Institute of Technology, University of Central Florida, and Cornell University).
2. Nanoarchitectures for Adaptive Control and Intelligence Processing Chips, Office of Naval Research, $450,000 (PI)
3. Ultra-Low-Power Bio-inspired Nanoelectronics for Navigation in Autonomous Insect-Scale Robots, Air Force Office of Scientific Research, $790,000 (PI)

VI. Committees and Professional Activities

1. Nomination Committee Member for *The Blue Planet Prize,* an international environmental award sponsored awarded by Asahi Glass Foundation, Japan, 2015-
2. Member of Board of Editors, *Proceedings of the IEEE,* 1999-2002
3. Associate Editor, *IEEE Transactions on VLSI Systems*, 1997-2000
4. Guest Editor, *IEEE Transactions on VLSI Systems* - A Special Issue on Impact of Emerging Technologies on VLSI Systems, December 1997

5. Guest Editor (with Prof. A. Seabaugh), *Proceedings of the IEEE* - A Special Issue on Nanoelectronic Devices and Circuits, June 1998.
6. Guest Editor (with Prof. S. M. Kand and Prof. R. Wasser), *Proceedings of the IEEE* - A Special Issue on Memristors: Device, Models, and Applications, June 2012.
7. Guest Editor (with Prof. A. Benso and Prof. Y. Makris), *IEEE Transaction on Computer* – A Special Issue on Architectures for Emerging Technologies and Applications, June 2008
8. Guest Editor, *Journal of Electronic Testing - Theory and Application* - A Special Issue on Multi-megabit Memory Testing, April 1994
9. Guest Editor (with Prof. J.P. Hayes), *IEEE Design & Test Magazine* - A Special Issue on Memory Testing, 1993
10. Editorial Advisory Board, *The Arabian Journal for Science and Engineering*, King Fahd University of Petroleum and Minerals, Saudi Arabia.
11. Council of Editors, *International Society for Genetic and Evolutionary Computation* (ISGEC)
12. As lead NSF Program Director, organized the Emerging Models and Technology Workshop on Bio-Inspired Computing and Bio-Computing at Princeton University on July 24-25, 2008.
13. As lead NSF Program Director, organized the EMT Workshop on Nanoelectronics on October 29-30, 2007.
14. As lead NSF Program Director, held the EMT Workshop on Quantum Information Science and Engineering on September 10-11, 2007.
15. Member, University of Michigan Research Policies Committee of Senate Assembly, 2002-05.
16. Member, Electrical Engineering and Computer Science Curriculum Committee, 2002-03.
17. Member, Electrical Engineering and Computer Science DCO Committee, 2002-03.
18. Member, Computer Science and Engineering Graduate Curriculum Committee, 1988-89, 1998-00, 2002-06.
19. Counselor, Computer Engineering Undergraduate Students, 1990-95.
20. Member, Computer Science and Engineering Graduate Admission Committee, 1995-96.
21. Member, IEEE Standards Subcommittee for Semiconductor Memories, 1989-90.
22. Member, IEEE Test Technologies Committee
23. Member, IEEE VLSI Technical Committee
24. General Chair, 2007 High Performance Computing (HPC) for Nanotechnology
25. General Chair, 1999 IEEE Great Lakes VLSI Conference
26. Program Committee, 1992 Fault-Tolerant Computing Symposium Workshop
27. Program Committee, 1992 IEEE Defects and Fault Tolerance Workshop
28. Program Committee, 1993 IEEE Intl. Conference on Memory Testing
29. Program Committee, 1994 IEEE Intl. Conference on Memory Testing
30. Program Committee, 1994 IEEE Asian Testing Symposium
31. Program Committee, 2000 IEEE Great Lakes VLSI Conference
32. Serving on organizing committee for Department of Defense Nano Conference, 2009
33. Served regularly on NSF panels in Engineering and CISE Directorates
34. Proposals Reviewed for: US National Science Foundation, The Israel Science Foundation, Louisiana University Board of Regents, and US Army Research Office, New Jersey Center for Science and Technology, Saudi Arabia King Fahd University Research Foundation, and private venture capitalist firms.

VII. Professional Experience

Details of My Professional Accomplishments

US Government at National Science Foundation (3 years)

In 2007 and 2008, I worked as the lead Program Director for Emerging Models and Technologies (EMT) program in the Division of Computing and Communication Foundations (having nearly $140 Million annual budget) of the Directorate for Computer and Information and Science and Engineering, National Science Foundation, Arlington, Virginia. My mandate was to manage research grants in Nanoelectronic Modeling and Systems, Quantum Computing, and Biologically Inspired Computing for which I had an operating annual budget of about $18 Million. Additionally, I participated in several NSF crosscutting programs such as Cyber-Enabled Discovery and Innovation (CDI), Expeditions in Computing, Major Research Instrumentation (MRI), Computing Research Infrastructure (CRI) and Cyber Physical Systems (CPS). In 2009, I worked as a Program Director in the Engineering

Directorate where I managed research in three broad areas: Adaptive Intelligent Systems (Machine Learning), Quantum, Molecular and High-Performance Modeling, and Electronic and Photonic Devices. During these three years, I interacted with several program managers and administrators of NSF, DARPA, ARO, ONR, and AFOSR to help launch national-level major research initiatives. I consider that serving the US government for a stint of three years has provided me an exceptional opportunity to acquire a vast amount of knowledge in various fields of science and engineering, to network with numerous researchers around the nation, and to gain divergent administrative experience.

Teaching Experience (29 years)

Since 1988, I have been teaching at the Department of Electrical Engineering and Computer Science of the University of Michigan, Ann Arbor, Michigan.

Graduate courses developed and taught: 1) VLSI System Design, 2) Optimization and Synthesis of VLSI Layout, 3) Testing of Digital Circuits and Systems, 4) Advanced Computer Architectures, 5) Nanocircuits and Nanoarchitectures, 6) Ultra-Low-Power Subthreshold CMOS Circuits, and 7) Terahertz Technology and Applications.

Undergraduate courses upgraded and taught: 1) Introduction to Digital Logic Design (sophomore level), 2) Digital Integrated Circuit Design (junior level), and 3) VLSI System Design (senior level).

Industrial Experience (6.5 years)

After my baccalaureate degrees in Physics and Electrical Engineering, I worked for six years (1976-1982) as a Senior R&D Engineer at Bharat Electronics Ltd. (BEL) in its Integrated Circuits Division. I designed several bipolar and CMOS analog and digital integrated circuits for consumer electronic systems. I was associated with the following chip development projects: i) Raster-scan vertical deflection system microchip for TV display, ii) Sync processing and horizontal deflection system microchip for TV display, iii) Video and audio IF stage IC's for vestigial-AM and FM signal detection in TV receiver, iv) High-gain audio amplifier microchip for TV audio stage, v) Tape Recorder IC with automatic gain adjustments, vi) Hearing-aid IC, vii) Analog clock driver IC, and viii) LCD and AC Plasma display drive IC's. Several million commercial chips were fabricated based on these designs.

After finishing my MSc degree in Computer Science and while working towards my PhD degree in Electrical and Computer Engineering, I worked during the summers of 1985 and 1986 as a Member of Technical Staff at AT&T Bell Laboratories. I was one of the two engineers who started the Bell Laboratory *Cones/Spruce* project - a new behavioral synthesis and layout automation tool for rapid prototyping of digital circuits. The main contribution of this effort was to demonstrate how a restricted version of C language could be used to model digital hardware much before commercial hardware description language (HDL) software tools like Verilog and System C were designed.

Teaching Accomplishments and Evaluations:

I have endeavored to pursue multidimensional education frontiers that transcend the confines of classroom and impact students as well as other professionals alike. My teaching contributions include authoring an undergraduate textbook and a video book, developing four advanced graduate courses, developing courseware for practicing engineers in industry, editing special issues in professional journals to stimulate research in emerging technologies, and fostering STEM education for K-12 students. Highlights of my teaching accomplishments are enumerated below:

- Breakdown of my course offering at the University of Michigan over the past 30 years: (i) nearly 60% of courses I taught are on *three* undergraduate courses for sophomore, junior and senior; approximately 10% of courses are on *two* regular graduate courses; and about 30% of courses are on *four* new graduate courses designed and developed by me to promote the state-of-the-art CMOS research and train the future engineering workforce. I have taught *three* distinct undergraduate and *six* graduate courses at the University of Michigan.

- Authored an undergraduate textbook, "Lectures on Digital Logic Design", about 500 pages. This book is based on my lectures in an introductory *Digital Logic Design* (EECS 270) course that I taught nearly twenty times at the University of Michigan.

- Developed an "on-line course" on *Digital Logic Design* (NEEP 2221), which was produced in June 2005 at the Disney MGM Studio, Orlando, Florida by National Technological University (NTU), now acquired by Walden University that is widely regarded as a global leader in on-line education. With the support of major technology companies such as IBM, Motorola, and Hewlett-Packard, the NTU was founded in 1984 to deliver academic courses to training facilities of corporations via a unique satellite network.

- Developed a new graduate course on *Ultra-Low-Power Sub-threshold CMOS Design* (EECS 598-1):

- Developed a new graduate course on *Nanocircuits and Nanoarchitectures* (EECS 598-2):

- Developed a new graduate course on *Terahertz Engineering: Theory and Applications* (EECS 598-6) to promote research in spoof plasmonics, photonics, and microwave electronics.

- Developed a new graduate course on *Optimization and Synthesis of VLSI Layout* (EECS 527) that I taught nearly half-a-dozen times. When I taught the course for the first time in 1988, there was no suitable textbook at that time. Therefore, I developed course materials, which were also adopted in other universities to teach new VLSI computer-aided design (CAD) course at that time.

- Co-authored six advanced VLSI books to promote education in VLSI chip design and semiconductor memory technology. Our book on "Genetic Algorithms for VLSI Design, Layout and Testing", *Prentice Hall*, 2000 provides the foundation for developing distributed VLSI design automation tools by exploiting the multidimensional optimization capability of GA's running concurrently on a network of workstations to rapidly solve problems. The book not merely brings the evolutionary computing and the broader engineering community together enabling them to solve complex engineering problems. The book also unravels many mathematical insights for constructing multidimensional chromosome operators, and challenges mathematicians to develop theoretical models for the evolutionary algorithms. Two of books I coauthored on semiconductor memory systems are "Testing and Testable Design of Random-Access Memory", *Kluwer Academic Publisher*, 1996; and "Fault Tolerance and Reliability Aspects of Random-Access Memories," *Prentice Hall*, 2002. They are being widely used by practicing engineers and researchers in semiconductor memory technologies because of their pedagogical values. The names of other books are listed in Publications section.

- Edited a Special Issue in *The Proceedings of the IEEE* on Memristors: Devices, Models and Circuits, which can be adapted for teaching the next generation nano-circuits and nano-architectures.

- To promote STEM education among K-12 students through imaginative mathematics software, I started developing Math Guru with the help of one of my ex advisees. The software was demonstrated in 1996-97 at local schools and distributed. http://web.eecs.umich.edu/~mazum/mathguru.pdf.

Numerous studies conducted by professional societies such as American Society for Engineering Education (ASEE) and National Academy of Engineering (NAE) have ardently advocated for educator's multidimensional impact, in addition to conventional measures such as numerical rating and student feedback that serve as a rough metric for classroom performance. My numerical scores for teaching in courses I taught are provided below. While these data reflect my deeper commitments for education and training, I continually strive to impart broader impact by pursuing multidimensional teaching activities and training the future engineering workforces through integration of research and teaching.

Teaching Rating

Q#1: This is an excellent teacher
Q#2: This is an excellent course

EECS 427: VLSI Design

Winter 2018 Evaluation: 4.88/5.0 (Q#1:excellent teacher) and 4.88/5.0 (Q#2:excellent course);
Winter 2016 Evaluation: 4.71/5.0 (Q#1) and 4.58/5.0 (Q#2);
Winter 2015 Evaluation: 4.71/5.0 (Q#1) and 4.55/5.0 (Q#2);
Winter 2014 Evaluation: 4.58/5.0 (Q#1) and 4.42/5.0 (Q#2)
Winter 2013 Evaluation: 4.2/5.0 (Q#1) and 4.33/5.0 (Q#2)
Fall 1997 Evaluation: 4.71/5.0 (Q#1) and 4.58/5.0 (Q#2
Fall 1995 Evaluation: 4.55/5.0 (Q#1) and 3.94/5.0 (Q#2)
Fall 1994 Evaluation: 4.81/5.0 (Q#1) and 4.12/5.0 (Q#2)
Fall 1993 Evaluation: 4.32/5.0 (Q#1) and 3.83/5.0 (Q#2)

EECS 527: Computer-Aided Design for VLSI Systems

Winter 1988 Evaluation: 3.83/5.0 (Q#1) and 4.00/5.0 (Q#2)
Fall 1989 Evaluation: 4.81/5.0 (Q#1) and 4.67/5.0 (Q#2)
Winter 1992 Evaluation: 4.00/5.0 (Q#1) and 4.25/5.0 (Q#2)
Winter 1995 Evaluation: 4.25/5.0 (Q#1) and 4.08/5.0 (Q#2)
Winter 1996 Evaluation: 4.50/5.0 (Q#1) and 4.10/5.0 (Q#2)

EECS 598: Ultra-Low-Power CMOS System Design

Fall 2012: Evaluation: 4.0/5.0 (Q#1) and 4.17/5.0 (Q#2)
Fall 2013 Evaluation: 4.5/5.0 (Q#1) and 4.5/5.0 (Q#2)

EECS 570: Advanced Computer Architecture
Winter 1989: Evaluation: 4.08/5.0 (Q#1) and 3.67/5.0 (Q#2)
Winter 1991: Evaluation: 4.20/5.0 (Q#1) and 3.89/5.0 (Q#2)

EECS 270: Digital Logic Design (Regular term class size is frequently above 100 students)

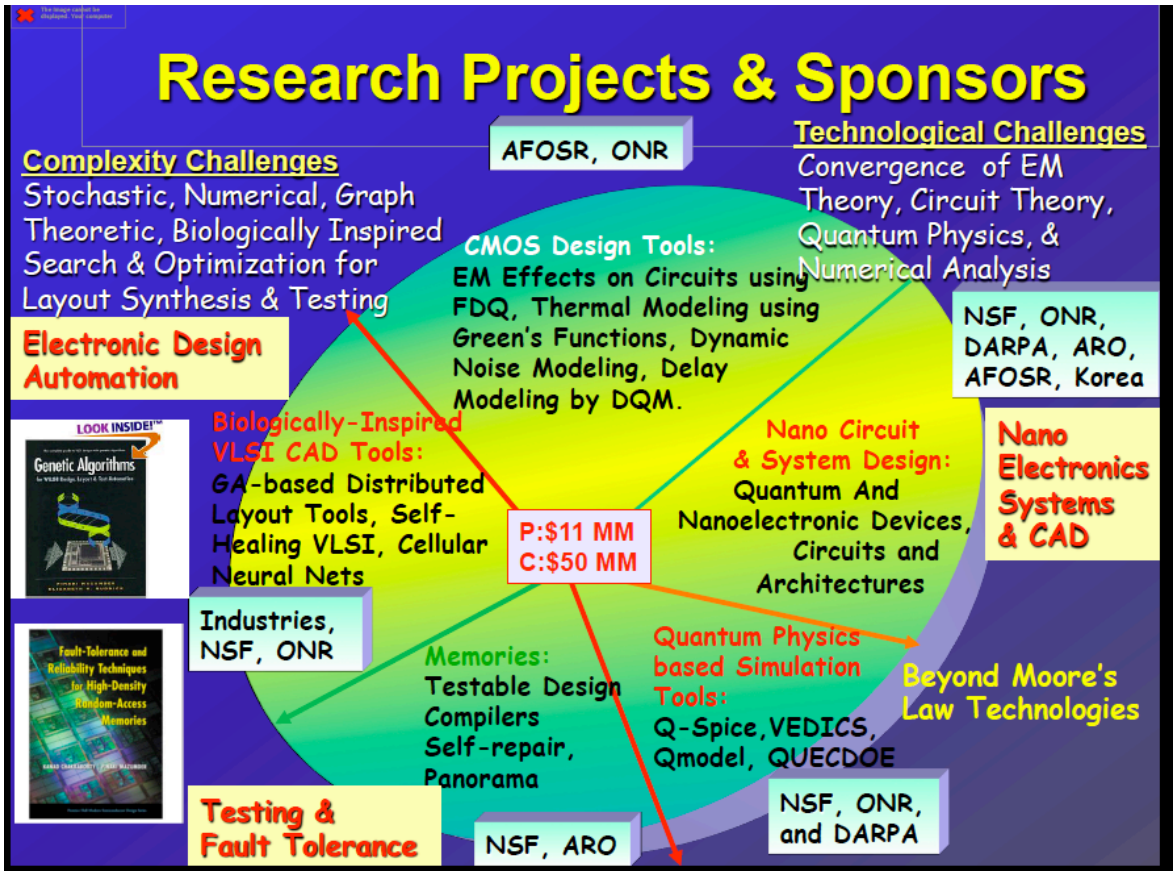
Winter 1988: Evaluation: 3.84/5.0 (Q#1) and 3.45/5.0 (Q#2)
Fall 1990: Evaluation: 4.41/5.0 (Q#1) and 3.80/5.0 (Q#2)
Spring 1991: Evaluation: 4.54/5.0 (Q#1) and 4.71/5.0 (Q#2)
Spring 1992: Evaluation: 4.6/5.0 (Q#1) and 4.43/5.0 (Q#2)
Spring 1993: Evaluation: 4.24/5.0 (Q#1) and 4.59/5.0 (Q#2)
Winter 1998: Evaluation: 3.76/5.0 (Q#1) and 3.41/5.0 (Q#2)
Winter 2001: Evaluation: 4.02/5.0 (Q#1) and 4.32/5.0 (Q#2)
Fall 2011: Evaluation: 4.17/5.0 (Q#1) and 3.75/5.0 (Q#2)

Legend: 5.0 – Excellent, 4.0 – Very Good, 3.0 – Good, 2.0 – Fair, 1.0 – Poor.

Research Accomplishments:

In 1984, when I started my MS thesis at University of Alberta in the field of VLSI, I was inspired by the local (Edmonton, Canada) hockey legend, Wayne Gretzky whose famous quote ("*A good hockey player plays where the puck is. A great hockey player plays where the puck is going to be*") defined the compass of my research work for the next 28 years as explained below. In Evolutionary CMOS research, I solved numerous use-inspired research problems that were 10 to15 years ahead of their time and eventually Moore's Law has vindicated the practical merits of my research by impacting the memory and FPGA industry as pointed out below. In Revolutionary emerging technologies such as quantum tunneling devices, THz plasmonic devices (in THz regime), ionic devices (as non-volatile memories), and electron spin based devices (as ultra-low-power nonvolatile memories) I have made sustained impact for the past 23 years by collaborating with multiple leading researchers in universities and companies. In my research career, I have endeavored to emulate the *Vannevar Bush* model of triad synergy between University, Industry and Government establishments that was conceived at the aftermath of the Second World War to challenge academics to undertake enterprising and leadership role for catalyzing innovations, accelerated economic growth, and sustained US leadership in science and engineering.

Details of my Research Accomplishments are provided at pp. 47-48 of this CV.



VIII. Publications

Summary of Significant Publications

Books: 13; **Journal Publications:** 123; **Reviewed Conference Papers:** 191; **Book Chapters:** 6; **US Patents Granted:** 10; **US Patents under Review:** 3.

A. Books

1. P. Mazumder and K. Chakraborty, "Testing and Testable Design of Random-Access Memories", ***Kluwer Academic Publishers***, 1996 (428 pages).

2. P. Mazumder and E. Rudnick, "Genetic Algorithms for VLSI Layout and Test Automation", ***Prentice Hall***, 1999 (460 pages).

3. K. Chakraborty and P. Mazumder, "Fault Tolerance and Reliability Aspects of Random-Access Memories," ***Prentice Hall***, 2002. (440 pages).

4. V. Ramachandran and P. Mazumder, "Handbook for VLSI Routing – Serial and Parallel Models", ***Tsinghua University Publisher,*** 2018 (340 pages).

5. P. Mazumder and I. Ebong, "Lectures on Digital Logic Design", ***Pan Stanford Publishing***, 2018 (550 pages).

6. N. Zheng and P. Mazumder, "Learning in Energy-Efficient Neuromorphic Computing: Algorithm and Architecture Co-Design", ***John Wiley and Sons***, 2018 (275 pages).

Books under Preparation

7. P. Mazumder, Y. Yalcin, I. Ebong, and W.H. Lee, "Neuromorphic Circuits for Nanoscale Devices," ***Springer Verlag***, 2018 (300 pages).

8. P. Mazumder. K. Song, X. Zhao and M. Aghdajani, "Terahertz Spoof Plasmonics: Theory and Applications," (Publisher to be decided).

9. P. Mazumder, S. Kulkarni, A. Gonzalez, S. Mohan, and M. Bhattcharya, "Quantum Electronic Devices: Modeling and Circuits," (Publisher to be decided).

Edited Books & Other Categories

10. R. Rajasuman (Editor) and P. Mazumder (Editor), "Semiconductor Memories: Testing and Reliability", ***Computer Science Press***, May 1998.

11. R. J. Lomax (Editor) and P. Mazumder (Editor), "Great Lakes Symposium on VLSI, 1999", ***Computer Science Press***, March 1999.

12. P. Mazumder, "Introduction to Digital Systems", Video Book on DVD, produced at MGM Studio (Orlando, Florida), ***Laureate Education, Inc.,*** 2005.

13. P. Mazumder and K. Shahookar, "MathGuru Tutorial" for K-12 Education Software.

B. Reviewed Journal Publications

SEMICONDUCTOR MEMORIES

Dynamic Random Access Memory (DRAM)

14. P. Mazumder, J. H. Patel and W. K. Fuchs, "Methodologies for Testing Embedded Content-Addressable Memories", ***IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems***, Vol. 7, No. 1, Jan. 1988, pp. 11-20.

15. P. Mazumder, "Parallel Testing of Parametric Faults in a Three-Dimensional Dynamic Random-Access Memory", ***IEEE Journal of Solid-State Circuits***, Vol. 23, No. 4, Aug. 1988, pp. 933-942.

16. P. Mazumder and J. H. Patel, "Parallel Testing of Pattern-Sensitive Faults in Random-Access Memory", ***IEEE Transactions on Computers*****,** Vol. 38, No 3, Mar. 1989, pp. 394-404.

17. P. Mazumder and J. H. Patel, "An Efficient Built-In Self-Testing Algorithm for Random-Access Memory", ***IEEE Transactions on Industrial Electronics*** (Special Issue on Testing) Vol. 36, No. 3, May 1989, pp. 394-407.

18. J. S. Yih and P. Mazumder, "Circuit Behavior Modeling and Compact Testing Performance Evaluation", ***IEEE Journal of Solid-State Circuits***, Vol. 26, No. 1, Jan. 1991, pp. 62-65.

19. P. Mazumder and J. H. Patel, "A Comprehensive Study of Random Testing for Embedded RAM's Using Markov Chains", ***Journal of Electronic Testing: Theory and Applications***, Vol. 3 No. 4, Nov. 1992, 235-250.

20. P. Mazumder and J. P. Hayes, "Testing and Improving the Testability of Multi-megabit Memories", ***IEEE Design and Test of Computers***, Vol. 10, Issue 1, Mar. 1993, pp. 6-7.

21. P. Mazumder, J. H. Patel and J. A. Abraham, "A Reconfigurable Parallel Signature Analyzer for Concurrent Error Correction in Dynamic Random-Access Memory", ***IEEE Journal of Solid-State Circuits***, Vol. 25, No. 3, Jun. 1990, pp. 866-870.

22. P. Mazumder and J. Yih, "Restructuring of Square Processor Arrays by Built-in Self-Repair Circuit," ***IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*****,** Vol. 12, No. 9, Sept. 1993, pp. 1255-1265.

23. P. Mazumder, "A New On-Chip ECC Circuit for Correcting Soft Errors in DRAM's with Trench Capacitors," ***IEEE Journal of Solid-State Circuits***, Vol. 27, No. 11, Nov. 1992, pp. 1623-1633.

24. R. Venkateswaran, P. Mazumder and K. G. Shin, "On Restructuring of Hexagonal Arrays," ***IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems****,* Vol. 11, No. 12, Dec. 1992, pp. 1574-1585.

25. P. Mazumder, "Design of a Fault-Tolerant Three-Dimensional Dynamic Random-Access Memory with On-Chip Error-Correcting Circuit," ***IEEE Transactions on Computers****,* Vol. 42, No. 12, Dec. 1993, pp. 1453-1468.

26. H. Zhang, P. Mazumder, L. Ding, and K. Yang, "Performance Modeling of Resonant Tunneling Random-Access Memories," ***IEEE Transactions on Nanotechnology,*** July 2005, pp. 472-480.

Static Random Access Memory (SRAM)

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150. H. Chan and P. Mazumder, "A Systolic Architecture for High-Speed Hyper-graph Partitioning Using a Genetic Algorithm", Book Chapter in "Progress in Evolutionary Computation", Vol. 956***, Springer- Verlag***, Heildelberg, 1995, pp. 109-126.

D. Reviewed Archival Conference Publications

Generally these conferences have acceptance ratio between 15% and 35% and they require rigorous review of full paper before the decision on a paper is made. The conference publications are pertaining to work performed under various sponsored research program as indicated below.

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E. Workshop Presentations

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F. Technical Reports

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Publications in Industry (during 1976-1982)

Mixed Signal Analog and Digital VLSI Chip Design

Published over ***fifteen*** technical papers and application ideas while working at the Bharat Electronics Ltd. Topics included

- An Integrated Circuit Design for the Raster-Scan Vertical Deflection System.
- An Integrated Circuit Design for the Sync Processing Circuit
- Integrated Chip Set for Laser Range Finder in Military Applications
- An Integrated Circuit Design for High-Gain Pre-Amplifier with Automatic Level Controller
- A Integrated Circuit Design for Hearing-Aid Amplifier
- An Integrated Circuit Design for Quadrant Detection and Amplification of Frequency-Multiplexed Voice Signal
- A Large-Scale Integrated Circuit Design for Stepper-Motor-Driven Analog Clock Chip
- Study of Failure Modes in CMOS ICs During Handling
- Leakage-Current-Based Fault Characterization in a Non-planar Gas Discharge Display
- IC Design Considerations in Fabrication of Large Planar Plasma Display
- Application Notes on Analog and Digital Circuits

All these articles were published in ***BEL Application Notes*** and ***BEL Technical Report***.

IX. Book Reviews

1. J.V. Oldfield, J.P. Gray, T.A. Kean, and R.C. Dorf, "Field-Programmable Gate Arrays for Implementation and Rapid Prototyping of Digital Systems", ***John Wiley and Sons, Inc.***, New York.
2. J. Beetam, "Computer Architectures", ***Aksen Associates Inc. Publishers,*** California.
3. "The Science and Technology of Microelectronic Processing", ***Saunders College Publishing***, Pennsylvania.

4. D. Pradhan, "Fault-Tolerant System Design", ***Prentice Hall***, New Jersey.
5. Price, "Introduction to VLSI Design", ***Prentice Hall*****,** New Jersey.
6. C.P. Ravi Kumar, "Computer-Aided Design for VLSI Systems", ***Kluwer Academic Publishers*****,** Massachusetts.
7. Fu, "Neural Networks in Computer Intelligence", ***Prentice Hall*****,** New Jersey.
8. P. Banerjee, "Parallel Algorithms for VLSI Computer-Aided Design Applications", ***Prentice Hall*****,** New Jersey.
9. R. Karri, "Automatic Synthesis of Fault-tolerant VLSI Systems", ***Kluwer Academic Publishers*****,** Massachusetts.
10. A. S. Sedra and K. C. Smith, "SPICE Simulation: Microelectronics Circuits", ***Prentice Hall.***
11. A. B. Marcovitz, "Introduction to Logic Design," ***McGraw Hill.***
12. N. Jha and S. Gupta, "Testing of Digital Systems," ***Cambridge Press.***

X. Patents and Inventions

1. US Patent on Static Random Access Memory Cell having Improved Write Margin for use in Ultra-Low Power Application; US 9,627,042 issued on April 18, 2017 (Inventors: P. Mazumder, Z. Nan and J. Kim).
2. US Patent on Adaptive Reading and Writing of a Resistive Memory, US 9,111,613, issued on August 18, 2015, (Inventors: P. Mazumder and E. Idong; Assigned to Regents of University of Michigan).
3. US Patent on High-Speed, Compact, Edge-Triggered Flip-Flop Circuit Topologies Using NDR Diodes and FET's, US 6,323,709, issued on November 21, 2001, (Inventors: S. Kulkarni and P. Mazumder; Assigned to Regents of University of Michigan).
4. US and International Patents on Method and Apparatus to Improve Noise Tolerance of Dynamic Circuits, US 7,088,143, issued on August 8, 2006, (Inventors: L. Ding and P. Mazumder; Assigned to Regents of University of Michigan).
5. US Patent on Digital Logic Design Using Negative Differential Resistance Diodes and Field-Effect Transistors, US 5,903,170, awarded on May 11, 1999, (Inventors: S. Kulkarni, P. Mazumder, G. Haddad; Assigned to Regents of University of Michigan).

6. US Patent on Terahertz Analog-to-Digital Converter Employing Active-Controlled Spoofed Surface Plasmon Polariton Architecture; US 9,341,921 issued on May 17, 2016 (Inventors: P. Mazumder and Z. Xu; Assigned to Regents of University of Michigan).
7. US Patent on Mach-Zehnder Interferometer Having a Doubly-Corrugated Spoofed Surface Plasmon Polariton Waveguide; US 9,557,223 issued on January 31, 2017 (Inventors: P. Mazumder, Z. Xu and K. Song; Assigned to Regents of University of Michigan).
8. US Patent on Dynamic Terahertz Switching Device Comprising Sub-Wavelength Corrugated Waveguides and Cavity that Utilizes Resonance and Absorption for Attaining On and Off States, US 8,842,948, issued on September 23, 2014 (Inventors: P. Mazumder and K. Song; Assigned to P. Mazumder).
9. US Patent on Dynamic Terahertz Switch Using Periodic Corrugated Structures, US 8,837,036, issued on September 16, 2014 (Inventors: P. Mazumder and K. Song; Assigned to P. Mazumder).
10. US Patent on Metamaterial Sensors Platform for Terahertz Sensing; US 9,551,655 issued on January 4, 2017 (Inventors: Z. Nan, K. Song, M. Aghdajani, and P. Mazumder).

11. US Patent Provisional Application Filed on Memristor Crossbar Memory for Hybrid Ultra Low Power Hearing Aid Speech Processor. (Inventors: J. Shah, P. Mazumder and M. Barangi).
12. US Provisional Patent on Multi-Level Resistive Memory Structure; (Inventors: Y. Yalcin and P. Mazumder).
13. US Provisional Patent on Baseband Processing Techniques for Low Power Wake-up Receiver; (Inventors: N. Zheng and P. Mazumder).

Registered Inventions:

13. On-Chip Double-Bit Error-Correcting Code for 3-D Dynamic Random-Access Memory, July 28, 1989 (Inventor: P. Mazumder).

14. Yield Improvement of VLSI Chips by Using Electronic Neural Networks for Built-in Self-Repair, Feb. 15, 1990 (Inventor: P. Mazumder).
15. A Zero-Delay Overhead Circuit Technique for Built-in Self-Repair of Random-Access Memories, Oct 17, 1996 (Inventors: K. Chakraborty and P. Mazumder).
16. Dual-Rail Static Pulse Clocked Flip-flop, July 12, 2001 (Inventors: L. Ding and P. Mazumder).
17. Circuit Simulator for Quantum and Resonant Tunneling Devices, Sept. 21, 2001; (Inventors: M. Bhattacharya and P. Mazumder).
18. Multivariate Normal Distribution Based on Statistical Timing Analysis Algorithm for Digital VLSI Circuits, May 5, 2005 (Inventors: B. Wang and P. Mazumder).
19. Self-Healing Memory Design Using Low Overhead Adaptive Circuit, March 8, 2010; (Inventors: P. Mazumder and E. Idong).
20. Multi-Bit Memory Read Method for Nonvolatile Memory, Dec 19, 2011; (Inventors: Y. Yilmaz and P. Mazumder)
21. 16 T Static Random Access Memory Cell Design for Improved Performance in Asynchronous Digital Systems, Oct. 29, 2012 (Inventors: J. Kim and P. Mazumder).
22. EM Based Terahertz Logic Design, June 4, 2015 (Inventors: Y. Yilmaz and P. Mazumder)

XI. Software Package Developed

After finishing my MSc degree in Computer Science and while working towards my PhD degree in Electrical and Computer Engineering, I worked during the summers of 1985 and 1986 as a Member of Technical Staff at AT&T Bell Laboratories. I was one of the two engineers who started the Bell Laboratory *Cones/Spruce* project - a new behavioral synthesis and layout automation tool for rapid prototyping of digital circuits. The main contribution of this effort was to demonstrate how a restricted version of C language could be used to model digital hardware much before commercial hardware description language (HDL) software tools like Verilog and System C were designed.

After joining the University of Michigan, I have assisted my doctoral students in developing the following software packages that were written using C and C++ languages.

1. **Q-SPICE:** A Spice-based circuit simulator for CMOS, GaAs, InP and GaSb devices for RTD, and RHET. New homotopy based convergence algorithms were developed to improve DC convergence of RTD based nonlinear circuits that regular SPICE program fails to simulate.

2. **VEDICS:** Variable-mesh Electromagnetic Device and IC simulator, a full-chip detail simulator for estimating circuit performance at high speed. It uses transmission line matrix method to solve Maxwell-like wave equations and thereby VEDICS can account for reflections, scattering and inductive effects in a VLSI chip.

3. **BISRRAMGEN:** A VLSI compiler for automatic generation of embedded byte-oriented memories with built-in self-testing and self-repair capabilities.

4. **GASP:** A VLSI layout generation tool that generates chip layout with optimized standard cells and macro cells placement and routing.

XII. Consulting Activities

1. Served as ***Expert*** for the US National Science Foundation, Arlington, Virginia.
2. Served as a member of ***Technical Advisory Board*** for. Sequence Design Automation (Santa Clara, CA), Silicon Value Inc. (Jerusalem, Israel), and Tioga Technology (San Jose, CA).
3. Served as ***Technical Advisor and Expert Witness*** in 15 lawsuits involving DRAM, SRAM, Flash and FPGA. (For details see Section XIII).

4. Served as ***Consultant*** in the areas of SRAM self-healing circuits; radiation hardening and soft-error problems in SRAM and FPGA's; JTAG testing of FPGA's; ultra-low-power CMOS circuits; nanoelectronic circuits and simulation tools.

Legal Expert Services Rendered

Served as ***Technical Advisor and Expert Witness*** in the following lawsuits between 1999 and now. My expert services involved (i) Analysis of alleged patents; (ii) Producing prior art; (iii) Writing Expert Reports for Invalidation of claims and Non-infringement of claims working for Defendant, and Infringement claims working for Plaintiff; (iv) SPICE circuit simulation of accused products; (v) VHDL and Verilog source code analysis; (vi) Computer hardware testing. (vii) Testimony by deposition over 50 hours; and (viii) Testimony in trial as invalidity and non-infringement expert.

Fields of Expertise for Expert Services

- Semiconductor memories (DRAM, SRAM, Flash, and emerging non-volatile memories);
- Field-Programmable Gate Arrays (FPGA) hardware and software;
- Mixed-signal VLSI chip testing; boundary scan testing; design for testability
- VLSI chip design including analog, digital and RF circuits;
- Nanoscale CMOS VLSI system design;
- VLSI layout tools for placement, routing, floorplanning with timing and power constraints;
- VHDL, Verilog and C based complex system simulation and verification;
- Sensing and detecting devices and amplifying circuits.

Consulting in Legal Cases performed in 1999-2015

i) **DRAM Testing Methods and Circuits**
Hyundai v. Siemens (1999)

Law firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP
Type of appointment: Testifying Expert for Plaintiff
Expert Work rendered for **Plaintiff** involved the following:

- Analyzing 5 European and US patents including 5,208,776, a 293 page patent on DRAM;
- Producing prior art;
- Preparing Expert Report;
- Testimony in trial.

Outcome in trial: Plaintiff won in trial and Defendant's patent was invalidated.

ii) **Posted CAS Method and Determination of CAS Latency in Synchronous DRAM**
Samsung Electronics Co. v. NVIDIA Corporation (2015)

Law firm for Defendant: Latham & Watkins
Type of appointment: Testifying Expert for Defendant
Expert Work rendered for **Defendant** involved the following:

- Analyzing the alleged patent, US 6,262,938: Synchronous DRAM having posted CAS latency and method for controlling CAS latency;
- Analyzing six prior art;
- Establishing non-infringement in accused NVIDIA products;
- Writing a 282-page Invalidity Expert Report
- Writing a 84-page Non-infringement Expert Report
- Writing a 20-page Damages Expert Report
- Giving testimony at deposition; Samsung dropped 4 claims based on my testimony

- Preparation for direct and cross-examination in mock trial

Outcome: Samsung lost in trial

iii) **DRAM Redundancy Techniques for Yield Improvement**
Limestone Memory Systems LLC v. Apple, Inc. (2016)

Law firm for Defendant: Kenyon & Kenyon, LLP
Type of appointment: Testifying Expert for *Inter Partes* Review (IPR)
Expert Work rendered for **Petitioner** involved the following:

- Analyzing the alleged patent, US 5,894,441: Semiconductor Memory Device with Redundancy Circuit;
- Analyzing prior art;
- Preparing Declaration for IPR nearly 105 pages;

Outcome: Settled.

iv) **DRAM Improved Flexible Redundancy Techniques**
Limestone Memory Systems LLC v. Apple, Inc. (2016)

Law firm for Defendant: Kenyon & Kenyon, LLP
Type of appointment: Testifying Expert for *Inter Partes* Review (IPR)
Expert Work rendered for **Petitioner** involved the following:

- Analyzing the alleged patent, US 6,23,381: Semiconductor memory device with improved flexible redundancy scheme;
- Analyzing prior art;
- Preparing Declaration for IPR nearly 90 pages;
- Deposed by *LMS* attorney

Outcome: Settled after PTAB instituted the petition.

v) **Memory Board with Self-Testing Capability**
Netlist, Inc. v. SK Hynix, Inc. (2016)

Law firm for Defendant: Sidle Austin
Type of appointment: Testifying Expert for *Inter Partes* Review (IPR)
Expert Work rendered for **Petitioner** involved the following:

- Analyzing the alleged related patent US 8,001,434: Memory Board with Self-Testing Capability; US 8,359,501.
- Analyzing Prior art;
- Preparing Declaration for IPR nearly 100 pages for '434 Patent;
- Deposed by *Netlist* attorney;

Outcome: Defendant's Petition is instituted by PTAB.

vi) **Self-Testing of Memory Modules such as RDIMM and LRDIMM**
Netlist, Inc. v. SK Hynix, Inc. (2016)

Law firm for Defendant: Sidle Austin
Type of appointment: Testifying Expert for *Inter Partes* Review (IPR)
Expert Work rendered for **Petitioner** involved the following:

- Analyzing the alleged related patent US 8,359,501: Memory Board with Self-Testing Capability.
- Analyzing Prior art;
- Preparing Declaration for IPR nearly 100 pages for '501 Patent;
- Deposed by *Netlist* attorney;

Outcome: Defendant's Petition is instituted by PTAB.

vii) **Method for Self-Testing of Multi-Rank Memory Modules**

Netlist, Inc. v. SK Hynix, Inc. (2016)

Law firm for Defendant: Sidle Austin
Type of appointment: Testifying Expert for *Inter Partes* Review (IPR)
Expert Work rendered for **Petitioner** involved the following:

- Analyzing the alleged related patent US 8,689,064: Apparatus and Method for Self-Test in a Multi-Rank Memory Module.
- Analyzing Prior art;
- Preparing Declaration for IPR nearly 100 pages for '064 Patent;
- Deposed by *Netlist* attorney;

Outcome: Defendant's Petition is instituted by PTAB.

viii) **SDRAM and NAND Flash Memory Controllers for Solid-State Drive**
North Star Innovations, Inc. v. Micron Technology (2018)

Law firm for Defendant: Weil, Gotshal & Manges LLP
Type of Appointment: Testifying Expert for *Inter Partes Review* (IPR)
Expert Work rendered for **Petitioner** involved the following:

- Analyzing the alleged patents, US 7171526: Memory controller useable in a data processing system
- Analyzing Prior art;
- Preparing Declaration for IPR for '526 Patent

Outcome: Petition and Declaration submitted to PTAB in May 2018.

ix) **Current and Voltage Sense Amplifiers for SRAM**
Progressive Semiconductor Solutions, LLC v. Marvell Semiconductor (2013)

Law firm for Defendant: Fish & Richardson P.C.
Type of Appointment: Non-infringement Expert for Defendant
Expert Work rendered for **Defendant** involved the following:

- Analyzing the alleged patents, US 6,473,349: Cascode Sense Amp and Column Select Circuit and Method of Operation; and US 6,862,208: Memory Device with Sense amplifier and Self-Timed Latch;
- Analyzing a group of accused products manufactured by the Defendant for non-infringement of asserted claims;
- Studying Prior Art for Invalidation Contentions
- Preparation of draft for the non-infringement claim

Outcome: Case settled.

x) **FPGA Debugging and Testing through Boundary Scan Circuits**
Intellitech Corp. v. Xilinx and Lattice Semiconductor (2011)

Law firm for Defendant: Kirkland & Ellis LLP
Type of Appointment: Expert for Defendant
Expert Work rendered for **Defendant** involved the following:

- Analyzing the alleged patent, US 6,594,802: Method and Apparatus for Providing Optimized Access to Circuits for Debug, Programming, and Test;
- Producing prior art;
- Establishing non-infringement in testing protocols used in a group of Xilinx and Lattice Semiconductor FPGA products;
- Assisting in preparation of Invalidation Contentions;
- Analyzing over 1000 lines of VHDL codes (open domain) used for Xilinx and Lattice Semiconductor FPGA testing and reconfiguring

Outcome: Settlement and licensing arrangement.

xi) **DRAM Cell and Voltage Pump Circuits**
Mosaid Technologies v. Samsung (2004)

Law firm: The Morgan Lewis
Type of appointment: Consultant for Morgan Lewis
Consulting Work rendered involved the following:

- Performing SPICE simulation of DRAM word-line timing circuits and Vpp pump circuits for all types of defendant's accused products that included two different types of SDRAMs (synchronous memory chips), three types of DDR RAMs (fast double data rate memory chips), one type of SGRAM (graphics RAM chip), and one type of Rambus RAM (fast memory chip);
- Demonstration of SPICE simulation to attorneys.

xii) **Synchronous Link DRAM for Fast Memory Access and Digital Locked Loop in SDRAM**
Mosaid Technologies v. Nanya Technology Corp. (2010)

Law firm: Shore Chan DePumpo LLP
Type of appointment: Consultant and Expert for Defendant
Expert Work rendered for **Defendant** involved the following:

- Analyzing three different patents: US 7,299,330: High Bandwidth Memory Interface; US 6,992,950: Delay Locked Loop Implementation in a Synchronous DRAM; and US 5,903,511: Flexible DRAM Array;
- Producing prior art;
- Non-infringement technical report.

Outcome: Case settled.

xiii) **Texture Cache Memory and Memory Controller in Graphics Chips**
Advanced Silicon Technologies v. NVIDIA Corp. (2016)

Law firm for Defendant: Latham & Watkins
Type of appointment: Consultant and Expert for Defendant
Expert Work rendered for **Defendant** involved the following:

- Analyzing and helping in preparation of Invalidity Contention charts for two different patents: US 6339428 B1: Method and apparatus for compressed texture caching in a video graphics system, and US 6546439 B1: High Bandwidth Memory Interface; Method and system for improved data access
- Producing prior art

xiv) **Reliability Testing of Display Driver Chips in CRT Monitor**
Hyundai v. Princeton Graphics (2000)

Consulting work for **Defendant** involved (i) Analyzing the complete drive circuits for CRT based displays comprising several digital and analog ICs, high-voltage devices, and passive components; (ii) Studying failures of the display monitor under elevated temperatures; (iii) Writing the reliability report of display drive of the CRT monitor.
Outcome: Settled.

xv) **SDRAM Timing Verification**

Worked as a consultant for Perkins Coie LLP in infringement contention on*:*

- US 6,574,759: A method of generating and verifying a memory test

xvi) **NAND Flash Memory Scrubbing, Wear-leveling and Error-correction**

Worked as a consultant for Bunsow, De Mory, Smith & Allison LLP in infringement contention on the following flash memory patents:

- US 8,050,095: Flash memory data correction and scrub techniques
- US 6,510,488: Method for fast wake-up of a flash memory system
- US 7,120,729: Automated wear leveling in nonvolatile storage systems
- US 6,831,865: Maintaining erase counts in nonvolatile storage systems
- US 7,181,611: Power management block for use in a nonvolatile memory system

xvii) **3-D NAND Flash Memory Systems**

Reviewed for WilmerHale LLP in a pre-suit infringement analysis on following patents:

- US 8,830,755: Reducing weak-erase type Read disturb in 3-D nonvolatile memory;
- US 6,771,536: Operating techniques for reducing Program and Read Disturbs nonvolatile memory;
- US 6,954,394: Integrated circuit and method for selecting a set of memory-cell-layer-dependent or temperature-dependent operating conditions;
- US 7,251,160: Nonvolatile memory and method with power-saving Read and Program-Verify operations;
- US 8,520,441: Word line kicking when sensing nonvolatile storage.

xviii) **Hall-Effect Magnetic Field Sensing and Amplification by Chopper Amplifier Chip**
Consulting work for **Defendant** involved (i) Analyzing the alleged patent; (ii) Simulation of chopper amplifier for magnetic sensor; (iii) Producing prior art.
Outcome: Settled.

XIII. Teaching Accomplishments

i) Received a letter of commendation from Dean of Engineering for excellence in undergraduate teaching
ii) Received a certificate of recognition from Vice Provost of Academic Affairs and Vice Provost of International Affairs for global outreach activities

Undergrad Courses Taught:

- **Sophomore Level:**
  EECS 270: Digital Logic Design
  Sample Lecture Slides | Course Outline | Old Course Materials

- **Junior Level:**
  EECS 312: Digital Integrated Circuit Design
  Sample Lecture Slides | Course Outline

- **Senior Level:**
  EECS 427: VLSI Design
  Sample Lecture Slides | Course Outline

Regular Graduate Courses Taught:

- EECS 570: Parallel Architectures
  Sample Lecture Slides | Course Outline

- EECS 579: Digital System Testing
  Sample Lecture Slides | Course Outline

New Graduates Courses Developed:

- EECS 527: VLSI Layout Automation
  Sample Lecture Slides | Course Outline

- EECS 598-2: Nanocircuits and Nanoarchitectures
  Sample Lecture Slides | Course Outline

- EECS 598-3: Terahertz Engineering and Applications

- EECS 598-6: Ultra-Low-Power CMOS Design
  Sample Lecture Slides | Course Outline

On-line Courses for Practicing Engineers:

- NTU-Walden University Distant Learning Course on Logic Design

Integration of Research with Teaching:

VLSI Courseware Developed and Distributed:
- Cell Placement Algorithms
- VLSI Routing Algorithms
- Gate Matrix Algorithms

Advanced Books Written for Practicing Engineers:

- Genetic Algorithms for VLSI Design
- SRAM & DRAM Testing
- Reliability of Semiconductor Memories
- Proceedings of the IEEE: Special Issue on Memristors

STEM Education and K-12 Math Software Developed:

- MathGuru

Teaching Evaluations:

- Numerical Evaluations | Student Comments | Vice Provost's Letter

XIV. Student Theses Supervised

A. Ph.D. Theses Completed

1. J. Yih, "*Built-In Self-Repair of Embedded Memory and Logic Arrays*," 1990. Currently at IBM T. J. Watson Research Center, Yorktown, New York.
2. K. Shahookar, "*Genetic Algorithms for CAD Layout Problems*," 1994. Currently at his start-up company in Pakistan.
3. H. Esbensen, "*Application of Genetic Algorithms for Cell Placement and Routing Problems*," 1994. Currently at Avant! Fremont, California.

4. V. Ramachandran, "*Parallel Architectures for Multilayer Wire Routing Problems*," 1994. Currently at Cadence Design Systems, San Jose, California.
5. S. Mohan, "*Design of Ultra-fast Digital Circuits using Quantum Electronic Devices*," Dec. 1994. Currently at Xilinx Corporation, Campbell, California.
6. K. Chakraborty, "*Built-In Self-Repairable RAM Compiler Design*," Mar. 1997. Currently at Agere Design, Murray Hills, New Jersey.
7. M. Bhattacharya, "*Simulation and Emulation of Digital Integrated Circuits Containing Resonant Tunneling Diodes,*" Oct 1999. Currently at Avant! Fremont, California.
8. S. Kulkarni, "*Quantum MOS Circuits and Systems*," Oct 1999. Working in IDT, Atlanta, Georgia.
9. A. Gonzalez, "*Multiple-Valued Logic and High-Speed Digital Circuits Using Resonant Tunneling Diodes*," June 2001. Currently at IDT, Atlanta, Georgia.
10. Li Ding, "*Dynamic Noise Analysis in Deep Sub-micron CMOS VLSI Systems*," Feb. 2004. Currently at Synopsis, Sunnyvale, California.
11. Q. W. Xu, "*Accurate Interconnect Modeling for Efficient Transient Simulation in VLSI Chip Design,*" May 2006, currently at Cadence Design Systems, California.
12. B. Wang, "*Accelerated Chip-level Thermal Analysis Using Multilayer Green's Function*," May 2008, currently at VmWare, California.
13. W. H. Lee, "*Applications of Nanoelectronic Technology to Image Processors, Velocity-Tuned Filters and Crossbar Memories*", Dec 2008, currently working at Intel Corporation, California.
14. K. Song, "*The Modeling, Simulation and Design Plasmonic Nanoarchitecture for Ultrafast Circuit Systems*," Aug. 2010, currently working at Korean Institute of Machinery and Materials, Daejeon, Korea.
15. I. Ebong, "*Methods of Training Memristors for Next Generation Computing*," Dec. 2012, currently working as a Technical Advisor for Leydig, Voit & Mayer, Ltd., Chicago, Illinois.
16. X. Zhao, *"Terahertz (THz) Waveguiding Architecture Featuring Doubly-Corrugated Spoofed Surface Plasmon Polariton (DC-SSPP): Theory and Applications in Micro-Electronics and Sensing ,"* Dec. 2016, currently working at Apple, Inc., California.
17. M. Barangi, "*Straintronics: A Leap towards Ultimate Energy Efficiency of Magnetic Memory and Logic*", Dec. 2016, currently working at Apple, Inc., California.
18. Y. Yalcin, "*Bio-inspired Hardware Architectures for Memory, Image Processing, and Control Applications*," Dec. 2016, currently working at Cadence, California.
19. J. Kim, "*Ultra Low-power Wireless Sensor Node Design for ECG Sensing Applications,*" Dec. 2016, currently working at Oracle, Inc., California.
20. N. Zheng, "Algorithm/Architecture Co-Design for Low-Power Neuromorphic Computing" Dec. 2017, currently working at Apple, Inc. California
21. M. Aghdajani, "Spoof Plasmon Polariton Based THz Circuitry," Dec. 2017, working at a start-up company at Austin, Texas.

B. M.S. Theses/Projects Completed:

22. B. Brighton, *Pseudo-Random Testing for Embedded Memories*
23. K. Quasim, *Analog Circuit Testing*
24. J. Kapson, *Parallel CAD Architecture*
25. D. Berryman, *Parallel Processing for VLSI Routing*
26. M. Smith, *Self-Repairable Memory Array Using Digital Neural Circuit*
27. E. Chan, *RTD-based Multi-valued Circuit Design*
28. A. Arunachalam, *Fine-Grained Parallel Routing*
29. A. Gonzalez, *Multi-valued Adder Design Using CMOS and RTD*
30. A. Gupta, *Self-Repairable ROM Generator*
31. J. Xiong, *Quantum MOS Circuit Design*
32. G. Mittal, *Simultaneous Switching Noise Analysis in Embedded Memories*
33. V. Warraich, *Web-based Applets Design for Digital Logic*
34. M. Kumshikar, *Amorphous TFT-based Driver Logic Design for AMLCD Panel*
35. G. Shankar, *Amorphous TFT-based Operational Amplifier Design for AMLCD Panel*
36. V. Ramachandran, *Array Machine for VLSI Routing*
37. S. Mohan, *Parametric Testing for SRAM's Using GaAs High Electron Mobility Transistors*

38. S. Kulkarni, *CMOS and RTD-based Correlators Design*
39. K. Shahookar, *Genetic Algorithm for VLSI Placement*
40. H. Chan, *Macro-cell Placement Using Genetic Algorithm*
41. L. Ding, *Noises in Deep Sub-micron VLSI Chips*
42. Q. W. Xu*, VLSI Interconnect Modeling Using Differential Quadrature Method*
43. B. Wang, *3-Dimensional Full Chip Simulation by Transmission Line Matrix Method*
44. H. Zhang, *Ultra-fast RTD-based Circuit Design*
45. S.R. Li, *RTD-based Cellular Nonlinear Networks*
46. D. Shi, *Quantum Dot Based Image Processing*
47. M. Rajagopal, *Modeling of Resonant Tunneling Diodes*
48. W. Lee, *Image Processing Applications of Quantum Dots*
49. E. Ibong, *Subthreshold Low-power Operational Amplifier Design*
50. K. Song, *Plasmonics Applications in VLSI*
51. C. Ting, *Modeling of Ionic Current through Memristors*
52. Y. Yilmar, *Straintronics Pipelined Adder Design*
53. J. Qian, *Green Function based Thermal Modeling*
54. H. Liu, *Straintronics SRAM Design*
55. N. Zheng, *Nanoscale Subthreshold Mixed Signal Chip Design*
56. D. Hu, *STDP based Learning Chip Design*

Number of Doctoral Students Currently Being Supervised: 7.

C. Visiting Scholars (International Outreach)

1. Dr. T. Ueymura, NEC, Japan; 2. Prof. H. Choi, Hanyang University, South Korea; 3. Mr. H. Esbensen, Aarhus University, Denmark.; 4. Dr. Q. W. Xu, China; 5. Dr. J. P. Sun, Shanghai Jiao Tong University, China; 6. Prof. S. Duan, South East University, China; 7. Prof. Y. Yongbin, University of Electronic Science and Technology, China; 8. Mr. T. Glotzner, Germany; 9. Prof. L. Feng, University of Electronic Science and Technology, China; 10. Dr. M. Erementchouk, Russia

D. Undergrad Thesis & Project Supervised (International Outreach)

1. S. Sayyaparaju (Indian Institute of Technology, Roorkee), 2. H. Biswas (Indian Institute of Technology, Kanpur), 3. J. Induri (Indian Institute of Technology, Roorkee), 4. S. Kallia (Indian Institute of Technology, Kharagpur), 5. S. Panda (Indian Institute of Technology, Kahargpur), 6. A. Bhat (Birla Institute of Technology and Science, Pilani), 7. J. Shah (Birla Institute of Technology and Science, Pilani), 8. N. Talati (Birla Institute of Technology and Science, Goa), 9. Sun Li (Beijing University, China).

XVI. Technical Presentations (excluding conferences and workshops)

Formal Talks at Universities

1. Multilayer VLSI routing techniques at ***University of California***, Berkeley, California.
2. Memory testing at ***Stanford University***, Palo Alto, California.
3. Beyond CMOS technologies and architectures at ***California Institute of Technology***, Pasadena.
4. Beyond CMOS technologies and architectures at ***Columbia University***, New York.
5. Quantum electronic circuit design at ***University of Illinois***, Urbana-Champaign, Illinois.
6. Quantum electronic circuit design at ***University of California***, Berkeley, California.
7. Quantum electronic circuit design at ***Seoul National University***, Seoul, Korea.
8. Quantum electronic circuit design at ***Beijing University***, Beijing, China.
9. Quantum electronic circuit design at ***Gerhard-Mercater University***, Duisburg, Germany.
10. Quantum electronic circuit design at ***Fraunhofer Institute***, Freiburg, Germany.

11. Quantum electronic circuit design at ***South West University,*** Chongqing, China.
12. Quantum electronic circuit design at ***University of Santiago***, Spain.
13. VLSI layout design at ***Princeton University***, Princeton, New Jersey.
14. Memory testing at ***Purdue University***, West Lafayette, Indiana.
15. Memory testing at ***University of Southern California***, Los Angeles, California.
16. Built-in self-repairable IC design at ***University of Iowa***, Iowa City, Iowa.
17. Memory testing at ***King Fahd University***, Saudi Arabia.
18. Quantum electronic circuit design at ***Nanjing University,*** Nanjing, China.
19. Memory testing at ***Johns Hopkins University***, Baltimore, Maryland.
20. Quantum electronic circuit design at ***Ohio State University***, Columbus, Ohio.
21. Quantum electronic circuit design at ***Rice University***, Houston, Texas.
22. Quantum electronic circuit design at ***University of California*** at Riverside.
23. Quantum electronic circuit design at ***Notre Dame University***, South Bend, Indiana.
24. Memory testing at ***University of Minnesota***, Minneapolis, Minnesota.
25. Quantum electronic circuit design at ***University of Tokyo***, Tokyo, Japan.
26. Quantum electronic circuit design at ***Delft Technological University***, Delft, Netherlands.
27. Quantum electronic circuit design at ***King Fahd University***, Saudi Arabia.
28. Quantum electronic circuit design at ***Universidad de Las Palmas de Gran Canaries***, Spain.
29. Quantum electronic circuit design at ***South East University,*** Nanjing, China.
30. Beyond Moore's Law Disruptive Technologies at ***Riken Lab***, Wako-shi, Japan.
31. Beyond Moore's Law Disruptive Technologies at ***KAIST***, Daejeon, Korea.
32. Memory testing and repair algorithms at ***Indian Institute of Technology***, New Delhi, India.
33. Beyond Moore's Law Technology and Architectures at ***Riken Laboratory***, Tokyo, Japan.
34. Beyond Moore's Law Technology and Architectures at ***Pazmany Peter Catholic University***, Budapest, Hungary.
35. Beyond Moore's Law Disruptive Technologies at ***South West University***, Chonqing, China.
36. Versatile Applications of Memristors at ***Politecnico di Torino***, Torino, Italy.
37. Beyond Moore's Law Disruptive Technologies at ***Shanghai Jiao Tong University***, China.
38. Beyond Moore's Law Disruptive Technologies at ***University Electronic, Science and Technology***, Chengdu, China.
39. Memory testing at ***Texas A&M University***, College Station, Texas.
40. Beyond Moore's Law Disruptive Technologies at ***A*STAR***, Singapore.
41. Quantum electronic circuit design at ***Northwestern University***, Evanston, Illinois
42. Built-in self-repairable IC design at ***Wayne State University***, Detroit, Michigan.
43. VLSI layout design at ***Indian Institute of Science***, Bangalore, India.
44. Quantum electronic circuit design at ***Indian Statistical Institute,*** Calcutta (Kolkata), India.
45. Quantum electronic circuit design at ***Indian Institute of Technology***, Kharagpore, India.
46. Beyond Moore's Law Technology and Architectures, ***Asian Institute of Technology,*** Bangkok.
47. IEEE Distinguished Lecture at ***Indian Institute of Technology***, Madras (Chennai), India.
48. IEEE Distinguished Lecture at ***University of Illinois***, Chicago.
49. IEEE Distinguished Lecture at ***Indian Institute of Science,*** Bangalore, India.
50. IEEE Distinguished Lecture at ***Dhaka University***, Dhaka, Bangladesh.
51. IEEE Distinguished Lecture at ***Tata Institute of Fundamental Research***, Mumbai, India.
52. IEEE Distinguished Lecture at ***Indian Institute of Technology***, Bombay (Mumbai), India.
53. IEEE Distinguished Lecture at ***Jadavpur University***, Calcutta (Kolkata), India.
54. Quantum electronic circuit design at ***Nanyang Technological University***, Singapore.

Formal Visits to University Laboratories

55. VLSI Design and Education Center, ***University of Tokyo***, Tokyo, Japan.
56. Nanoscale Science and Engineering Center, ***Harvard University***, Harvard, Massachusetts
57. Computer Engineering Research Center, ***University of Texas***, Austin, Texas.
58. Nanoelectronics Laboratory, ***University of Texas***, Dallas, Texas.
59. ***Technical University of Budapest***, Budapest, Hungary.
60. ***Massachusetts Institute of Technology***, Cambridge, Massachusetts.
61. ***University of North Carolina***, Chapel Hill.

62. ***Virginia Commonwealth University***, Richmond, Virginia.
63. ***Duke University***, Durham, North Carolina
64. ***Oxford University***, Oxford, England.
65. ***Zheng Zhou Light Industry University,*** Zheng Zhou, China
66. Nanocenter at ***University of Virginia,*** Charlottesville, Virginia
67. Supercomputing Center at ***University of California at San Diego,*** California.
68. Quantum Information Center at ***California Institute of Technology,*** Pasadena, California.

XVII. List of Courses Taken During M.Sc. (in CS) and Ph.D. (in CE) Study

My BS degrees were in Physics Honors and Electrical Engineering, while my MSc and PhD degrees were in CS and CE, respectively. I took the following CS and CE courses while doing my MSc and PhD:

1) Analysis of Algorithms, 2) Artificial Intelligence, 3) Computer Networks, 4) Computer Architecture, 5) Software Engineering, 6) Local Area Networks, 7) Adaptive Systems, 8) VLSI Complexity Theory, 9) Switching Theory and Digital Logic Design, 10) Parallel Computer Architectures, 11) Minicomputer System Architectures, 12) VLSI Layout Automation and Circuit Simulation, 13) VLSI System Design, 14) AI Based CAD for VLSI, 15) Digital Testing and Fault Tolerance, and 16) Programming Languages.

Ph.D. Thesis Title: ***Testing and Fault-Tolerance Aspects of High-Density Random-Access Memory,*** *University of Illinois at Urbana-Champaign, 1988. Synopsis:* The thesis introduced the "line-mode plurality testing technique" for high-density DRAM and CAM chips. Based on this design-for-testability approach, fast parallel testing algorithms were developed for testing a broad class of parametric and pattern-sensitive faults. The resulting test procedures are significantly more efficient than previous approaches due to test length optimization by applying the chromatic plane ornamentation theory. In many embedded memory applications where neither the input address and read/write lines are externally controllable nor are the output lines directly observable, the proposed algorithms can be adapted for implementing deterministic built-in self-test (BIST) circuits by designing the read/write sequences through Hamiltonian tours on the hypercube graph. Also, the thesis presented an extensive amount of Markov modeling and probabilistic analysis in order to determine the lengths of randomly applied test patterns for various classes of functional faults in scattered and small embedded-memories where the proposed deterministic BIST technique cannot be incorporated. Finally, the thesis addressed the improvement of storage reliability by two orders of magnitude by introducing a new on-chip error correcting (ECC) technique capable of correcting the double-bit errors due to alpha particles striking between the 3-D vertically integrated trench DRAM cells. The thesis also analyzed the limitations of popular types of double-bit ECC techniques like the Projective Geometry Code in VLSI applications. The research resulted in 6 archival journal papers, 6 conference papers, and several chapters in two books on semiconductor memories coauthored by me.

NB: Even though when the thesis was written in 1987 DRAM chip size was merely 1 Mega bit and the proposed "line-mode plurality testing technique" was not necessary, the proposed method has been widely adopted by memory chip manufacturers in Giga-bit DRAM chips in order to reduce the memory chip testing time by a significant margin (nearly a thousand times).

XVIII. Details of My Research Accomplishments:

I have secured 54 research grants (21 NSF, 19 Department of Defense, 8 Industrial, 2 Korean Govt., and 3 others) amounting to nearly $14 Million (for my share) and over $40 Million (collective) to conduct the above research projects. Diversity, girth, vision, and synergistic problem solving are the hallmark of my group's research that integrates multidimensional knowledge from solid-state devices, circuit theory, numerical analysis, electromagnetic theory, and quantum physics. While such innovative research approach has enabled us to establish the theoretical foundation for solving complex problems in nanoscale VLSI systems, they have also been widely adopted in commercial VLSI systems, thereby providing technology transitioning of our federally and privately funded research work.

I. Evolutionary Research -- Where the Puck is Going to be

My MS thesis described a vision for "multicore parallel processor" (Intel and AMD built multicore chip about 20 years later and on-chip parallel processing is now being widely adopted) by combining VLSI complexity theory, parallel computer architectures, and mathematical theory of chromatic plane ornament, which appeared in 3 major computer journals and 3 archival conference proceedings. I extended my MS thesis work to design efficient quad-tree data-structures for 2- dimensional query processing in computer vision, video image processing, and geographical map analysis.

1. **Conventional Semiconductor Memories**

In 1985, when I joined the University of Illinois for my PhD, I was recruited to work in a Semiconductor Research Consortium (SRC) research project to develop new testing methodologies for semiconductor memory chips. At that time, commercial test equipment used simple functional testing methods to detect rudimentary manufacturing defects, and the university research was primarily confined in incremental refinement of functional test algorithms. Since I had worked six years in industrial R&D laboratories after my BS degree, I could envision the need for new way of accelerated memory chip testing with the aggressive increase in density of integration due to scaling. For the first time, I combined the concepts of VLSI process technology, memory layout, circuit design, and theoretical techniques like graph theory and Markov chain modeling to invent "In-line testing" circuitry and comprehensive accelerated test procedures that curtailed "chip testing time" by nearly a thousand times.

Also, 10 years after my doctoral work on testable memory design, several semiconductor manufacturers adopted my invention in their products, thereby impacting the DRAM industry. I was hired as Expert Witness to help Samsung, Hyundai, Hynix, Nvidia and Nanya in 10 different major lawsuits. Some of these companies adopted my published papers in their memory products and were later sued by companies who had secured patents based on my research ideas that predated those patents. In 1997, Professor Sudhakar Reddy of University of Iowa, a pioneer in the field of VLSI testing affirmed my fundamental contributions in memory testing: "*Dr. Mazumder was the first to argue that testing of random-access memories will require parallel and built-in testing of RAMs. This is now the practice in both off-line and built-in testing of RAMs*."

My student and I invented an innovative testing method of embedded memories for programming FPGAs through the newly introduced IEEE/JTAG standard for boundary-scan port in 1997. I was hired in 2011 to help Xilinx, Altera, and Lattice Semiconductor who were sued by a test company for infringing on its 2003 patent, which was derived from our previously published papers. Our invention on boundary- scan testing was widely adopted by FPGA industry.

In 1991, for the first time our group developed an efficient *self-healing* methodology for VLSI chips, which was later adapted (in 1997) in our *self-repairable* RAM compiler. In Oct. 1995 by Prof. Kent W. Fuchs who is currently the President of University of Florida at Gainesville recognized my original contributions: "*Dr. Mazumder also initiated the area of built-in self-repair for memories. He was the first to develop designs for embedded repair of memory and computational arrays*." I have coauthored two definitive books on testing and reliability of high-density semiconductor memories that are widely used by VLSI practicing engineers in industry as well as academic researchers. "*Simplicity is the ultimate sophistication*" is the key to numerous design ideas proposed in our books.

2. Emerging Memory Technologies

As conventional static and dynamic random-access memories are confronting multiple formidable challenges with CMOS technology rapidly shrinking to its fundamental limits, our research transcended the realms of conventional memory technologies by pursuing *three* disparate types of emerging memory technologies. We made key inventions that resulted in *five* US patents and several archival journal papers. Our group studied co-integration of quantum tunneling diodes with DRAM and invented key circuit elements for "*tunneling dynamic memory* (TRAM)" technology that eliminated refreshing of DRAM cells and saved energy consumption and soft errors significantly. Our group subsequently invented adaptive programming and erasing techniques for nonvolatile "*resistive memory* (RRAM)" technology that is now poised to replace conventional flash memories due to the superior integration density and lifespan of RRAM memories. Further, to push the frontiers of high-performance and reliable computing by developing nonvolatile magnetic memories inside microprocessor chips, my research group has worked on electron spin-based "*straintronics tunneling junction memory* (STJ-RAM)" technology. These memories have life span comparable to conventional SRAM and DRAM, thereby providing a roadmap for magnetic

solid-state memories that will slowly replace traditional SRAM-based cache memories as well as the bulk of main memories and solid-state disks that currently employ a combination of DRAM and flash memories.

II. Biology-inspired Disruptive Computing 1. Evolutionary Computing Using Genetic Algorithms

My research group has also done extensive research in biology-inspired computation to develop distributed VLSI chip layout algorithms over networked workstations and desktop computers. Our group developed evolutionary class of algorithms that mimic the Darwinian principle of "survival of the fittest" for biological species by designing multi-dimensional chromosome-encoding schemes to solve various types of VLSI layout automation problems. My overall vision in VLSI layout automation was to equip distributed networks of workstations with a specialized hardware accelerator board containing the polymorphic chips developed by my research group to accelerate different styles of VLSI routing algorithms, while Genetic Algorithms would speed up the cell placement algorithms over a cluster of networked workstations. Parallel implementations of the distributed algorithms demonstrated that super- linear speed-ups could be achieved not only for solving VLSI layout problems, but also for a wide variety of engineering problems. In order to promote research in mathematical modeling of the genetic algorithm, I coauthored a book with Dr. Elizabeth Rudnick to illustrate multidimensional genotype encoding schemes and phenotype optimization for different engineering applications. According to Professor Ernest Kuh of UC-Berkeley, who served as the Dean of Engineering and received numerous prestigious awards for his pioneering work in VLSI CAD: "*In physical design he is one of the top leaders especially in developing placement techniques: The genetic algorithms which he is a pioneer in applying to CAD has paid off*."

2. Biology-inspired Brain-like Neural Computing

Our research in early 1990's to empower VLSI memories and arrays *self-healing* and *self- repairable* by inventing compact neural networks was contemporaneous with Prof. Carver Mead's neuromorphic designs for artificial retina and cochlea on silicon substrates. Inspired by Caltech group's groundbreaking research, we invented hardware-friendly brain-like learning techniques such as spike time-dependent plasticity (STDP), reinforcement learning (Q-learning), and deep learning for real-time in-situ hardware learning. The innovative hardware was implemented on various low-power platforms to significantly accelerate the deployment of emerging Internet-of-Things (IoT) technology. We are presently designing ultra-low-power (ULP) brain-like learning chips with a view to enabling energy- constraint systems to sense, process, organize, and utilize the data more intelligently.

III. Revolutionary Computing using Disruptive Technologies

3. Quantum Tunneling Technology

In 1992, I started collaborating with my colleague, Prof. George Haddad on a new quantum device, resonant-tunneling diode (RTD) that was originally invented by Dr. Leon Esaki of IBM for which he received Nobel Prize in Physics. The invention of RTD spurred worldwide research for the next- generation digital circuits using quantum-tunneling devices. George's group at Michigan was at that time working on RF circuits using RTDs, but they wanted to develop innovative digital circuits like Dr. Federico Capasso of AT&T Bell Labs, Dr. Gary Frazier of Raytheon, Dr. Gerry Solner of MIT Lincoln Lab, and several Japanese companies like NTT, NEC and Fujitsu. One of the stumbling blocks in the design of digital circuits was that commercial SPICE simulators could not simulate quantum tunneling devices and circuits. Because I had studied quantum physics during my BSc Physics Honors, I started working with Dr. J. P. Sun, who was a postdoctoral fellow in George Haddad's group, to develop the SPICE compatible component models for several types of quantum devices, and then my research group made in-depth study of DC and transient analysis mechanisms in Berkeley SPICE simulator. We designed new convergence algorithms and developed Quantum SPICE simulator that attracted several US and Japanese companies to collaborate with my research group in order to accurately simulate their circuits. Our research group received DARPA Research Award for our inventive work on RTD circuits and quantum circuit simulator. Prof. Richard Newton, Dean of Engineering of University of California at Berkeley and a co-inventor of SPICE commented in Oct. 1996: "*I have studied his simulation work for quantum devices (e.g., his extensions to the SPICE program) and found it insightful, solid and practical, a necessary step to extend the research in this area*".

In 1996, DARPA initiated a move to introduce quantum tunneling in commercial VLSI by combining Silicon-based RTDs with CMOS transistors. My research group developed several patented Quantum MOS circuits

by working in a consortium of US universities and semiconductor companies. QMOS was our "first" response to the call for discovering Beyond Moore's Law (BML) disruptive technologies that would push the frontier of commercial VLSI industry. At the end, Texas Instruments evaluated the commercial feasibility of QMOS VLSI chips and decided not to introduce QMOS in their production line because of yield and other constraints. Though DARPA ended its premiere Ultra research program in 1999, NSF continued to provide me with research grants to develop QMOS circuit and simulation technology and it may bounce back as commercial CMOS transistors become 3-D. Dr. Alan Seabaugh of Raytheon TI Systems who led the QMOS consortium observed in 1997: "*Dr. Mazumder is unquestionably one of the principal leaders in the design of resonant tunneling circuits, and also unquestionably has simulated the largest systems based on these devices. His designs of RTD/transistor circuits have provided some of the first looks at this technology.*" Dr. Masafumi Yamamoto of NTT Research Laboratories in Japan concurred: "*Dr. Mazumder is regarded as being a leading professional in the field of quantum functional circuit design*."

Subsequently, I undertook more challenging revolutionary computing through fusion of sensing and processing by using self-assembled quantum dots and nanowires. Besides innovations for nanoarchitectures for sensing and in situ data processing, our major contributions entailed solving the Schrodinger equation in three-dimensionally constrained nano-structures and developing suitable transport models for tunneling currents through these structures. But for Hitachi Cambridge Research group in UK, none others had developed such transport models for quantum dots in electronic applications. I also received collaborative grants along with UCLA and Virginia Commonwealth University to fabricate nanocircuits consisting of quantum dots. Further, my research group had collaborated with Prof. Leon Chua of UC-Berkeley who invented CNN in 1987 and developed several cellular neural networks (CNNs) using quantum dots and quantum tunneling diodes.

4. Terahertz Systems Research – Discoveries and Foundations

The terahertz spectral region, despite significant efforts, is still grossly underdeveloped and underexploited with the main obstacle being an efficient control of the flow of terahertz electromagnetic signals. AFOSR provided me with multi-year funding for developing VLSI applications of plasmonics and invited me to collaborate with Caltech, Stanford and Harvard researchers who received two MURI contracts for developing materials and process technologies for plasmonics devices. We utilized our Quantum SPICE experience to develop for the first time the SPICE-compatible circuit models for plasmonic structures such as nanoparticles and nanowires by developing innovative electrodynamic models. The original intent of this research was to develop an alternative interconnect technology for VLSI chips. However, the signal attenuation in "light on wire" (plasmonics at optical frequencies) interconnect was prohibitively high which led my research group to develop spoof surface plasmon polariton (SSPP) modes that allow terahertz signal to propagate without much attenuation. Terahertz spoof plasmons not only provide solutions to traditional problems such as efficient delivery and control of radiation, but also open new vistas that are unavailable in microwave and too challenging in optical spectral regions. Our work entails three key ingredients of emerging classes of THz applications enabled by SSPP: i) efficient delivery of the THz radiation, ii) precise control over the phase of the THz electromagnetic field, and iii) giant enhancement of the field-matter interaction. My research group has invented several terahertz components such as Boolean switches, interferometer, analog-to-digital converter, and beam-splitter for which we were granted five US patents.

IV. Other Significant Research in CMOS VLSI

Over the course of the last 24 years, my research group has developed many other cross-cutting and synergistic problem solving methodologies for VLSI systems which have been cataloged into 6 different topical areas at my website. Notably, fusion of electromagnetic (EM) theory, VLSI circuit theory, and numerical analysis has led to thermal modeling and failure analysis of electro magnetic radiation effect on integrated circuits. Rigorous VLSI optimization techniques have been developed to maximize the circuit speed, noise, and energy performance metrics. My research group has also designed several types of innovative VLSI chips around new applications such as polymorphic architectures for unified VLSI routing, neuromorphic chips for self-repair of VLSI arrays, ultra-low-power wireless sensing network (WSN) processor for wearable electronics, and many others as displayed at my website.