PINAKI MAZUMDER[1]

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I. Visa Status

U.S. Citizen (from 1995); Permanent Resident (1989-1995).

II. Educational Qualification

Ph.D. in Computer Engineering	University of Illinois, Urbana-Champaign	1988
M. Sc. in Computer Science	University of Alberta, Edmonton, Canada	1985
B.S. in Electrical Engineering	Indian Institute of Science, Bangalore, India	1976

I also received a degree in B.Sc. Physics Honors securing first rank in the Gauhati University, India amongst estimated 100,000 students in all disciplines of liberal arts and basic sciences.

III. Work Experience

US Government (National Science Foundation):

2007-2008	Program Director for Emerging Models and Technologies Program (funding areas: Nanoelectronics, Quantum Computing, and Biologically Inspired Computing with an annual budget of $18 Million) in the Directorate for Computer and Information and Science and Engineering, National Science Foundation, Arlington, Virginia.
2009	Program Director in Electrical, Communications and Cyber Systems Division (funding areas: Quantum, Molecular and High Performance Computing, Adaptive Intelligent Systems, Electronic and Photonic Devices, and Major Research Instrumentation) of the Engineering Directorate, National Science Foundation, Arlington, Virginia.

Academic Teaching and Research:

1998- to date	Tenured Professor, Division of Computer Science and Engineering, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, Michigan.
1996-1997	Research Fellow, Division of Electrical and Computer Engineering, Department of Electrical Engineering and Computer Science, University of California, Berkeley, California.
1996-1997	Visiting Associate Professor, Department of Computer Science and Engineering, Stanford University, Palo Alto, California.
1997 (Summer)	Visiting Professor, NTT Research Laboratories, Atsugi-shi, Japan.

[1] Fellow of AAAS, Fellow of IEEE, Member of Sigma Xi, and Member of Phi Kappa Phi

1992-1998	Tenured Associate Professor, Division of Computer Science and Engineering, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, Michigan.
1987-1992	Assistant Professor, Division of Computer Science and Engineering, Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, Michigan.
1985-1987	Graduate Student Research Assistant, University of Illinois at Urbana-Champaign, Illinois.
1982-1984	Teaching Assistant at University of Alberta, Edmonton, Canada.
1974-1975	Undergraduate Research Assistant at Indian Institute of Science, Bangalore, India.

Industrial Research and Development:

1985, 1986 (Summer)	Member of Technical Staff, AT&T Bell Laboratories, Indian Hill, Chicago, Illinois.
1976-1982	Senior R&D Engineer, Bharat Electronics Ltd., Bangalore, India.

IV. Research Interest

Nanoelectronics and Plasmonics, Disruptive Nanoarchitectures, Modeling and Simulation Tools for Nanoelectronic Devices and Circuits; Nanoscale CMOS VLSI System Design Issues: Modeling of Thermal Dissipation, Electromagnetic Effects, Leakage Currents, Interconnect Delays, and Chip Noises; Mixed Signal System Design; Testing and Self-Repair Methodology; and VLSI Layout Automation Algorithms.

V. Awards

- Fellow of American Association for the Advancement in Science (AAAS), 2007 for "distinguished contributions to the field of very large scale integrated (VLSI) systems". The honor of being elected a Fellow of AAAS is given to those whose "efforts on behalf of the advancement of science or its applications are scientifically or socially distinguished."
- Fellow of IEEE, 1999 for "contributions to the field of VLSI Design."
- IEEE Distinguished Lecturer
- Digital Equipment Corporation Faculty Award: Excellence in Research
- Departmental Research Excellence Award (1995), The University of Michigan
- BF Goodrich National Collegiate Invention Award
- DARPA Research Excellence Award for the work in Quantum MOS Project
- Best Undergraduate Student Medal
- IETE Best Student Paper Award, and IETE Best Paper Presentation Award
- NSF Research Initiation Award
- Bell Northern Research Laboratory Faculty Development Grant
- Commendation Letter from the Dean of College of Engineering, University of Michigan, for Excellence in Teaching
- Member, Sigma Xi
- Member, Phi Kappa Phi
- US Patent on Digital Logic Design Using Negative Differential Resistance Diodes and Field-Effect Transistors, US Patent No. 5903170, awarded on May 11, 1999.
- US Patent on High-speed, Compact, Edge-Triggered Flip-Flop Circuit Topologies Using NDR Diodes and FET's, US Patent No. 6,323,709, awarded on Nov. 21, 2001.
- US and International Patents on Method and Apparatus to Improve Noise Tolerance of Dynamic Circuits, US Patent No. 7,088,143, awarded on Aug. 8, 2006.

VI. Research Funding

1. National Science Foundation (RIA): $69,948; 1988 – 1991 (Single PI)
2. Bell Northern Research Laboratory: $20,900; 1988 – 1989 (Single PI)
3. National Science Foundation: $90,620; 1989 – 1990 (Single PI)
4. Digital Equipment Corporation: $180,000; 1989 – 1992 (Single PI)
5. Office of Naval Research: $420,000; 1988 - 1991, (Co-PI)
6. National Science Foundation: $125,000; 1991 – 1993 (Single PI)
7. Rackham Faculty Research Grant: $9,980; 1991 – 1993 (Single PI)
8. U.R.I. Program (US Army): $6,000,000 (total); $250,000 (my portion); 1988 - 1992
9. General Motors: $20,000; 1992 – 1992 (Single PI)
10. International Business Machines: $45,000 (student fellowship); 1990 – 1993
11. National Science Foundation: $47,000; 1992 – 1993 (Single PI)
12. Hewlett Packard: $81,400; 1993 – 1995 (Single PI)
13. Office of Vice President Research: $52,300; 1995 - 1996
14. Defense Advanced Research Projects Agency (DARPA): $825,000; 1993 -1997 (Co-PI)
15. National Science Foundation: $182,400; 1994 – 1998 (Single PI)
16. U.R.I. Program (US Army): $5,000,000; $200,000; 1993 - 1997
17. State of Michigan Display Technology Center: $2,000,000; My portion: $200,000; 1995 - 1998
18. Texas Instruments (subcontract of a DARPA project): $304,000; 1995 – 1998 (Single PI)
19. Army Research Office's MURI-95 (Co-PI with 7 others): $4,000,000; 1995-2000 + 1 year.
20. Army Research Office's MURI-96 (Co-PI with 13 others): $5,000,000; 1996-2001 + 1 year.
21. Defense Advanced Research Projects Agency: $750,000; June 1997- May 2000 (PI)
22. National Science Foundation: $300,000; 1998 – 2002 (Single PI)
23. Nippon Electric Company, Japan: $40,000; 1998 (Single PI)
24. National Science Foundation: $195,000; 1998 – 2002 (Single PI)
25. Hughes Research Laboratory (Office of Naval Research project); $270,000; 1998-2001 (Single PI)
26. NanoLogic Inc. $10,000; 1999-2000 (Single PI)
27. Air Force Office of Scientific Research: $5,000,000: 2001-2006 (Co-PI with 9 other investigators)
28. Naval Research Laboratory: $303,000: 2001-2002; (Single PI)
29. National Science Foundation: $210,000: 2001-2004 (Single PI)
30. Korean Government Nanoelectronics Research: $200,000: 2001-2002 (PI: Prof. G.I. Haddad).
31. Naval Research Laboratory: $820,000: 2002-2005 (PI)
32. Tera-Level Nanoelectronics Project, Korean Government: $170,000: 2003-2006; (Single PI)
33. National Science Foundation: $120,000: 2004-2007 (Single PI)
34. Air Force Office of Scientific Research, $480,000: 2006-2009 (Single PI)
35. National Science Foundation IPA Assignment Grant: $620,000; 2007-2009 (Single PI)
36. DARPA SyNAPSE Program on Brain Plasticity: $807,812; Co-PI: Hughes Research Laboratory
37. National Science Foundation, NIRT: **$1,000,000**: 2006-2012 (Co-PI).
38. SRC NRI Center (MIND): **~$200,000**: 2008-2011 (Single PI)
39. National Science Foundation: EAGER Grant, **$200,000**; 2009-2012. (Single PI)
40. National Science Foundation**: $400,281**; 2010-2013. (Single PI)
41. Army Research Office: **$580,000**; 2010-2013. (Single PI)
42. National Science Foundation: **$149,111**; 2011-2012. (Single PI)
43. Army Research Office, MURI: **$6,500,000**; 2010-2015. (Co-PI)
44. National Science Foundation: **$400,415**; 2011-2014. (Single PI)
45. National Science Foundation**: $1,750,000**; 2011-2015. (Co-PI)
46. Defense Advanced Research Projects Agency (DARPA): **$150,000;** 2011-2013 (Single PI)

In the above list, the <u>Active</u> research grants are indicated in Bold (#37-#46).

Summary of Research Grants:

Individual portion of **active** grants = **$2,808,807 + $300,000** (gift grants).
Total individual portion of all grants awarded till to date = **$9,560,355** without the IPA grant
Total individual portion of all grants awarded = **$10, 180,355** with NSF IPA grant
Total of all active grants including portions of all collaborators = **$11,329,807**
Total of all grants awarded so far including portions of all collaborators > **$40,000,000**

Pending Proposals:

1. Expedition: Foundation for Integrative Research Storage Technologies, $10,000,000 (PI)
2. Plasmonic Interconnect Design, Simulation, and Fabrication for VLSI Applications, National Science Foundation, $480,000. (PI)
3. NEB: Hybrid Spintronics and Straintronics: A New Technology for Ultra Low Energy Computing and Signal Processing Beyond the Year 2020. (Co-PI).
4. MURI: All-plasmonic THz components for quantum communication (QC) and quantum imaging (QI) in the THz regime, Air Force Scientific Research Office, $4,600,000 (PI)
5. Ultra-Low Energy Nanoscale Architecture for Algorithmic Pattern Recognition, Video Data and Image Processing, Army Research Office, $550,000 (PI)
6. STDP CMOS and Memristor-Based Neurodynamic Programming Design for Sensorimotor Neuromorphic Systems, National Science Foundation, $3,000,000. (PI)

VII. Consulting Activities

1. Served as ***Expert*** for the US National Science Foundation, Arlington, Virginia.
2. Served as a member of ***Technical Advisory Board*** for. Sequence Design Automation (Santa Clara, CA), Silicon Value Inc. (Jerusalem, Israel), and Tioga Technology (San Jose, CA).
3. Served as ***Advisor and Expert Witness*** in 5 lawsuits involving DRAM, Flash, and FPGA.
4. Served as ***Consultant*** for many semiconductor companies in the areas of testable and self-repairable designs of embedded cache memories, soft-error problems in FPGA's, circuit design for spread-spectrum communications, AMLCD display hardware, nanoelectronic circuits and simulation tools.

VIII. Committees and Professional Activities

1. Member of Board of Editors, *Proceedings of the IEEE*
2. Associate Editor, *IEEE Transactions on VLSI Systems*, 1997-2000
3. Guest Editor, *IEEE Transactions on VLSI Systems* - A Special Issue on Impact of Emerging Technologies on VLSI Systems, December 1997
4. Guest Editor (with Prof. A. Seabaugh), *Proceedings of the IEEE* - A Special Issue on Nanoelectronic Devices and Circuits, June 1998
5. Guest Editor (with Prof. A. Benso and Prof. Y. Makris), *IEEE Transaction on Computer* – A Special Issue on Chips and Architectures for Emerging Technologies and Applications, June 2008
6. Guest Editor, *Journal of Electronic Testing - Theory and Application* - A Special Issue on Multi-megabit Memory Testing, April 1994
7. Guest Editor (with Prof. J.P. Hayes), *IEEE Design & Test Magazine* - A Special Issue on Memory Testing, 1993
8. Editorial Advisory Board, *The Arabian Journal for Science and Engineering*, King Fahd University of Petroleum and Minerals, Saudi Arabia.

9. Council of Editors, *International Society for Genetic and Evolutionary Computation* (ISGEC)
10. As lead NSF Program Director, organized the Emerging Models and Technology Workshop on Bio-Inspired Computing and Bio-Computing at Princeton University on July 24-25, 2008.
11. As lead NSF Program Director, organized the EMT Workshop on Nanoelectronics on October 29-30, 2007.
12. As lead NSF Program Director, held the EMT Workshop on Quantum Information Science and Engineering on September 10-11, 2007.
13. Member, University of Michigan Research Policies Committee of Senate Assembly, 2002-05.
14. Member, Electrical Engineering and Computer Science Curriculum Committee, 2002-03.
15. Member, Electrical Engineering and Computer Science DCO Committee, 2002-03.
16. Member, Computer Science and Engineering Graduate Curriculum Committee, 1988-89, 1998-00, 2002-06.
17. Counselor, Computer Engineering Undergraduate Students, 1990-95.
18. Member, Computer Science and Engineering Graduate Admission Committee, 1995-96.
19. Member, IEEE Standards Subcommittee for Semiconductor Memories, 1989-90.
20. Member, IEEE Test Technologies Committee
21. Member, IEEE VLSI Technical Committee
22. General Chair, 2007 High Performance Computing (HPC) for Nanotechnology
23. General Chair, 1999 IEEE Great Lakes VLSI Conference
24. Program Committee, 1992 Fault-Tolerant Computing Symposium Workshop
25. Program Committee, 1992 IEEE Defects and Fault Tolerance Workshop
26. Program Committee, 1993 IEEE Intl. Conference on Memory Testing
27. Program Committee, 1994 IEEE Intl. Conference on Memory Testing
28. Program Committee, 1994 IEEE Asian Testing Symposium
29. Program Committee, 2000 IEEE Great Lakes VLSI Conference
30. Serving on organizing committee for Department of Defense Nano Conference, 2009
31. Served regularly on NSF panels in Engineering and CISE Directorates
32. Proposals Reviewed for: US National Science Foundation, The Israel Science Foundation, Louisiana University Board of Regents, and US Army Research Office, New Jersey Center for Science and Technology, Saudi Arabia King Fahd University Research Foundation, and private venture capitalist firms.

IX. Professional Experience

Summary of My Professional Accomplishments

My 27-year accumulative accomplishments in academia, industrial R&D laboratories, and US Government funding agency are briefly enumerated below.

My contributions to semiconductor memories have profoundly impacted the DRAM industry. I invented the "line-mode plurality testing" scheme for high-density dynamic random-access memory (DRAM) chips that is now widely adopted in Giga-bit DRAM chips by major semiconductor memory manufacturers around the world enabling them to significantly reduce memory chip testing time and cut the price of memories. I proposed layout and process based parallel test algorithms to improve reliability of DRAM chips. I also studied the mechanism of double-bit errors due to alpha particles striking between trench DRAM cells, and proposed a new on-chip double-bit error correcting circuit to improve memory storage reliability. My research group developed a unified approach to built-in self-repair of VLSI chips by proposing adaptive self-healing circuits that can perform combinatorial optimization algorithms such as maximum matching and node covering on bipartite graphs in order to substitute the faulty circuit elements by spare elements in memory and processor arrays. I have co-

authored two definitive books on semiconductor memories covering various aspects of design for testability, self-testing, self-repair, parallel test algorithms, radiation induced errors, error correction techniques, yield modeling, self-repairable memory compilers, and so on. These books are widely used by practicing memory designers to design and test nano-scale memory products.

In the late 1980s, prior to the current upsurge in nanotechnology, my research group broke ranks with traditional VLSI system designers and explored the unchartered territory of quantum tunneling digital system design and computer-aided design (CAD) tools for emerging meso-scale systems. My research group steered the way to the development of Quantum SPICE simulator that incorporated physics-based closed form analytical models of a number of quantum-effect devices and mathematically robust homotopy based convergence routines which were introduced to circumvent DC and transient convergence problems arising from the non-monotonic device characteristics of the quantum-effect devices. This allowed us to demonstrate numerous innovative applications of quantum tunneling-based circuits in digital architectures such as nanopipelined signal processing and communication systems, as well as in analog cellular non-linear/neural networks such as static and dynamic image processing. The Quantum SPICE simulator that my research group developed played a key role in designing numerous large-scale quantum tunneling integrated circuits which were fabricated and tested by Raytheon, HRL Laboratories, Martin Marietta, NEC (Japan), and KAIST (Korea).

Subsequently, my research group extended our work to three- and two-dimensionally confined nanoscale devices such as quantum dots and nanowires. Using an envelope-function-based model, we spearheaded the development of nano-architectures for full-range color image processing, video motion detection, and spatio-temporal filtering. Our recent research on analytical modeling of plasmonic nanowire, chain of metallic nanoparticles, and long-range spoof plasmon propagation on corrugated metallic surface have built the groundwork for simulating these devices using conventional electronic circuit simulator (SPICE) as well as the possibility of designing Tera Hertz (THz) plasmonic systems which will allow nanoscale electronic devices to interface with microscale optical components in a VLSI chip.

In the realm of nanoscale CMOS systems, we synthesized disparate areas of research, namely electromagnetic theory, numerical analysis and quantum physics in order to solve several mathematically challenging VLSI system design problems, to wit: a) Schrodinger and Poisson solver to model leakage currents in gate dielectrics of nanoscale CMOS devices, b) optimal tapering of FET chains in high-speed CMOS circuits, c) foundational work on Finite Differential Quadrature Method (FDQM) to quantify the interaction of electromagnetic noise and signal waveforms, and d) mathematical models for a fast multi-layer Green's function solver to perform thermal analysis during the physical placement of cells to avoid thermal hot spots.

I served as the lead Program Director of the Emerging Models and Technologies Program at the National Science Foundation where I designed innovative research programs that transcend the boundaries of computing and biological systems, quantum information science, and nanoscale engineering. I was also in charge of development of innovative curricula and courseware that will help train future generations of engineers and scientists in emerging models and technologies for computation. At the University of Michigan, I have taught new graduate courses in Nanoarchitectures, VLSI design, and VLSI layout synthesis in order to train and motivate graduate students to embark upon their research in emerging fields in the Pasteur quadrant where application-inspired basic research makes significant economic and societal impacts. My service to professional societies comprise editing journals, chairing conferences, organizing workshops to identify grand challenges and develop new funding opportunities, visiting numerous universities and VLSI companies to deliver

over 80 invited technical talks, establishing international research collaboration in emerging technologies, and serving on various types of policy-making panels.

Details of My Professional Accomplishments

US Government at National Science Foundation **(3 years)**

In 2007 and 2008, I worked as the lead Program Director for Emerging Models and Technologies (EMT) program in the Division of Computing and Communication Foundations (having about $140 Million annual budget) of the Directorate for Computer and Information and Science and Engineering, National Science Foundation, Arlington, Virginia. I managed research in the areas of Nanoelectronics, Quantum Computing, and Biologically Inspired Computing for which I had an annual budget of about $18 Million. In 2009, I worked as the Program Director in the Engineering Directorate where I managed research in three areas: for Adaptive Intelligent Systems, Quantum and Molecular Modeling, and Electronic and Photonic Devices and Technology. During these three years, I became broadly familiar with various research and education programs in NSF as well as in DOE and DOD (DARPA, ARO, ONR, and AFOSR).

Teaching Experience **(22 years)**

Currently I am working as a Professor at the Department of Electrical Engineering and Computer Science of the University of Michigan, Ann Arbor, Michigan.

Graduate courses developed and taught: 1) Optimization and Synthesis of VLSI Layout, 2) Testing of Digital Circuits and Systems, 3) Advanced Computer Architectures, and 4) Nanocircuits and Nanoarchitectures.

Undergraduate courses upgraded and taught: 1) Introduction to Digital Logic Design (sophomore level), 2) Digital Integrated Circuit Design (junior level), 3) VLSI System Design (senior level), and 4) Nanocircuits and Nanoarchitectures (adapted from the above graduate course for senior students).

In addition to teaching the afore-said courses, I have been developing courseware to establish the following two advanced courses for senior undergraduate and graduate students: 1) Biologically Inspired Computing Models and Technologies, and 2) Low-Power Mixed Signal Circuit Design (with an emphasis on consumer electronics design).

Industrial Experience **(6.5 years)**

After my baccalaureate degrees in Physics and Electrical Engineering, I worked for six years (1976-1982) as a Senior R&D Engineer at Bharat Electronics Ltd. (BEL) in its Integrated Circuits Division. I designed several bipolar and CMOS analog and digital integrated circuits and developed consumer electronic systems around these integrated chips. I was associated with the following chip development projects: i) Raster-scan vertical deflection system microchip for TV display, ii) Sync processing and horizontal deflection system microchip for TV display, iii) Video and audio IF stage IC's for vestigial-AM and FM signal detection in TV receiver, iv) High-gain audio amplifier microchip for TV audio stage, v) Tape Recorder IC with automatic gain adjustments, vi) Hearing-aid IC, vii) Analog clock driver IC, and viii) LCD and AC Plasma display drive IC's. Several million commercial chips were fabricated based on these designs.

After finishing my Masters degree in Computer Science and while working towards my doctoral degree in Electrical and Computer Engineering, I worked during the summers of 1985 and 1986 as a Member of Technical Staff at AT&T Bell Laboratories. I was one of the two engineers who started Bell Lab's

Cones/Spruce project - a new behavioral synthesis and layout automation tool for rapid prototyping of digital circuits. The main contribution of this effort was to demonstrate how a restricted version of C language could be used to model digital hardware much before Verilog and System C hardware description language (HDL) software tools were developed.

Student Theses Supervised

Ph.D. Theses Completed

1. J. Yih, ”Built-In Self-Repair of Embedded Memory and Logic Arrays,” 1990. Currently at IBM T. J. Watson Research Center, Yorktown, New York.

2. K. Shahookar, ”Genetic Algorithms for CAD Layout Problems,” 1994. Currently at his start-up company.

3. H. Esbensen, ”Application of Genetic Algorithms for Cell Placement and Routing Problems,” 1994. Currently at Avant! Fremont, California.

4. V. Ramachandran, ”Parallel Architectures for Multilayer Wire Routing Problems,” 1994. Currently at Cadence Design Systems, San Jose, California.

5. S. Mohan, ”Design of Ultra-fast Digital Circuits using Quantum Electronic Devices,” Dec. 1994. Currently at Xilinx Corporation, Campbell, California.

6. K. Chakraborty, ”Built-In Self-Repairable RAM Compiler Design,” Mar. 1997. Currently at Agere Design, Murray Hills, New Jersey.

7. M. Bhattacharya, ”Simulation and Emulation of Digital Integrated Circuits Containing Resonant Tunneling Diodes,” Oct 1999. Currently at Avant! Fremont, California.

8. S. Kulkarni, ”Quantum MOS Circuits and Systems,” Oct 1999. Working in IDT, Atlanta, Georgia.

9. A. Gonzalez, ”Multiple-Valued Logic and High-Speed Digital Circuits Using Resonant Tunneling Diodes,” June 2001. Currently at IDT, Atlanta, Georgia.

10. Li Ding, “ Dynamic Noise Analysis in Deep Sub-micron CMOS VLSI Systems,” Feb. 2004. Currently at Synopsis, Sunnyvale, California.

11. Q. W. Xu, “Accurate Interconnect Modeling for Efficient Transient Simulation in VLSI Chip Design,” May 2006, currently at Cadence Design Systems.

12. B. Wang, “Accelerated Chip-level Thermal Analysis Using Multilayer Green's Function," May 2008, currently at VmWare.

13. W. H. Lee, “Applications of Nanoelectronic Technology to Image Processors, Velocity-Tuned Filters and Crossbar Memories”, Dec 2008, currently at Intel.

14. K. Song, “Applications of Surface Plasmon Polariton Plasmonic Devices,” Aug. 2010, currently working as a Research Scientist, University of Michigan.

M.S. Theses/Projects Completed:

1. B. Brighton, Pseudo-Random Testing for Embedded Memories
2. K. Quasim, Analog Circuit Testing
3. J. Kapson, Parallel CAD Architecture
4. D. Berryman, Parallel Processing for VLSI Routing
5. M. Smith, Self-Repairable Memory Array Using Digital Neural Circuit
6. E. Chan, RTD-based Multi-valued Circuit Design
7. A. Arunachalam, Fine-Grained Parallel Routing
8. A. Gonzalez, Multi-valued Adder Design Using CMOS and RTD
9. A. Gupta, Self-Repairable ROM Generator
10. J. Xiong, Quantum MOS Circuit Design
11. G. Mittal, Simultaneous Switching Noise Analysis in Embedded Memories
12. V. Warraich, Web-based Applets Design for Digital Logic
13. M. Kumshikar, Amorphous TFT-based Driver Logic Design for AMLCD Panel
14. G. Shankar, Amorphous TFT-based Operational Amplifier Design for AMLCD Panel
15. V. Ramachandran, Array Machine for VLSI Routing
16. S. Mohan, Parametric Testing for SRAM's Using GaAs High Electron Mobility Transistors
17. S. Kulkarni, CMOS and RTD-based Correlators Design
18. K. Shahookar, Genetic Algorithm for VLSI Placement
19. H. Chan, Macro-cell Placement Using Genetic Algorithm
20. L. Ding, Noises in Deep Sub-micron VLSI Chips
21. Q. W. Xu, VLSI Interconnect Modeling Using Differential Quadrature Method
22. B. Wang, 3-Dimensional Full Chip Simulation by Transmission Line Matrix Method
23. H. Zhang, Ultra-fast RTD-based Circuit Design
24. S.R. Li, RTD-based Cellular Nonlinear Networks
25. D. Shi, Quantum Dot Based Image Processing
26. M. Rajagopal, Modeling of Resonant tunneling Diodes
27. W. Lee, Image Processing Applications of Quantum Dots
28. E. Ibong, Subthreshold Low-power Operational Amplifier Design
29. K. Song, Plasmonics Applications in VLSI
30. C. Ting, Modeling of Ionic Current through Memristors

Number of Doctoral Students Currently Being Supervised: 6.
Visitors:

1. Dr. Ueymura, NEC, Japan;
2. Prof. Choi, Hanyang University, South Korea;
3. Mr. T. Glotzner, Germany;
4. Mr. H. Esbensen, Aarhus University, Denmark.;
5. Dr. Q. W. Xu, China;
6. Mr. P. Kelly, Ulster University, UK;
7. J. P. Sun, China
8. S. Duan, China

XII. Publications

Books and Book Chapters

Books

1. P. Mazumder and K. Chakraborty, "Testing and Testable Design of Random-Access Memories", ***Kluwer Academic Publishers***, 1996 (428 pages).

2. P. Mazumder and E. Rudnick, "Genetic Algorithms for VLSI Layout and Test Automation", ***Prentice Hall***, 1999 (460 pages).

3. K. Chakraborty and P. Mazumder, "Fault Tolerance and Reliability Aspects of Random-Access Memories," ***Prentice Hall***, 2002. (440 pages)

4. P. Mazumder, "Introduction to Digital Systems", Video Book on DVD, produced at MGM Studio (Orlando, Florida), ***Laureate Education, Inc.,*** 2005.

5. P. Mazumder, "Models and Techniques for VLSI Routing", ***Springer Verlag***, (under preparation)

6. R. Rajasuman (Editor) and P. Mazumder (Editor), "Semiconductor Memories: Testing and Reliability", ***Computer Science Press***, May 1998.

7. R. J. Lomax (Editor) and P. Mazumder (Editor), "Great Lakes Symposium on VLSI, 1999", ***Computer Science Press***, March 1999.

8. P. Mazumder and K. Shahookar, "MathGuru Tutorial" for K-12 Education Software.

Book Chapters

9. K. Shahookar and P. Mazumder, "Standard Cell Placement and the Genetic Algorithm", Book chapter in "Advances in Computer-Aided Engineering Design, Vol. II", I. N. Hajj (editor), ***Jai Press***, Greenwich, Connecticut, 1990, pp. 159-234.

10. W. K. Fuchs, M. F. Chang, S. Y. Kuo, P. Mazumder and C. B. Stunkel, "The Impact of Parallel Architecture Granularity on Yield", Book chapter in "Designing for Yield," Moore, Strowjas and Maly (editors), ***Adam Hilger Publisher***, 1988.

11. P. Mazumder and J. H. Patel, "Parallel Testing of Parametric Faults in DRAM", in "Advanced Research in VLSI: Design and Applications of Very Large Scale Systems", Leighton and Allen (editors**), *MIT Press***, 1988. (Presented at the 5-th Massachusetts Institute of Technology Conference on VLSI).

12. P. Mazumder, "Design of a Fault-Tolerant DRAM with New On-Chip ECC", Book Chapter in "Defects and Fault Tolerance in VLSI Systems", I. Koren (editor), ***Plenum Press***, 1989.

13. H. Chan and P. Mazumder, "A Systolic Architecture for High-Speed Hyper-graph Partitioning Using a Genetic Algorithm", Book Chapter in "Progress in Evolutionary Computation", Vol. 956**, *Springer-Verlag***, Heildelberg, 1995, pp. 109-126.

Reviewed Journal Publications

14. P. Mazumder, J. H. Patel and W. K. Fuchs, "Methodologies for Testing Embedded Content-Addressable Memories", ***IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems***, Jan. 1988, pp. 11-20.

15. P. Mazumder, "Parallel Testing of Parametric Faults in a Three-Dimensional Dynamic Random-Access Memory", ***IEEE Journal of Solid-State Circuits***, Vol. 23, No. 4, Aug. 1988, pp. 933-942.

16. P. Mazumder and J. H. Patel, "Parallel Testing of Pattern-Sensitive Faults in Random-Access Memory", ***IEEE Transactions on Computers,*** Vol. 38, No 3, Mar. 1989, pp. 394-404.

17. P. Mazumder and J. H. Patel, "An Efficient Built-In Self-Testing Algorithm for Random-Access Memory", ***IEEE Transactions on Industrial Electronics*** (Special Issue on Testing) Vol. 36, No. 3, May 1989, pp. 394-407.

18. J. S. Yih and P. Mazumder, "Circuit Behavior Modeling and Compact Testing Performance Evaluation", ***IEEE Journal of Solid-State Circuits***, Vol. 26, No. 1, Jan. 1991, pp. 62-65.

19. P. Mazumder and J. H. Patel, "A Comprehensive Study of Random Testing for Embedded RAM's Using Markov Chains", ***Journal of Electronic Testing: Theory and Applications***, Vol. 3 No. 4, Nov. 1992, 235-250.

20. S. Mohan and P. Mazumder, "Analytical and Simulation Studies of Failure Modes in SRAM's Using High-Electron Mobility Transistors", ***IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems***, Vol. 12, No. 12, Dec. 1993, pp. 1885-1896.

21. P. Mazumder and J. P. Hayes, "Testing and Improving the Testability of Multi-megabit Memories", ***IEEE Design and Test of Computers***, Mar. 1993, pp. 6-7.

22. K. Chakraborty and P. Mazumder, "Technology and Layout Related Testing in Static Random-Access Memories", ***Journal of Electronic Testing: Theory and Applications***, Aug. 1994.

23. P. Mazumder, J. H. Patel and J. A. Abraham, "A Reconfigurable Parallel Signature Analyzer for Concurrent Error Correction in Dynamic Random-Access Memory", ***IEEE Journal of Solid-State Circuits***, Vol. 25, No. 3, Jun. 1990, pp. 866-870.

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Publications in Industry (during 1976-1982)

Mixed Signal Analog and Digital VLSI Chip Design

Published over ***fifteen*** technical papers and application ideas while working at the Bharat Electronics Ltd. Topics included

- An Integrated Circuit Design for the Raster-Scan Vertical Deflection System.
- An Integrated Circuit Design for the Sync Processing Circuit
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All these articles were published in ***BEL Application Notes*** and ***BEL Technical Report***.

XIII. Book Reviews

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2. J. Beetam, "Computer Architectures", ***Aksen Associates Inc. Publishers,*** California.
3. "The Science and Technology of Microelectronic Processing", ***Saunders College Publishing***, Pennsylvania.
4. D. Pradhan, "Fault-Tolerant System Design", ***Prentice Hall***, New Jersey.
5. Price, "Introduction to VLSI Design", ***Prentice Hall,*** New Jersey.
6. C.P. Ravi Kumar, "Computer-Aided Design for VLSI Systems", ***Kluwer Academic Publishers,*** Massachusetts.
7. Fu, "Neural Networks in Computer Intelligence", ***Prentice Hall,*** New Jersey.
8. P. Banerjee, "Parallel Algorithms for VLSI Computer-Aided Design Applications", ***Prentice Hall,*** New Jersey.
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10. A. S. Sedra and K. C. Smith, "SPICE Simulation: Microelectronics Circuits", ***Prentice Hall.***
11. A. B. Marcovitz, "Introduction to Logic Design," ***McGraw Hill.***
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XIV. Technical Presentations (excluding conferences and workshops)

At Industries and National Laboratories

Formal Talks

1. Quantum electronic circuit design at ***Intel Corporation***, Santa Clara, California.
2. Quantum electronic circuit design at ***Samsung,*** Korea
3. Quantum electronic circuit design at ***Nippon Telegraph and Telephone***, Atsugi-shi, Japan.
4. Quantum electronic circuit design at ***Silicon Value***, Jerusalem, Israel.
5. Quantum electronic circuit design ***at Fraunhofer Institute***, Freiburg, Germany.
6. Quantum electronic circuit design at ***A-STAR Research Laboratories,*** Singapore
7. Quantum electronic circuit design at ***Hitachi Central Research Laboratories***, Kokubunji, Japan.
8. Quantum electronic circuit design at ***NEC Corporation***, Tsukuba, Ibaraki, Japan.
9. Quantum electronic circuit design at ***Fujitsu***, Morinosato-Wakamiya, Japan.
10. Quantum electronic circuit design at ***Texas Instruments***, Dallas, Texas.
11. Quantum electronic circuit design at ***Hughes Research Laboratories***, Los Angeles, California.
12. Memory testing at ***Nippon Telegraph and Telephone***, Atsugi-shi, Japan.
13. Memory testing at ***Digital Equipment Corporation***, Hudson, Massachusetts
14. Memory testing at ***Fujitsu***, Morinosato-Wakamiya, Japan.
15. Memory testing at ***Intel***, Santa Clara, California
16. Memory testing at ***Hitachi Central Research Laboratories***, Kokubunji, Japan.
17. Memory testing at ***AT&T Bell Laboratories***, Murray Hill, New Jersey.
18. Memory testing at ***Bell Northern Research Laboratories***, Ottawa, Canada
19. Embedded memory compilation at ***Synopsys,*** Palo Alto, California.
20. Embedded memory compilation at ***Neo-Magic Corporation***, Santa Clara, California.
21. Embedded memory compilation at ***Ambit Design Systems***, Santa Clara, California.
22. Memory testing at ***Micron Technology***, Boise, Idaho.
23. Memory testing at ***MCC***, Austin, Texas

24. Memory testing at ***Texas Instruments***, Bangalore, India.
25. Memory testing at ***AT&T Bell Laboratories***, Holmdel, New Jersey.
26. VLSI chip testing at ***ERIM Research Laboratory***, Ann Arbor, Michigan.
27. VLSI layout techniques at ***Nippon Telegraph and Telephone***, Atsugi-shi, Japan.
28. VLSI layout techniques at ***General Motors Research***, Warren, Michigan.
29. VLSI layout techniques at ***Bell Northern Research Laboratories***, Ann Arbor, Michigan.
30. VLSI layout techniques at ***Cypress Semiconductor***, Santa Clara, California
31. VLSI layout techniques at ***National Semiconductor***, Santa Clara, California
32. Built-in self-repairable IC design at ***Nippon Electric Company***, Princeton, New Jersey.
33. Built-in self-repairable IC design at ***Bell Communications Research***, Morris Town, New Jersey.
34. Built-in self-repairable IC design at ***Ford Motors Company***, Dearborn, Michigan.
35. Built-in self-repairable IC design at ***Nippon Telegraph and Telephone***, Atsugi-shi, Japan.
36. Research activities on circuit design at ***IBM Watson Research Center***, New York.
37. Research activities on circuit design at ***Hitachi Development Laboratories***, Mobarra, Japan.
38. Research activities on circuit design at ***David Sarnoff Research Center***, Princeton, New Jersey.
39. Research activities on circuit design at ***NEC Central Research*** Laboratories, Kanagawa, Japan.
40. Quantum electronic circuit design at ***Sun Microsystems,*** Sunnyvale, California
41. Dynamic noise analysis methodology for VLSI design at ***Sun Microsystems***, Mountainview, California
42. Dynamic noise analysis methodology for VLSI design at ***Sequent Design Automation***, San Jose, California
43. Quantum electronic circuit design at ***AMD,*** Sunnyvale, California
44. Memory testing at ***Texas Instruments***, Houston, Texas.
45. Embedded memory testing at ***Logic Vision***, San Jose, California.
46. VLSI layout techniques at ***Avant!,*** Fremont, California.
47. VLSI layout techniques at ***International Business Machine***, Fishkill, New York.
48. Memory testing at ***LSI Logic***, Milpitas, California.
49. VLSI chip layouts at ***Xilinx***, Inc., San Jose, California.
50. Built-in self-repairable design at ***Phillips Laboratories***, Kirtland, New Mexico.
51. Built-in self-repairable design at ***Altera Corporation,*** San Jose, California.

Formal Talks at Universities

52. Multilayer VLSI routing techniques at ***University of California***, Berkeley, California.
53. Memory testing at ***Stanford University***, Palo Alto, California.
54. Beyond CMOS technologies and evolutionary architectures at ***California Institute of Technology***, Pasadena.
55. Beyond CMOS technologies and evolutionary architectures at ***Columbia University***, New York.
56. Quantum electronic circuit design at ***University of Illinois***, Urbana-Champaign, Illinois.
57. Quantum electronic circuit design at ***University of California***, Berkeley, California.
58. Quantum electronic circuit design at ***Seoul National University***, Seoul, Korea.
59. Quantum electronic circuit design at ***Beijing University***, Beijing, China.
60. Quantum electronic circuit design at ***Gerhard-Mercater University***, Duisburg, Germany.
61. Quantum electronic circuit design at ***University of Santiago***, Spain
62. VLSI layout design at ***Princeton University***, Princeton, New Jersey.
63. Memory testing at ***Purdue University***, West Lafayette, Indiana.
64. Memory testing at ***University of Southern California***, Los Angeles, California.
65. Built-in self-repairable IC design at ***University of Iowa***, Iowa City, Iowa.
66. Memory testing at ***King Fahd University***, Saudi Arabia.

67. Quantum electronic circuit design at ***Nanjing University,*** Nanjing, China
68. Memory testing at ***Johns Hopkins University***, Baltimore, Maryland.
69. Quantum electronic circuit design at ***Ohio State University***, Columbus, Ohio
70. Memory testing at ***University of Minnesota***, Minneapolis, Minnesota.
71. Quantum electronic circuit design at ***University of Tokyo***, Tokyo, Japan.
72. Quantum electronic circuit design at ***Delft Technological University***, Delft, Netherlands.
73. Quantum electronic circuit design at ***King Fahd University***, Saudi Arabia.
74. Quantum electronic circuit design at ***Universidad de Las Palmas de Gran Canaries***, Spain.
75. Quantum electronic circuit design at ***South East University,*** Nanjing, China
76. Memory testing and repair algorithms at ***Indian Institute of Technology***, New Delhi, India.
77. Memory testing at ***Texas A&M University***, College Station, Texas.
78. Quantum electronic circuit design at ***Northwestern University***, Evanston, Illinois
79. Built-in self-repairable IC design at ***Wayne State University***, Detroit, Michigan.
80. VLSI layout design at ***Indian Institute of Science***, Bangalore, India.
81. Built-in self-repairable design at ***Association of Computing Machine Symposia***, Ann Arbor, Michigan.
82. Quantum electronic circuit design at ***Indian Statistical Institute,*** Kolkata, India.
83. Quantum electronic circuit design at ***Indian Institute of Technology***, Khragpore, India
84. Beyond Moore's Law CMOS Technology and Revolutionary Architectures, ***Asian Institute of Technology,*** Bangkok
85. IEEE Distinguished Lecture Beyond Moore's Law CMOS Technology and Revolutionary Architectures at ***Indian Institute of Technology***, Chennai, India.
86. IEEE Distinguished Lecture Beyond Moore's Law CMOS Technology and Revolutionary Architectures at ***University of Illinois***, Chicago.
87. IEEE Distinguished Lecture on Beyond Moore's Law CMOS Technology and Revolutionary Architectures ***at Indian Institute of Science,*** Bangalore, India.
88. IEEE Distinguished Lecture Beyond Moore's Law CMOS Technology and Revolutionary Architectures at ***Dhaka University***, Dhaka, Bangladesh.

Formal Visits to University Laboratories

89. VLSI Design and Education Center, ***University of Tokyo***, Tokyo, Japan.
90. Nanoscale Science and Engineering Center, ***Harvard University***, Harvard, Massachusetts
91. Computer Engineering Research Center, ***University of Texas***, Austin, Texas.
92. Nanoelectronics Laboratory, ***University of Texas***, Dallas, Texas.
93. Testing Laboratory, ***Technical University of Budapest***, Budapest, Hungary.
94. ***Rice University***, Houston, Texas.
95. ***University of North Carolina***, Chapel Hill.
96. ***Virginia Commonwealth University***, Richmond, Virginia.
97. ***Oxford University***, Oxford, England.
98. ***Zheng Zhou Light Industry University,*** Zheng Zhou, China
99. ***Syracuse University,*** New York
100. ***University of Virginia,*** Charlottesville, Virginia

XV. Teaching Accomplishments

Received Letter of Commendation for Teaching from the Dean of College of Engineering.

Courses Taught and Developed

1. Winter 2003: EECS 270: Logic Design
   Evaluation: 4.02/5.0 (first item) and 3.77/5.0 (second item)
2. Fall 2002: EECS 579: Digital Testing
   Evaluation: 3.88/5.0 (first item) and 3.90/5.0 (second item)
3. Winter 2002: EECS 270: Digital Logic Design
   Evaluation: 4.25/5.0 (first item) and 4.33/5.0 (second item)
4. Winter 2001: EECS 270: Logic Design
   Evaluation: 4.02/5.0 (first item) and 4.32/5.0 (second item)
5. Fall 2000: EECS 270: Digital Logic Design
   Evaluation 3.74/5.0 (first item) and 4.17/5.0 (second item)
6. Fall 1999: EECS 427: VLSI Design
   Evaluation: 4.05/5.0 (first item) and 3.50/5.0 (second item)
7. Fall 1998: EECS 270: Logic Design
   Evaluation: 4.00/5.0 (first item) and 3.99/5.0 (second item)
8. Winter 1999: EECS 579: Digital Testing
   Evaluation: 3.42/5.0 (first item) 3.20/5.0 (second item)
9. Fall 1998: EECS 270: Digital Testing
   Evaluation: 4.00/5.0 (first item) and 3.99/5.0 (second item)
10. Winter 1998: Digital Logic
    Evaluation: 4.00 (first item) and 3.99 (second item)
11. Fall 1997: Taught EECS 427: VLSI Design
    Evaluation: 4.71 (first item) and 4.58 (second item)
12. Winter 1996: Taught EECS 527: Computer-Aided Design for VLSI Systems
    Evaluation: 4.50 (first item) and 4.10 (second item)
13. Fall 1995: Taught EECS 427: VLSI Design
    Evaluation: 4.55 (first item) and 3.94 (second item)
14. Winter 1995: Taught EECS 527: Computer-Aided Design for VLSI Systems
    Evaluation: 4.25 (first item) and 4.08 (second item)
15. Fall 1994: Taught EECS 427: VLSI Design
    Evaluation: 4.81 (first item) and 4.12 (second item)
16. Fall 1993: Taught EECS 427: VLSI Design
    Evaluation: 4.32 (first item) and 3.83 (second item)
17. Spring 1992: Taught EECS 270: Digital Logic Design
    Evaluation: 4.6 (first item) and 4.43 (second item)
18. Winter 1992: Taught EECS 527: Computer-Aided Design for VLSI Systems
    Evaluation: 4.00 (first item) and 4.25 (second item)
19. Fall 1991: Taught EECS 427: VLSI Design
    Evaluation: 4.13 (first item) and 3.88 (second item)
20. Spring 1991: Taught EECS 270: Digital Logic Design
    Evaluation: 4.54 (first item) and 4.71 (second item)
21. Winter 1991: Taught EECS 570: Advanced Computer Architecture
    Evaluation: 4.20 (first item) and 3.89 (second item)

Legend: 5.0 – Excellent, 4.0 – Very Good, 3.0 – Good, 2.0 – Fair, 1.0 – Poor.

XVI. List of Courses Taken During M.Sc. and Ph.D. Study

I took the following CS and CE courses while I was a graduate student:

1) Analysis of Algorithms, 2) Artificial Intelligence, 3) Computer Networks, 4) Parallel Computer Architectures, 5) Software Engineering, 6) Local Area Networks, 7) Adaptive Systems, 8) VLSI Complexity Theory, 9) Switching Theory and Digital Logic Design, 10) Computer Architecture, 11) Minicomputer

System Architecture, 12) VLSI Layout Automation and Circuit Simulation, 13) VLSI System Design, 14) AI Based CAD for VLSI, 15) Digital Testing and Fault Tolerance, and 16) Programming Languages.

M.Sc. Thesis Title: *Networks and Embedding Aspects of Cellular Structures for On-Chip Parallel Processing in VLSI* (resulted in 3 archival journal papers and 3 conference papers).

Ph.D. Thesis Title: *Testing and Fault-Tolerance Aspects of High-Density Random-Access Memory* (resulted in 6 archival journal papers and 6 conference papers).

XVII. Extracurricular Activities

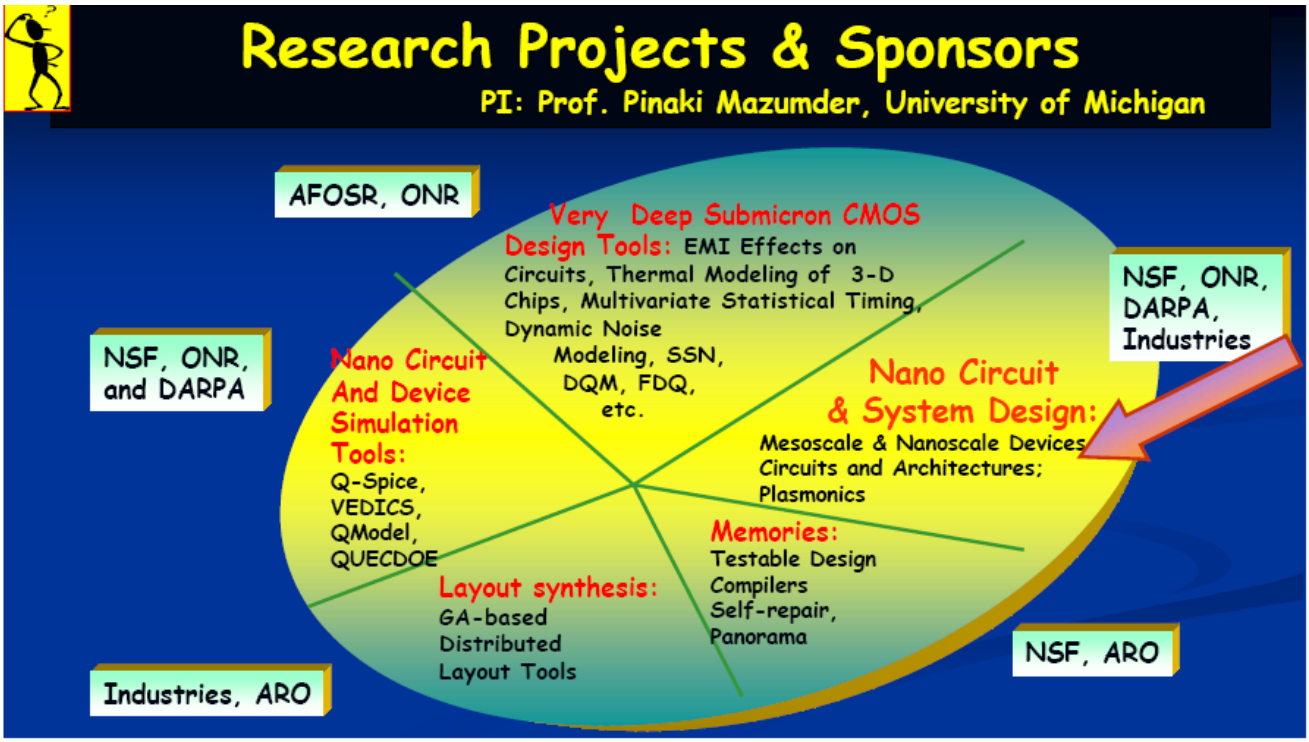
I am an avid tennis player and have been playing the game for the past 30 years, whenever I am not injured. Some of my sports awards that perhaps I am more proud of than my professional achievements are listed below. Of course, I belong to the category of hackers who pay to play rather than get paid to play. So these awards are small consolations for my efforts in these games.

- **Tennis**: Between 1975 and 2002, won several prizes in Singles and Doubles Events (between 4.0 and 4.5 NTRP levels) in Ann Arbor City Open Tennis Tournament, Ypsilanti (Michigan) City Open Tennis Tournament, Bangalore City Industrial Tennis Tournament, Indian Institute of Science Tennis Tournament, Bharat Electronics Ltd. Club Tennis Tournament, Huron Valley Tennis Club Tournament, etc.

- **Badminton**: Represented Indian Institute of Science in Karnataka State University Tournament and due to the presence of Pradeep Padukone, the brother of legendary World Badminton Champion Prakash Padukone, on our I.I.Sc. team, we won the tournament in 1975. Also won 3 prizes in I.I.Sc. Intramural Tournaments.

- **Table Tennis**: Between 1974-1976, won 4 prizes in I.I.Sc. Intramural Tournaments.

Summary of Research Activities



Nano-scale CMOS Design Issues
Prof. P. Mazumder, NDR Group

EM Effects on VLSI Circuits	Thermal Modeling of a 3-D Chips	Device and Interconnect Modeling	Statistical Timing Analysis	Dynamic Noise Analysis
Chebyshev's Approx & Pade Approx. for Distributed Noise Sources Finite Difference Quadrature Method	Green's Function based full-chip thermal analysis Direct Cosine Transform and IDCT for Fast Computation Hankel Transformation for Fast Computation	Envelope Function based quantum tunnel modeling of Nanoscale CMOS FET Differential Quadrature Method (DQM) for Interconnect Delay Modeling	Multivariate Normal Distributions for multi-input Domino gates Min/Max Correlation Analysis through Recursive Moment computation	Dynamic Noise Margins and Algorithms for Noise Analysis Simultaneous Switching Noise Estimation Coupling Noise Modeling for Automatic Routers

Quantum/Nano Systems Research Overview
Prof. P. Mazumder, NDR Group

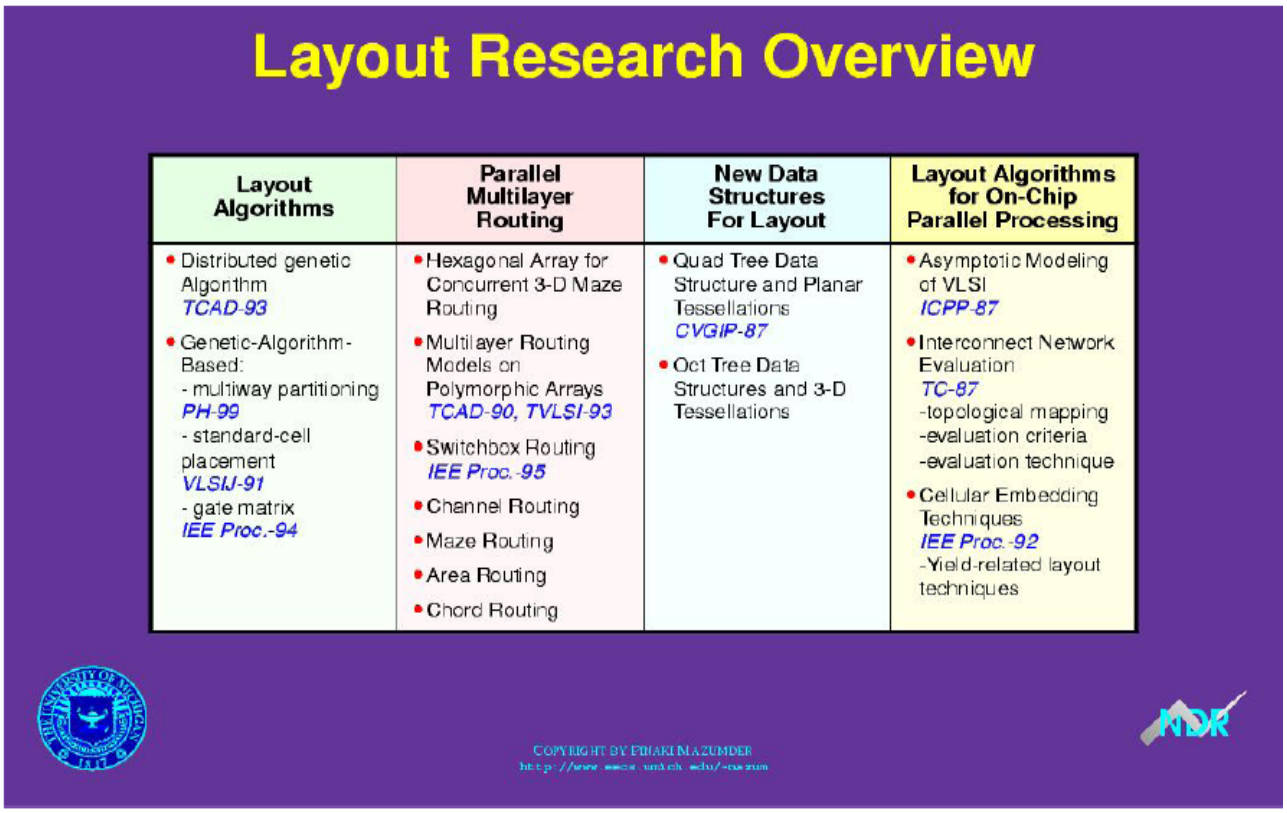
Challenges: From Quantum Physics to Circuit Theory and Software Tools

CAD Tools	Circuits	Theory	Fabrication
Q-Spice * QMOS * HEMT/HBT **QModel** * RTD * Quantum Dots & Wires **QUECDOE** * 3-D Opt **VEDICS** * FD-TLM * Full Chip	▪ New Logic Families ▪ MVL Circuits ▪ Memories ▪ Nanopipelining ▪ Correlator, DDFS ▪ Turbocode Decoder ▪ Cellular Nonlinear Networks (CNN) ▪ Quantum Dot Image and Video Processors ▪ Plasmon Nanowire	▪ PDE and ODE based Nonlinear Circuit Analysis ▪ Quantum Physics based RTD & QD Modeling ▪ FD-TLM Ckt. Simulation	▪ SiO_2/Si-Ge based QMOS NRL, OSU ▪ InP based RTD+HEMT Raytheon ▪ InP based RTD+HBT KAIST, HRL ▪ GaSb Based RTD+HEMT HRL, ND

RAM Research Overview

Circuit Techniques	Test Algorithms	Error Correction	Self Repair	Compiler
• DFT for DRAM *TC-89* • DFT for CAM *TCAD-88* • DFT for random test *JETTA-92* • BIST for RAM *TIE-89* • ASIC for memory testing *JSSC-91*	• Parallel PSF *DAC-87, ITC-87* • Parallel parametric tests *JSSC-89* • Parallel stress tests *JETTA-94* • Tests for device-related faults *TCAD-93* • Board-level test *JETTA-2000*	• Double-bit ECC *JSSC-92* • Parallel signature analyzer based ECC *JSSC-93* • Projective geometric code *TC-93* • Radiation study • Reliability analysis	• Pseudo-analog adaptive circuits for self-repair *TCAD-96* • Digital adaptive circuits for self-repair *TCAD-93* • Generalized adaptive self-repair circuit techniques *TCAD-92,93*	• RAM compiler - Self-testing - Self-repair *EDAC-99* • ROM compiler - Self-testing - Self-repair *ICCD-99 VLSIJ-99*

- Books written by P. Mazumder
  - Testing and Testable Design of High-Density RAM, 1996
  - Fault Tolerance of RAM, 2000
  - Circuit Techniques for DRAMs (under preparation)



X. Research Projects

I have been conducting research on ***six*** different aspects of VLSI system design: i**) Nanoelectronic Circuits**: **Modeling, Simulation and Applications**, ii) **Quantum MOS circuit and CAD tools**, iii) **Nanoscale CMOS design**, iv) **Random-access memories testing and fault-tolerance**, v) **Self-repairable VLSI design techniques**, vi) **Layout automation of high-performance VLSI chips.**

- **Nanoelectronic Circuits Using Quantum Dots:** Modeling of I-V characteristics using Schrödinger equation and scattering matrix; Image processing with self-assembled array of quantum dots. (2002 --- i.e., sarted in 2002 and continuing)

- **Nanoelectronic Circuits Using Mesoscopic Quantum MOS:** Visual computing by Cellular Nonlinear Networks consisting of ensemble of Q-MOS cells: hardware and algorithms. (2001--)

- **RTD-based High-speed Circuits:** Nanopipelined high-speed (60 GHz and above) communication circuits using resonant tunneling devices. (1994 ---)

- **Very Deep Submicron CMOS Circuits and Design Methodology:** Optimal adiabatic low-power CMOS circuit design, Optimal transistor sizing for high-speed CMOS design, CMOS dynamic noise modeling, Interconnect noise modeling, Simultaneous switching noise modeling, Methodology for fast detection of noise violation in SoC/VLSI, etc. (1998 ---)

- **Simultion Tool for Nanoelectronics:** Augmented SPICE simulator (QSPICE) design for quantum and other non-linear devices. (1994 ---)

- **Simulation Tool for RTD-based Ultra-fast Circuits:** 3-Dimensional full chip simulation tool design for high-

speed circuits by using Transmission Line Matrix (TLM) method. (1998 --)

- **Interconnect Delay Modeling:** High-speed interconnect delay modeling in VLSI chips by using Differential Quadrature methods that converge faster than Finite Difference methods. (1999 ---)

- **EMI Effects on VLSI Chips:** Krylov subspace solver and Green's function solver for VLSI chip design simulation. An EMI full-chip simulation tool is built for estimating delay and thermal failures in VLSI chips due to electromagnetic interferences (EMI). This research will lead to the development of nanometric FET models that will require solving Schrodinger equation, Poisson equntion and Maxwell's equations to derive the device charcateristics. (2000 ---)

- **Semiconductor Memory Testing:** Testing algorithms for high-density silicon DRAM's and SRAM's; built-in self-testing; random pattern testing, error correction; memory chip yield; failure diagnosis. (1985 --)

- **Self-Healing Techniques for VLSI Chips:** Silicon compilers for RAM, ROM, PLA, etc. with built-in self-repair capabilities; self-repairable processor, systolic and cellular arrays. (1989 --)

- **VLSI Layout SynthesisTools:** Distributed layout tools using genetic algorithms for concurrently running on a network of workstations– partitioning, placement, routing, floorplnning, etc. (1988-96)

- **Hardware Accelerator for VLSI Routing:** Polymorphic array architecture for unified parallel routing to describe maze, channel, switchbox, and area connectivities; Design of a routing chip using polymorphic array architecture; HAM: Multilyer maze router using hexagonal array machine. (1988-95).

- **VLSI Data-structures:** General theory of planar tessellations on triangular and quadrilateral lattices yielding quad-tree data-structures and their applications in VLSI layout synthesis and gridded image processing (1985—1989).

Software Developed by NDR Research Group

- ***Q-SPICE***: A Spice-based circuit simulator for two and three terminal CMOS, GaAs, InP and GaSb devices with negative differential resistance characteristics such as RTD, RTT and RHET. New homotopy based convergence algorithms were developed to improve DC convergence of RTD based nonlinear circuits that regular SPICE program fails to simulate

- ***VEDICS***: Variable-mesh Electromagnetic Device and IC simulator, a full-chip detail simulator for estimating circuit performance at high speed. It uses transmission line matrix method to solve Maxwell-like wave equations and thereby VEDICS can account for reflections, scattering and inductive effects in a VLSI chip.

- ***DQM Timing Tool***: A Differential Quadrature Method based interconnect delay modeling tool has been developed t estimate signal delays through non-uniform multiple interconnects having parasitic capacitances and mutual inductances

- ***BISRRAMGEN***: A VLSI compiler for automatic generation of embedded byte-oriented memories with built-in self-testing and self-repair capabilities

- ***RTD Modeling Tools***: Envelope function based RTD modeling tool that is used in optimizing RTD structures along with Q-Spice.

- ***Quantum Dot Modeling Tool***: This tool solves Three-Dimensional the Schrödinger equation and the Poisson equation self-consistently to model tunneling currents in pyramidal quantum dots.

- ***Thermal Simulator***: This Green function solver can estimate thermal distribution in a 3-D CMOS VLSI chip with multiple active layers.

- ***Wolverines***: Genetic algorithm based VLSI standard cell layout generation tool that runs concurrently on distributed workstations to search in parallel near optimal layout solutions. The GA-based tool also utilized a meta genetic process to select various parameters like crossover rate, mutation rate, population size, etc. by using a second-level GA technique.

- ***QECDOE***: Quantum Electronic Circuit Design Optimization Environment is a tool that is utilized to optimize circuit-level electrical parameters like power consumption, speed, noise margin, etc. by optimizing both two dimensional transistor areas and three-dimensional structures of mesoscopic devices such as quantum wells in RTD's.