Resonant Tunneling Diode Based Digital Circuits And Quantum SPICE Simulator

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Collaborators: Prof. George I. Haddad, Dr. Jack East, Dr. J. P. Sun, and C.H. Lin

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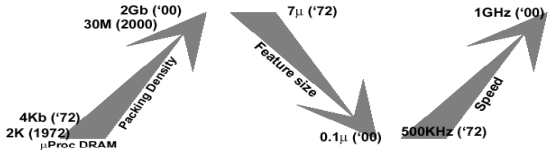
Motivation

Shrinking Era (CMOS)



Nanoelectronic Era (Future Technologies)

ULTRA-SPEED > 10GHz ULTRA-SMALL 0.1μ-0.01μ LOW-INTERCONNECT MVL

Quantum Electronic Devices	Single Electron Devices	Molecular Electronic Devices	Ferroelectric Devices
Speed >12 GHz Power <300μW/gate Telecom, Logic, RAMs	**Ultra dense SRAM Quantum Cellular Automata**	**Nanoprobes Massively parallel biological computer**	**Terabit memories Non-volatile DRAM**
U. Mich., Texas Instr., MIT LL, Hughes, Lockheed-Martin	Fujitsu, Hitachi, U. Minn., SUNY, MIT, U. Notre Dame	Yale, U. South Carolina	Sandia National Labs, Radiant Tech., Virginia Tech

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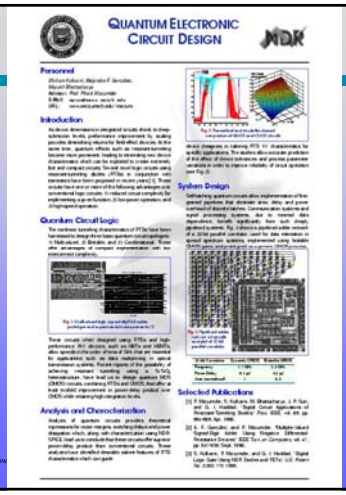
Quantum Electronic Circuit Design



Quantum Circuits Overview

CAD Tools	Circuit Design	Theory	Fabrication
NDR-Spice for quantum devices *TCAD 98, 00* ***Physics-based*** device models *Proc IEEE 98*	***Logic Circuits*** *Proc. IEEE 98* ***MVL*** *T. Comp 98* ***Bistable Logic*** *U.S. Pat. 99*	***DC characterization*** of Quantum circuit topologies	***Silicon-based tunneling devices*** Si-Ge diodes
Interconnect extraction and simulation using DQM and MMC *TMTT 00*	***Memories*** *IEICE 99* ***Nanopipelining*** *Proc. IEE 93*	***Transient analysis*** of QMOS circuit topologies	***QMOS Integrated Circuit Prototypes*** NAND/Majority/NOR Full Adder/SDA, DFF 32-bit Correlator
Statistical ***circuit optimization*** tool	***Communication Circuits*** Correlator DDFS Turbocode Decoder	***Circuit analysis*** Noise margin Power and delay Stability	***RTD-HBT, RTD-HEMT Circuits*** Majority gate, NAND/NOR gates

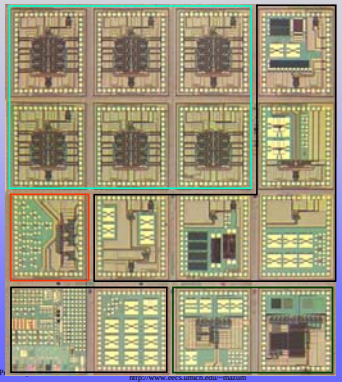
MIXED-SIGNAL NANOELECTRONICS

FLASH ADCs

ΔΣ ADCs

Time Delays

Logic



FIBER RX

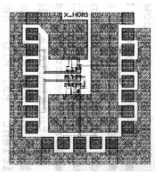
SRAM Memory

MUX DEMUX

LOW JITTER CLOCKS

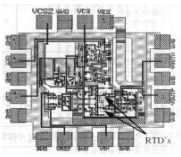
Fabricated quantum circuits

RTD/HBT Three-Input NOR Circuit
Mayo Foundation



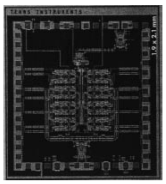
- 15 GHz

RTD/HBT Latching Comparator for ADCs
Hughes Research Labs



- > 10 GHz

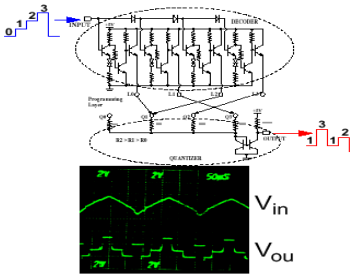
Resonant Tunneling ADC
Texas Instruments



- 3 GHz Shift Register
- 3.5 GHz Sample/ Hold
- 6-bit 25 GSps ADC

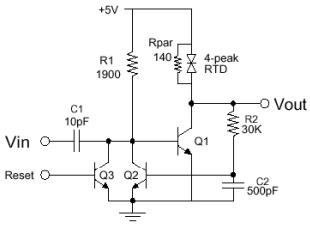
Multi-valued circuits using NDR devices

Multiple-Valued Gate Array

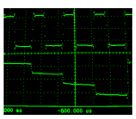


- Mask-programmable, one- and two- input, four-valued. (2GHz, 527mW) Fabrication by Lockheed-Martin

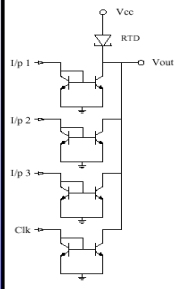
4-step down-count circuit



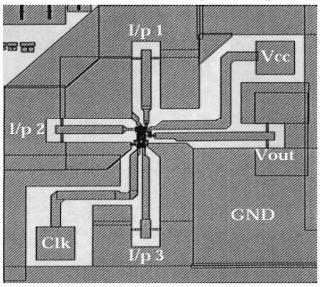
- Extremely compact. Uses 3 transistors and 1 RTD
- Similar 2-bit counter in CMOS requires > 30 transistors
- To be fabricated by Lockheed-Martin



Inverted Majority gate - circuit and layout



Fabricated at the University of Michigan



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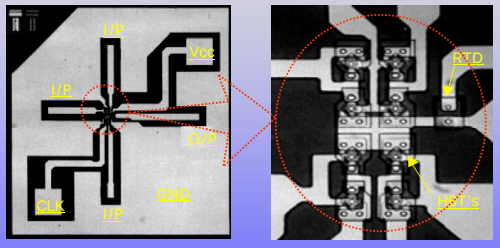
NDR

IC microphotographs of the minority gate



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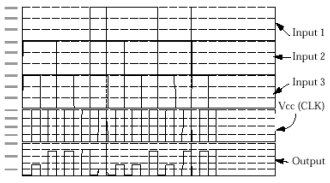
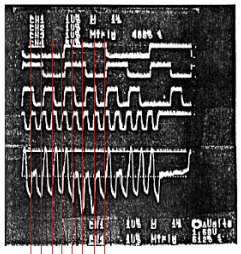
Simulation and test results for Minority gate

NDR-SPICE Simulation Results



Clock frequency: 1.6 MHz **Output Swing: 1.68V**



Input 1	0	0	0	0	1	1	1	1
Input 2	1	1	0	0	1	1	0	0
Input 3	1	0	1	0	1	0	1	0
Output	0	1	1	1	0	0	0	1

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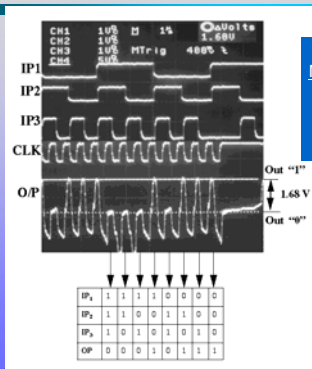
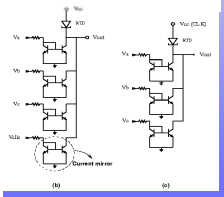
Measurement results of the fabricated minority gate



Measured at 1.6MHz using a low frequency measurement setup



IP1	1	1	1	1	0	0	0	0
IP2	1	1	0	0	1	1	0	0
IP3	1	0	1	0	1	0	1	0
OP	0	0	0	1	0	1	1	1

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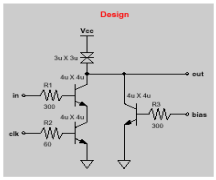
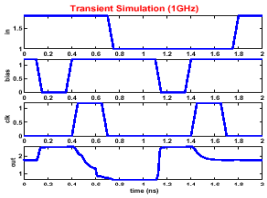
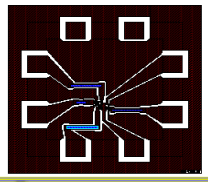
Example: Latching Inverter
Design and Optimization with NDR-Spice







Simulation Results

Max clock freq	2 GHz
Power Dissipation	9.7 mW @ 1GHz

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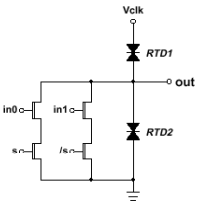
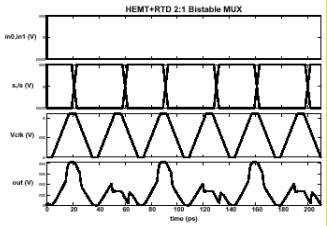
HEMT+RTD Bistable 2:1 MUX





- Frequency of operation: 28.6 GHz
- Combines multiplexing and latching properties

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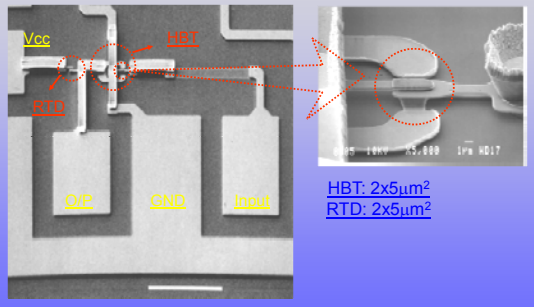
IC microphotograph of fabricated HBT and RTD



HBT: 2x5μm²
RTD: 2x5μm²

Fabricated by Prof. Haddad, Dr. East and Lin (GSRA)

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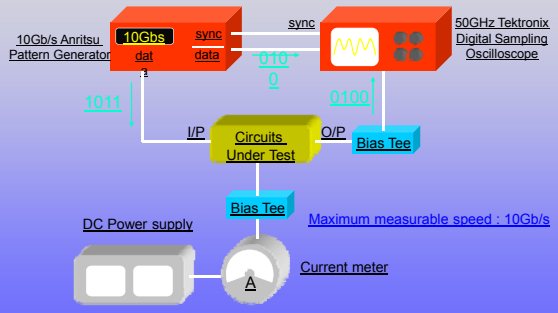
Logic function measurement Setup



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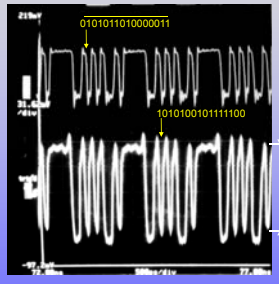
Measurement results of a fabricated inverter



- performed at 10Gb/s
- Vdata = 1.05V
- Vcc = 2.5V

inverted input data stream

measured output voltage swing ~ 110mV expected ~ 500mV

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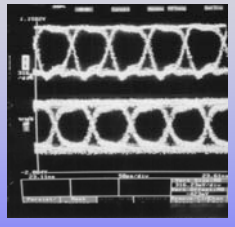
Eye diagram measurement of a fabricated inverter



10Gb/s with PRBS of 2^{31}-1

PRBS : pseudo-random binary sequence

percentage eye closure ~ 41%

percentage jitter ~ 13.8%

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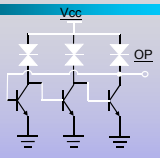
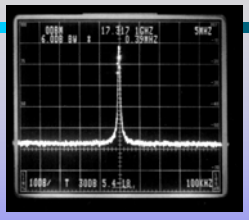
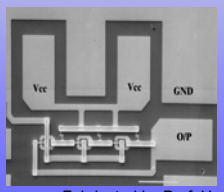
3-stage ring oscillator







Center oscillation frequency = 17.31GHz
Delay on interconnection = 1.33ps
Propagation delay per gate = 18.79ps

Fabricated by Prof. Haddad, Dr. East and Lin (GSRA)

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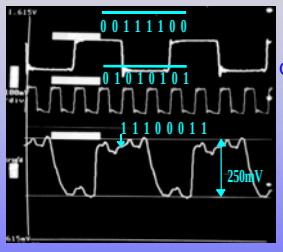
Measurement results of the fabricated consensus element



@2GHz
Input: Vp-p=1V
Output: Vswing=0.25V
Input pattern :
I/P_1=00111100
I/P_2=01010101
O/P=11100011

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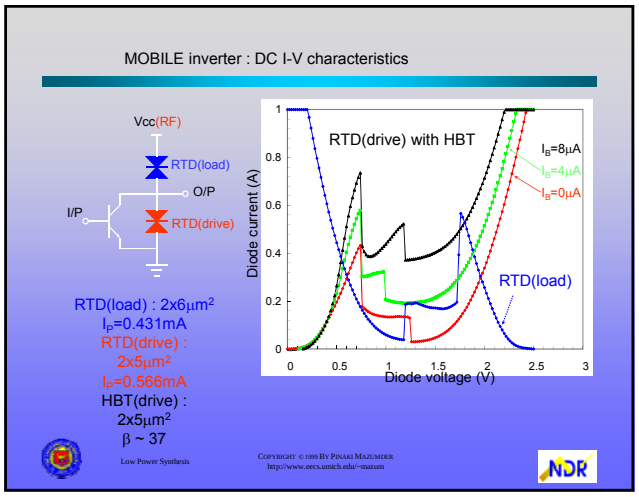
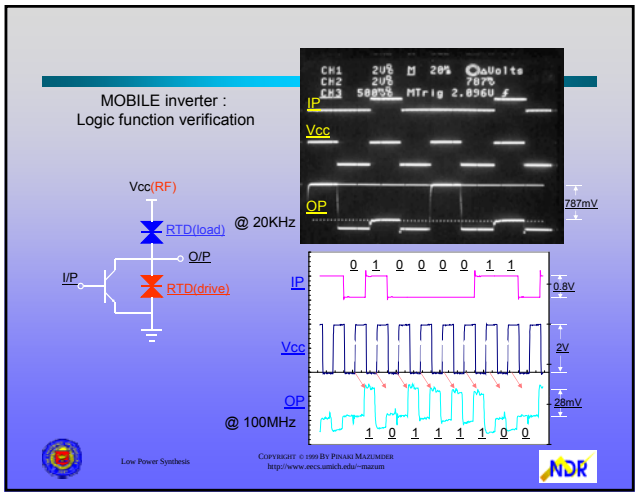
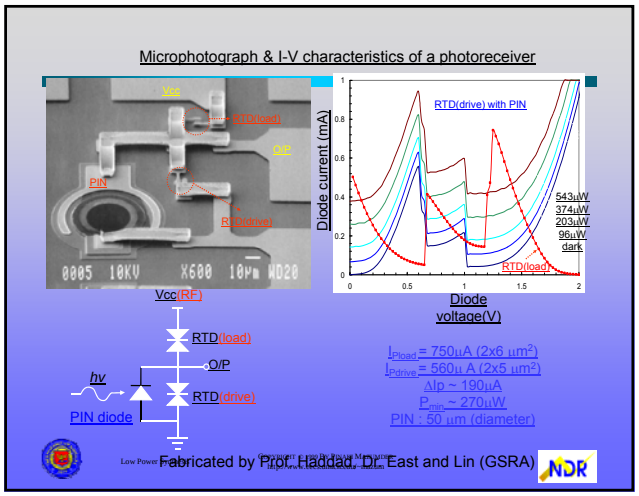
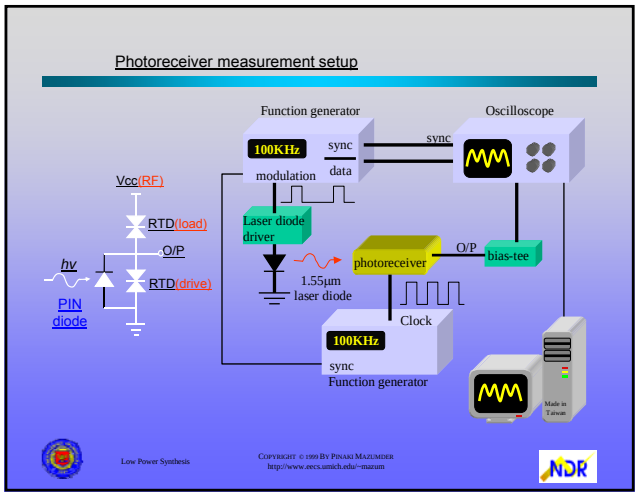
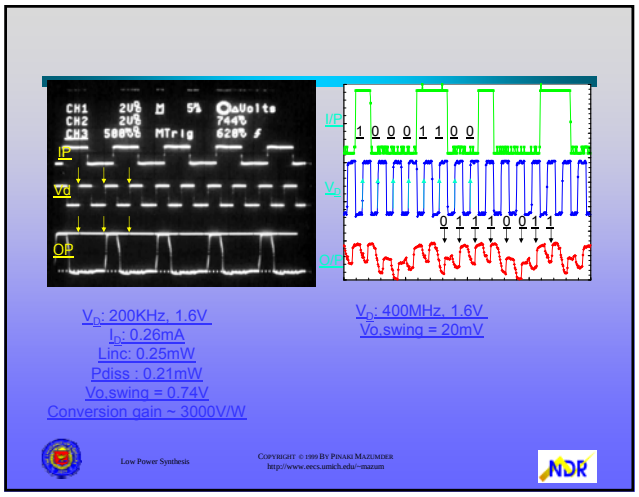

MOBILE inverter : DC I-V characteristics
Vcc(RF)
RTD(load)
O/P
I/P
RTD(drive)
RTD(load) : 2x6μm²
I_P=0.431mA
RTD(drive) :
2x5μm²
I_P=0.566mA
HBT(drive) :
2x5μm²
β ~ 37
RTD(drive) with HBT
I_B=8μA
I_B=4μA
I_B=0μA
RTD(load)
Diode current (A)
Diode voltage (V)
Low Power Synthesis
NDR


MOBILE inverter :
Logic function verification
IP
Vcc
OP
787mV
Vcc(RF)
RTD(load)
O/P
I/P
RTD(drive)
@ 20KHz
0 1 0 0 0 0 1 1
0.8V
2V
28mV
@ 100MHz
1 0 1 1 1 1 0 0
Low Power Synthesis
NDR


Microphotograph & I-V characteristics of a photoreceiver
Vcc
RTD(load)
O/P
PIN
RTD(drive)
RTD(drive) with PIN
543μW
374μW
203μW
96μW
dark
RTD(load)
Diode current (mA)
Diode voltage(V)
Vcc(RF)
RTD(load)
O/P
hv
RTD(drive)
PIN diode
I_Pload = 750μA (2x6 μm²)
I_Pdrive = 560μ A (2x5 μm²)
ΔIp ~ 190μA
P_min ~ 270μW
PIN : 50 μm (diameter)
Fabricated by Prof. Haddad, Dr. East and Lin (GSRA)
NDR


Photoreceiver measurement setup
Function generator
Oscilloscope
100KHz
sync
data
modulation
sync
Vcc(RF)
RTD(load)
O/P
RTD(drive)
hv
PIN
diode
Laser diode
driver
1.55μm
laser diode
photoreceiver
O/P
bias-tee
Clock
100KHz
sync
Function generator
Low Power Synthesis
NDR


CH1 2V/ M 5% 0.0Volts
CH2 2V/ 7.14%
CH3 500mV/ MTrig 620% f
IP
Vo
OP
I/P
O/P
1 0 0 0 1 1 0 0
0 1 1 1 0 0 1 1
V_D: 200KHz, 1.6V
I_D: 0.26mA
Linc: 0.25mW
Pdiss : 0.21mW
Vo,swing = 0.74V
Conversion gain ~ 3000V/W
V_D: 400MHz, 1.6V
Vo,swing = 20mV
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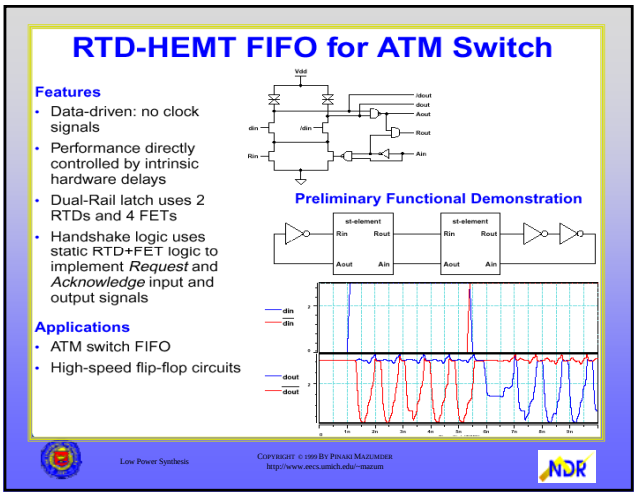
NDR


RTD-HEMT FIFO for ATM Switch
Features
Data-driven: no clock signals
Performance directly controlled by intrinsic hardware delays
Dual-Rail latch uses 2 RTDs and 4 FETs
Handshake logic uses static RTD+FET logic to implement *Request* and *Acknowledge* input and output signals
Applications
ATM switch FIFO
High-speed flip-flop circuits
Preliminary Functional Demonstration
st-element
Rin
Rout
Aout
Ain
din
dout
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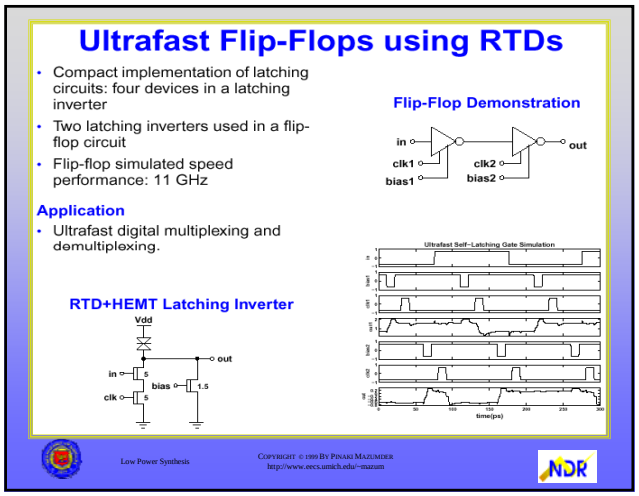
Ultrafast Flip-Flops using RTDs
Compact implementation of latching circuits: four devices in a latching inverter
Two latching inverters used in a flip-flop circuit
Flip-flop simulated speed performance: 11 GHz
Application
Ultrafast digital multiplexing and demultiplexing.
RTD+HEMT Latching Inverter
Vdd
in
clk
bias
out
Flip-Flop Demonstration
clk1
clk2
bias1
bias2
Ultrafast Self-Latching Gate Simulation
time(ps)
Low Power Synthesis
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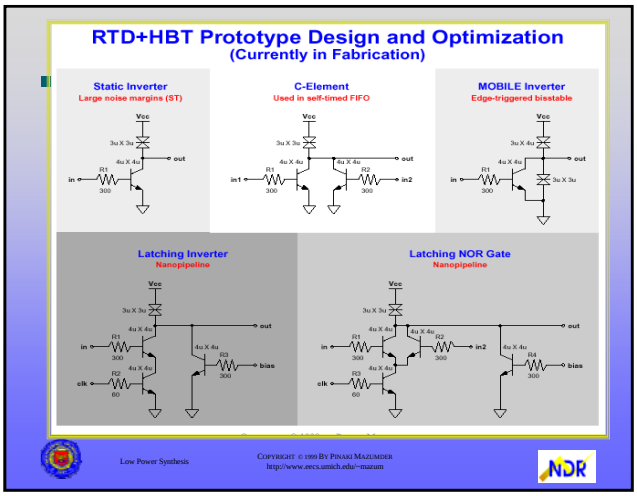
NDR


RTD+HBT Prototype Design and Optimization
(Currently in Fabrication)
Static Inverter
Large noise margins (ST)
C-Element
Used in self-timed FIFO
MOBILE Inverter
Edge-triggered bistable
Latching Inverter
Nanopipeline
Latching NOR Gate
Nanopipeline
Vcc
in
in1
in2
out
clk
bias
Low Power Synthesis
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NDR

Summary of basic self-latching NDR circuits

Circuit	Technology	Power	Speed/Delay	Noise Margins
AND3 OR3 CARRY	RTBT	10 mW 10 mW 10 mW	40 ps 37 ps 34 ps	0.3 V 0.3 V 0.3 V
NOR3 MINORITY NAND3	RTD-HEMT (depletion)	0.48 mW 0.6 mW	5 GHz (25 GHz max)	IH=90mA,IL=0 NMH=17mA, NML=9mA
NOR3 MINORITY	RTD-HEMT (enhancement)	0.3 mW	5 GHz (25 GHz max)	same as above
NOR3 MINORITY 32-bit Adder	RTD-HBT	0.5 mW 10 mW	25 GHz 560 ps	0.3V
MAJORITY Full Adder	QMOS	0.1 mW 0.4 mW	200 ps 2.5 GHz	0.5 V
32-bit Correlator	RTD-HBT RTD-HEMT QMOS	1.5 W 1 W 0.6 W	10 GHz 3 GHz 2.5 GHz	
T-gate MVL Gate-Array	RTD-HBT	327 mW 3.2 mW 500 mW	2.87 ns 33.33 ns 2 GHz	0.3V

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Comparison of various logic families

Parameter	0.5 μm CMOS	MODFET-RTD	HBT-RTD	GaAs CHFET
Power/Gate	0.3 mW	0.3 mW	0.5 mW	0.1 mW
Gate Delay	500ps	200ps	40ps	250ps
Noise Margin	1.5V @ 3V*op*	17μA @ 90μA*op*	0.3V @ 1V*op*	0.75 @ 1.5V*op*
Device Count per Function	Large due to regular V-I Chrs	Small due to NDR V-I Chrs	Small due to NDR V-I Chrs	Large due to regular V-I Chrs
Packing Density	Very high	Low	Low	Low

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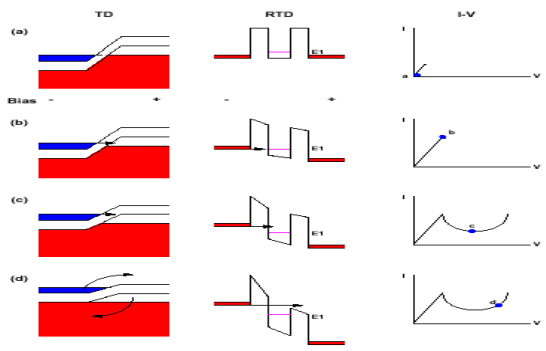
RTD device operation



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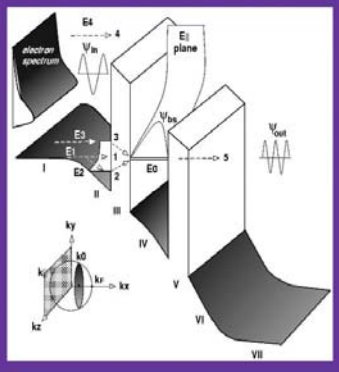
Processes in Double-Barrier Tunneling



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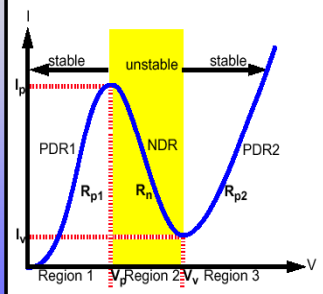
RTD's I-V characteristics



Various RTD parameters

RTD	PVR	$V_V V_P$
TI RTD	4	0.35V
UMA-1174	10	0.30V

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RTD's I-V equation

$$J = \frac{em^*kT}{2\pi^2\hbar^3}\int_0^\infty T(E,V)\cdot \ln\left[\frac{1+e^{(E_F-E)/kT}}{1+e^{(E_F-E-eV)/kT}}\right]dE$$

where,

$$T(E,V) = \frac{\left(\frac{\Gamma}{2}\right)^2}{\left[E-\left(E_r-\frac{eV}{2}\right)\right]^2+\left(\frac{\Gamma}{2}\right)^2}$$

E_r is energy of the resonant level w.r.t. bottom of well at its center.

For small Γ(resonance width), $T(E,V)$ is negligible except for $E \sim (E_r - eV/2)$.

Replacing E with $(E_r - eV/2)$, we get:

$$J = \frac{em^*kT\Gamma}{4\pi^2\hbar^3}\ln\left[\frac{1+e^{(E_F-E_r+eV/2)/kT}}{1+e^{(E_F-E_r-eV/2)/kT}}\right]\cdot\left[\frac{\pi}{2}+\text{atan}\left(\frac{E_r-\frac{eV}{2}}{\frac{\Gamma}{2}}\right)\right]$$

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RTD's I-V equation (contd.)

$$J(V) = J_1(V) + J_2(V)$$

where,

$$J_1(V) = A\ln\left[\frac{1+e^{(B-C+n_1V)q/kT}}{1+e^{(B-C-n_1V)q/kT}}\right]\left[\frac{\pi}{2}+\text{atan}\left(\frac{C-n_1V}{D}\right)\right]$$

represents the *tunneling current*, and

$$J_2(V) = H(e^{n_2qV/kT}-1)$$

represents the *diode current*.

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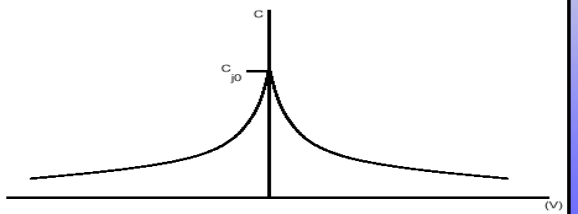
RTD's C-V equation

$$C(V) = \frac{C_{j0}}{\left(1+\frac{|V|}{V_{bi}}\right)^M}$$



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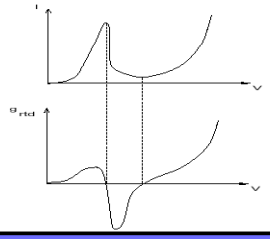
The conductance

$$g_{rtd}(V) = \frac{Aqn_1}{kT}\left(\frac{\beta}{1+\beta}+\frac{\alpha}{1+\alpha}\right)\left(\frac{\pi}{2}+\text{atan}\left(\frac{C-n_1V}{D}\right)\right)+\frac{An_1^2\ln\left(\frac{1+\beta}{1+\alpha}\right)}{D^2+(C-n_1V)^2}+\frac{qHn_2}{kT}e^{\frac{qn_2V}{kT}}$$

where,

$$\alpha = e^{((B-C-n_1V)q/kT)}, \beta = e^{((B-C+n_1V)q/kT)}$$



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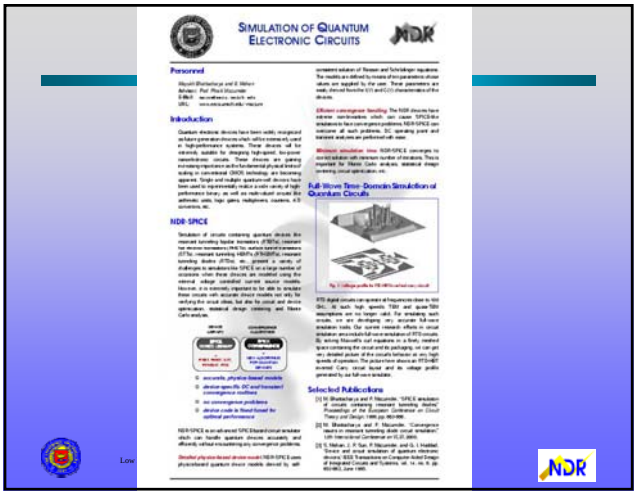
SIMULATION OF QUANTUM ELECTRONIC CIRCUITS

Personnel

Introduction

Full-Wave Time-Domain Simulation of Quantum Circuits

NDR-SPICE

Selected Publications

SPICE representation of a device

1. The arbitrary source model:

- Good ad-hoc technique; useless for circuits with many devices
- Limited representation capability
- Inefficient
- Does not allow device specific algorithms

2. A SPICE library model:

- Incorporation needs effort
- Can represent the device characteristic in great detail
- Good efficiency (e.g. derivatives are easily found)
- Most importantly, allows device specific algorithms

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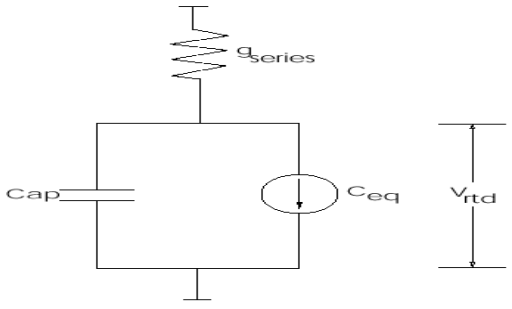
SPICE3f5 model of the RTD



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Iterative solution procedure

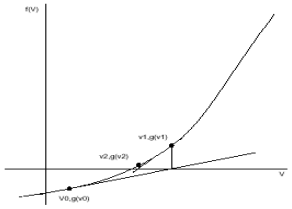
Newton-Raphson Algorithm:

$$J(v^{(k)})(v^{(k+1)} - v^{(k)}) = -f(v^{(k)})$$

or,

$$v^{(k+1)} = v^{(k)} - J^{-1}(v^{(k)}) f(v^{(k)})$$

with Update Criterion: $|v^{(k+1)} - v^{(k)}| < \delta_v$ and Residue Criterion: $F(v^{(k+1)}) < \delta_f$



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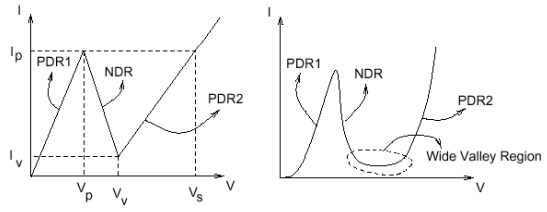
The features of the I-V curve



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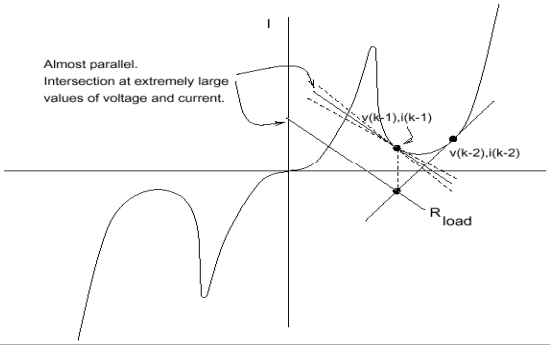
The numerical instability problem



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Solving the DC convergence problems

Proposed techniques:

- A modified limiting algorithm
- An artificial parameter homotopy method

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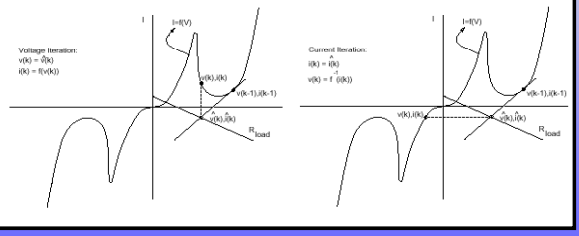
Different iteration techniques



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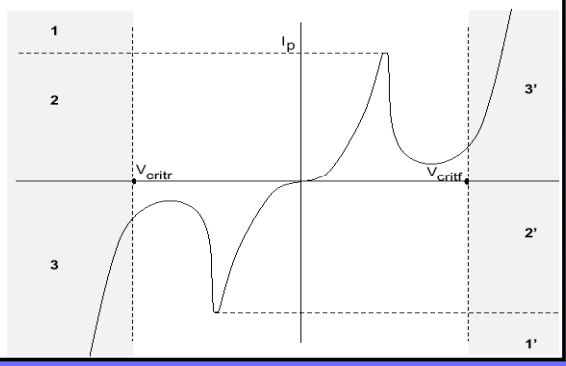
The modified limiting algorithm



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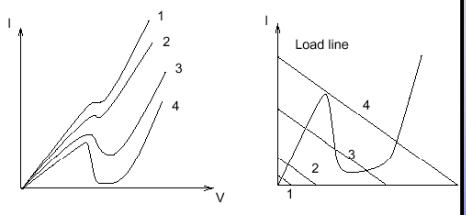
SPICE3f5's continuation techniques



Homotopy technique:

$$H(x,\lambda) = (1-\lambda)(x-a) + \lambda F(x)$$

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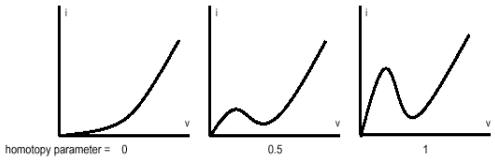
'RTD-stepping' - a homotopy technique

The basic idea:

$$J(V) = \lambda J_1(V) + J_2(V)$$



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Transient convergence problems

1. Time-step too small problem
   - Time is the continuation parameter during transient convergence.
   - Basic assumption used by SPICE: the solution points move slowly from time-point to time-point.
2. Coarse time-step problem
   - Sudden change in number of possible solutions can be hazardous.
   - Simulator must be smart enough to detect such a possibility.

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NDR

The 'time-step too small' problem

Traditional techniques:

- Extremely fast changing of a node-voltage is considered 'unrealistic' in traditional thinking
- Attaching capacitor across problematic node can slow down switching.

Problems:

- RTDs are different from 'traditional' devices.
- Extreme fast switching is possible across NDR regions.
- Device capacitance is extremely small.

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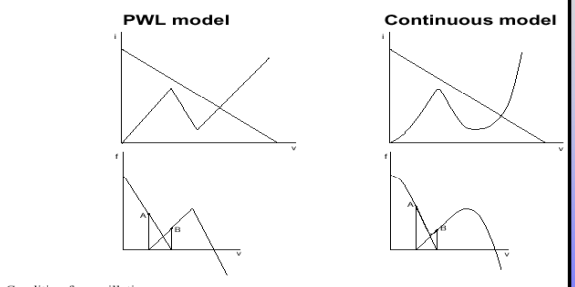
NDR

Why force-convergence is necessary



Condition for oscillation:

$$\frac{1}{f_A}\left(\frac{df}{dV}\right)_A + \frac{1}{f_B}\left(\frac{df}{dV}\right)_B \cong 0$$

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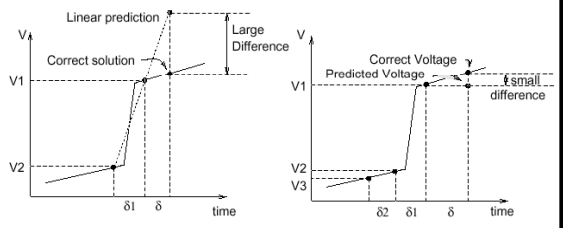
Changing SPICE's voltage prediction algorithm



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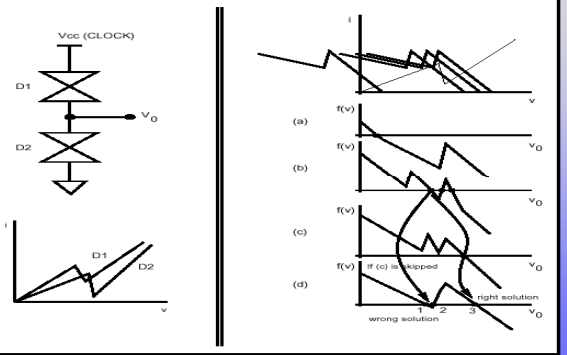
NDR

The coarse time-step problem



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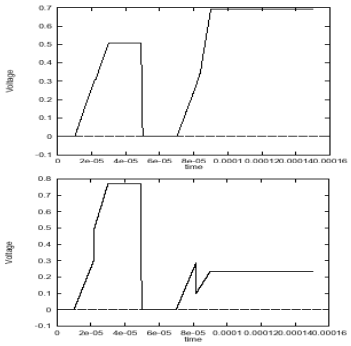
The coarse time-step problem (contd.)



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Changing the time-step adjustment algorithm

Traditional:

- User defines: T_{start}, T_{stop} & T_{step}.
- Internal time-step starts with:

$$T_{step} = MIN\left(\frac{T_{stop} - T_{start}}{50}, T_{step}\right)$$

- Internal time-step varies with time depending on local truncation error (LTE).
- ***T_{step} = 2*T_{step}, if LTE < allowable error.***
- $T_{step} = T_{step}/8$, if LTE > allowable error.
- T_{step} has a lower limit, beyond which *'time-step too small'* problem arises. Simulation is aborted.

Modified:

- Sense if the operating point is close to the peak region.
- Reduce T_{step} to $T_{step}/8$.

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DC operating point simulation results

R_{ext}	V_{ni}	D	Iterations before failing
5050	4.6	0.0055	509
2080	1	0.0064	459
5050	4.6	0.0058	474
5050	4.6	0.0064	503
6040	5.5	0.0052	504
7030	6.4	0.0058	464
8020	7.3	0.0049	433

P = Plain Newton's Method
G = Gmin-stepping
S = Source-stepping
R = RTD-stepping
PL = Plain Newton's Method with Limiting Algorithm

R_{series}	A	D	H	SPICE3f5	RTD-stepping	Limiting Algo.
0	8e-05	0.0055	1.011e-09	P 93	P 93	PL 35
0	8e-05	0.0046	2.211e-09	P 87	P 87	PL 42
0	8e-05	0.0043	4.110e-10	P+G 159	P+R 147	PL 26
2	9.2e-05	0.0043	6.110e-10	P+G 159	P+R 151	PL 37
4	1.12e-04	0.004	4.110e-10	P+G 158	P+R 152	PL 39
0	1.12e-04	0.0067	1.411e-09	P+G+S 368	P+R 145	PL 50
0	1.16e-04	0.0052	2.211e-09	P+G+S 368	P+R 145	PL 19
2	8e-05	0.0058	1.211e-09	P+G+S 386	P+R 152	PL 26
2	8e-05	0.0064	1.211e-09	P+G+S 434	P+R 152	PL 32
4	8.8e-05	0.0064	8.110e-10	P+G+S 369	P+R 152	PL 42
4	1.08e-04	0.0043	1.211e-09	P+G+S 380	P+R 152	PL 36
4	1.12e-04	0.0064	1.211e-09	P+G+S 368	P+R 152	PL 28
2	1e-04	0.0061	2.211e-09	FAILURE 428	P+R 152	PL 20
4	1.04e-04	0.0046	1.011e-09	FAILURE 434	P+R 152	PL 26
6	1e-04	0.0055	1.411e-09	FAILURE 427	P+R 152	PL 25
10	1.04e-04	0.0046	1.211e-09	FAILURE 436	P+R 152	PL 53
16	9.6e-05	0.0052	1.411e-09	FAILURE 429	P+R 152	PL 28
18	8.8e-05	0.0055	1.011e-09	FAILURE 437	P+R 152	PL 44
18	8.8e-05	0.0058	1.011e-09	FAILURE 429	P+R 152	PL 31
18	9.2e-05	0.0061	1.211e-09	FAILURE 429	P+R 152	PL 21
18	1.12e-04	0.0046	1.011e-09	FAILURE 429	P+R 152	PL 24
18	1.12e-04	0.0058	2.211e-09	FAILURE 429	P+R 152	PL 30

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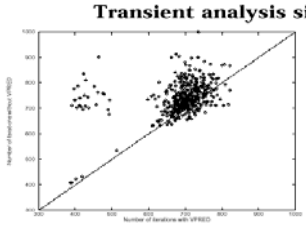
Transient analysis simulation results



R_{load}	A	D	Without FC	With FC	With FC & VPRED
2000	8.40e-05	6.1e-03	SUCCESS, 535	535	513
2000	8.80e-05	6.7e-03	SUCCESS, 409	409	387
2000	9.20e-05	6.7e-03	SUCCESS, 423	423	402
2000	9.60e-05	6.7e-03	SUCCESS, 409	409	391
2000	8.00e-05	4.6e-03	FAILURE, 539	763	692
2000	8.00e-05	5.5e-03	FAILURE, 576	792	661
2400	8.00e-05	5.8e-03	FAILURE, 595	742	701
2400	1.04e-04	4.9e-03	FAILURE, 545	735	708
2800	8.80e-05	5.5e-03	FAILURE, 552	705	667
2800	1.04e-04	5.8e-03	FAILURE, 707	779	736
3200	8.40e-05	4.9e-03	FAILURE, 717	913	742
3200	8.40e-05	6.4e-03	FAILURE, 672	786	737
3200	1.04e-04	6.1e-03	FAILURE, 818	898	766
3200	1.12e-04	5.8e-03	FAILURE, 757	841	709

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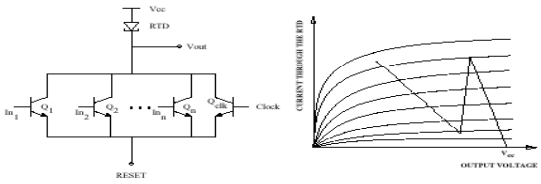
Circuit topology and load line



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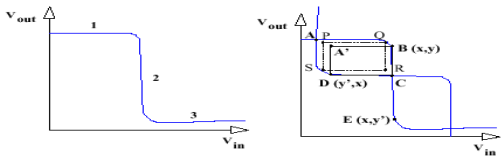
The noise margin criterion



$$NM_H = (V_{cc} - V_p) + (I_H - I_Q)R_{p1} - V_T \log\left(\frac{I_p - I_H}{I_s\left(1 - \exp\left(-\frac{V_{cc} - V_p}{V_T}\right)\right)}\right)$$

$$NM_L = V_T \log\left(\frac{I_p - I_H}{I_s\left(1 - \exp\left(-\frac{V_{cc} - V_p}{V_T}\right)\right)}\right) - (V_{cc} - V_f) - (I_H - I_Q)R_{p2}$$

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Industry Interaction

- Industrial Collaboration
  - Texas Instruments
    - Fabrication of RTD+HEMT logic circuits and RTD+FET logic circuits
  - Hughes Research Laboratory
    - Fabrication of RTD-based digital logic and parallel correlator
  - Mayo Clinic
    - Testing of ultrafast RTD-based circuits

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Tunneling Random Access Memory (TRAM) Performance Analysis

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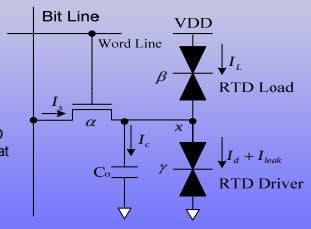
Tunneling Random Access Memory (TRAM) Performance Analysis

- TRAM Topology

  Traditional DRAM being augmented by a RTD pair



- Advantages
  - The bistable property of the RTD pair gives the TRAM a lot of great advantages over traditional DRAM
  - Faster access speed
  - Better soft error immunity ability
  - Less power consumption

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Fast Access Speed

- Analytically studied the READ and WRITE operation of the TRAM by using piece-wise Linear RTD model
  - Analytical study
    - READ operation

      We have derived the bit line waveform for READ operation, READ '1' and READ '0' has the same expression with different parameters

$$\Delta V = \frac{\alpha}{C_{bit}}\left\{\frac{B}{\lambda^*}(x_0 - \frac{A^*}{B^*})(e^{-\lambda^* t} - 1) + (A - B\frac{A^*}{B^*})t\right\}$$

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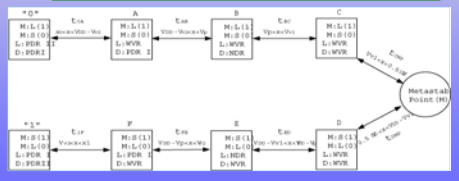
Fast Access Speed (cont'd)

- Analytical Study
  - WRITE operation

    We have derived the write access time expression by using microstate transition diagram:

$$T_1 = t_{0A} + t_{AB} + t_{BC} + t_{CMP} \qquad T_0 = t_{1F} + t_{FE} + t_{ED} + t_{DMP}$$

$$t = \frac{1}{\lambda}\ln\frac{a^* - b^* x_{t0}}{a^* - b^* x} + t_0$$



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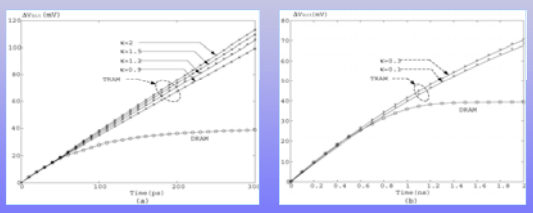
Fast Access Speed (cont'd)

- Model Verification and Comparison with Traditional DRAM



READ '0' operation READ '1' operation

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Soft Error Immunity

- Due to the self-latching property of the RTD pair, TRAM is more robust than DRAM in terms of soft error immunity
- Analytical study of the Critical Charge in TRAM

$$Q_{r1} = Q_{sc} - C_0(x_1 - x)$$
$$Q_{r0} = Q_{sc} - C_0(x - x_0)$$

- Comparison with conventional DRAM

	DRAM $Q_C(fC)$						TRAM Q_C (fC)		
$C_{bit}(fF)$	250		300		350				
C_0 (fF)	$\Delta V_{sen}(mV)$		$\Delta V_{sen}(mV)$		$\Delta V_{sen}(mV)$		Q_{sc} (fC)	Q_{r1} (fC)	Q_{r0} (fC)
	40	50	40	50	40	50			
40	20.4	17.5	18.4	15.0	16.4	12.5	28.0	27.2	22.1
35	16.6	13.8	14.6	11.3	12.6	8.80	24.5	23.8	19.4
30	12.8	10.0	10.8	7.50	8.80	5.00	21.0	20.4	16.6
25	9.00	6.25	7.00	3.80	5.00	1.25	17.5	17.0	13.8

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Power Consumption

- TRAM can eliminate the requirement of the refreshing operation that is essential in DRAM and thus decrease the power consumption
- We have derived the TRAM versus DRAM power consumption ratio

$$\eta = \frac{(\frac{1}{\delta} + \frac{1}{PVCR-1})}{\delta(1+\frac{C_{bit}}{C_0})\frac{1}{(1-\frac{C_{bit}}{C_0})(\frac{2V_r}{V_{DD}-2V_r})}}$$

If we assume ideal sense amplifier with $V_r = 0$, and $\delta = 50$, PVCR $= 10$, $\frac{C_{bit}}{C_0} = 10$, the power consumption ratio η can be as low as 10^{-2}.

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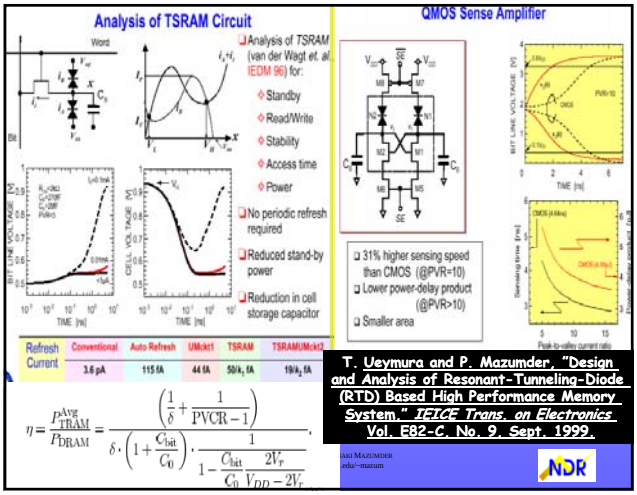

$$\eta = \frac{P_{TRAM}^{Avg}}{P_{DRAM}} = \frac{\left(\frac{1}{\delta} + \frac{1}{PVCR-1}\right)}{\delta \cdot \left(1+\frac{C_{bit}}{C_0}\right) \cdot \frac{1}{1-\frac{C_{bit}}{C_0}\frac{2V_r}{V_{DD}-2V_r}}}$$

TUNNELING RANDOM-ACCESS MEMORY OPERATION MICROSTATES

TABLE I
PARAMETERS FOR WRITE "1" OPERATION

	State Transition			
	"0"→"A"	"A"→"B"	"B"→"C"	"C"→"M"
a'	$A+\kappa I_q+BV_{bi0}$ $+\kappa V_{pc}$	$A+\kappa(I_{d1}+BV_{bi0}$ $+\kappa(\frac{V_{DD}-V_{d1}}{R_d}-I_{d1})$	$A+BV_{bi0}+\kappa(I_{d1}-I_p)$ $+\kappa(\frac{V_{d1}}{R_d}+\frac{V_{DD}-V_{d1}}{R_d})$	$A+BV_{bi0}+\frac{\kappa V_{DD}}{R_d}$
b'	$B+\frac{\kappa}{R_{d1}}$	$B+\frac{\kappa}{R_{d1}}$	$B+\frac{\kappa}{R_{d1}}$	$B+\frac{\kappa}{R_d}$

TABLE II
PARAMETERS FOR WRITE "0" OPERATION

	State Transition			
	"1"→"F"	"F"→"E"	"E"→"D"	"D"→"M"
$A-\kappa I_q+BV_{bi0}$ $+\kappa V_{DD}$	$A-\kappa(I_{d1}+BV_{bi0}$ $+\kappa(\frac{V_{DD}}{R_d}+\frac{I_{d1}}{R_d})$	$A+\kappa(I_p-I_{d1})+BV_{bi0}$ $+\kappa(\frac{V_{DD}-V_{d1}}{R_d}+\frac{I_{d1}}{R_d})$	$A+BV_{bi0}+\kappa\frac{V_{DD}}{R_d}$	
$B+\frac{\kappa}{R_{d1}}$	$B+\frac{\kappa}{R_{d1}}$	$B+\frac{\kappa}{R_{d1}}$	$B+\frac{\kappa}{R_d}$	

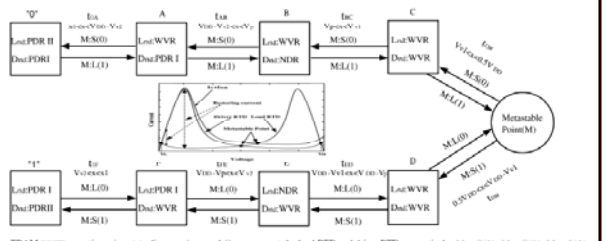

Fig. 4. TRAM WRITE operation microstate diagram. L_{rtd} and D_{rtd} represent the load RTD and driver RTD, respectively. $M:S(1), M:S(0), M:L(1)$, and $M:L(0)$ represent the saturation (S) and linear (L) operation region of the access transistor. (1) denotes WRITE "1" operation and (0) denotes WRITE "0" operation.

COMPARISON OF QC FOR TRAM & DRAM

H. Zhang, P. Mazumder, L. Ding, and K. Yang, "Performance Modeling of Resonant Tunneling Based Random Access Memories," *IEEE Transactions on Nanotechnology*, July 2005, pp. 472-480.

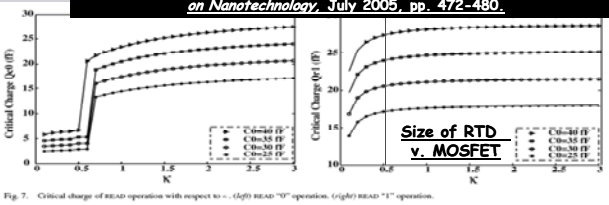

Fig. 7. Critical charge of READ operation with respect to κ. (*left*) READ "0" operation. (*right*) READ "1" operation.

TABLE III
CRITICAL CHARGE COMPARISON OF TRAM AND CONVENTIONAL DRAM.

150%-- 200% SER Improvement

	DRAM Q_C (fC)									TRAM Q_C (fC)						
C_{bit}(fF)	150			200			250			Q_{C1} (fC)			Q_{C0} (fC)			Q_{cr}
C_0	ΔV_{sen}(mV)			ΔV_{sen}(mV)			ΔV_{sen}(mV)			ΔV_{sen}(mV)			ΔV_{sen} (mV)			(fC)
(fF)	50	60	70	50	60	70	50	60	70	50	60	70	50	60	70	
25	11.3	9.5	7.8	8.8	6.5	4.3	6.3	3.5	0.8	17.1	17.0	17.0	14.4	14.4	14.5	17.8
30	15.0	13.2	11.4	12.5	10.2	7.9	10.0	7.2	4.4	20.5	20.5	20.4	17.2	17.3	17.3	21.4
35	18.8	16.9	15.1	16.3	13.9	11.6	13.8	10.9	8.1	24.0	23.9	23.8	20.1	20.1	20.2	24.9
40	22.5	20.6	18.7	20.0	17.6	15.2	17.5	14.6	11.7	27.4	27.3	27.2	22.9	23.0	23.1	28.5

Three-Dimensional Full Chip Simulation Tools for Design and Fabrication of RTD based Circuits

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VEDICS: a variable-mesh electromagnetics-based device and interconnect simulator

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VEDICS

- **Finite-Difference TLM (FD-TLM) method as the simulation engine of VEDICS**
  FDTLM: Finite-difference representation of expanded-node transmission line matrix method.
- **Integrating semi-conductor device models**
  RTD, HBT, CMOS, HEMT, HFET
- **A user-friendly GUI interface is provided.**
  Circuit Layout design and high-fidelity circuit simulation processes are integrated together
- **Subgridding approach for improving speed**
  Subgridding method leads to 2x speedup to traditional FD-TLM method

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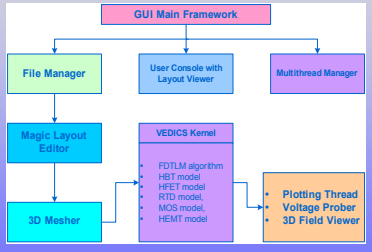
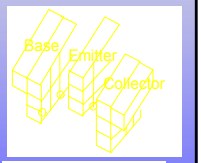
VEDICS

- VEDICS Simulation Framework



FD-TLM simulation engine, device models, and peripheral tools are integrated together



Example: HBT device model in VEDICS

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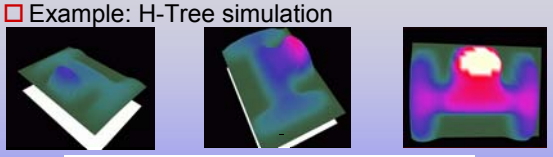
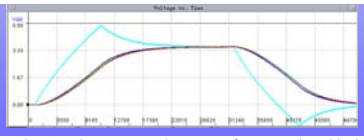
VEDICS

- Example: H-Tree simulation



Field distribution plot at different instants, produced by VEDICS



Transient input and response voltage waveforms produced by VEDICS

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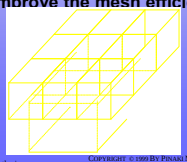
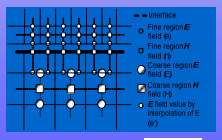
VEDICS

The entanglement of coarse and fine cells in subgridding method

- **Subgridding method**
  Variable mesh method: the mesh size in each coordinate can be varied, however, the planes orthogonal to the same axes must have same resolutions.
  Subgridding method: localizes the mesh resolution to specific regions and improve the mesh efficient over the variable mesh method





The interface between fine and coarse region

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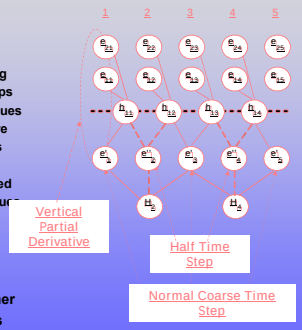
VEDICS

- Subgridding Method
  - Meshes in different subgridding regions have different time steps
  - Half time step denotes field values in the interface at finer grids are obtained by interpolating fields at coarse time steps
  - Vertical partial derivative is used to interpolate the finer field values using field values at three consecutive grids
- The coarse and fine grid interface fulfill the conversion of field values at coarser and finer spatial and temporal resolutions



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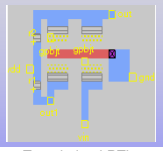
VEDICS

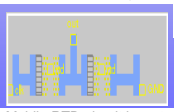
- Examples using subgridding



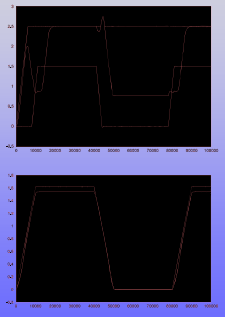
Two chained RTL inverters circuit layout

Comparison of simulation using subgridding and not

Negligible Differences



Mobile RTD circuit layout



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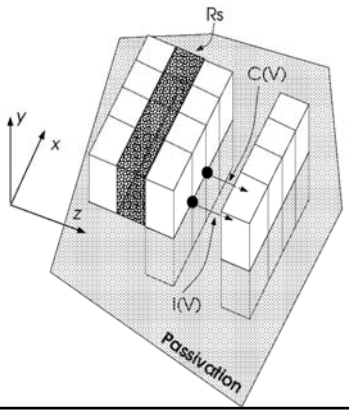
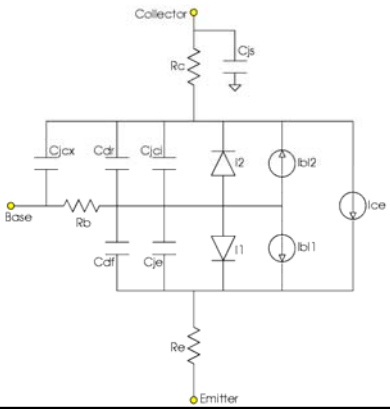
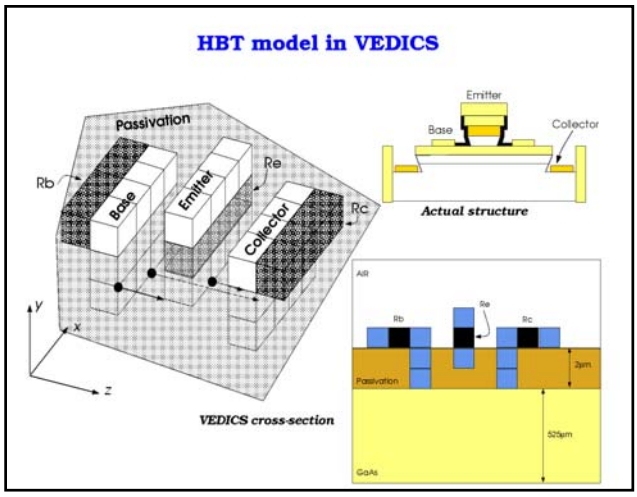
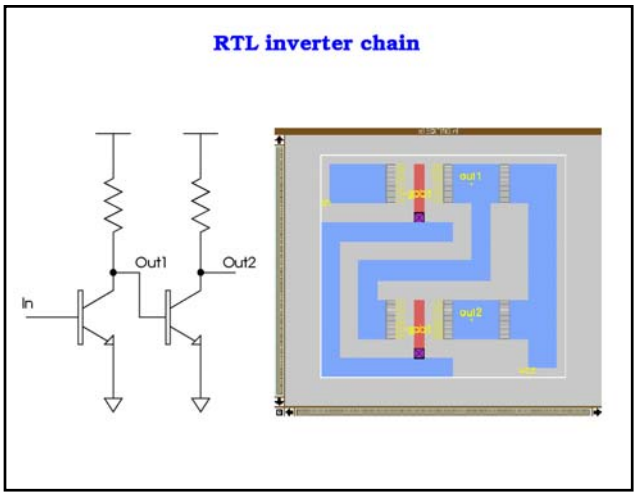
RTD model in VEDICS

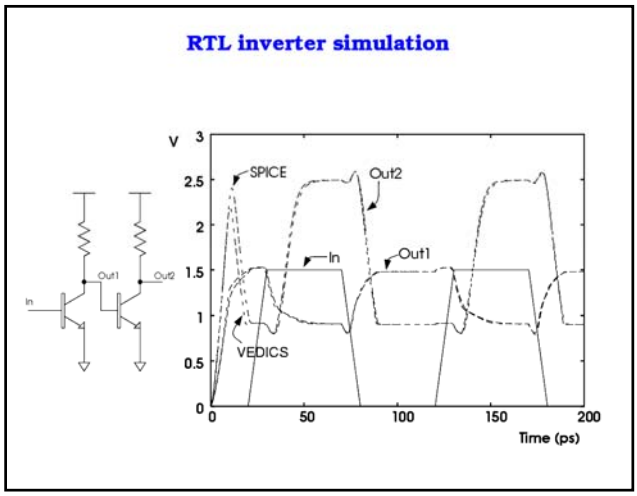


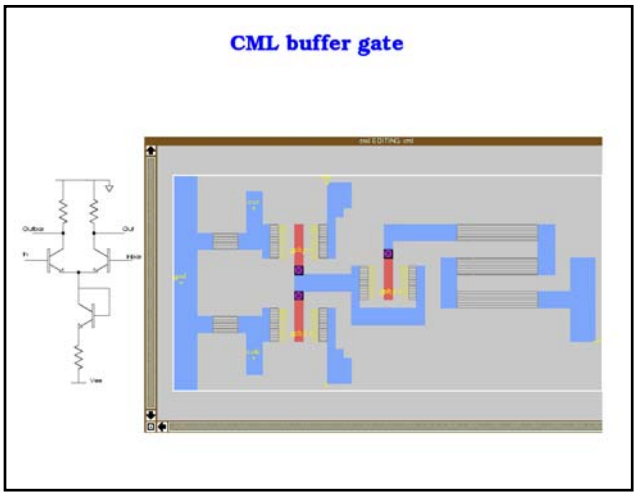
HBT model in SPICE

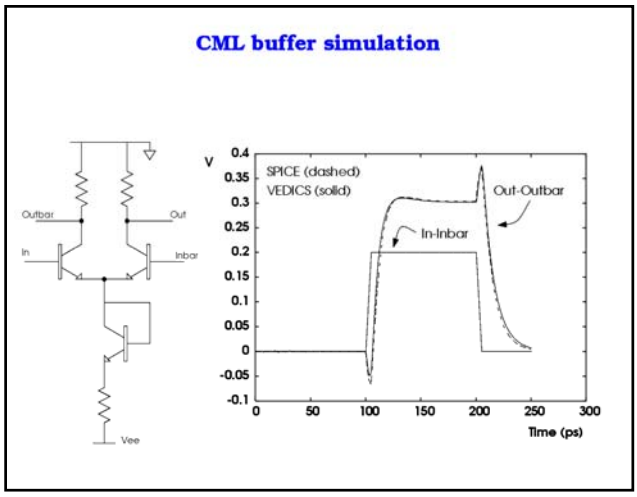


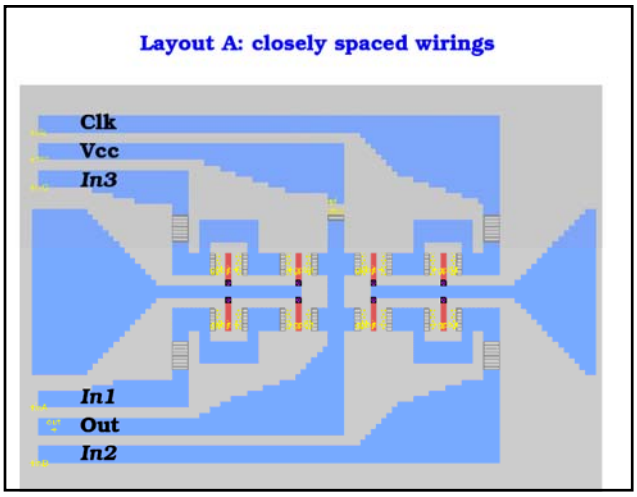

HBT model in VEDICS
Passivation
Rb
Base
Emitter
Re
Collector
Rc
y
x
z
VEDICS cross-section
Emitter
Base
Collector
Actual structure
AIR
Rb
Re
Rc
Passivation
2μm
525μm
GaAs

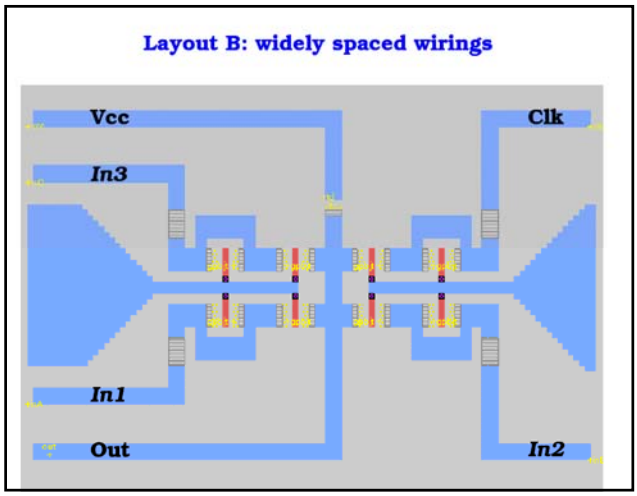

RTL inverter chain
In
Out1
Out2

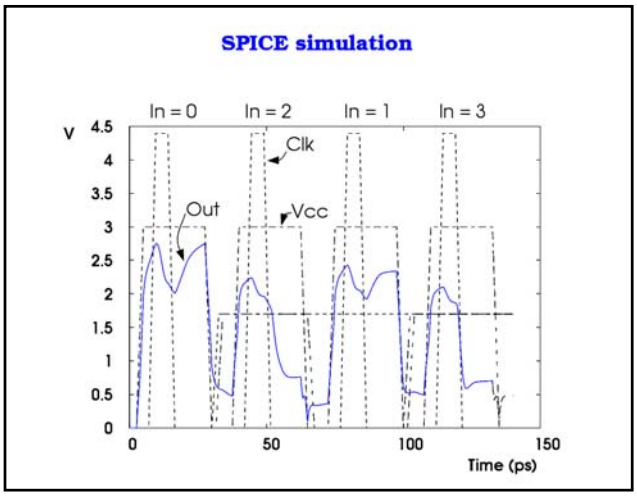

RTL inverter simulation
In
Out1
Out2
V
3
2.5
2
1.5
1
0.5
0
SPICE
Out2
In
Out1
VEDICS
0
50
100
150
200
Time (ps)

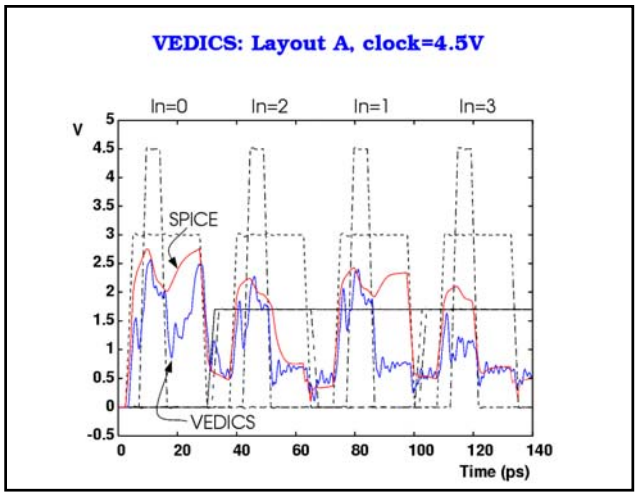

CML buffer gate

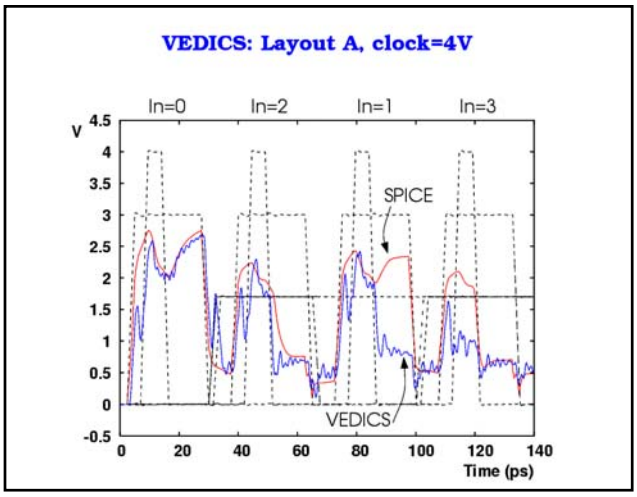

CML buffer simulation
Outbar
Out
In
Inbar
Vee
V
SPICE (dashed)
VEDICS (solid)
Out-Outbar
In-Inbar
Time (ps)

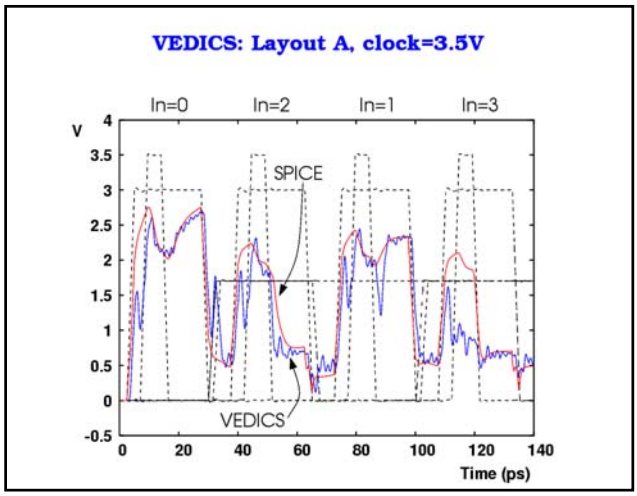

Layout A: closely spaced wirings
Clk
Vcc
In3
In1
Out
In2

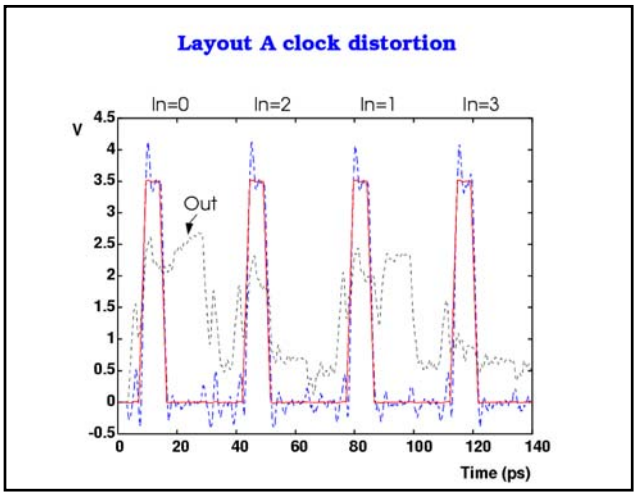

Layout B: widely spaced wirings
Vcc
Clk
In3
In1
Out
In2

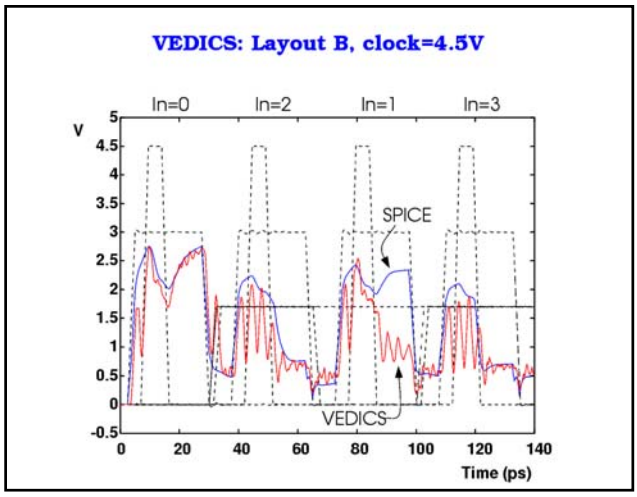

SPICE simulation
In = 0
In = 2
In = 1
In = 3
V
Clk
Out
Vcc
Time (ps)

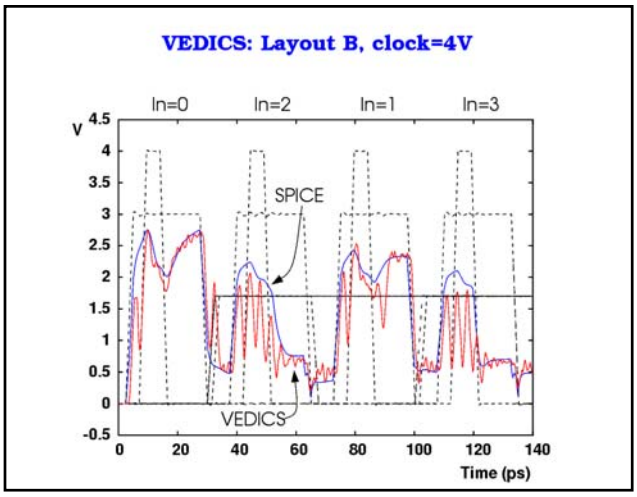

VEDICS: Layout A, clock=4.5V
In=0
In=2
In=1
In=3
V
SPICE
VEDICS
Time (ps)

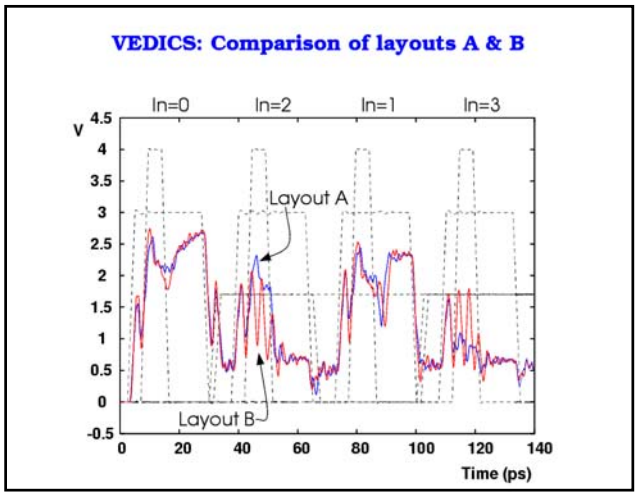

VEDICS: Layout A, clock=4V
In=0
In=2
In=1
In=3
V
SPICE
VEDICS
Time (ps)

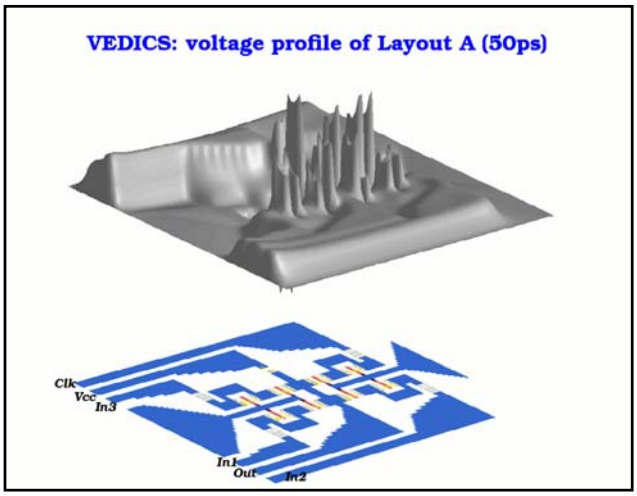

VEDICS: Layout A, clock=3.5V
In=0
In=2
In=1
In=3
V
SPICE
VEDICS
Time (ps)


Layout A clock distortion
In=0
In=2
In=1
In=3
V
Out
Time (ps)


VEDICS: Layout B, clock=4.5V
In=0
In=2
In=1
In=3
V
SPICE
VEDICS
Time (ps)


VEDICS: Layout B, clock=4V
In=0
In=2
In=1
In=3
V
SPICE
VEDICS
Time (ps)


VEDICS: Comparison of layouts A & B
In=0
In=2
In=1
In=3
V
Layout A
Layout B
Time (ps)


VEDICS: voltage profile of Layout A (50ps)
Clk
Vcc
In3
In1
Out
In2

Ultra-Fast Circuit Applications of RTD and HEMT's

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Outline

- **Simulation Environment and Device Model Description**
  - RTD model description and parameters extraction
  - HEMT model description and parameters extraction
- **Design and Simulation of HEMT/RTD based circuits**
  - HEMT-RTD based D-type Flip Flop
    - Circuit configuration and operation principle description
    - Design consideration and simulation results
  - MOBILE-SR Latch based D-type Flip Flop
    - Circuit configuration and operation principle description
    - Design consideration and simulation results
  - HEMT-RTD based Clocked Multiplexer
    - Circuit configuration and operation principle description
    - Design consideration and simulation results
  - MOBILE-SR Latch based Frequency Divider
    - Circuit configuration and operation principle description
    - Design consideration and simulation results
  - Design of QMOS and RTD/HEMT based multi-valued address stretchable decoder
    - Concept and Operation principle of four-valued address stretchable decoder
    - Design Principle and QMOS, RTD/HEMT based circuit structures.
    - Simulation results
- **Conclusion and Future Work**

Simulation Environment and Device Model Description

- **Simulation Environment**
  - QSPICE developed by University of Michigan.
  - Device (RTD/HEMT) models are integrated in QSPICE.
- **Device Model Description**
  - UM RTD model description
    - UM RTD model is based on the RTD envelope function as follows:

$$J(V) = J_1(V) + J_2(V) \qquad J_2(V) = h(e^{\frac{n_2 q V}{kT}} - 1)$$

$$J_1(V) = a \ln\left[\frac{1+e^{(b-c+n_1 V)\frac{q}{kT}}}{1+e^{(b-c-n_1 V)\frac{q}{kT}}}\right] \bullet \left[\frac{\pi}{2} + a\tan\left(\frac{c-n_1 V}{d}\right)\right]$$

    - The RTD capacitance is described by $C_{rtd} = \frac{C_{j0}}{\left(1+\frac{|V|}{V_{bi}}\right)^m}$

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Simulation Environment and Device Model Description

- **Device Model Description**
  - **UM RTD model parameters extraction**
    - UM RTD model parameters are extracted from KAIST RTD I-V Characteristic as well as the measured RTD key parameters with DC supply voltage of 0.8V. Parameters are extracted for unit size RTD with the area given by KAIST model.
    - **Example**: For KAIST RTD model of 2(um)x2(um), UM RTD model parameters are extracted with area=4(umxum). The parameters are shown in the table. The fitting results are shown in Figure 1. Figure 1(a) is the fitting result of UM RTD model v.s. KAIST RTD model. Figure 1 (b) shows the fitting result of UM RTD model v.s. measured RTD DC characteristic.

area	4	n1	2.122024
a	1.469e-5	n2	0.2660
b	0.322732	Cj0	5f
c	0.328346	Rs	29.2
d	0.046344	Vbi	0.0368
h	1.008e-7	m	0.19

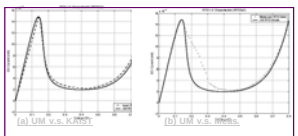

Figure 1: Fitting results of UM RTD model (2x2) with Measured RTD DC I-V characteristic and UM RTD model(2x2) With KAIST RTD(2x2) model

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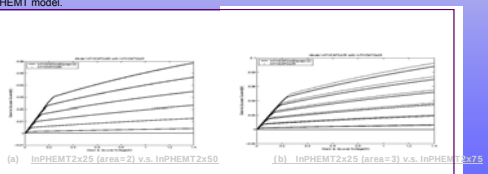
Simulation Environment and Device Model Description

- **Device Model Description**
  - **UM HEMT model description**
    - UM HEMT model is developed by using Statz GaAs MESFET model in QSPICE, the parameters are chosen to fit the DC I-V characteristic of the KAIST InP HEMT model with area of 2x25x01 as well as the measured HEMT DC I-V characteristic.
  - **UM HEMT model parameters extraction**
    - UM HEMT model parameters are extracted from InPHEMT2x25 developed by KAIST because InPHEMT2x25 model fits InPHEMT2x50 model with doubled device size. InPHEMT2x75 model also has no much deviation from InPHEMT2x25 model with triple device size.
    - In circuit design, HEMT size is always less than InPHEMT2x50 to obtain the best accuracy in terms of HEMT model.

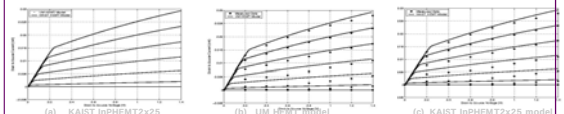


(a) InPHEMT2x25 (area=2) v.s. InPHEMT2x50 (b) InPHEMT2x25 (area=3) v.s. InPHEMT2x75

Figure 2. Verification of InPHEMT2x25 model with InPHEMT 2x50 model and InPHEMT2x75 model

Simulation Environment and Device Model Description

- **Device Model Description**
  - **UM HEMT model parameters extraction**
    - UM HEMT model parameters are extracted from KAIST InPHEMT2x25 model, the parameters are shown in the table.
    - Fitting results of UM HEMT model with KAIST HEMT model, UM HEMT model with measured HEMT DC I-V characteristic as well as KAIST HEMT model with measured HEMT DC I-V characteristic are shown in Figure 3. Since KAIST model is also developed based on Statz MESFET model in HSPICE, the fitting result of UM HEMT model with KAIST HEMT model is perfect.

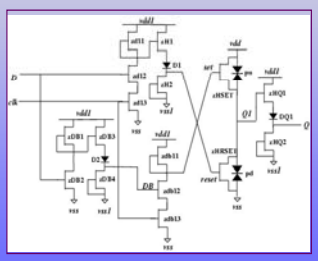


(a) KAIST InPHEMT2x25 model v.s. UM HEMT model (b) UM HEMT model v.s. measured HEMT DC I-V (c) KAIST InPHEMT2x25 model v.s. measured HEMT DC I-V

Fitting results of UM HEMT model with KAIST InPHEMT2x25 model, UM HEMT model with measured HEMT DC I-V characteristic and KAIST InPHEMT2x25 model with measured HEMT DC I-V characteristic.

Design and Simulation of HEMT/RTD based circuits

- **HEMT-RTD based D-type Flip Flop**
  - Circuit configuration and operation principle description



Operation Principle

Clk	D	DB	set	reset	Q
Low→ High	1	0	1	0	1
	0	1	0	1	0
High→ Low	1	0	1	1	Q_{pre}
	0	1	1	1	Q_{pre}

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Design and Simulation of HEMT/RTD based circuits

- **HEMT-RTD based D-type Flip Flop**
  - **Design consideration**
    - The sizing of the paralleled HEMT device in Set-Reset RTD latch is critical to the correct functionality of this circuit
    - The input signal voltage level of Set-Reset RTD Latch is critical to the correct functionality of this circuit
    - Circuit has different device parameters when it operates at 10GHz/20GHz and 40GHz/60GHz
    - Inverted input signal is generated locally
    - Output signal is level shifted to satisfy the cascade requirement
  - **Advantages and Disadvantages of this circuit**
    - **Advantages**
      - **Static HEMT/RTD based DFF, which can keep output voltage level when clock goes low.**
      - **Output Set-Reset Latch increases the output voltage swing.**
      - **Can work at high operation frequency (60GHz) with good output voltage swing (comparable to the input signal logic swing)**
    - **Disadvantages**
      - **Functionality is sensitive to the HEMT device size in Set-Reset RTD Latch as well as the input signal voltage level of the SR RTD Latch**

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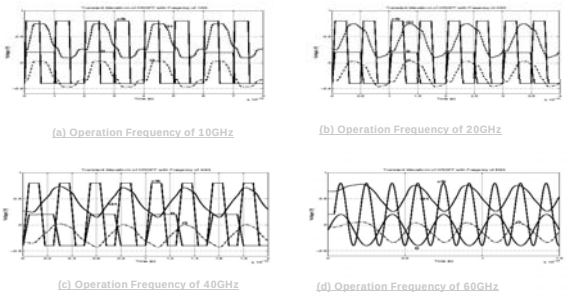
Design and Simulation of HEMT/RTD based circuits

- HEMT-RTD based D-type Flip Flop
  - Circuit Simulation Results

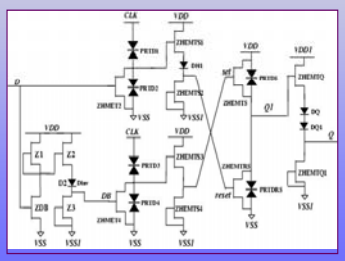


(a) Operation Frequency of 10GHz (b) Operation Frequency of 20GHz

(c) Operation Frequency of 40GHz (d) Operation Frequency of 60GHz

Design and Simulation of HEMT/RTD based circuits

- MOBILE-SR Latch based D-type Flip Flop
  - Circuit configuration and operation principle description



Operation Principle

Clk	D	DB	set	reset	Q
Low→ High	1	0	1	0	1
	0	1	0	1	0
High→ Low	~	~	0	0	Q_{pre}

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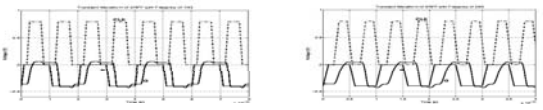
Design and Simulation of HEMT/RTD based circuits

- **MOBILE-SR Latch based D-type Flip Flop**
  - **Design consideration**
    - MOBILE-type circuit is used in sampling stage to increase the output voltage swing at higher operational frequency
    - The improved internal node output voltage swing reduces the HEMT sizing limitation of the last stage Set-Reset RTD Latch.
    - Inverted input signal is generated locally; need to consider the setup time of the MOBILE circuit driven by the inverted input signal.
    - Output voltage level is level shifted to satisfy the cascade requirement
  - **Advantage and Disadvantage**
    - **Advantages**
      - **Static RTD based DFF instead of the return-to-zero mode MOBILE based DFF found in the literature**
      - **High operation frequency due to the ultra-fast switching speed of MOBILE-type circuit**
      - **Increased internal node logic swing**
      - **Sizing is uniform for different operation frequency**
    - **Disadvantages**
      - **Clock load is heavy, which is common to all MOBILE type circuit**

Design and Simulation of HEMT/RTD based circuits

- **MOBILE-SR Latch based D-type Flip Flop**
  - **simulation results**

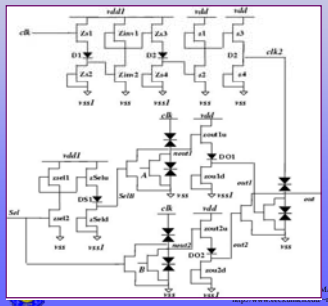


(a) Operation frequency of 10GHz (b) Operation frequency of 20GHz

(c) Operation frequency of 40GHz (d) Operation frequency of 60GHz

Design and Simulation of HEMT/RTD based circuits

- HEMT-RTD based Clocked Multiplexer
  - Circuit configuration and operation principle description



Operation Principle

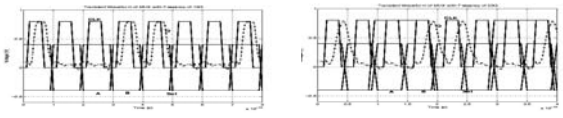
Clk	Sel	SelB	A	B	Q
Low→ High	1	0	~	~	A
	0	1	~	~	B
High→ Low	~	~	~	~	0

Design and Simulation of HEMT/RTD based circuits

- **HEMT-RTD based Clocked Multiplexer**
  - **Design consideration**
    - Basic elements is RTD based NOR gate instead of RTD based NAND gate because of the better performance of RTD based NOR gate at higher operation frequency.
    - Inverted select signal is generated locally, the setup time of the MOBILE-type NOR gate driven by inverted select signal should be satisfied.
    - The setup time of MOBILE type circuit needs to be satisfied, therefore, a delayed clock is generated to guarantee the correct functionality of the last stage MOBILE based NOR gate.
  - **Advantage and Disadvantage of this circuit**
    - **Advantage**
      - **High operation frequency due to the ultra-fast switching speed of the MOBILE-type NOR gate**
      - **Large voltage swing introduced by the RTD pair compared to the pure HEMT circuit**
    - **Disadvantage**
      - **With the increase of the operation frequency, the delayed clock has decreased logic swing which reduce the output voltage swing of this circuit**
      - **Large clock load, which is common to all MOBILE type circuit**

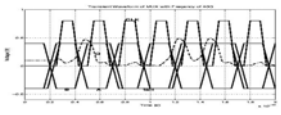
Design and Simulation of HEMT/RTD based circuits

- HEMT-RTD based Clocked Multiplexer
  - simulation results



(a) Operation frequency of 10GHz

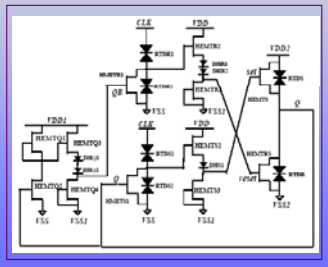
(b) Operation frequency of 20GHz



(c) Operation frequency of 40GHz

Design and Simulation of HEMT/RTD based circuits

- MOBILE-SR Latch based Frequency Divider
  - Configurations and operation principles



Operation Principle

CLK	Qpre	QB	SET	RESET	Qc
L→H	1	0	0	1	0
H→L	0	1	1	0	1

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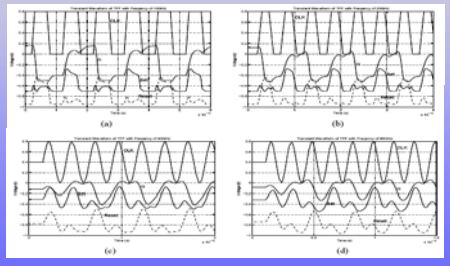
Design and Simulation of HEMT/RTD based circuits

- **MOBILE-SR Latch based Frequency Divider**
  - **Design Considerations**
    - Setup time of MOBILE circuit can be slightly negative.
    - Choose MOBILE-SR latch based DFF as the core circuitry in order to achieve high operation frequency.
    - Minimize the propagation delay while maximize the output voltage swing
    - Redesign the Set-Reset latch such that the output can directly connect to the input gate.
  - **Advantages and Disadvantages**
    - **Advantages**
      - **Only single phase clock is needed to perform correct operation instead of two phase clock reported in literature.**
      - **Output voltage swing is improved by using Set-Reset latch which has the self-latching property.**
      - **Our MOBILE-SR latch based frequency divider can correct operate up to 60GHz while in literature, the reported working frequency is 34GHz**
    - **Disadvantages**
      - **Using MOBILE based circuit which has large power dissipation.**
      - **Using level shifter due to the negative threshold of D-HEMT, which increase the propagation delay.**

Design and Simulation of HEMT/RTD based circuits

- MOBILE-SR Latch based Frequency Divider
  - Simulation Results



Simulation waveform for proposed TFF for operation frequency of (a) 10G, (b) 20G, (c) 40G; (d) 60G.

Conclusion and Future Work

- **Conclusion**
  - RTD/HEMT device model as well as the device parameters extraction results have been described.
  - Three HEMT/RTD based Flip-flops, one RTD/HEMT based clocked multiplexer have been designed and simulated. The design considerations are discussed and the simulation results are shown with various frequencies.
  - We have designed a RTD/HEMT based multi-valued pre-decoder. The different design style are discussed and evaluated.
- **Future work:**
  - FDTLM based RTD/HEMT DFF design and simulation.
  - FDTLM based RTD/HEMT frequency divider design and simulation.
  - Multiplexer and Demultiplexer design using RTD/HEMT devices.
  - Clock recovery circuitry design.
  - RTD based ADC architecture exploration and design.

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On The Implementation of RTD Based CNNs

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Motivation: Wide Applications of CNNs

Real Time Inspection and other Industrial Applications
- Textile or paper fault detection
- Rail inspection from high-speed train
- Detection of debris particles in oil flow
- High Speed Inspection during production
- Agricultural products - grains fruits and vegetables inspection/classification
- Visual sensors in robot control
- Speed and displacement measurement

Automotive Applications
- Collision avoidance
- Air bag control
- Smart rearview mirror
- Live spark plug inspection
- Quality Control

Medical Applications
- Real-time 2D/3D echocardiography

Entertainment and Household
- Vision toys and games
- Intelligent lighting
- TV image enhancement
- Eye sensor
- Magic eyeglasses

Security and Defense
- Multi-target tracking
- Night vision
- Missile guidance/targeting
- Automatic target detection

Signal Processing
- Optimization of narrow-bandwidth data transmission systems
- On-the-fly analog video signal processing
- CAC in ATM switching

CNN v.s. Other Signal Processors

	MOPS /mm²	GOPS/W	Processor Type	Technology
Microprocessor DECchip 21064	1.72	0.013	High performance 64-bit and floating point RISC µP	0.7um CMOS
DSP TI TMS320C80	5.85	0.16	superscalar/VLIW processors	0.6um CMOS
Pixel parallel processor	64.1	9.34	Bit-serial PE from a massively parallel SIMD processor array	0.6um CMOS
CNNUM	81.8	4.37	Single cell from the CNNUM array with gray scale I/O	0.8um CMOS

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Talk Outline

- **RTD based CTCNN**
  - Operation principle
  - Analysis of circuit design
  - Simulation results
- **MOBILE based DTCNN**
  - Operation principle
  - Cell for horizontal line detection (HLD)
  - Cell for connected component detection (CCD)

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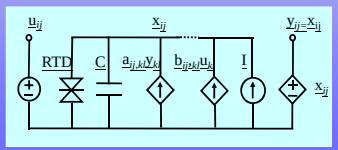
CTCNN Cell Model

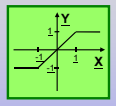
Chua's model

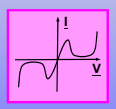
$$C\frac{dX_{ij}(t)}{dt} = -\frac{X_{ij}(t)}{R} + \sum_{C(k,l)\in N_r(i,j)} (AY_{kl} + BU_{kl}) + I$$

RTD model

$$C\frac{dX_{ij}(t)}{dt} = -h(X_{ij}(t)) + \sum_{C(k,l)\in N_r(i,j)} (AX_{kl} + BU_{kl}) + I$$







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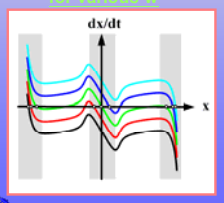
2 or 3 Equilibrium States

$$C\frac{dx_{ij}(t)}{dt} = \left[-h(x_{ij}(t)) + a_{ij,ij}x_{ij}(t)\right] + w$$

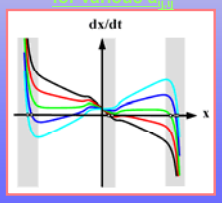
$$w = \sum_{C(k,l)\in N,\,(i,j)} b_{ij,kl}u_{kl} + I$$

Driving point plots

for various w



for various $a_{ij,ij}$



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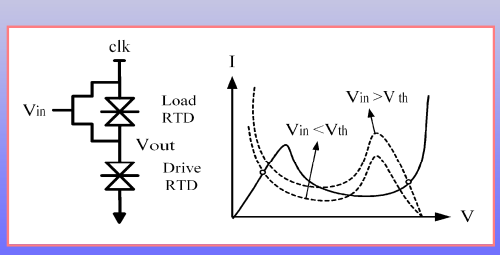
RTD Quantizer (1 bit A/D)

V_{th} can be designed by sizing load and drive RTDs



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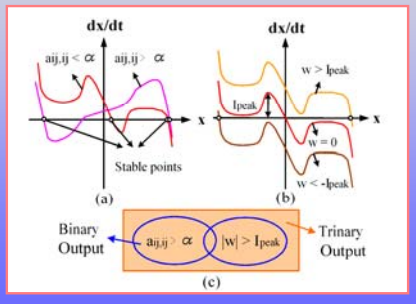
Criteria for Binary Output

α: 1st partial differential resistance of RTD
I_{peak}: peak current of RTD



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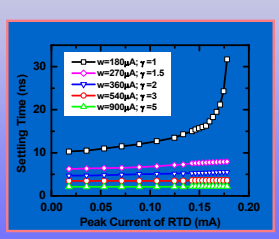
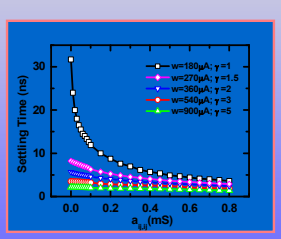
Settling Time

γ : w/ I_{peak}

S. T. ↑ as I_{peak} ↑ (g → 1)

S. T. ↑ as $a_{ij,ij}$ ↓ (especially for g = 1)





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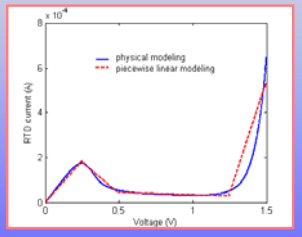
Mathematical Modeling



$$h(x)=\begin{cases} a_0x & 0<x<0.25V, \quad a_0>0 \\ b_0+b_1x & 0.25<x<0.5V, \quad b_0>0, \quad b_1<0 \\ c_0+c_1x & 0.5<x<1.25V, \quad c_0>0, \quad c_1<0 \\ d_0+d_1x & 1.25<x, \quad d_0>0, \quad d_1>0 \end{cases}$$

Unit	A		A/V
a_0	0	a_1	6.96e-4
b_0	2.95e-4	b_1	-4.84e-4
c_0	5.41e-5	c_1	-2.27e-6
d_0	-2.96e-3	d_1	2.41e-3

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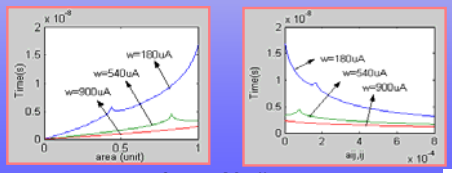
NDR

Settling Time Modeling

$$t=\left(\frac{C}{a_{ij,ij}-d_1}\right)*\ln\left[\frac{x_{ij}-\left(\frac{d_0-w}{a_{ij,ij}-d_1}\right)}{1.25-\left(\frac{d_0-w}{a_{ij,ij}-d_1}\right)}\right]+\left(\frac{C}{a_{ij,ij}-c_1}\right)*\ln\left[\frac{1.25-\left(\frac{c_0-w}{a_{ij,ij}-c_1}\right)}{0.5-\left(\frac{c_0-w}{a_{ij,ij}-c_1}\right)}\right]$$
$$+\left(\frac{C}{a_{ij,ij}-b_1}\right)*\ln\left[\frac{0.5-\left(\frac{b_0-w}{a_{ij,ij}-b_1}\right)}{0.25-\left(\frac{b_0-w}{a_{ij,ij}-b_1}\right)}\right]+\left(\frac{C}{a_{ij,ij}-a_1}\right)*\ln\left[\frac{0.25-\frac{w}{a_1-a_{ij,ij}}}{\frac{w}{a_{ij,ij}-a_1}}\right]$$



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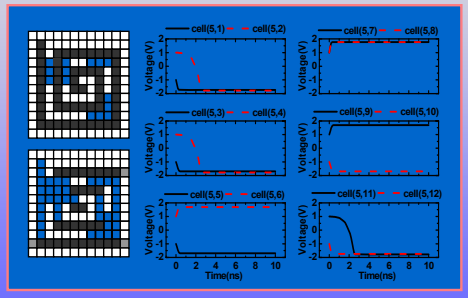
Horizontal Line Detection (HLD)

Binary input
White : -1
Dark : 1

$C=1pF$

$$A=\begin{bmatrix}0&0&0\\0&2&0\\0&0&0\end{bmatrix}mA \qquad B=\begin{bmatrix}0&0&0\\1&1&1\\0&0&0\end{bmatrix}mA$$

$I=-1mA$



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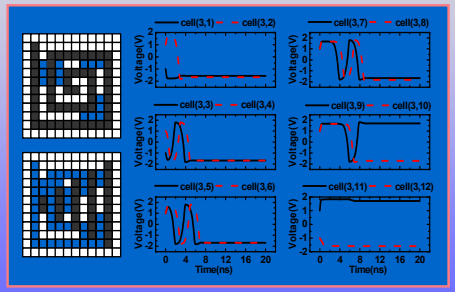
Horizontal Connected Component Detection (HCCD)

Binary input
White : -1
Dark : 1

$C=1pF$

$$A=\begin{bmatrix}0&0&0\\1&2&-1.2\\0&0&0\end{bmatrix}mA \qquad B=\begin{bmatrix}0&0&0\\0&0&0\\0&0&0\end{bmatrix}mA$$

$I=0mA$



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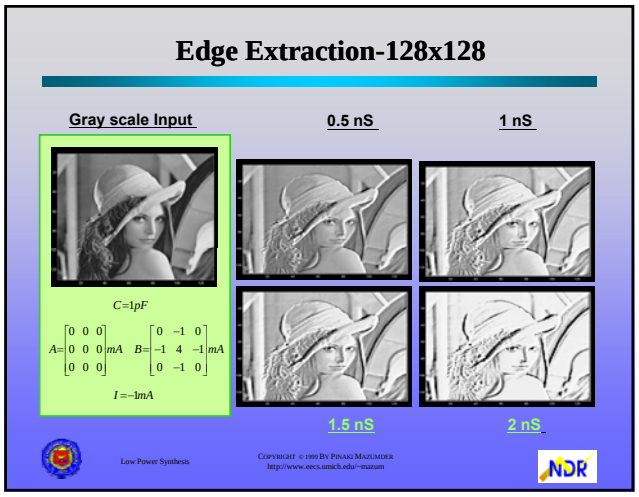
Edge Extraction-128x128
Gray scale Input
0.5 nS
1 nS
C=1pF
A=[0 0 0; 0 0 0; 0 0 0]mA
B=[0 −1 0; −1 4 −1; 0 −1 0]mA
I=−1mA
1.5 nS
2 nS
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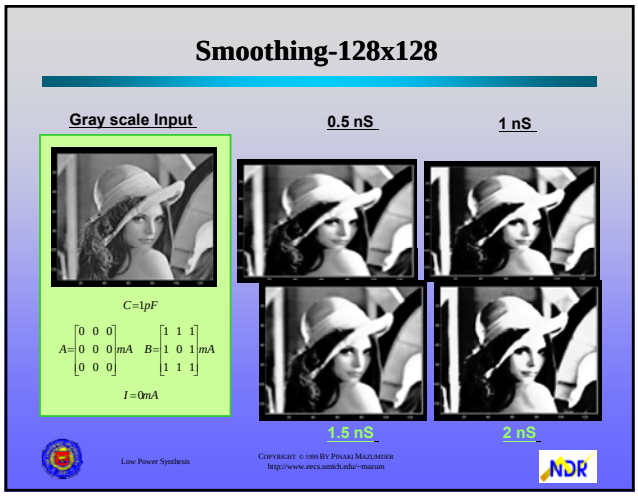
Smoothing-128x128
Gray scale Input
0.5 nS
1 nS
C=1pF
A=[0 0 0; 0 0 0; 0 0 0]mA
B=[1 1 1; 1 0 1; 1 1 1]mA
I=0mA
1.5 nS
2 nS
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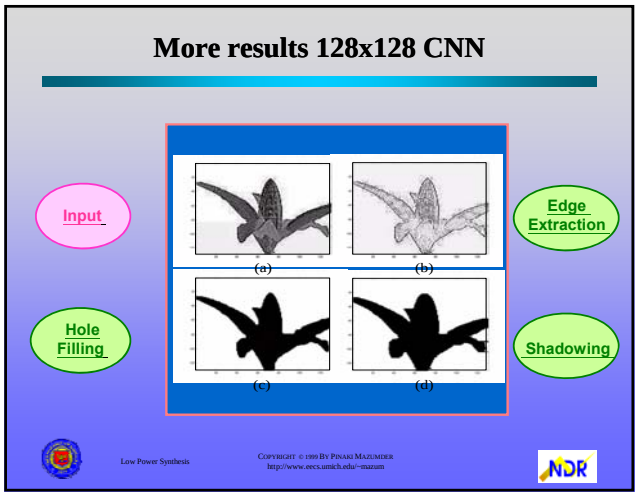
More results 128x128 CNN
Input
Hole Filling
Edge Extraction
Shadowing
(a)
(b)
(c)
(d)
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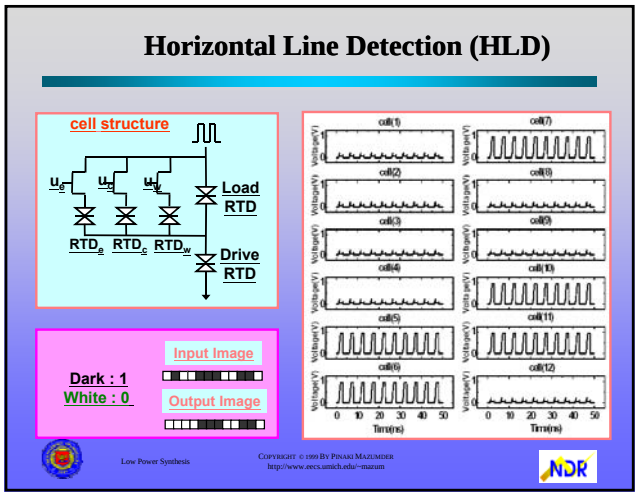
Horizontal Line Detection (HLD)
cell structure
Load RTD
Drive RTD
RTDe RTDc RTDw
Dark : 1
White : 0
Input Image
Output Image
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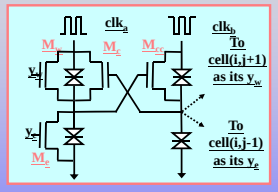
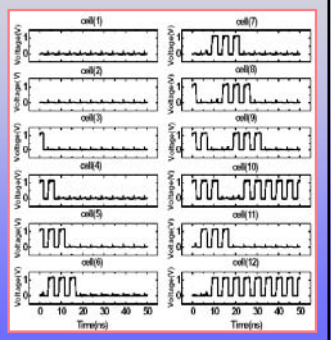
Horizontal Connected Component Detection (HCCD)





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Conclusion

- RTD based CNN has excellent performance in terms of density, speed.
- Two new and compact MOBILE cell structures for HLD and HCCD operations are proposed.
- Several image processing functions are successfully verified through SPICE simulation.

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On the Functional Failure and Switching Time Analysis of the MOBILE Circuit

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GSRA: S.R. Li
May 25, 2005
Presented at ISCAS

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Outline

- Motivation
- Review the operation principle of MOBILE
  - Proposed new circuit model
- Functional failure analysis
  - Analytical solution
  - Model based on SPICE simulation
- Switching time analysis
  - Optimal clock's rising time
- Conclusion

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Motivation—Analysis of MOBILE

- Construction of MOBILE circuits
  - a pair of series connected RTD's and transistors
- Advantages
  - High speed
    - high electron mobility and small intrinsic capacitance of RTD
  - Compact and functional
    - Negative differential resistance of RTD
- Disadvantages
  - Limited fan-out / low driving capability
    - High sensitivity to loading effect

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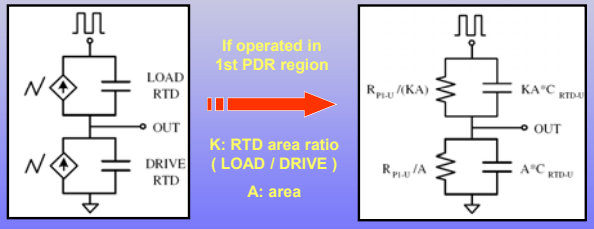
Operation of An Ideal RTD Pair



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An Ideal RTD Pair (con't)

To find $V_{OUT}(t)$, apply KCL theorem:

$$KA * C_{RTD-U} * \frac{d(V_{CLK}(t)-V_{OUT}(t))}{dt} + \frac{V_{CLK}(t)-V_{OUT}(t)}{R_{P1-U}/(KA)} = A * C_{RTD-U} * \frac{dV_{OUT}(t)}{dt} + \frac{V_{OUT}(t)}{R_{P1-U}/A}$$

$V_{CLK}(t)=S*t$
S: slew rate = VDD/T_{RS}

$$\frac{dV_{OUT}}{dt} + \frac{V_{OUT}}{C_{RTD-U}R_{P1-U}} = \frac{K}{K+1}S\left(1 + \frac{t}{C_{RTD-U}R_{P1-U}}\right)$$

$$V_{OUT}(t) = \frac{K}{K+1}St$$

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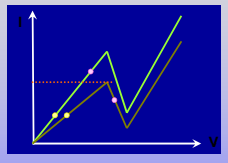
An Ideal RTD Pair (con't)



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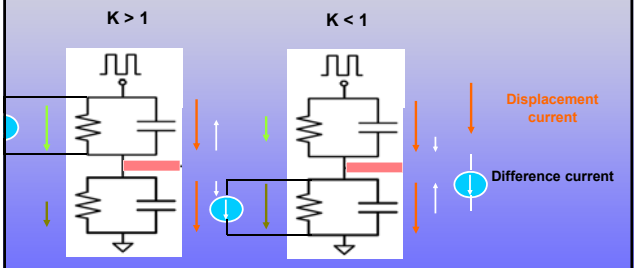
An Ideal RTD Pair (con't)



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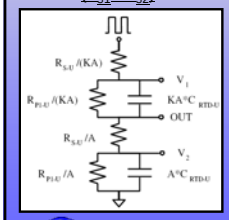
Functional Failure : An RTD-Pair w/ contact resistance R_S

- Charging speed depends on time constant R_SC
- Max. displacement current ~ $V_{CLK}/(R_{S1}+R_{S2})$



$$KA * C_{RTD-U} * \frac{d(V_1 - V_{OUT})}{dt} + \frac{V_1 - V_{OUT}}{R_{P1-U}/(KA)} = A * C_{RTD-U} * \frac{dV_2}{dt} + \frac{V_2}{R_{P1-U}/A} = \frac{V_{CLK} - V_1}{R_{S-U}/(KA)} = \frac{V_{OUT} - V_2}{R_{S-U}/A}$$

$(V_1 - V_{OUT}) / V_2 = 1 / K$

$$\frac{dV_2}{dt} + \frac{1}{C_{RTD-U}}\left[\frac{1}{R_{P1-U}} + \frac{1}{R_{S-U}}\right] V_2 = \frac{K}{K+1}\frac{St}{R_{S-U}}$$

$$V_2 = \frac{KS}{K+1}\frac{C_{RTD\_U}^2 R_{P1\_U}^2 R_{S\_U}}{(R_{P1\_U} + R_{S\_U})^2}\left(e^{-\frac{R_{P1\_U}+R_{S\_U}}{C_{RTD\_U} R_{P1\_U} R_{S\_U}}t} - 1\right) + \frac{KS}{K+1}\frac{C_{RTD\_U} R_{P1\_U}}{R_{P1\_U} + R_{S\_U}}t$$

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Functional Failure : An RTD-Pair w/ contact resistance R_S

- Failure criteria: both RTD's are still in 1st PDR region @ t =T_{RS}
- Using voltage dividing theorem,

$$V_{DD}\left(\frac{\frac{R}{A}\|\frac{1}{sAC}}{\frac{Rs}{A}+\frac{Rs}{KA}+\frac{R}{KA}\|\frac{1}{sKAC}+\frac{R}{A}\|\frac{1}{sAC}}\right) < V_P \qquad \frac{V_{DD}}{(1+\frac{1}{K})(1+R_{S\_U}(\frac{C_{RTD\_U}}{T_{RS}}+\frac{1}{R_{P1\_U}}))} < V_P$$

For T_{RS} > 1 ps,

$$R_{S\_U,critical} \approx R_{P1\_U}\left[\frac{V_{DD}}{(1+\frac{1}{K})V_P} - 1\right]$$

For T_{RS} < 1 ps,

$$R_{S-U,critical} \approx \frac{T_{RS}}{C_{RTD\_U}}\left[\frac{V_{DD}}{(1+\frac{1}{K})V_P} - 1\right]$$

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Functional Failure : An RTD-Pair w/ load C_L

- Sources of C_L
  - Gate cap at the following stage
  - Drain-to-bulk and Source-to-bulk junction cap of parallel connected transistors
- Location of C_L
  - Output to GND or Output to CLK
- Impact
  - Depending on the MOBILE configuration, may help or impair output evaluation due to additional displacement current in C_L

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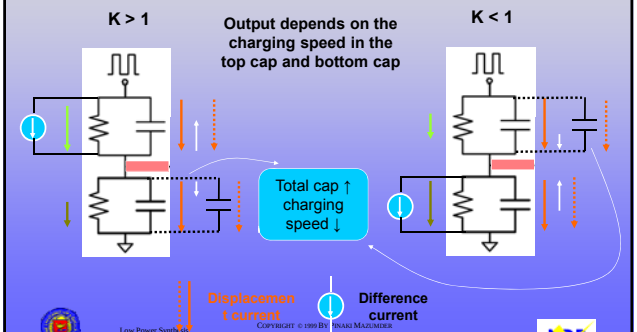
Functional Failure : An RTD-Pair w/ load C_L



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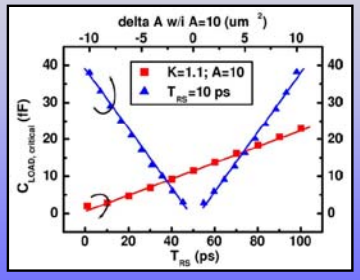
Functional Failure : An RTD-Pair w/ load C_L



Factors that govern the charging speed :
1. Size of loading cap
2. Displacement current level (VDD / TRS)
3. Difference current level (area ratio K or delta A)

Loading effect cap must be smaller than a critical value to ensure

$$C_{LOAD,critical} = 0.218A|K-1| * T_{RS} \quad (fF)$$

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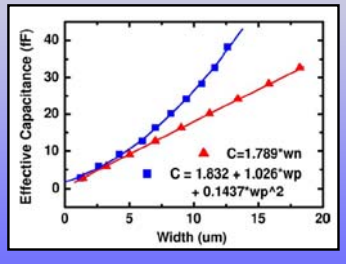
C_L Extraction from FET's



Procedure:
1. One FET is in parallel with the bottom RT
2. Input signal is low (FET is off)
3. Fix K, A, T_{RS}
4. Find the critical width leading to functional failure
5. Map the critical width to the corresponding critical loading cap w/i such K, A, T_{RS}

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Maximum Size of FET's

Observation:
1. Effective loading cap of FET's is independent of length (junction cap of D-B or S-B)
2. Linear relationship in N-FET; Nonlinear in P-FET (asymmetric process and biasing condition for P/N-FET's)

Model of max. width of FET's (K>1, FET at bottom):

$$wn_{max} = \frac{0.81A(K-1)}{1.798} * \frac{T_{RS}}{10p} \ (um)$$

$$wp_{max} = 3.57\left[\left(1 - \frac{0.81A(K-1)}{1.798} * \frac{T_{RS}}{10p}\right)^{0.5} - 1\right] \ (um)$$

Model of max. width of FET's for K<1, FET at top can be obtained using similar procedure

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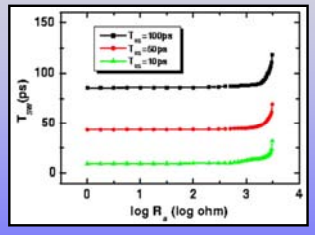
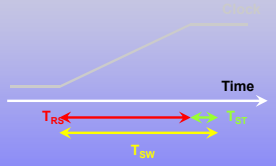
Switching Time : An RTD-Pair w/ contact resistance R_S





Observation: Rs has little impact with normal process (Rs<2 KΩ)
Model of switching time for T_{RS} >10 ps:

$$T_{SW} = 0.9T_{RS} + 0.017 * \exp\frac{\log R_{S\_U} + \log(K+1/1.91K) - 2.637}{0.12}$$

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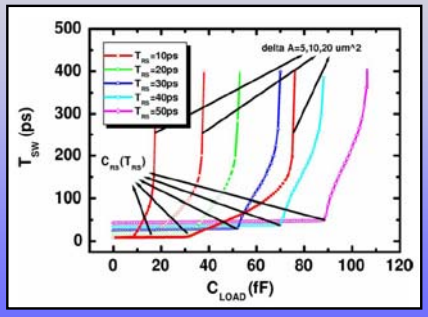
Switching Time: An RTD-Pair w/ load C_L



Factors determining the charging speed:
1. loading cap
2. T_{RS}
3. delta A

For red lines, T_{RS} is fixed.

For color lines, delta A is fixed.

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Switching Time: An RTD-Pair w/ load C_L

- Observation
  - For T_{RS} fixed, the curves have the same waveform, but expanded in the x-axis with a factor proportional to delta A
  - For delta A fixed, waveforms are different for different T_{RS}
  - The onset point (denoted as C_{RS}) of the rapid growth of T_{RS} is roughly proportional to delta A (T_{RS} fixed) or T_{RS} (delta A fixed)
  - There exists a minimal T_{SW} (T_{ST}=0; T_{SW}= T_{RS}) for a certain MOBILE configuration (given K, A, C_{LOAD})
- Model

$$T_{SW} = 0.9T_{RS} \quad if\ C_{LOAD} < C_{RS}$$
$$T_{SW} = 0.9T_{RS} + f(T_{RS}, C_{LOAD}/\delta)\ if\ C_{RS} < C_{LOAD} < C_{LOAD,critical}$$

$$C_{RS} = 18.4\delta\alpha\ (fF),\quad \delta = |K-1|A/10,\quad \alpha = T_{RS}/10p$$

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Conclusion

- The operation principle of MOBILE circuits has been revisited with the proposed model and observation.
- Contact resistance under normal process is not a big issue.
- Functional failure depends on the charging and discharging speed of the caps due to the displacement current and the difference current.
- For a given MOBILE configuration, there is an optimal clock's rising time that leads to minimum switching time.

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