IEICE TRANS. ELECTRON., VOL.E82–C, NO.9 SEPTEMBER 1999

PAPER *Special Issue on Integrated Electronics and New System Paradigms*

Design and Analysis of Resonant-Tunneling-Diode (RTD) Based High Performance Memory System

Tetsuya UEMURA[†a)] ***and*** **Pinaki MAZUMDER**[††], ***Nonmembers***

SUMMARY A resonant-tunneling-diode (RTD) based sense amplifier circuit design has been proposed for the first time to envision a very high-speed and low-power memory system that also includes refresh-free, compact RTD-based memory cells. By combining RTDs with n-type transistors of conventional complementary metal oxide semiconductor (CMOS) devices, a new quantum MOS (Q-MOS) family of logic circuits, having very low power-delay product and good noise immunity, has recently been developed. This paper introduces the design and analysis of a new QMOS sense amplifier circuit, consisting of a pair of RTDs as pull-up loads in conjunction with n-type pull-down transistors. The proposed QMOS sensing circuit exhibits nearly 20% faster sensing time in comparison to the conventional design of a CMOS sense amplifier. The stability analysis done using phase-plot diagram reveals that the pair of back-to-back connected static QMOS inverters, which forms the core of the sense amplifier, has meta-stable and unstable states which are closely related to the I-V characteristics of the RTDs. The paper also analyzes in details the refresh-free memory cell design, known as tunneling static random access memory (TSRAM). The innovative cell design adds a stack of two RTDs to the conventional one-transistor dynamic RAM (DRAM) cell and thereby the cell can indefinitely hold its charge level without any further periodic refreshing. The analysis indicates that the TSRAM cell can achieve about two orders of magnitude lower stand-by power than a conventional DRAM cell. The paper demonstrates that RTD-based circuits hold high promises and are likely to be the key candidates for the future high-density, high-performance and low-power memory systems.

key words: *resonant-tunneling diode, DRAM, sense amplifier, instability, refresh-free*

1. Introduction

The present large demand for high-speed and low-power memory systems has mainly fueled by the explosive growth of large-scale computing and communication systems. Over the past few decades, device dimensions have progressively diminished using the well-known device scaling law in order to meet the increasing needs for higher computing and communication speeds as well as lower energy consumption of pervasive communication and portable electronic systems. Memory devices, especially dynamic random access memories (DRAMs), owing to the tiny size of its memory cell consisting of a vertically integrated capacitor and a pass transistor, define the cutting edge of the VLSI technology. Taking advantages of device scaling, the DRAM industry has relentlessly quadrupled the memory chip size every three years or so, since their first introduction in the early 1970's. The DRAM chip integration density has recently reached the gigabit mark and is projected to grow to 64 Gbits before the device scaling reaches its final limits somewhere near 2010 [1].

This growth potential of DRAM chips, however, is possible if the industry can grapple with the concomitant problems of rising chip power consumption and diminishing improvement in chip access time. As the density of integration increases, the accompanying increase in RC delays of longer bit and word lines reduce the memory read/write access times. Also, larger memory chips with billion transistors require significantly more energy consumption for cell refreshing. Furthermore, increased junction leakage currents associated with deeper sub-micron CMOS technology not only increases the refresh power dissipation of a gigabit DRAM chip, but it also mandates the use of more reliable cells with higher storage capacitance.

Since these are intrinsic problems of CMOS technology emanating from progressive device scaling, alternative avenues must be explored to incorporate radical changes in the existing CMOS technology as well as to design new circuit configurations that may obviate cell refreshing and compensate for increasing interconnect delays. Quantum effect devices are envisioned as a viable solution to these two formidable problems that stand as roadblocks for the future growth of DRAM chips. These devices have extremely fast switching speed and fold-back I-V characteristics owing to electron tunneling through quantum barriers. These two features can be utilized to design ultra-fast and complex digital gates which use less active devices and can perform pipelining at the gate level due to the bistability of quantum devices. Though a large number of quantum effect devices have been proposed by the device researchers, resonant tunneling diodes (RTDs) have gained much attention because of their compatibility with many conventional technologies such as HBTs, HEMTs, HFETs and MOSFETs. Such RTD-based emerging technologies hold tremendous potential for dramatic improvements in VLSI circuits [2].

Recently, Wagt, et al. proposed a revolutionizing

Manuscript received January 20, 1999.
Manuscript revised March 16, 1999.

[†]The author is with the Fundamental Research Laboratories, NEC Corporation, Tsukuba-shi, 305-8501 Japan.
[††]The author is with the Department of Electrical Engineering and Computer Science, The University of Michigan, MI, USA.
a) E-mail: uemura@frl.cl.nec.co.jp

DRAM cell design, called tunneling SRAM (TSRAM), consisting of a pair of RTDs to store the cell information. RTDs, connected in tandem, can hold the charge level of the cell indefinitely replenishing continually the charge loss caused by the cell leakage currents, like the weak inversion current, field current and dark current. Unlike in DRAM cell design, where capacitors are dynamically and periodically refreshed through highly capacitive bit lines, TSRAM cells do not require separate refreshing, and thereby the power consumption of a TSRAM memory chip is considerably lower than a DRAM chip employing external or auto-refreshing [3]. In this paper, a novel RTD-based sense amplifier circuit, called a quantum MOS (QMOS) sense amplifier, is also proposed and its operation is analyzed and verified through SPICE simulation. The sense amplifier is shown to have better response time than a pure CMOS sense amplifier. Finally, the paper demonstrates how by combining RTDs with CMOS devices, low-power and high-speed memory system can be built.

2. RTD-Based Memory System

Figure 1 represents the proposed RTD-based memory system, consisting of QMOS sense amplifier and TSRAM cell. In the TSRAM, a pair of negative differential resistance (NDR) devices ($N3$ and $N4$), such as RTDs or Esaki tunneling diodes (TDs), with their current densities comparable to the cell leakage current, is added between access transistor ($M7$) and storage capacitance (C_S) [3]. The QMOS sense amplifier is formed by the cross-coupled inverter latch. It consists of the RTD pull-up loads ($N1$ and $N2$), NMOS transistors ($M1$ and $M2$), and switching transistors ($M5-M8$). The bit-line pair is connected to the drain of $M1$ and $M2$.

2.1 Stand-by Mode

In the stand-by mode, each cell is isolated from the bit line. As shown in Fig. 2, the cell voltage stored in the cell capacitor is latched at either V_H or V_L, which corresponds to logic *'high'* and *'low,'* respectively. In the diagram, i_A and i_B indicate the currents through $N3$ and $N4$, respectively, and i_l is the cell leakage current. Because of this bistable property, the cell can indefinitely hold its information and consequently the memory array does not require any periodic refreshing as is required in conventional DRAM chips. In order to reduce the stand-by power consumption, the currents through both $N3$ and $N4$ should be held as low as possible. The current drive capabilities of $N1$ and $N2$, on the other hand, should be as large as those of the $M1$ and $M2$ transistors, because the sense amplifier circuit should drive the bit-line pair quickly.

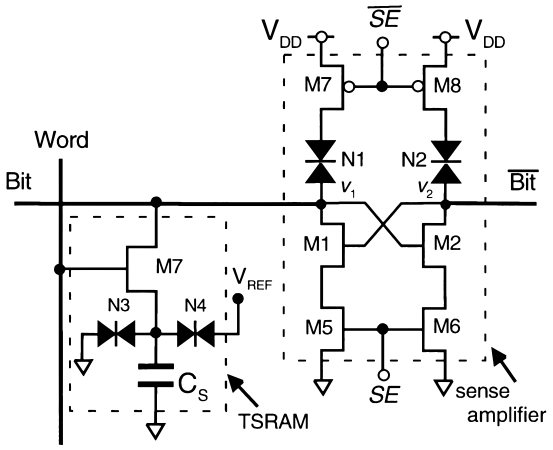


Fig. 1 Proposed RTD-based memory system.

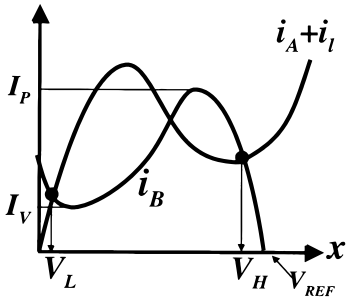


Fig. 2 Load line diagram of TSRAM cell.

2.2 READ/WRITE Operation

In the *READ* operation, the bit lines are precharged to half-V_{DD}. When the access transistor ($M7$), turns *ON*, charge sharing between the bit-line and the accessed cell induces a small voltage difference between the BIT and $\overline{BIT}$ nodes. Once the voltage difference is established, control signals (SE and $\overline{SE}$), activate the cross-coupled latch, and the small voltage difference is amplified to push the BIT voltage to either V_{DD} or 0, depending on the sign of initial voltage difference. Although the stored data is destroyed due to the charge sharing, it is restored by the sense amplifier like in a normal DRAM read operation. The RTD-pair circuit in the TSRAM has no influence on this *READ* operation, because the current drive capability of $N3$ and $N4$ is much smaller than the drive capabilities of the access transistor and the sense amplifier circuit.

In the *WRITE* operation, the input data is written to the cell through the access transistor by charging the bit line connected to the selected cell to either $V_H + V_T$ or $V_L - V_T$, depending on the input data, where V_T is the threshold voltage of the access transistor. The RTD pair circuit, $N3$ and $N4$, has no influence on the *WRITE* operation.

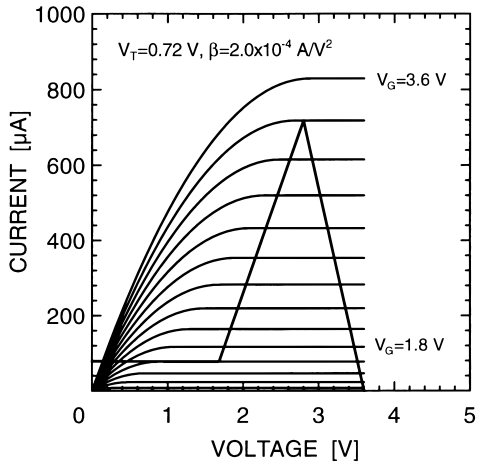


Fig. 3 Load line diagram for QMOS inverter circuit.

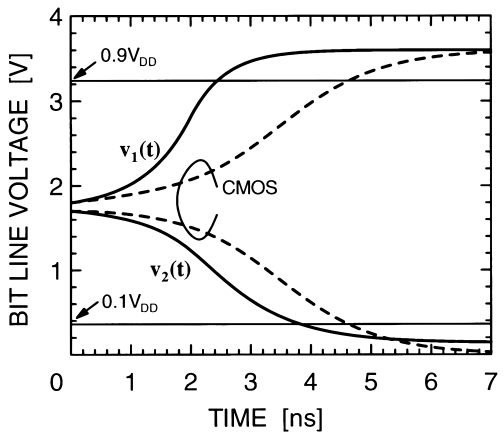


Fig. 4 Simulation results for QMOS and CMOS sense amplifier circuit.

3. Analysis of RTD-Based Memory System

In this section, the circuit performance of the RTD-based memory system is analyzed in detail and compared with the conventional DRAM system.

3.1 Operation Speed

As described in the previous section, the RTD pair circuit has no influence on the READ/WRITE operation. Hence, the access time is determined mainly by the time needed for charging/discharging of the bit line through its sense amplifier. Figures 3 and 4 show a load line diagram of a QMOS inverter used for this analysis, and the SPICE simulation result of sensing time of the coupled QMOS inverter, respectively. The RTDs with $I_P = 718\,\mu$A, $V_P = 0.8\,$V, $I_V = 77.4\,\mu$A, $V_V = 1.92\,$V, and $V_{SEC} = \infty$, and the NMOS transistors with $\beta = 2.0 \times 10^{-4}\,$A/V^2 and $V_T = 0.72$, are used, where the I_P, V_P, I_V, V_V, and V_{SEC} represent a peak current, a peak voltage, a valley current, a valley voltage and a second peak voltage for the RTD characteristics, respectively. The β and V_T denote the gain and threshold voltage, respectively, for the NMOS transistor. The initial value of the bit line voltage is 1.8 V and 1.7 V, and its capacitance is assumed to be 0.5 pF.

The dashed line in Fig. 4 indicates the sensing time of CMOS sense amplifier shown for the comparison. The NMOS characteristics are assumed to be the same in the both sense amplifier circuits. The PMOS characteristics of the CMOS sense amplifier is assumed to be symmetric to the NMOS characteristics ($\beta_P = \beta_N$, $V_{TP} = -V_{TN}$). The sensing time, defined as a time at which both conditions $v_1 > 0.9V_{DD}$ and $v_2 < 0.1V_{DD}$ are simultaneously satisfied, is about 20% faster than that of the CMOS. Since the RTD, as a pull-up load device, can drive more current than an equivalent PMOS load device, the sensing time improves in the Q-MOS sense amplifier. As the current drive capability of the pull-up load is larger, the charging time of the bit-line capacitance becomes shorter. This fast charging time induces the reduction of discharging time of other bit-line capacitance also, because the NMOS transistor of the discharging circuit quickly turns ON due to the cross-coupled connection.

Another improvement of speed performance in this system comes from the refresh-free operation due to the TSRAM configuration. Unlike in memory chips that require periodic refreshing, in TSRAM the *READ/WRITE* operation can be done at any time.

3.2 Stand-by Power Consumption

Since the switching transistors, $M5 - M8$, inactivate the cross-coupled latch during the stand-by mode, the sense amplifier circuit consumes no static power. The static power of the TSRAM cell, on the other hand, is determined by the cell leakage current and latching current. As shown in Fig. 2, in order to guarantee the bistability, the peak currents of $N3$ and $N4$ should be satisfied by the condition given by:

$$I_P > I_V + I_l, \tag{1}$$

where I_P and I_V are the peak and valley currents of $N3$ and $N4$, and I_l is the cell leakage current. Here the latching current of the RTDs is assumed to be I_V. Because of their extremely small sizes, DRAM cells are very sensitive to chip defects. As the density of DRAM increases, the chip yield could be very low. Let γ be the ratio between the maximum cell leakage current (I_l^{max}) and the average leakage current (I_l). The value of γ as high as 50 were reported in the 16 Mb DRAM, although the fraction of the *bad* cell is as small as 10^{-6} [4]. Since Eq. (1) should be satisfied for all cells, the valley current should be larger than the I_V^{min}, which is given by,

$$I_V^{min} = \frac{\gamma}{PVCR - 1} I_l, \tag{2}$$

where $PVCR$ is the peak-to-valley-current-ratio of the RTDs. The stand-by power per cell is given by,

$$\begin{aligned} P_{TSRAM} &= (I_V + I_l)V_{DD} \\ &= \left(\frac{\gamma}{PVCR-1}+1\right) I_l V_{DD} \end{aligned} \quad (3)$$

3.2.1 Comparison with DRAM

The most significant difference between the TSRAM and DRAM is the stand-by operation. The DRAM needs a repeated refresh operation to hold the cell information, while the TSRAM has no refresh operation due to the data latching by RTD circuit. In this section, power consumption of the DRAM refresh operation and that of the TSRAM stand-by operation are compared.

As shown in the Appendix, the power consumption of the DRAM due to the refresh operation is given by,

$$P_{DRAM} = \frac{1}{t_R}(C_B + C_S)V_{DD}\left(\frac{1}{2}V_{DD}, -\Delta v\right) \quad (4)$$

where t_R is the cell retention time, Δv is the bit-line voltage change due to charge sharing. When the detection limit of the sense amplifier circuit, V_r, is ideally 0, the above equation simply becomes

$$P_{DRAM} = \gamma\left(1+\frac{C_B}{C_S}\right) I_l V_{DD} \quad (5)$$

As γ increases, the power for both DRAM and TSRAM increases almost linearly. The ratio between P_{DRAM} and P_{TSRAM} is proportional to the C_B/C_S as well as the $PVCR$. Because of the factor, C_B/C_S, which is typically more than 10, the P_{DRAM} becomes much larger than the P_{TSRAM}. In other words, one of the reasons for larger power consumption in DRAM emerges from the fact that it necessitates charging the bit line having much larger capacitance than a cell for each refresh operation. The increase in the $PVCR$ value also increases the power ratio, P_{DRAM}/P_{TSRAM}.

Furthermore, when V_r has a finite value, the power, P_{DRAM} increases, resulting in larger power ratio. Figure 5 shows the comparison between power consumptions in TSRAM (Eq. (3)) and in DRAM (Eq. (4)) as a function of V_r, when $V_{DD} = 3.6\,\mathrm{V}$, $C_S = 27\,\mathrm{fF}$, $C_B = 270\,\mathrm{fF}$, $I_l = 1\,\mathrm{fA}$, and $\gamma = 50$. The P_{DRAM} is normalized by the $P_{TSRAM} = 0.048$ pW. The $PVCR$ of TSRAM is assumed to be 5. Despite the value of P_{DRAM} is slightly underestimated in the calculation, it is still about two orders of magnitude higher than the power consumption of a TSRAM, in the practical V_r range ($\simeq 0.1$ V).

It should be noted that considering the effect of variation in the RTD currents, the power consumption of the TSRAM is increased. This variation can be treated as an increase of the γ value in Eq. (3). The power consumption increases almost linearly against the γ. However, the redundancy cell scheme, which is widely used in the recent high density DRAM, can avoid a significant increase of γ value.

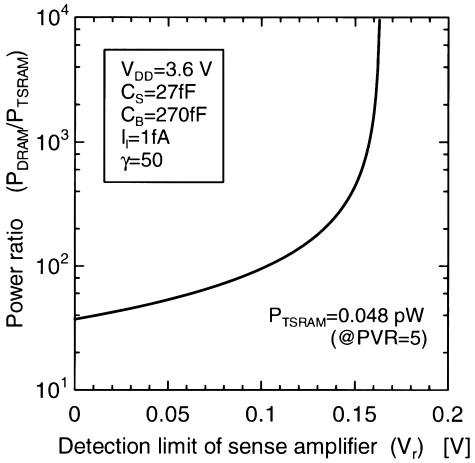


Fig. 5 Comparison of power consumption for the DRAM and TSRAM.

3.3 Stability

The sense amplifier detects the small bit-line voltage difference and accordingly pushes the bit-line voltage to V_{DD} or 0 V, as shown in Fig. 4. The sensing time as well as the convergence value are sensitive to the initial conditions. In this section, the stability of the QMOS sense amplifier against the fluctuation of initial bit-line voltage is discussed by using phase diagram.

The circuit equation of Fig. 1 during the sensing is given by

$$C_B\frac{dv_1}{dt} = I_{RTD}(V_{DD}-v_1) - I_{TR}(v_2, v_1) \quad (6)$$

$$C_B\frac{dv_2}{dt} = I_{RTD}(V_{DD}-v_2) - I_{TR}(v_1, v_2) \quad (7)$$

where C_B is the bit-line capacitance, v_1 and v_2 are BIT and $\overline{BIT}$ voltages. The $I_{RTD}(v)$ and $I_{TR}(v_g, v_{ds})$ indicate the current-voltage characteristics of the RTDs ($N1$ and $N2$) and the NMOS transistors ($M1$ and $M2$), respectively, which are given by

$$I_{RTD}(v) = \begin{cases} \frac{I_P}{V_P}v & (0 \le v < V_P) \\ I_P - \frac{I_P - I_V}{V_V - V_P}(v - V_P) & (V_P \le v < V_V) \\ I_V + \frac{I_P - I_V}{V_{SEC} - V_V}(v - V_V) & (V_V \le v) \end{cases} \quad (8)$$

and

$$I_{TR}(v_g, v_{ds}) = \begin{cases} 0 & (v_g < V_T) \\ \beta[(v_g - V_T)v_{ds} - v_{ds}^2/2] & (v_{ds} < v_g - V_T) \\ \frac{\beta}{2}(v_g - V_T)^2 & (v_{ds} \ge v_g - V_T) \end{cases} \quad (9)$$

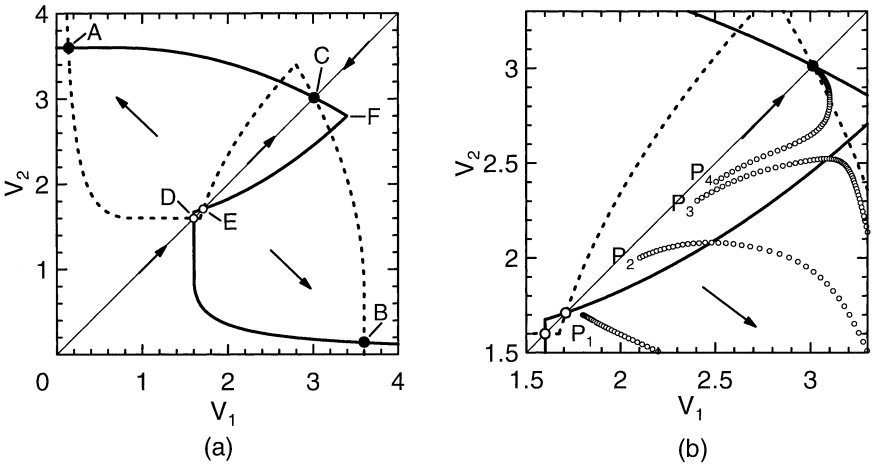


Fig. 6 Voltage transfer characteristics of QMOS inverter pair.

where the I_P, V_P, I_V, V_V, and V_{SEC} represent the peak current, the peak voltage, the valley current, the valley voltage and the second peak voltage for the RTD characteristics, respectively. The β and V_T are gain and threshold voltages, respectively, for the NMOS transistor.

Figure 6 shows voltage transfer characteristics (VTC) of each inverter. The solid and dashed VTC lines indicate the solution for $dv_2/dt = 0$ and $dv_1/dt = 0$, respectively. The intersection points, therefore, represent the equilibrium points of Eqs. (6) and (7). Unlike the CMOS sense amplifier, the QMOS sense amplifier circuit has three stable points (A, B, and C), one metastable point (D), and one unstable point (E), due to its Z-shaped VTC, as shown in Fig. 6.

The solution of Eqs. (6) and (7) for a given initial condition is discussed using phase diagram. The dotted lines in Fig. 6(b) indicate the trajectory curves of Eqs. (6) and (7) for different initial conditions. From the point $P_1(1.8, 1.7)$, where $dv_1/dt > 0$ and $dv_2/dt < 0$, the solution directly goes to the stable point B (Fig. 4). From $P_2(2.0, 1.9)$ or $P_3(2.4, 2.3)$, where both dv_1/dt, and dv_2/dt, > 0, the trajectory once goes upward, and when it reaches to the solid VTC curve, it turns to the downward, resulting in going to the point B. When it starts from the point $P_4(2.5, 2.4)$, however, the solution reaches to the dashed VTC curve, resulting in convergence to the point C, exhibiting an erroneous operation of the sense amplifier.

This erroneous behavior can be controlled by optimizing the RTD parameters. If the point F on the solid VTC curve, corresponding to the peak position of RTD characteristics, is moved closer to the line of $v_2 = v_1$, the instability is reduced. The v_1 and v_2 values at point F, which is determined by the peak current and voltage of the RTD characteristics, are given by

$$v_1|_F = V_T + \sqrt{\frac{2I_P}{\beta}}$$

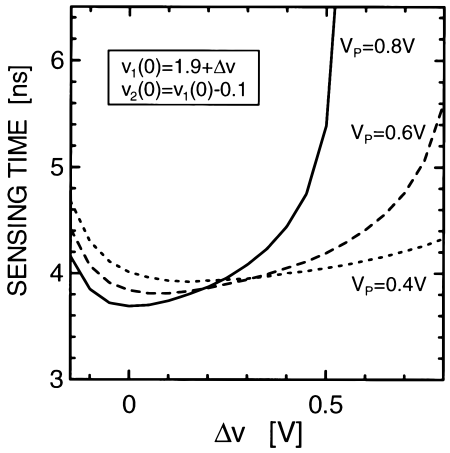


Fig. 7 Initial voltage fluctuation dependence of the sensing time.

$$v_2|_F = V_{DD} - V_P \tag{10}$$

From the above equations, when I_P is decreased, the point F is moved to left. When V_P is decreased, on the other hand, the point F is moved upward. Therefore, the decrease of I_P and/or V_P can reduce the instability. Figure 7 shows an initial condition dependence of the sensing time for three different peak voltage values (V_P =0.8, 0.6, and 0.4 V). The initial condition for $v_1(t)$ and $v_2(t)$ are assumed to be,

$$\begin{aligned} v_1(0) &= v_2(0) + 0.1 \\ v_2(0) &= V_{DD}/2 + \Delta v \end{aligned} \tag{11}$$

where Δv indicates the voltage fluctuation during the bit-line precharge cycle. As shown in Fig. 6 (b), when Δv equals to 0.6 V at $V_P = 0.8$ V, which corresponds to the point P_4 in Fig. 6 (b), the sensing time becomes infinity due to the erroneous operation. Figure 7 indicates that the reduction of V_P can increase the normal operation margin against the initial voltage fluctuation without degrading the sensing speed.

3.4 Memory Cell Capacitor

One of the most critical challenges which gigabit density DRAM designers confront now is the memory cell capacitance. Memory cell capacitance is a critical parameter that determines the sensing signal voltage, sensing speed, data retention time, and vulnerability for soft error. From Eq. (A· 3) and Eq. (A· 4) in the Appendix, the minimum capacitance value, C_S^{min}, is given by,

$$C_S^{min} = \frac{V_r C_B + I_l t_R}{V_{DD}/2 - V_r} \tag{12}$$

Because of the lower supply voltage and increased junction leakage current due to high doping density, the higher memory cell capacitance will be needed in the gigabit density DRAMs [1].

The TSRAM cell can alleviate the cell capacitor limitation to some extent. The required minimum cell capacitance of the TSRAM cell is independent of the cell leakage current, and is given by

$$C_{S\,TSRAM}^{min} = \frac{V_r C_B}{V_{DD}/2 - V_r} \tag{13}$$

This condition shows that the bit-line voltage shift due to charge sharing during a *READ* operation should be larger than the detection limit of the sense amplifier. In addition, the intrinsic capacitance of $N3$ and $N4$ also works as a node capacitance.

3.5 Cell Area

Disadvantages of the TSRAM include slight increase in cell area and the addition of one extra bias line in the cell layout. Since the current level needed for the RTDs is small, the area could be reduced by adjusting the peak current density. For example, in order to obtain the peak current density of 0.1 pA, which is about 100 times larger than the typical cell leakage current, the RTD with its peak current density of 10^{-3} A/cm^2 occupies only a 0.01 μm^2. The area of the RTD is limited by the size of the contact hole. By forming the RTD pairs on the drain region of the access transistor, the cell area becomes minimum. Since the TSRAM cell needs a contact between upper RTD and power supply (V_{REF}) and a contact between lower RTD and cell plate in addition to the bit-line contact, the word line contact, and the cell capacitance contacts, the theoretical limitation of the cell area is estimated to be $10\lambda^2$, where λ is the minimum technological feature size. An example of the TSRAM cell layout is shown in Fig. 8. The area of TSRAM cell is larger than that of the DRAM whose theoretical lower bound is $6\lambda^2$ (open bit-line scheme). However, recent needs for high cell capacitance in the gigabit density DRAMs tends to increase the cell area from their theoretical bounds. Therefore, the difference for both cell areas is not significantly large.

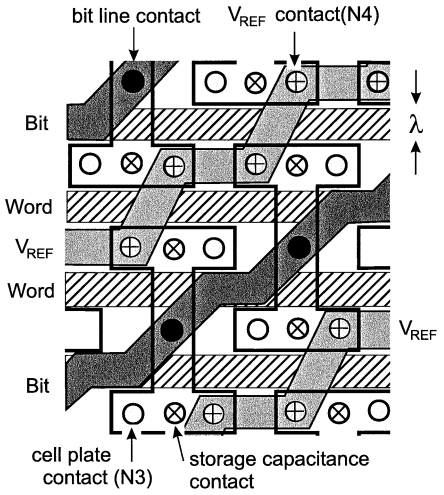


Fig. 8 Cell layout of TSRAM.

3.6 RTD Configuration

In our RTD-based memory system, two kinds of RTDs with different current densities are necessary. The current density of the RTD used in the TSRAM cell should be as low as possible to reduce the stand-by power consumption, while that in the sense amplifier should be as large as possible to increase the sensing speed. The fabrication of two kinds of RTDs at different places, however, induces an area penalty, which in particular is a serious problem in the TSRAM cell design. In this section, we would like to briefly discuss how to integrate two kinds of RTDs without increasing the area. Since the RTD is a vertical transport device, several RTDs can be stacked vertically. In this system, the RTD with smaller current density should be stacked on that with larger current density. In the sense amplifier circuit, where the lower-side RTD is used, the upper-side RTD is removed to make contact directly to the lower-side RTD. In the TSRAM cell, on the other hand, where the upper-side RTD is used for the data latching, the contact is made to the upper-side RTD. Because of much higher current density of the lower-side RTD, this lower-side RTD works as a resistor with low value.

4. Conclusion

This paper demonstrates the design, analysis and simulation of a novel QMOS sense amplifier circuit consisting of RTD pull-up loads and NMOS transistors. Compared to the conventional CMOS sense amplifiers, the QMOS design exhibits about 20% higher sensing speed due to the larger current drive capability of the RTD load. The instability against the initial condition has been analyzed by drawing phase plot diagram. It has been found that by reducing the peak current and/or

peak voltage of the RTDs instability problem can be circumvented.

In addition to a novel sense amplifier design, the paper also analyzes the power consumption of a refresh-free TSRAM cell in comparison with the power budget of a DRAM cell that needs periodic refreshing. The stand-by power consumption of the TSRAM was derived theoretically with reference to the DRAM cell dissipation, and it was observed that the TSRAM cell power consumption was about two orders of magnitude lower than DRAM. Further, because of its refresh-free nature, the TSRAM does not suffer from the high cell capacitance requirement. Due to increased junction leakage current in deep sub-micron CMOS technologies, DRAM cells require larger capacitances to optimize the design between cell stability, power consumption, cell area, soft error rate, etc. Since RTDs can be vertically integrated and can hold the charge level indefinitely, TSRAM design methodology may alleviate the critical cell design problems in the future multi-gigabit DRAM chips.

In order to meet the increasing needs for higher speeds and lower power budget in portable computing and communication systems, quantum-MOS (QMOS) technology with low power-delay product and high noise immunity may provide a viable solution. QMOS combines the integration level of CMOS technology with the bistable latching property of a tunneling device and thereby it can be employed for gigabit memory technology. Conventional CMOS technology is confronting major impediments in the design of high-performance and low-power DRAM chips. These roadblocks are due to the intrinsic limitations of the CMOS technology and a viable solution lies in developing a CMOS-based new technology that can radically change the conventional circuit design principle. The paper reveals the promises of QMOS being one such viable technology that can be co-integrated with the existing CMOS technology for enhancing the horizon of VLSI technology to 50-nm scaling.

References

[1] K. Kim, C-G. Hwang, and J.G. Lee, "DRAM technology perspective for Gigabit era," IEEE Trans. Electron Devices, vol.45, pp.598–608, 1998.
[2] P. Mazumder, S. Kulkarni, M. Bhattacharya, J.P. Sun, and G.I. Haddad, "Digital circuit application of resonant tunneling devices," Proc. IEEE, vol.86, pp.664–686, 1998.
[3] P. van der Wagt, A. Seabaugh, and E. Beam III, "RTD/HFET low standby power SRAM gain cell," 1996 IEDM Tech. Dig., pp.425–428, 1996.
[4] H. Yamauchi, T. Suzuki, A. Sawada, T. Iwata, T. Tsuji, M. Agata, T. Taniguchi, Y. Odake, K. Sawada, T. Ohnishi, M. Fukumoto, T. Fujita, and M. Inoue, "A 20 ns battery-operated 16 Mb CMOS DRAM," 1993 ISSCC Tech. Dig., pp.44–45, 1993.

Appendix A: Refresh Operation

In this appendix, the power dissipation due to the refresh operation of DRAM is analyzed. The refresh operation is made by repeatedly performing forced *READ* operations. Each forced *READ* refreshes all cells connected to the same word line. The cell retention time is limited by the cell leakage current of the worst cell. Let t_R be the cell retention time, which is given by

$$t_R = \frac{C_S}{I_l^{max}}(V_{DD} - V_R^{min}) \tag{A·1}$$

where V_R^{min} is the minimum cell voltage when the access transistor is *ON*. The bit-line potential change due to the charge redistribution is given by

$$\Delta v_0 = \frac{C_S}{C_S + C_B}\left(V_R^{min} - \frac{1}{2}V_{DD}\right) \tag{A·2}$$

Here it is assumed that the bit-line pair is initially precharged to $V_{DD}/2$. This charge sharing requires the power dissipation in the access transistor. From the condition that $\Delta v_0 > V_r$, where V_r is the detection limit of the sense amplifier, the V_R^{min} in the above equation is given by

$$V_R^{min} = \frac{1}{2}V_{DD} + \frac{C_S + C_B}{C_S}V_r \tag{A·3}$$

The node voltage and bit-line potential change of the normal cell with its leakage current of I_l, then, become

$$\begin{aligned} V_R &= V_{DD} - \frac{I_l}{C_S}t_R \\ &= V_{DD} - \frac{1}{\gamma}(V_{DD} - V_R^{min}) \end{aligned} \tag{A·4}$$

and

$$\Delta v = \frac{C_S}{C_S + C_B}\left(V_R - \frac{1}{2}V_{DD}\right), \tag{A·5}$$

respectively. After charge sharing occurs, the sense amplifier is activated, resulting that the bit line and cell node are charged from $1/2V_{DD} + \Delta v$ to V_{DD}, while the $\overline{\text{bit line}}$ is discharged from $1/2V_{DD}$ to 0. During this (dis)charging process, the sense amplifier dissipates some power.

At the end of the previous active cycle, one bit line is at V_{DD} and the other is at 0 V. Turning on the equalization device, which shorts two bit-line halves together, induces the charge sharing between the bit lines, resulting in an initial precharge level at nearly half V_{DD}. The cell voltage is reduced to V_R due to the cell leakage current. Table A·1 summarizes the voltage value for the cell, bit line, and $\overline{\text{bit line}}$ at each stage.

The total power dissipation comprises of dissipations due to the access transistor during charge sharing

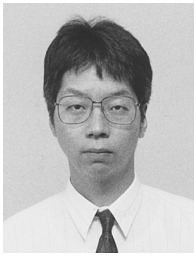
Table A· 1 Voltage value for the cell and bit-line pair.

	cell	bit line	$\overline{\text{bit line}}$
initial	V_R	$\frac{1}{2}V_{DD}$	$\frac{1}{2}V_{DD}$
charge sharing	$\frac{1}{2}V_{DD}+\Delta v$	$\frac{1}{2}V_{DD}+\Delta v$	$\frac{1}{2}V_{DD}$
sensing	V_{DD}	V_{DD}	0
precharging	V_R	$\frac{1}{2}V_{DD}$	$\frac{1}{2}V_{DD}$

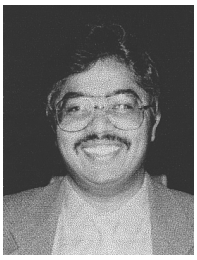
process, the sense amplifier circuit during the charging/discharging the bit lines, the equalization transistor during the precharging cycle, and the cell itself due to the leakage current. It is equal to the power drawn from the power supply during the bit-line charging. In order to estimate this value, we assume an ideal case, in which all the current from the power supply is used to charge the bit-line. Under this condition, the power drawn from the power supply is given by

$$\begin{aligned} P_{DRAM} &= \frac{1}{t_R}\int_0^T V_{DD} i(t)dt \\ &= \frac{1}{t_R}(C_B+C_S)V_{DD}\int_{V_{DD}/2+\Delta v}^{V_{DD}} dv \quad (\text{A}\cdot 6) \\ &= \frac{1}{t_R}(C_B+C_S)V_{DD}\left(\frac{1}{2}V_{DD}-\Delta v\right) \end{aligned}$$

where T is the sensing time, $i(t)$ is the charging current flowing from the power supply. From this equation, the Eq. (4) is obtained. And when the V_r is equals to 0, the Eq. (5) is obtained.



Tetsuya Uemura received his B.E., M.E., and Ph.D. degrees in electronic engineering from Kyoto University, Kyoto, Japan, in 1988, 1990, and 1996, respectively. He joined NEC Corporation, Japan, in 1990. During 1997–1998, he worked at the Department of Electrical Engineering and Computer Science of the University of Michigan, Ann Arbor, as a visiting researcher. His current interests are quantum effect devices and their circuit application. Dr. Uemura is a member of the Japan Society of Applied Physics.



Pinaki Mazumder received the Ph.D. degree from the University of Illinois at Champaign, USA in 1987. Presently, he is with the Department of Electrical Engineering and Computer Science of the University of Michigan, Ann Arbor as a Professor. He worked at various places that include BEL, India and AT&T Bell Labs in USA, and he spent his sabbatical leave (1996–97) as a visiting faculty at Stanford University, University of California at Berkeley, and Nippon Telegraph and Telephone Corporation, Japan. His research interests include VLSI testing, physical design automation, and ultrafast circuit design. He has published over 100 papers on these topics in archival journals and proceedings of the international conferences. He is the co-author of two books — *"Testing and Testable Design of High-Density Random Access Memories,"* Kluwer Academic Publishers, and *"Genetic Algorithms for VLSI Design, Layout and Test Automation,"* Prentice Hall, 1999. He is a Fellow of IEEE and member of Sigma Xi, Phi Kappa Phi, and ACM SIGDA.