

# On Circuit Techniques to Improve Noise Immunity of CMOS Dynamic Logic

Li Ding, *Member, IEEE*, and Pinaki Mazumder, *Fellow, IEEE*

**Abstract**—Dynamic CMOS logic circuits are widely employed in high-performance VLSI chips in pursuing very high system performance. However, dynamic CMOS gates are inherently less resistant to noises than static CMOS gates. With the increasing stringent noise requirement due to aggressive technology scaling, the noise tolerance of dynamic circuits has to be first improved for the overall reliable operation of VLSI chips designed using deep submicron process technology. In the literature, a number of design techniques have been proposed to enhance the noise tolerance of dynamic logic gates. An overview and classification of these techniques are first presented in this paper. Then, we introduce a novel noise-tolerant design technique using circuitry exhibiting a negative differential resistance effect. We have demonstrated through analysis and simulation that using the proposed method the noise tolerance of dynamic logic gates can be improved beyond the level of static CMOS logic gates while the performance advantage of dynamic circuits is still retained. Simulation results on large fan-in dynamic CMOS logic gates have shown that, at a supply voltage of 1.6 V, the input noise immunity level can be increased to 0.8 V for about 10% delay overhead and to 1.0 V for only about 20% delay overhead.

**Index Terms**—Digital integrated circuits, domino logic style, dynamic circuits, negative differential resistance, noise-tolerant design.

## I. INTRODUCTION

DIGITAL integrated circuit noise has become one of the foremost issues in the design of very deep submicron VLSI chips [1], [2]. Noise in digital integrated circuits refers to any phenomenon that causes the voltage at a node to deviate from its nominal value. While these noises always existed, in the past they had little impact on the performance of integrated circuits and were often neglected. It is the unstopped aggressive technology scaling in an effort to continuously improve chip performance and integration level that makes noise play an increasingly important role in comparison with conventional design metrics like area, speed, and power consumption.

Together with technology scaling, aggressive design practices like employing dynamic logic styles have also seen wider use in recent years to achieve higher performance of integrated circuits. Circuits designed using dynamic logic styles can be considerably faster and more compact than their static CMOS counterparts. This is especially the case with wide fan-in dynamic logic gates where a single gate can realize the logic function that otherwise would require multiple levels of static CMOS

logic gates. Therefore, wide fan-in dynamic gates are routinely employed in performance-critical blocks of high-performance chips, such as in microprocessor, digital signal processor, and so on.

Criticism on dynamic circuits is often related to their relatively poor noise tolerance. The switching threshold voltage of a dynamic CMOS logic gate, defined as the input voltage level at which the gate output changes state, is usually the transistor threshold voltage  $V_T$ . In comparison, the switching threshold voltage of static CMOS logic gate is typically around half the supply voltage. Therefore, dynamic logic gates inherently have less noise immunity than static CMOS logic gates and are the weak link in a high-performance VLSI chip designed using deep submicron process technology.

A number of design techniques have been developed in the past two decades in an effort to reinforce this weak link. For example, feedback keepers were proposed to prevent the dynamic node from floating; internal nodes were precharged to eliminate the charge sharing problem; and weak complementary p-network is constructed to improve the noise tolerance to the level of skewed static CMOS logic gates. However, existing remedial techniques improve dynamic circuit noise tolerance at a significant cost in terms of one or more other important design metrics like circuit area, speed, and power consumption. The fact is that the amount of overhead increases dramatically when the noise tolerance requirement is increased along with the continuous down-scaling of the process technology. Therefore, effective noise-tolerant design techniques that incur little overhead in silicon area, circuit speed and power consumption are highly demanded.

In this paper, we propose a novel design method to enhance the noise tolerance of dynamic circuits. We will show that dynamic logic gates are not necessarily less noise tolerant if proper noise-tolerant design techniques are employed. In fact, using the proposed method in this paper, noise tolerance of dynamic logic circuits can be improved beyond the level of static CMOS logic gates while still retain their advantage in performance. Furthermore, in contrast to most previous papers which describe only one new circuit in a paper, the proposed noise-tolerant design method can be realized using a number of different circuits and therefore having broader impact.

The rest of this paper is organized as follows. Section II briefly explains various noises sources in dynamic logic circuits designed using deep submicron process technology. Section III presents an extensive overview and classification of existing noise-tolerant design techniques. In Section IV, the proposed noise-tolerant design method is described. The noise margin

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The authors are with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109 USA (e-mail: ld@eecs.umich.edu; mazum@eecs.umich.edu).

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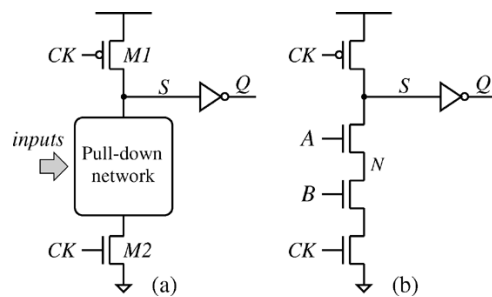


Fig. 1. Domino logic gate. (a) Circuit schematic. (b) Two-input AND gate.

and delay of dynamic circuits using the proposed technique are analyzed in Section V. In Section VI, experimental results on wide fan-in domino gates based on HSPICE simulation are presented.

## II. NOISES IN DYNAMIC LOGIC CIRCUITS

For ease of presentation, in this paper our discussion will be focused on one type of dynamic circuits known as domino CMOS logic circuits [3], which is probably the most widely used dynamic logic style. However, it is noted that the noise-tolerant design techniques discussed in this paper can also be applied to other types of dynamic circuits.

A typical n-type domino CMOS logic gate, as shown in Fig. 1(a), consists of clock controlled transistors  $M1$  and  $M2$ , a pull-down n-type transistor network, and an output driver. The operation of a domino CMOS logic gate can be divided into two phases. In the *precharge* phase when the clock  $CK$  is low, the dynamic node  $S$  is charged to logic high through  $M1$  and the output of the gate  $Q$  is low. The *evaluation* phase starts when the clock goes high. In this phase,  $M1$  is OFF and  $M2$  is ON. The dynamic node  $S$  discharges or retains its charge depending on the inputs to the pull-down network. An example 2-input domino AND gate is illustrated in Fig. 1(b).

Noise sources in dynamic logic circuits can be broadly classified into two basic types: i) gate internal noises, including charge sharing noise, leakage noise, and so on and ii) external noises, including input noise, power and ground noise, and substrate noise.

- 1) Charge sharing noise is caused by charge redistribution between the dynamic node and the internal nodes of the pull-down network. Charge sharing reduces the voltage level at the dynamic node causing potential false switching of a dynamic logic gate.
- 2) Leakage noise refers to the possible charge loss in the evaluation phase due to subthreshold leakage current. Leakage current increases exponentially with respect to transistor threshold voltage, which is continuously being down-scaled as the power-supply voltage reduces. Therefore, leakage in transistors can be a significant source of noise in wide dynamic logic gates designed using very deep submicron process technology.
- 3) Input noise refers to noise presented at the inputs of a logic gate. They are primarily caused by the coupling effect, also known as crosstalk, among adjacent signal wires. This type of noise has become a prominent source

of failures for deep submicron VLSI circuits because of the aggressive interconnect scaling in the lateral dimensions with relatively unchanged vertical dimensions.

- 4) Power and ground noise is mainly caused due to the parasitic resistance and inductance at the power and ground networks and at the chip package. Power and ground networks can also be contaminated by external noises from chip pins. Besides obviously reducing gate noise margin due to possibly lowered supply voltage, the power and ground voltage mismatch between a driver gate and a receiver gate can translate to a dc noise at the input of the receiver.
- 5) Substrate noise can affect the signal integrity of a logic gate through substrate coupling. Furthermore, since transistor threshold voltage is a function of the substrate voltage, noise in the substrate can momentarily lower the threshold voltage of the transistors in the pull-down network rendering them more susceptible to other noises.

In all, those noises, together with other sources of disturbance like process variation, alpha particle radiation, and so on, can endanger the correct function of dynamic logic circuits designed using very deep submicron process technology. And a desired noise-tolerant design technique should be able to improve the noise immunity of dynamic logic gates against all aforementioned noises.

## III. OVERVIEW OF PREVIOUS WORKS

In the past two decades, a number of circuit techniques have been developed with a view to improve the noise immunity of dynamic CMOS logic gates. While it is impractical to include every technique in the literature, in this section we present an overview of some significant techniques. And we have classified those techniques into four main categories based on the principle of their operations: 1) using keeper; 2) precharging internal nodes; 3) raising source voltage; and 4) constructing complementary p-network.

### A. Employing Keeper

Perhaps the simplest way to enhance the noise tolerance of dynamic CMOS logic gates is to employ a weak transistor, known as keeper, at the dynamic node as shown in Fig. 2. The keeper transistor supplies a small amount of current from the power-supply network to the dynamic node of a gate so that the charge stored in the dynamic node is maintained. In the original domino dynamic logic work [3], the gate of the pMOS keeper is tied to the ground, as shown in Fig. 2(a). Therefore, the keeper is always on. Later, feedback keepers, illustrated in Fig. 2(b), became more widely used because they eliminate the potential dc power consumption problem using the always-on keeper in the evaluation phase of domino gates [4].

The use of keeper causes contention when the pull-down network is ON during the evaluation phase, resulting in slower overall gate performance. In wide fan-in gates designed using very deep submicron process technology, the large leakage current through the n-network necessitates a very strong keeper to retain the voltage at the dynamic node. To reduce the serious

contention problem associated with the strong keeper, new keeper design techniques have been recently proposed by Anis

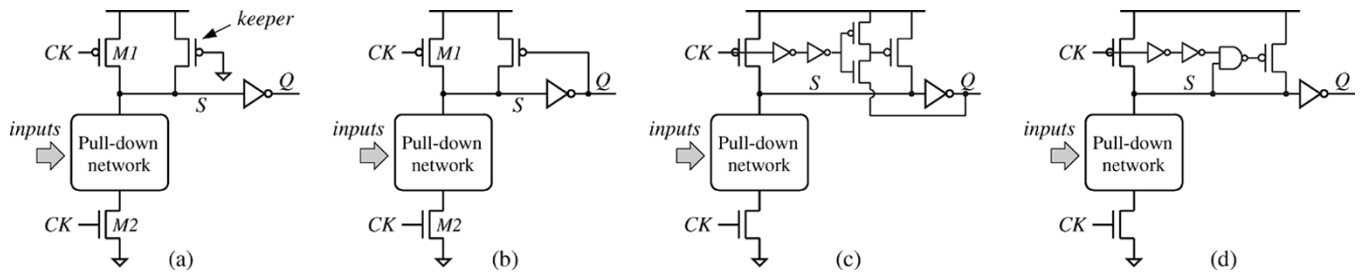


Fig. 2. Improving noise immunity of dynamic logic gates using keeper. (a) Weak always-on keeper [3]. (b) Feedback keeper [4]. (c) HS feedback keeper [5]. (d) Conditional feedback keeper [7].

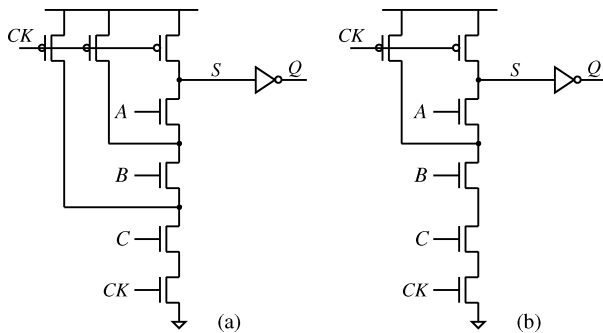


Fig. 3. Precharging internal nodes (3-input AND gate). (a) Precharge all internal nodes [9]. (b) Partial precharge [10].

*et al.* in [5] and [6] [see Fig. 2(c)] and Alvandpour *et al.* in [7] and [8] [see Fig. 2(d)]. Both techniques share the same basic principle, that is, to temporarily disable the keeper during the small time window when the dynamic gate switches. These two techniques have been shown to be very effective in enhancing the noise tolerance of dynamic gates against gate internal noises like leakage noise. However, dynamic gates with those keepers are still susceptible to external noise glitches because the dynamic node is not adequately protected during the gate switching time window. We will explain this in detail in Section IV and show a novel class of keeper design techniques that increases gate noise immunity against both internal and external noises with minimal contention.

### B. Precharging Internal Nodes

In complex dynamic logic gates with large pull-down network, charge sharing between the dynamic node and the internal nodes in the pull-down network often results in false gate switching. A simple yet effective way to prevent the charge sharing problem is to precharge the internal nodes in the pull-down network along with precharging the dynamic node  $S$  [9], [10]. An example dynamic 3-input AND gate using this technique is illustrated in Fig. 3(a). When all internal nodes are precharged, this technique is able to eliminate the charge sharing problem at the cost of using a large number of precharge transistors and the increased load capacitance on the clock net. Partial precharge, as shown in Fig. 3(b), has also been used in design practice as a tradeoff between noise immunity and overheads

in chip area and in clock load. NMOS transistors can also be used to precharge the internal nodes if the cost of an inverter to generate the complementary clock signal can be justified. Since the internal nodes are only precharged to  $V_{DD} - V_T$ , dynamic logic gates using nMOS precharge transistors have reduced discharging time and decreased dynamic power consumption. Finally, it is noted that techniques based on precharging internal nodes alone are not very effective against external noises.

### C. Raising Source Voltage

One effective way to improve noise tolerance against both internal and external noises is to increase the source voltage of the transistors in the pull-down network. Since the gate voltage has to be greater than the sum of the source voltage and the transistor threshold voltage when a transistor is turned on, higher source voltage directly leads to increased gate turn-on voltage. Furthermore, due to the body effect, transistor threshold voltage is increased when the source voltage rises. This also contributes to improving gate turn-on voltage.

The pMOS pull-up technique [11], shown in Fig. 4(a), employs a pMOS transistor at node  $N2$  forming a resistive voltage divider with the bottom clock controlled transistor. The voltage at node  $N2$ , which determines the switching threshold voltage of the dynamic logic gate, can be adjusted by changing the relative size of the pMOS pull-up transistor. One major drawback of this technique is the dc power consumption in the resistive voltage divider. Furthermore, since the voltage level at the dynamic node  $S$  can never get lower than the voltage at node  $N2$ , the voltage swing at node  $S$  is not rail-to-rail. When the size of the pMOS pull-up transistor is large in an effort to aggressively raise gate noise immunity, the gate output may also not have a rail-to-rail swing.

An improved method, shown in Fig. 4(b), employs a pull-up transistor with feedback control [12]. Here an nMOS transistor  $M1$  is used to pull up the voltage of an internal node. The gate of the pull-up transistor is connected to the dynamic node of the domino gate. This design allows the pull-up transistor to be shut off when the voltage of the dynamic node goes low, therefore, the dynamic node  $S$  undergoes rail-to-rail voltage swing. Also, the dc power consumption problem is partially solved. It occurs only under certain input combinations that do not turn on the pull-down network. Note that a pMOS transistor can similarly

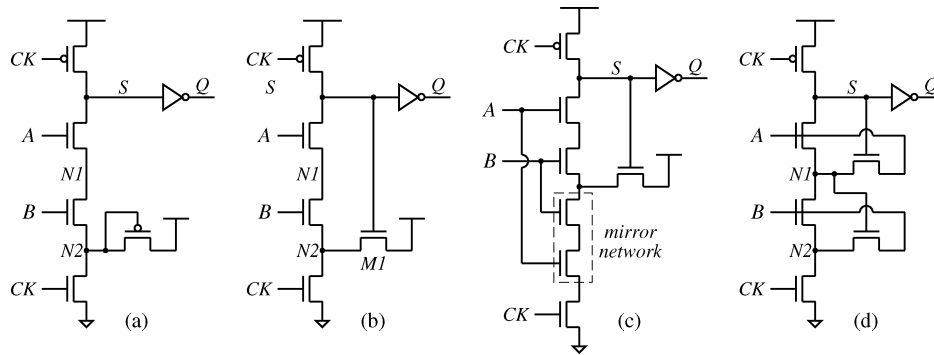


Fig. 4. Raising source voltage (2-input AND gate). (a) pMOS pull-up technique [11]. (b) NMOS pull-up (with feedback) [12]. (c) Mirror technique [13]. (d) Twin transistor technique [15].

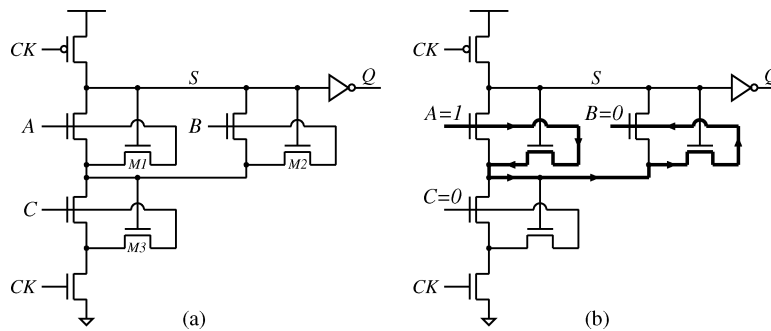


Fig. 5. Possible short circuit problem using twin transistor technique. (a) A 3-input OR-AND gate. (b) Direct conducting path.

be used in this technique provided that the gate of the pMOS transistor is connected to the output of the dynamic logic gate.

The mirror technique [13], [14] employs a feedback controlled nMOS transistor similar to the nMOS pull-up technique. In addition, it duplicates the pull-down network in an effort to further reduce dc power consumption and to further improve gate noise tolerance. A 2-input dynamic AND gate designed using the mirror technique is shown in Fig. 4(c). Whenever the pull-down network is OFF, the mirror network is also OFF, hence, cutting off the potential dc conducting path from the nMOS pull-up transistor through the bottom clock controlled transistor. Therefore, the dc power consumption problem is completely solved. However, this technique significantly lengthens the discharge path in the pull-down network, which potentially leads to slower circuit or considerably increased circuit active area when the transistors are aggressively sized.

The twin transistor technique [15], [16] adopts nMOS pull-up transistors at all internal nodes to further improve dynamic gate noise immunity. In addition, the drain nodes of the pull-up nMOS transistors are connected to the inputs instead of to the power-supply network, as illustrated in Fig. 4(d). By doing so, unnecessary injection of current by the pull-up transistors is avoided, resulting in lower gate power consumption. However, this technique leads to increased gate input capacitance which may slow down the switching of the gates in the previous stage. Further, this technique is not suitable for certain logic functions because it may short input nodes. As an example, in Fig. 5(a) we show a 3-input OR-AND gate implementing the logic function of  $(A + B) \cdot C$ . Assume input  $A$  is high while inputs  $B$  and  $C$  are low. The dynamic node  $S$  stays high because

$C$  is low and there is no discharging path to the ground. Under such scenario, there is a dc conducting path between the two inputs  $A$  and  $B$ , as illustrated in Fig. 5(b). Therefore, the logic states at node  $A$  or node  $B$  are unclear. Note that the resulting damage can go far beyond the single dynamic gate under study if these ambiguous nodes feed to a large number of other gates.

#### D. Constructing Complementary p-Network

The basic principle of this class of techniques is to construct a weak complementary p-network to prevent the dynamic node from floating in the evaluation phase. One such technique [17], [18] is illustrated in Fig. 6(a). The gate operates in a similar way as a normal domino gate in the precharge phase. In the evaluation phase, the logic gate behaves as a skewed CMOS logic gate. Therefore, the switching threshold voltage of the dynamic logic gate is equivalent to that of a skewed CMOS logic gate. In addition to the silicon area overhead associated with the pull-up network, a major drawback of this technique in practice is its ineffectiveness in dealing with very wide logic gates, for example, wide OR gates, where dynamic logic styles really outshine static CMOS logic gates in performance.

pMOS transistors can also be employed at a per transistor level, as shown in Fig. 6(b). This technique is known as CMOS inverter technique [19]. The relative size of the pMOS transistors can be varied to adjust the switching threshold of the dynamic logic gate. One advantage of this technique is that it can be selectively applied to a subset of inputs if they can be identified as noisy in advance. The main drawback of this technique is that it is not suitable for OR type logic gates because of possible serious dc currents under certain input combinations. Again we

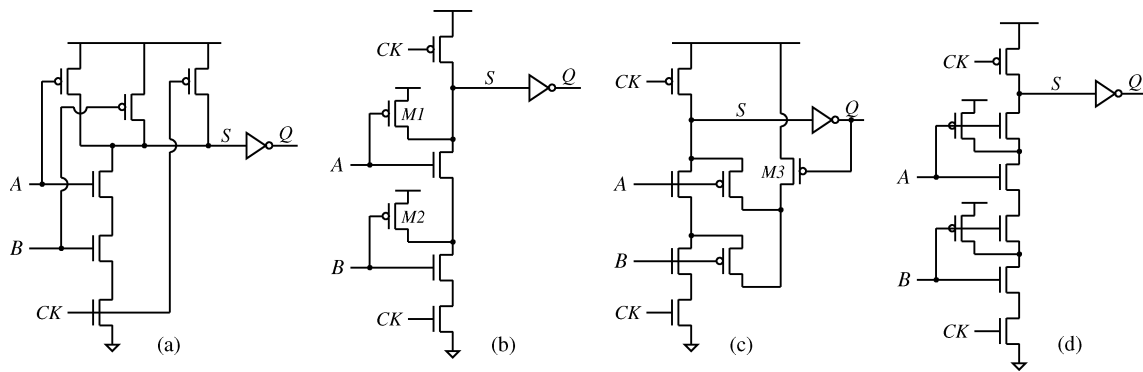


Fig. 6. Constructing complementary PFET network (2-input AND gate). (a) Complementary p-network technique [17]. (b) CMOS inverter technique [19]. (c) Gated CMOS inverter technique [20]. (d) Triple transistor technique [21].

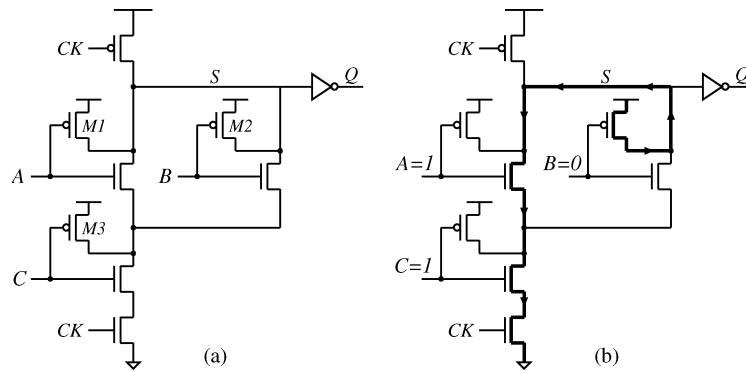


Fig. 7. Possible short circuit problem using CMOS inverter technique. (a) A 3-input OR-AND gate. (b) Direct conducting path.

will use the simple 3-input OR-AND gate as an example. When inputs  $A$  and  $C$  are high and input  $B$  is low, there is a direct conducting path between the power-supply network and the ground node, as shown in Fig. 7(b). More hazardous than the obvious problem of dc power consumption, the voltage at node  $S$  is determined by the relative strength of the pull-up transistor  $M2$  and that of the transistors in the discharge path. The gate may fail to switch when the pull-up transistor is sized relatively strong in an effort to aggressively improve gate noise tolerance.

Note that the dynamic node can be false reset with certain input combinations using either of the two above techniques. In Fig. 6(b), for example, if input  $A$  stays high and input  $B$  falls from high to low during the evaluation phase, the dynamic node may be reset to high by the pull-up pMOS transistor  $M2$ . With a view to solve this false reset problem, Evans in [20] used an additional transistor  $M3$ , shown in Fig. 6(c).  $M3$  is ON when the gate output remains low. When the evaluation is executed and the output rises,  $M3$  is turned off disconnecting the pull-up transistors from the power-supply network. Similar tactic can also be applied to improve the simple complementary p-network technique. It is noted that this gated CMOS inverter technique does not completely solve the dc conducting problem for certain logic circuits.

Fig. 6(d) illustrates a noise-tolerant 2-input AND gate using a triple transistor technique [21], where each nMOS transistor in the pull-down network of a simple dynamic logic gate is replaced by three transistors. The technique can be considered as a variation of the CMOS inverter technique where an additional nMOS transistor is used to prevent the possible dc conducting

path problem in the evaluation phase. Similar to the mirror technique, this technique significantly lengthens discharge paths in the pull-down network. While it can be useful for certain logic gates like wide-OR gates, it is not practical to be applied to general pull-down nMOS network because of its overhead in circuit area and performance.

### E. Comparison of Techniques

In this section, we compare the noise-tolerant design techniques described in the previous sections. We start by listing the set of basic requirements that a desirable noise-tolerant design technique should meet.

- 1) It improves gate noise tolerance against all types of noises.
- 2) It is suitable for all logic functions.
- 3) It has minimal circuit area overhead.
- 4) It has minimal circuit speed overhead.
- 5) It consumes no dc power and has minimal ac power consumption overhead.

Dynamic circuit noise enhancing techniques discussed in this section are compared in Table I. The first four columns are self-explanatory. The fifth column is the approximate number of transistors needed in a large dynamic logic gate, where  $N$  is the number of transistors in the pull-down network of the original dynamic logic gate. The sixth and seventh columns indicate whether the input load capacitance and clock load capacitance are unchanged when a noise-tolerant design technique is used. The eighth column shows whether the length of the discharge

TABLE I  
COMPARISON OF EXISTING DYNAMIC CIRCUIT NOISE TOLERANCE ENHANCING TECHNIQUES

Class	Technique	Reference	Illustration	Num. tran.	Input load <sup>a</sup>	Clock load <sup>a</sup>	Dischrg path <sup>a</sup>	DC current <sup>a</sup>	All noises <sup>a</sup>	All func. <sup>a</sup>
A	Always-on keeper	[3]	Fig. 2(a)	$N$	o	o	o	×	o	o
	Feedback keeper	[4]	Fig. 2(b)	$N$	o	o	o	o	o	o
	HS feedback keeper	[5]	Fig. 2(c)	$N$	o	o	o	o	×	o
	Conditional feedback keeper	[7]	Fig. 2(d)	$N$	o	o	o	o	×	o
B	Precharge internal nodes	[9]	Fig. 3(a)	$2N$	o	×	o	o	×	o
	Partial precharge	[10]	Fig. 3(b)	$N$	o	×	o	o	×	o
C	PMOS pull-up	[11]	Fig. 4(a)	$N$	o	o	o	×	o	o
	NMOS pull-up (feedback)	[12]	Fig. 4(b)	$N$	o	o	o	×	o	o
	Mirror technique	[13]	Fig. 4(d)	$2N$	×	o	×	o	o	o
	Twin transistor	[15]	Fig. 4(c)	$2N$	^	o	o	o	o	^
D	Complementary p-network	[17]	Fig. 6(a)	$2N$	×	o	o	o	o	o
	CMOS inverter	[19]	Fig. 6(b)	$2N$	×	o	o	o	o	×
	Gated CMOS inverter	[20]	Fig. 6(c)	$2N$	×	o	o	o	o	×
	Triple transistor	[21]	Fig. 6(d)	$3N$	×	o	×	o	o	o

<sup>a</sup>Symbol o represents ‘good’ and symbol × represents ‘not good’.

paths in the pull-down network is intact. The ninth column indicates whether the dynamic gate maintains the zero dc power consumption property. The tenth column shows whether the technique enhances noise tolerance against both internal and external noises. And finally, the last column shows whether the technique can be applied to all logic gates.

It is shown in the table that the twin transistor technique and CMOS inverter based techniques are not suitable for all logic functions. Techniques based on precharging internal nodes as well as the two new feedback keeper techniques only improve gate noise immunity against certain types of noises. Both the pMOS pull-up technique and the nMOS pull-up (with feedback) technique consumes dc power. The Mirror technique and the triple transistor technique increase the length of gate discharge path. Techniques based on raising source voltage usually either have dc power consumption or require significantly larger silicon area. Techniques based on constructing complementary p-network often require larger silicon area and they increase the previous stage gate delay due to greater gate input capacitance.

In all, simple feedback keeper is the only general-purpose technique that improve dynamic logic gate noise immunity against all types of noise without significant increase in silicon area (device count), speed, and power consumption.

#### IV. PROPOSED NOISE-TOLERANT DESIGN TECHNIQUE

The simple feedback keeper technique is effective against noises and is easy to design. However, there is a fundamental dilemma in choosing the size of the keeper. On one hand, a strong keeper is required to achieve high gate noise tolerance. On the other hand, large keeper leads to significant contention during normal gate switching, therefore deteriorates gate performance. The conditional keeper techniques [5]–[8] temporarily disable the keeper or reduce keeper strength to alleviate the contention problem. But dynamic gates equipped with those keepers are susceptible to input noise glitches because the dynamic node is not adequately protected during the gate switching time window.

Noise immunity against input noises is very difficult to achieve without significant sacrifice in circuit performance because the gate should not act before it identifies whether

the input is noise or real signal. This inevitable time needed to distinguish noise from real signal, which is obtained by monitoring the initial period of the input voltage waveform, causes degradation in circuit performance.

The performance overhead due to the additional circuitry that helps improve input noise immunity cannot be completely eliminated. However, it can be reduced to a large extent. In this paper, we propose a new technique that enhances dynamic gate noise immunity against all types of noises including the input noise. The proposed technique incurs very little cost in performance.

#### A. Basic Principle

First, let us carefully reexamine the noise tolerance versus speed conundrum. It may be observed that there is an ambiguity in the definition of the strength of the keeper. The keeper strength that determines gate noise tolerance is not necessarily the same as the keeper strength that governs the gate performance. Let us measure the keeper strength in terms of the current supplied by the keeper.

- Keeper strength that determines gate speed is approximately the *average* current when the applied voltage across the keeper is in the range  $[0, V_{DD}/2]$ ; this current is given by

$$I_{sp} = \frac{2}{V_{DD}} \int_0^{V_{DD}/2} I(V) dV. \quad (1)$$

- Keeper strength that determines gate noise robustness is the small-signal *maximum* current, defined as

$$I_{nm} = \max_{0 \leq V \leq V_D} (I(V)) \quad (2)$$

where  $V_D$  is the maximum allowed voltage deviation from the ideal voltage at the dynamic node  $S$  and it is much smaller than  $V_{DD}/2$  in practice.

It is the difference between keeper strength for gate performance and keeper strength for gate noise immunity that makes it possible to enhance the noise tolerance of a dynamic logic gate while still retaining its performance. We will hereafter call a keeper that aggressively explores this difference a *smart keeper*.

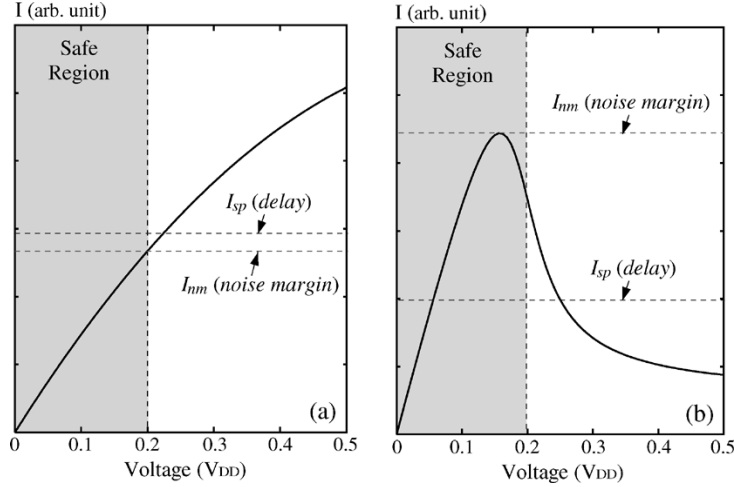


Fig. 8. Comparing keeper strengths for noise margin and for gate speed purposes.  $V_D = 0.2V_{DD}$ . (a) Field-effect transistor. (b) Circuit or device with negative differential resistance region.

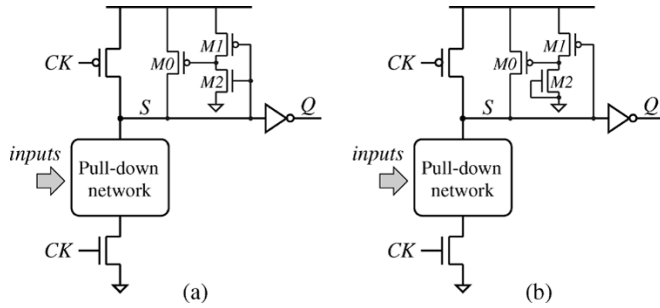


Fig. 9. Domino logic gate with optimized feedback keeper. (a) CMOS inverter feedback. (b) Pseudo-pMOS inverter feedback.

The goal of circuit designers is, therefore, to find a keeper that has a large  $I_{nm}$  and, at the same time, a small  $I_{sp}$ . However, this goal is not able to be materialized using a single field-effect transistor, which has a monotonous  $I-V$  characteristic where the current always rises when the applied voltage across the transistor is increased. Using such device as the keeper, it can be shown that  $I_{sp}/I_{nm}$  has a very loose lower bound of  $1 - 2V_D/V_{DD}$ .

*Theorem 1:* If the  $I-V$  characteristic of a keeper  $I(V)$  is monotonously increasing, the ratio of delay keeper strength and noise keeper strength has a lower bound of  $1 - 2V_D/V_{DD}$ .

*Proof:*

$$\begin{aligned} \frac{I_{sp}}{I_{nm}} &= \frac{2}{V_{DD}} \int_0^{V_{DD}/2} \frac{I(V)dV}{\max_{0 \leq V \leq V_D} (I(V))} \\ &\geq \frac{2}{V_{DD}} \int_{V_D}^{V_{DD}/2} \frac{I(V)dV}{I(V_D)} \\ &\geq \frac{2}{V_{DD}} (I(V_D) \cdot (\frac{V_{DD}}{2} - V_D)) \\ &= 1 - 2 \frac{V_D}{V_{DD}}. \quad \blacksquare \end{aligned}$$

In practice, this lower bound is a very loose one. To improve it, we further use the fact that the  $I-V$  characteristics of MOSFET devices are always concave. A function  $f(x)$  is

concave within  $(x_1, x_2)$  if and only if  $f(ax_1 + (1-a)x_2) \geq af(x_1) + (1-a)f(x_2)$  holds for any  $a \in (x_1, x_2)$ .

*Theorem 2:* If the  $I-V$  characteristic of a keeper  $I(V)$  is monotonously increasing and it is also concave, the ratio of delay keeper strength and noise keeper strength has a lower bound of  $1 - V_D/V_{DD}$ .

*Proof:*

$$\begin{aligned} \frac{I_{sp}}{I_{nm}} &= \frac{2}{V_{DD}} \int_0^{V_{DD}/2} \frac{I(V)dV}{\max_{0 \leq V \leq V_D} (I(V))} \\ &= \frac{2}{V_{DD}} \left( \int_0^{V_D} I(V)dV + \int_{V_D}^{V_{DD}/2} I(V)dV \right) \\ &= \frac{I(V_D)}{I(V_D)} \\ &\geq \frac{2}{V_{DD}} \left( \frac{I(V_D)V_D}{2} + I(V_D) \cdot (\frac{V_{DD}}{2} - V_D) \right) \\ &= 1 - \frac{V_D}{V_{DD}}. \quad \blacksquare \end{aligned}$$

For realistic MOSFET-based keeper, as shown in Fig. 8(a), the delay keeper strength  $I_{sp}$  is often comparable to, if not greater than, the noise keeper strength  $I_{nm}$ .

On the other hand, if the  $I-V$  characteristic of the keeper is not monotonic, i.e., it has one or more negative differential resistance (NDR) regions,  $I_{sp}$  can potentially be significantly smaller than  $I_{nm}$ , as illustrated in Fig. 8(b). This suggests that the noise margin of dynamic logic gates can be greatly improved with little cost in performance if the keeper has the NDR property. Note that the  $x$  axis in Fig. 8 ranges from 0 to half the power-supply voltage. The folded-back  $I-V$  characteristic has to occur within this range for the benefit of the NDR property to be fully appreciated.

*Remark:* The folded-back phenomenon should occur in the left half of the  $I-V$  plot.

## B. Optimizing Conventional Keepers

We will first optimize conventional feedback keepers such that the keeper strength for speed is minimized when the keeper

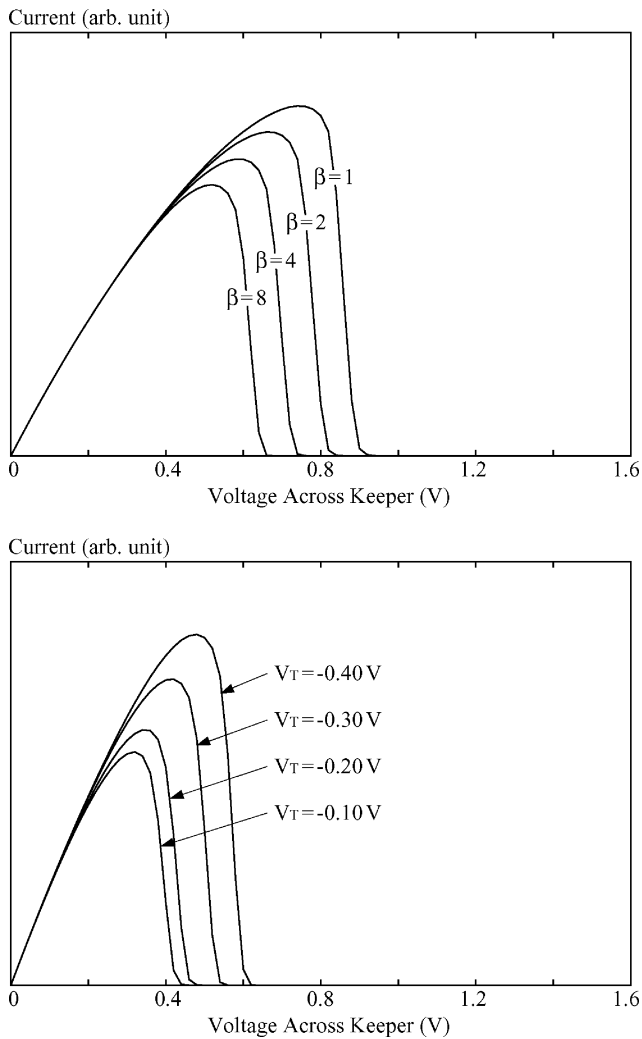


Fig. 10. Impacts of transistor sizing and threshold voltage on  $I$ - $V$  characteristic. (a) With respect to beta ratio. ( $V_T = -0.40$  V.) (b) With respect to threshold voltage ( $\beta = 4.0$ ).

strength for noise tolerance (that is, the gate noise-tolerant requirement) is given. Fig. 9(a) shows a dynamic logic gate with the conventional feedback keeper. Here a weak CMOS inverter is employed to generate the feedback signal instead of directly connecting gate output  $Q$  to the gate node of transistor  $M0$ . This has at least two advantages. First, the response time of the feedback process is independent of external gate load condition. Second, this gives us the freedom to independently optimize the feedback inverter without having to worry about the gate output. A variation of this design, where a pseudo-pMOS inverter feedback is used, is shown in Fig. 9(b). Since both keepers operates similarly, we will focus our discussion on the first keeper design.

The  $I$ - $V$  characteristic of the keeper circuit is very sensitive to the parameters of the transistors. Since we want the keeper current to quickly drop when the voltage level at the dynamic node  $S$  decreases, the two most important parameters are: 1) the size ratio of the pull-up transistor  $M1$  and the pull-down transistor  $M2$  and 2) the threshold voltage of the pull-up transistor  $M1$ . In Fig. 10, we have plotted the impacts of beta ratio of the feedback inverter and the threshold voltage of  $M1$  on the  $I$ - $V$

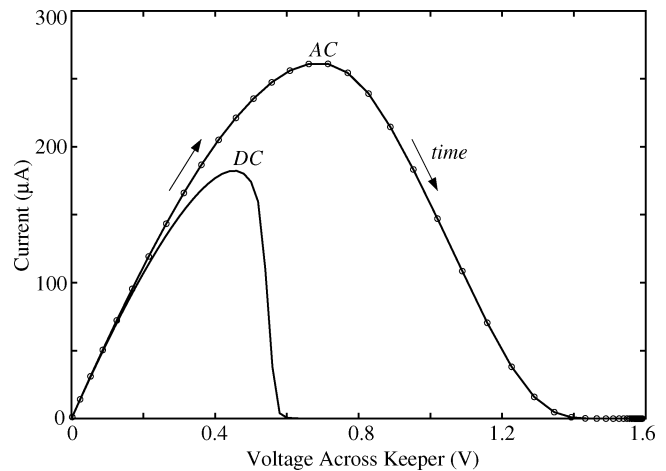


Fig. 11. Comparison of dc and ac  $I$ - $V$  characteristics. ( $V_T = -0.20$  V and  $\beta = 4.0$ . Time interval between adjacent points on the ac curve is 5 ps.)

characteristic of the keeper. Obviously, a large beta ratio and a low threshold voltage are preferred in this application.

At the first glance, it appears that the  $I$ - $V$  characteristic of this simple keeper is very suitable for the high-performance keeper application because: 1) the  $I$ - $V$  curves do have the folded-back property and 2) when proper beta ratio and transistor threshold voltage values are chosen, the folded-back phenomenon can occur in the left half of the plot. Experimental studies based on SPICE simulation have shown that this optimized conventional keeper can offer better performance than nonoptimized keeper. However, its advantage is very limited. This is mainly because of the fact that the  $I$ - $V$  curves shown in the previous plots are dc  $I$ - $V$  characteristics. Due to the delay of the feedback inverter, transistor  $M0$  is turned off much later than desired. In fact, if the delay of the feedback inverter is comparable to the discharge time of the pull-down network, the feedback effect will kick in too late to make much difference in reducing contention. In Fig. 11, we plot both the dc and ac  $I$ - $V$  characteristics of the keeper. It is shown that despite the dc  $I$ - $V$  curve folds back in the left half of the plot, the fold-back of the ac curve occurs mainly in the right half of the plot. Therefore, keepers having one or more feedback stages are not the best candidate as the desired smart keepers.

*Remark:* The ac  $I$ - $V$  characteristic should be used in determining the keeper strength for gate delay.

### C. Smart Keepers Designed Using MOSFETs

Circuits designed using MOSFET devices that exhibit the NDR property have been studied extensively in the literature [23], [24]. In fact, systematic methods have been developed to construct NDR circuits using transistors [24]. Those existing NDR circuits constitute a pool of potential circuits for MOSFET-based smart keepers. Here we will demonstrate how those NDR circuits can be employed in the keeper network by using one of the simplest of those NDR circuits.

This two-transistor simple NDR circuit, illustrated in Fig. 12(a), was first proposed in [22]. It is composed of a cross-coupled depletion-mode nMOS transistor  $M1$  and depletion-mode pMOS transistor  $M2$ . Since the gate of  $M1$  is connected to the dynamic node  $S$ , the current through the



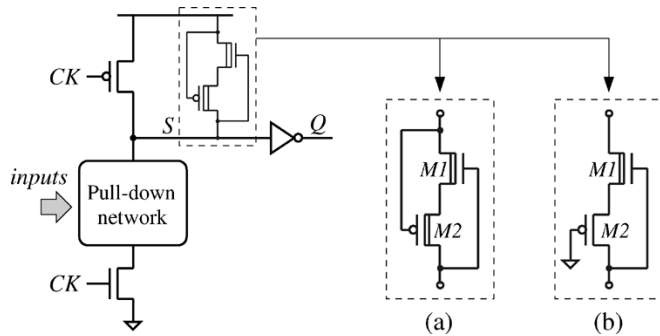


Fig. 12. Domino logic gates with MOSFET-based smart keeper. (a) Depletion-mode nMOS with depletion-mode pMOS. (b) Depletion-mode nMOS with enhancement-mode pMOS.

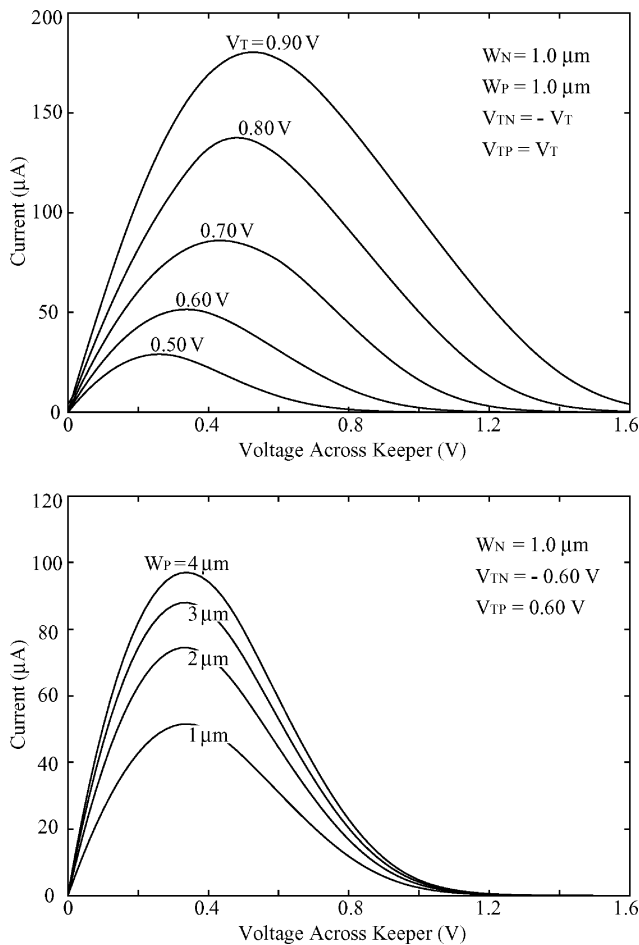


Fig. 13. Impacts of threshold voltage and transistor sizing on  $I-V$  characteristic. (a) With respect to threshold voltage. (b) With respect to transistor sizing.

two transistors will be cut off immediately when the voltage at  $S$  drops to the turn-off voltage of  $M1$ . It is noted that in our application the gate of transistor  $M2$  connects to a constant voltage source, the power-supply node. Therefore, we can alternatively use an enhancement-mode pMOS transistor whose gate is connected to the ground node, as shown in Fig. 12(b).

The impacts of transistor threshold voltage and transistor sizing on the  $I-V$  characteristic of the circuit are shown in Fig. 13. It is observed that the current peak moves leftward

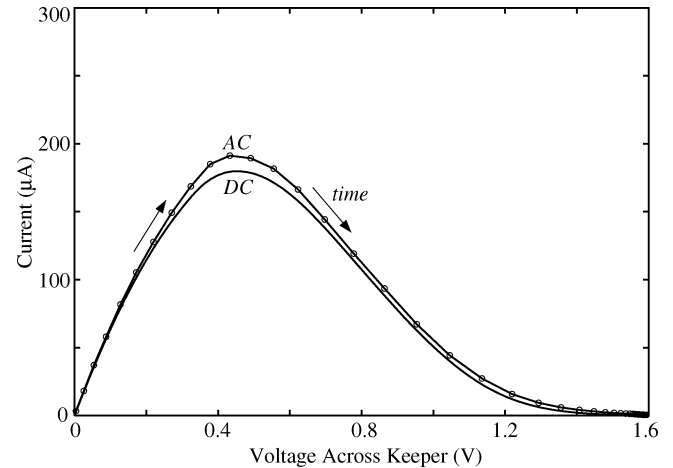


Fig. 14. Comparison of dc and ac  $I-V$  characteristics. ( $V_{TN} = -0.70 V$ ,  $V_{TP} = 0.80 V$ ,  $W_1 = 1.50 \mu m$  and  $W_2 = 1.50 \mu m$ . Time interval between adjacent points on the ac curve is 5 ps).

when the absolute value of the threshold voltage is reduced. However, at the same time the peak current value quickly decreases meaning that significantly larger keeper size is required to retain the same gate noise tolerance level. When the relative size of the transistors is changed, it is also observed that even though the magnitude of the current changes, the shape of the  $I-V$  characteristic remains largely unchanged.

A typical ac  $I-V$  characteristic of the proposed keeper, together with its corresponding dc  $I-V$  characteristic, is shown in Fig. 14. It can be seen that the two curves are very close to each other and they reach their peaks at approximately the same voltage value across the keeper. This is in distinct contrast to the case of the conventional feedback keeper discussed in the previous section (see Fig. 11). It is mainly because of the fact that the gate of transistor  $M1$  is directly wired to the dynamic node  $S$ , therefore is able to cut off the current through the keeper instantaneously when the voltage at  $S$  drops. The slight difference between the two  $I-V$  curves is caused by the small amount of time required to discharge the parasitic capacitance of the internal node residing between the two transistors  $M1$  and  $M2$ .

#### D. Smart Keepers Designed Using NDR Devices

Smart keepers can also be realized using devices that intrinsically have the folded-back  $I-V$  characteristic. The keeper can be either a three-terminal NDR device or series connected two-terminal NDR device and a feedback controlled MOS transistor, as illustrated in Fig. 15. Typical two-terminal NDR devices include tunneling diodes, resonant tunneling diodes, resonant-interband tunneling diodes, etc. And example three-terminal NDR devices are resonant-tunneling transistors, negative-resistance field-effect transistors, resonant-tunneling hot-electron transistors, etc. An extensive overview of semiconductor devices including those having the NDR property can be found in [25].

In the paper, we will take the RTD+FET implementation as an example. RTDs are semiconductor heterostructures with a low-bandgap quantum well being sandwiched between two barrier layers of high-bandgap materials. The energy levels in

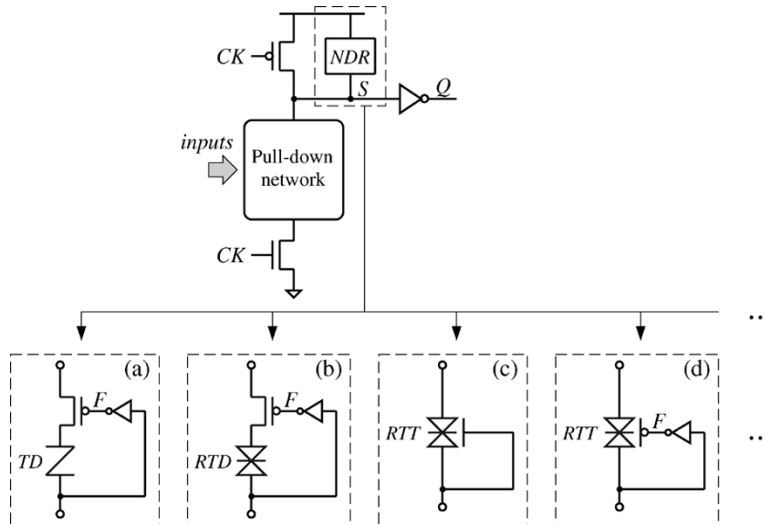


Fig. 15. Domino logic gates with smart keepers designed using intrinsic NDR devices. (a) Tunneling diode with MOS transistor. (b) Resonant-tunneling diode with MOS transistor. (c) and (d) smart keepers based on three-terminal NDR devices.

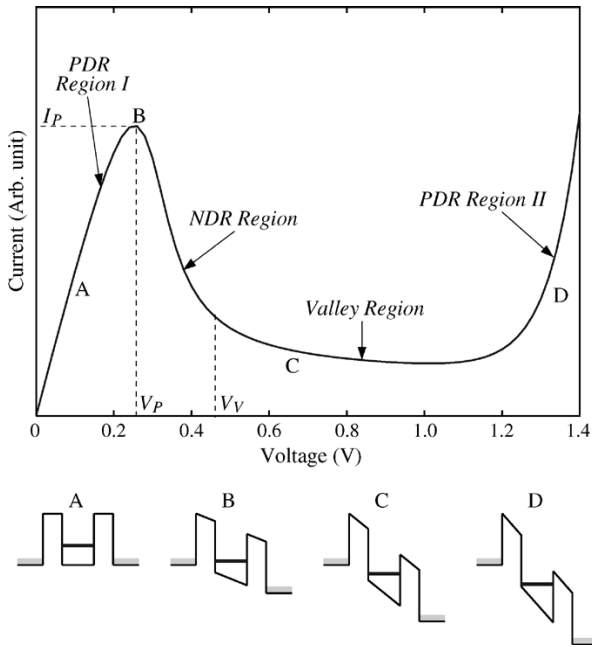


Fig. 16. Typical  $I$ - $V$  characteristic of resonant tunneling diodes and schematic band diagrams.

the narrow well are discretized due to the quantization effect. Quantum tunneling, also known as resonant tunneling, occurs when the applied voltage across the diode is aligned to one of the discrete energy levels in the well resulting in sharp current peak [28]. Schematic band diagrams at four different voltage values across the diode are illustrated in Fig. 16. Also shown in the figure is the  $I$ - $V$  characteristic of a typical RTD. It consists of a positive differential resistance (PDR) region, a negative differential resistance region, a valley region, and a second PDR region.

The operation of a domino logic gate with the RTD+FET keeper is as follows. In the precharge phase when the clock  $CK$  is low, the dynamic node  $S$  is precharged high and the feedback node  $F$  is low. Hence, the PFET in the keeper is ON and the

RTD operates in PDR Region I. The gate enters the evaluate phase when  $CK$  switches high. The RTD stays in the PDR Region I until the input voltage to the pull-down network is high enough such that the discharge current exceeds  $I_P$ , the peak current of the RTD. After this point, the gate starts to accelerate in switching because the combined effect of increasing in discharge current and the decrease in the pull-up current through the RTD. After the dynamic node  $S$  drops to a certain low voltage value, the PFET in the keeper is switched off allowing the dynamic node to fully reach the ground voltage.

In all, it can be observed that dynamic logic circuits designed using the proposed method maintain the following benefits that conventional domino logic gates possess: 1) area overhead is very small in comparison with other noise tolerant techniques; 2) there is no dc power consumption; 3) signals have rail-to-rail voltage swing; and 4) clocking scheme is simple and no delay element is required. It is noted that cointegrating resonant tunneling devices with conventional CMOS technologies is currently still a challenge.

### V. NOISE MARGIN AND DELAY ANALYSIS

In this section, we analytically study the noise margin as well as the discharge time of domino logic gates with the proposed NDR keepers. For simplicity of analysis, we assume the  $I$ - $V$  characteristic of the NDR keeper can be modeled using a piecewise linear waveform as shown in Fig. 17(a), where  $I_P$  is the peak current,  $V_P$  is the peak voltage, and  $V_Z$  is the voltage when the current first becomes negligible. The input signal is assumed to have a saturated ramp waveform with a rise time of  $t_r$ . To facilitate manual analysis, we have further assumed this ramp input can be approximated by a step waveform, as shown in Fig. 17(b), where the sizes of the shadowed areas are matched.

#### A. Noise Margin Analysis

Let us consider a noise input that partially turns on the n-network of the dynamic logic gate. As long as the discharge current caused by the input noise does not exceed the peak current of the

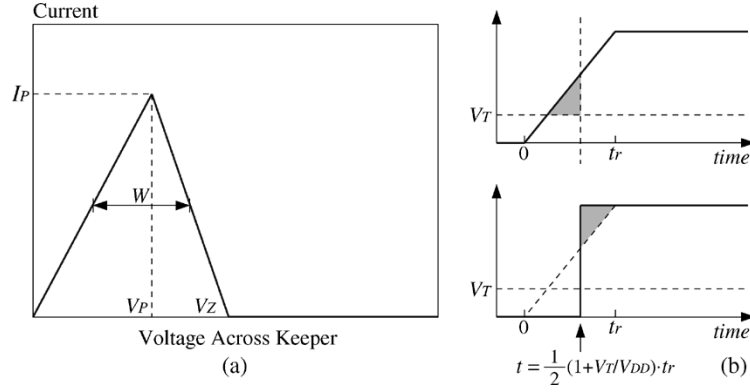


Fig. 17. Assumption for simple analysis. (a) Piecewise linear NDR keeper  $I$ - $V$  characteristic. (b) Input voltage waveform (top: saturated ramp waveform; bottom: equivalent step waveform).

keeper, the keeper operates in PDR region. The voltage drop at the dynamic node  $S$  is less than or equals to  $V_P$  and the output of the gate driver remains low. However, when the input noise is greater than  $I_P$ , the keeper operating point moves into the NDR region. The current supplied by the keeper reduces steeply and the voltage at the dynamic node  $S$  quickly drops resulting in a low-to-high switching of the gate driver. Overall, the maximum input noise level that the dynamic gate can withstand is the voltage that causes the voltage level at the dynamic node  $S$  to drop to  $V_P$ .

We assume the current of the n-network of a dynamic logic gate  $G$  can be formulated using the following simple expression:

$$I^G(V_{in}) = \begin{cases} 0, & \text{when } V_{in} \leq V_T \\ k \cdot (V_{in} - V_T), & \text{when } V_{in} > V_T \end{cases} \quad (3)$$

where  $k$  is the transconductance and  $V_T$  is the transistor threshold voltage. For circuits in the very deep submicron regime, this linear approximation is usually a good first-order estimation of the current [34]. The maximum noise voltage level that the gate can withstand is derived by equating (3) to the peak current of the keeper  $I_P$  and is calculated as

$$V_{max} = \frac{I_P}{I_0} \cdot (V_{DD} - V_T) + V_T \quad (4)$$

where  $I_0 = I^G(V_{DD})$  is the discharge current of the pull-down n-network when it switches fully on. The above equation shows that the gate noise margin is proportional to  $I_P$ , the peak keeper current. When the maximum input noise level  $V_{max}$  is specified in a design, the keeper peak current that is necessary to meet the noise specification can be derived from (4)

$$I_P = \frac{V_{max} - V_T}{V_{DD} - V_T} \cdot I_0. \quad (5)$$

The above simple equation can be used to quickly estimate the size of the keeper device.

### B. Delay Analysis

In this section, we study the discharge time of dynamic gates with NDR keeper, where the gate delay is measured from when

the latest switching input reaches half of the supply voltage to when the dynamic node  $S$  falls to half of the supply voltage. First, referring to Fig. 17(b), the time between when the original saturated ramp input reaches half of the supply voltage and when the step waveform rises is calculated as

$$t_0 = \frac{V_T}{2V_{DD}} t_r. \quad (6)$$

Next, the operation of dynamic logic gates with the proposed keeper can be divided into three stages depending on the operating regions of the keeper. In the first stage, the keeper device operates in PDR region, and the governing equation for the dynamic node  $S$  is

$$C \frac{dV(t)}{dt} - \frac{V_{DD} - V(t)}{V_P} I_P + I_0 = 0 \quad (7)$$

where  $V(t)$  is the voltage at the dynamic node  $S$  and  $C$  is the nodal capacitance at  $S$ . The above first-order differential equation can be solved to obtain the time for  $V(t)$  to drop from  $V_{DD}$  to  $V_{DD} - V_P$

$$t_1 = C \frac{V_P}{I_P} \ln \left( \frac{I_0}{I_0 - I_P} \right). \quad (8)$$

In the second stage, the keeper operates in the NDR region. The time to discharge the dynamic node  $S$  from  $V_{DD} - V_P$  to  $V_{DD} - V_Z$  can be similarly derived as

$$t_2 = C \frac{V_Z - V_P}{I_P} \ln \left( \frac{I_0}{I_0 - I_P} \right). \quad (9)$$

In the third stage, the keeper current is negligible. The time to discharge the dynamic node  $S$  from  $V_{DD} - V_Z$  to  $V_{DD}/2$  is simply calculated as

$$t_3 = \frac{C \left( \frac{V_{DD}}{2} - V_Z \right)}{I_0}. \quad (10)$$

The total discharge time is therefore the sum of the above four terms, which can be simplified to

$$t_d = \frac{V_T}{2V_{DD}} t_r + C \frac{V_Z}{I_P} \ln \left( \frac{I_0}{I_0 - I_P} \right) + \frac{C \left( \frac{V_{DD}}{2} - V_Z \right)}{I_0}. \quad (11)$$

It can be shown that given  $I_P$ , the discharge time calculated using the above equation rises monotonically when the cut-off

voltage  $V_Z$  increases. This is in accordance with the intuition that one needs to reduce the area beneath the  $I$ - $V$  characteristics of the keeper device in order to minimize the performance penalty. Equation (11) can be written in the following form:

$$t_d = t_{d,0} + S_W \cdot W \quad (12)$$

$$t_{d,0} = \frac{V_T}{2V_{DD}} t_r + \frac{CV_{DD}}{2I_0} \quad (13)$$

$$S_W = \frac{C}{I_P} \ln \left( \frac{I_0}{I_0 - I_P} \right) - \frac{C}{I_0} \quad (14)$$

where  $W$  is the width of the current peak in the  $I$ - $V$  plot as shown in Fig. 17 and  $S_W$  is a sensitivity metric of gate delay with respect to  $W$ . For realistic circuit parameters,  $S_W$  is positive definite meaning that designers should strike for smaller  $W$  values in order to minimize the performance overhead of using the keeper. The ideal case is when the width of the current peak approaches zero. Now despite the presence of the keeper with a peak current of  $I_P$ , the total discharge time is reduced to  $t_{d,0}$ , which is the same as the discharge time without any keeper. Intuitively, this is the case when the area bounded by the  $I$ - $V$  characteristics of the keeper is negligible, meaning the effective delay keeper strength approaches zero.

### C. Design and Engineering Guidance

Equations (5) and (11) constitute part of the main results of our analytical study. The peak current of the keeper that is required to meet a specified noise tolerance requirement in a design can be calculated by using (5). This peak current value can then be inserted into (11) to obtain an estimate of the discharge time of a dynamic logic gate using the NDR keeper.

On the other hand, (4) and (12) can be used as guidance in engineering the keeper device. As shown in (4), the noise margin of dynamic gates with NDR keeper is solely determined by the peak current  $I_P$  of the keeper. At the same time, (12) shows that the overhead in discharge time can be very close to zero regardless the value of  $I_P$ , as long as the width of the current peak  $W$  is very small. The design implication is that the  $I$ - $V$  characteristic of the NDR keeper should be engineered to minimize the width of the current peak so that the noise immunity of the circuit can be improved with minimal performance penalty.

## VI. EXPERIMENTAL RESULTS

In this section, we describe the simulation results for a number of wide domino logic gates with the conventional keeper and with the proposed smart keepers. The circuits are designed using a 0.18- $\mu\text{m}$  process technology and the simulation is carried out using HSPICE at 1.6 V supply voltage and at a temperature of 55°C.

We first study how gate delay increases when the gate noise robustness level is raised by adjusting keeper size. An 8-input domino OR gate is used as the test vehicle in this study. The load capacitance of the gate is 50 fF and the clock frequency used in the simulation is 500 MHz. The normalized gate delay versus maximum input noise voltage level plot obtained through SPICE simulations is shown in Fig. 18, where *SK1* refers to the MOSFET-based smart keeper and *SK2* refers to the RTD+FET-

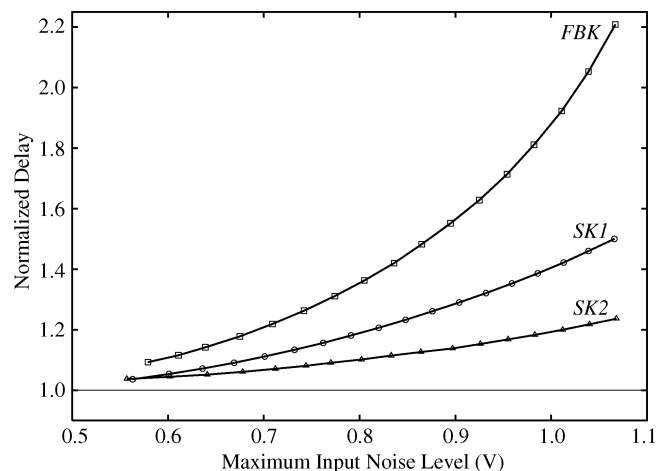


Fig. 18. Normalized gate delay at various gate noise-tolerant levels. (*FBK*: feedback keeper; *SK1*: MOSFET-based smart keeper; *SK2*: RTD+FET-based smart keeper.)

based smart keeper. It is clear that domino logic gates with proposed smart keepers have significantly reduced performance overhead in comparing with the conventional feedback keeper based design. The performance benefit of using the proposed keepers is even greater when the noise-tolerant requirement is high. It is also observed that the intrinsic NDR device based keeper is managed to offer the best in performance among the three designs.

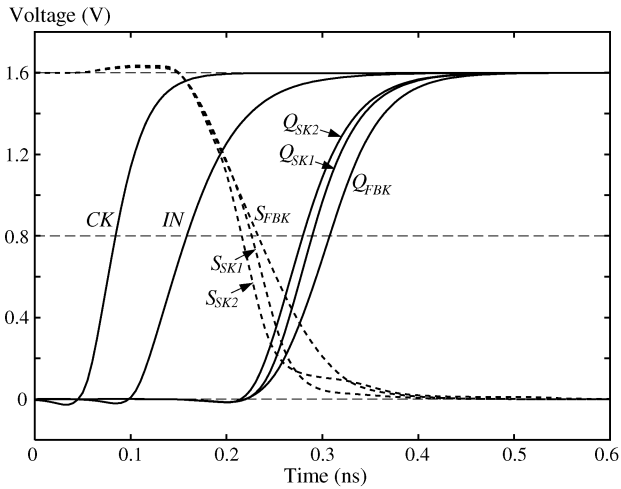
Performance comparisons in terms of both gate delay and power consumption at a set of given gate noise robustness levels are shown in Table II. The percentage values in the table measure the relative gate delay overhead caused by employing the keepers. The gate delay of the bare domino OR8 gate without keeper is 110.0 ps. If one wants to improve the noise tolerance of dynamic logic gates to the level of static CMOS logic gates, the sizes of the keepers should be increased such that the dynamic logic gate is able to resist a dc input noise of approximately half the power-supply voltage (0.8 V in this case). Using the conventional feedback keeper, the gate delay overhead is 35.5%. The delay overhead is reduced to 18.9% if Smart Keeper 1 is employed and is dropped to a mere 10.1% if Smart Keeper 2 is used. When the dynamic gate is aggressively sized to be able to withstand an input noise level of 1.0 V, the feedback keeper causes a delay penalty of 88.2%. On the contrary, the speed overhead is less than 20% using Smart Keeper 2.

Simulated results on gate power consumption are also reported in Table II. Since dynamic logic gates are used mainly in limited logic blocks where circuit speed is critical, the gate power consumption is sometimes less of a concern. Nevertheless, simulation results have also demonstrated that dynamic circuits with proposed keepers have less power consumption than their counterparts employing the conventional feedback keeper. This is mainly because of the faster switching of the internal dynamic node, which results in shorter period of contention. Gates employing Smart Keeper 1 have the least amount of power consumption because the sizes of the two transistors in the keeper are relatively small.

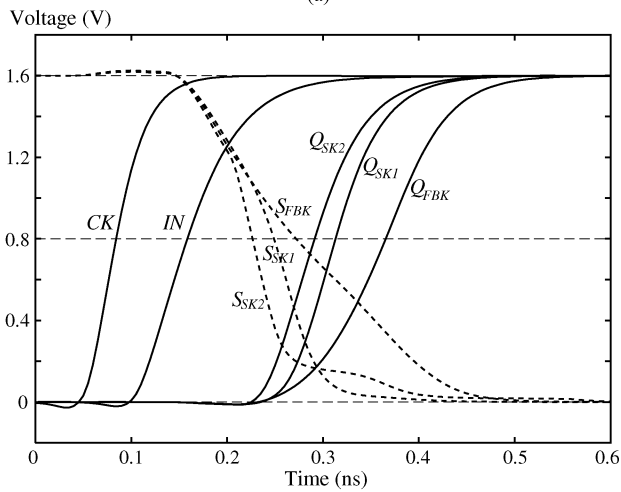
Next, we compare the voltage waveforms of domino gates with different keepers. In the first experiment, we have sized

TABLE II  
PERFORMANCE COMPARISON FOR OR8 AT SAME NOISE ROBUSTNESS LEVEL

Noise Level (V)	Feedback Keeper (FBK)		Smart Keeper 1 (SK1)		Smart Keeper 2 (SK2)	
	Delay (ps)	Power ( $\mu$ W)	Delay (ps)	Power ( $\mu$ W)	Delay (ps)	Power ( $\mu$ W)
0.6	121.8 (10.7%)	149.5	115.9 (5.4%)	141.0	114.9 (4.5%)	151.5
0.7	132.9 (20.8%)	158.7	122.3 (11.2%)	144.5	117.4 (6.7%)	158.1
0.8	149.0 (35.5%)	172.7	130.8 (18.9%)	149.3	121.1 (10.1%)	164.1
0.9	171.9 (56.3%)	193.3	141.5 (28.6%)	155.5	125.3 (13.9%)	176.4
1.0	207.0 (88.2%)	225.1	154.6 (40.5%)	163.4	131.2 (19.3%)	190.5



(a)



(b)

Fig. 19. Comparison of waveforms of domino logic gates with different keepers. (a) Noise-tolerance level at 0.8 V. (b) Noise-tolerance level at 1.0 V.

the keepers such that the resulting dynamic logic gates have same noise tolerance level. The transient waveforms when the inputs are normal signals are compared in Fig. 19. The noise-tolerance levels of the domino gates in Fig. 19(a) and (b) are 0.8 V and 1.0 V, respectively. It is observed that the dynamic nodes of the three circuits discharge approximately at the same rate initially. The difference is that both  $S_{SK1}$  and  $S_{SK2}$  have an accelerated discharge process after the voltage drops below about 1.2 V due to the reduced keeper current. Therefore, in addition to the reduction in  $IN$  to  $S$  delay, the  $S$  to  $Q$  delay is also decreased because of the faster input slope seen by the output driver. Overall, at same noise immunity level, dynamic logic

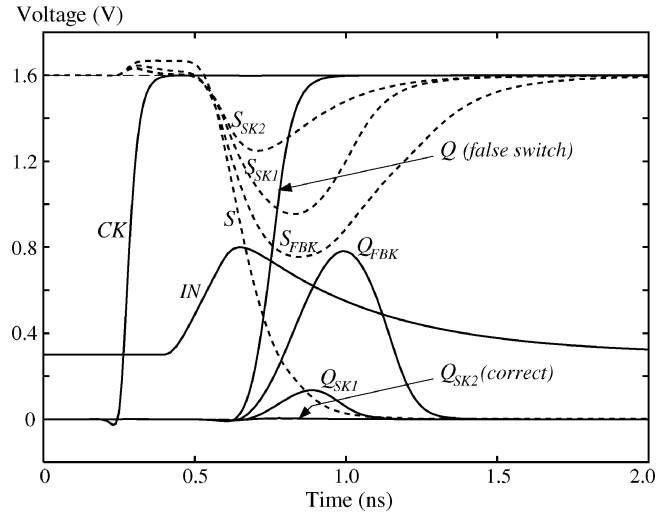


Fig. 20. Comparison of waveforms of domino logic gates with different keepers under noisy input.

gates using the proposed keepers switch considerably faster than their counterparts using conventional feedback keeper.

In the second experiment, we have sized the keepers such that the delay penalty over domino gate without any keeper is no more than 10%. The transient waveforms of the domino gates when the inputs are noisy signals are compared in Fig. 20. We have used an input noise waveform that is composed of both a dc component and an ac component to simulate real noise waveforms, as shown in the figure. The domino gate without keeper fails to operate correctly when this input noise is applied. Using the conventional feedback keeper, the gate output eventually reaches the correct value. However, the output of the domino gate has a large noise pulse, which, when combined with other injected noises like interconnect crosstalk noise at the output node, will lead to potential noise violation at the next gate. The output noise glitch is greatly reduced using Smart Keeper 1. And the output of the domino gate employing Smart Keeper 2 is correct and noise-free.

Logic gates are known to behave as low-pass filters. Gate noise immunity is considerably better against narrow noise pulses. Dynamic noise rejection curve is determined by the locus of the combination of input noise amplitude and duration that cause a gate to switch. An input noise will cause circuit failure if and only if the amplitude and duration combination of the noise lies above the dynamic noise rejection curve. In Fig. 21, the dynamic noise rejection curves of domino gates with different keepers are compared. The rejection curves of the proposed keepers are always higher than that of the feedback keeper meaning that they have higher noise immunity.

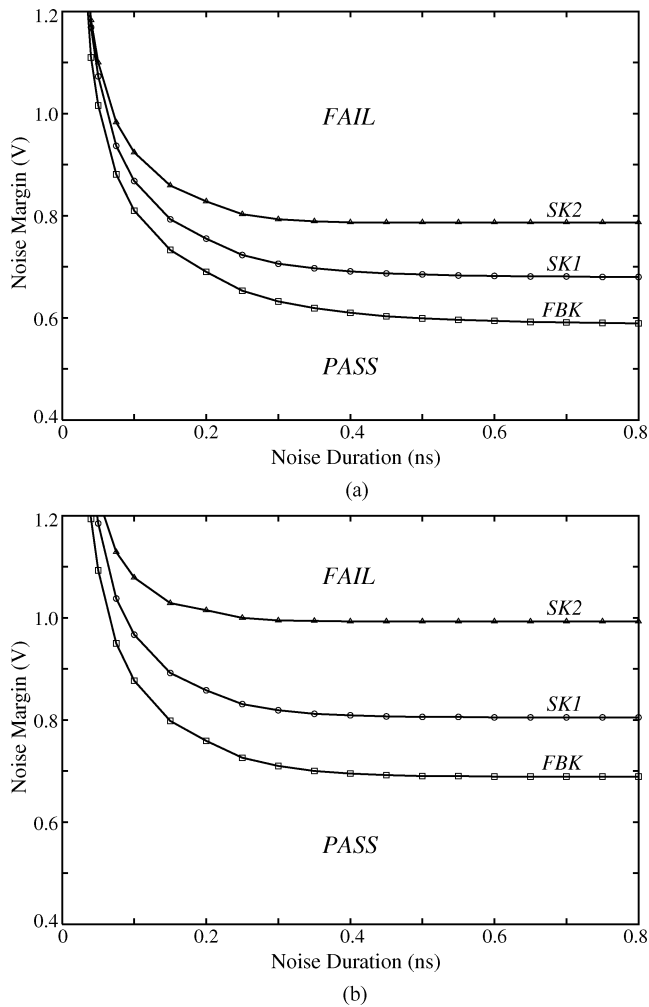


Fig. 21. Dynamic noise rejection curves. (a) When delay overhead is 10%. (b) When delay overhead is 20%.

It is also observed that the difference in dynamic noise immunity among the keepers are reduced when the input noise duration is extremely small. This is essential for high performance operation of dynamic logic gates employing the proposed keepers. This is because there is no real difference between an input noise with very high amplitude ( $\sim V_{DD}$ ) and a narrow duration  $\Delta t$  and the initial portion (from 0 to  $\Delta t$ ) of a normal input. Therefore, the delay overhead will be at least  $\Delta t$  if the combination ( $V_{DD}$ ,  $\Delta t$ ) is below the dynamic noise rejection curve.

We have further compared performance of dynamic logic gates with different keepers by designing a set of wide fan-in multiplexers (MUXes). The circuit schematic of dynamic MUXes used in this study is illustrated in Fig. 22. The number of inputs of the MUXes ranges from 8 to 32. Circuit performance comparisons in terms of both gate delay and power consumption are shown in Table III. The gate delays of bare domino gates without keeper are 122.4 ps, 144.9 ps, and 185.6 ps, respectively, for the 8-bit, 16-bit and 32-bit MUXes.

The delay overhead is a strong function of the gate noise robustness required while it varies little with respect to the number of inputs in the MUXes. At a relatively low-noise robustness

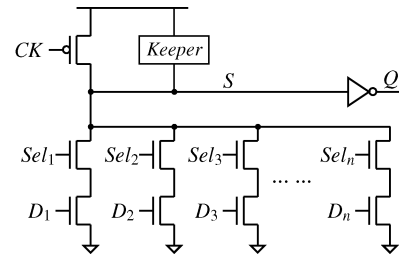


Fig. 22. Circuit schematic of an  $n$ -bit wide dynamic multiplexer.

level of 0.6 V, conventional feedback keeper results in an acceptable delay overhead of 10% on the average. MUXes equipped with NDR keepers, however, have even smaller performance penalty ranging from 3% to 5%. At a medium noise robustness level of 0.8 V, feedback keeper based MUXes are about 40% slower than original gates without any keeper. This penalty is usually too high to overlook in most circuit design applications. On the other hand, the average delay overhead is only 9.4% using Smart Keeper 2. At a very high-noise robustness level of 1.0 V, MUXes with the conventional keeper have a delay which is more than double the delay of the corresponding gates without any keeper. The delay penalty for the proposed smart keepers, on the other hand, can be as low as less than 20%.

Overall, the proposed keepers are consistently and significantly better than the conventional feedback keeper in preserving the performance of dynamic logic gates when gate noise tolerance is tuned up. Furthermore, it can also be observed from the table that the advantage of the proposed keeper is more evident when the gate noise robustness requirement is high. This suggests that it will be more rewarding to use the proposed technique as the process technology continues to scale down aggressively and the noise problem assumes more prominence in noise-aware design methodologies.

Experimental results also support that the noise tolerance of dynamic logic gates can be improved beyond the level of static CMOS logic gates while their advantage in performance is still retained. This is mainly due to the fact that dynamic logic circuits have a single polarity. Input noise signals are of either the low-high-low type or the high-low-high type. For static CMOS gates, when noise tolerance against one type of noise is improved, the noise tolerance against the other type of noise is always adversely affected. For dynamic logic gates, on the other hand, one can aggressively improve gate noise tolerance against the interested type of noise without having to worry about the other type.

## VII. CONCLUSIONS

Effective noise-tolerant design techniques are vital to the success of VLSI circuits as noises become an ever-increasing problem with the relentless scaling of process technology. A desirable noise-tolerant technique should be able to improve circuit robustness against all noise types, be suitable for all logic functions, and have very low overhead in silicon area, circuit speed, and power consumption. In this paper, such a noise-tolerant design technique is proposed.

TABLE III  
PERFORMANCE COMPARISON FOR MUXES AT SAME NOISE ROBUSTNESS LEVEL

Noise Level (V)	MUX (bit)	Feedback Keeper (FBK)		Smart Keeper 1 (SK1)		Smart Keeper 2 (SK2)	
		Delay (ps)	Pwr ( $\mu$ W)	Delay (ps)	Pwr ( $\mu$ W)	Delay (ps)	Pwr ( $\mu$ W)
0.6	8	136.7 (11.7%)	145.8	128.3 (4.8%)	137.2	127.1 (3.8%)	147.4
	16	159.5 (10.1%)	160.9	151.5 (4.6%)	151.2	150.0 (3.5%)	161.5
	32	203.1 (9.4%)	192.7	194.1 (4.6%)	181.3	191.6 (3.2%)	191.4
0.7	8	150.5 (23.0%)	156.0	136.2 (11.3%)	140.9	129.9 (6.1%)	153.8
	16	176.2 (21.6%)	172.5	159.3 (9.9%)	155.0	153.2 (5.7%)	168.0
	32	223.9 (20.6%)	206.9	204.5 (10.2%)	186.2	196.0 (5.6%)	197.9
0.8	8	175.6 (43.5%)	173.4	147.6 (20.6%)	146.4	134.3 (9.7%)	161.9
	16	204.4 (41.1%)	192.3	170.6 (17.7%)	160.5	158.3 (9.2%)	176.4
	32	258.7 (39.4%)	231.6	218.9 (17.9%)	193.3	202.9 (9.3%)	206.5
0.9	8	220.2 (79.9%)	204.2	163.4 (33.5%)	154.1	139.6 (14.1%)	177.4
	16	254.6 (75.7%)	227.6	185.8 (28.2%)	167.9	164.3 (13.4%)	182.2
	32	320.9 (72.9%)	275.9	238.5 (28.5%)	203.1	210.6 (13.5%)	222.8
1.0	8	333.7 (172.6%)	282.6	185.4 (51.5%)	164.8	146.8 (19.9%)	196.6
	16	383.1 (164.4%)	318.4	205.7 (42.0%)	177.8	172.4 (19.0%)	211.5
	32	479.6 (158.4%)	392.2	264.6 (42.6%)	216.3	221.4 (19.3%)	242.7

The main contributions of this paper are as follows. First, we have identified the difference between keeper strength for noise immunity and keeper strength for speed, which opens the possibility for circuit noise immunity improvement without a proportional increase in delay. Second, we have proposed to use a class of circuits having the folded-back  $I$ - $V$  characteristic (the NDR property) to explore the difference in keeper strength for speed and for noise immunity. And third, we have proposed two circuit realizations of the NDR keeper and have demonstrated the potential benefit of the proposed technique.

More specifically, we have shown that the proposed technique improves dynamic circuit noise immunity with little cost in area, speed, and power consumption. Simulation results on large fan-in domino gates have shown that, at a supply voltage of 1.6 V, the dc input noise voltage level can be raised to 0.8 V for about 10% delay overhead and to 1.0 V for about 20% delay overhead. Furthermore, in contrast to most existing noise tolerance enhancing remedies, the proposed technique does not modify/change the pull-down transistor network. Therefore it is easier to be adopted in circuit design practice. We have also shown that it will be more rewarding to use the proposed technique as the process technology continues to scale down and the noise problem becomes more prominence.

The proposed technique is not limited to domino logic gates. It can also be applied to other combinational dynamic logic circuits as well as sequential circuits like latches and flip-flops that have internal precharged nodes. This constitutes one direction of future researches. In the other direction, we will also search for other suitable circuit implementations that aggressively explore the benefit of the noise-tolerant design principle described in this paper.

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**Li Ding** (S'99–M'04) received the B.S. degree in physics from Peking University, Beijing, China, in 1997, and the M.S. and Ph.D. degrees in computer science and engineering from the University of Michigan, Ann Arbor, in 2000 and 2004, respectively.

He was a Graduate Student Research Assistant in the Electronic Engineering and Computer Science Department, University of Michigan, from 1998 to 2003. He has published over 20 journal and refereed conference papers in the areas of VLSI circuits and computer-aided design. Presently, he is a Senior Research and Development Engineer with Synopsys Inc., Mountain View, CA.



**Pinaki Mazumder** (S'84–M'88–SM'94–F'99) received the B.S.E.E. degree from the Indian Institute of Science, Bangalore, in 1976, the M.Sc. degree in computer science from the University of Alberta, Canada, in 1985, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign in 1987.

Presently, he is with the Department of Electrical Engineering and Computer Science of the University of Michigan, Ann Arbor. Prior to this, he was a Research Assistant with the Coordinated Science

Laboratory, University of Illinois at Urbana-Champaign for two years and was with the Bharat Electronics Ltd. (a collaborator of RCA), India, for over six years, where he developed several types of analog and digital integrated circuits for consumer electronics products. During the summer of 1985 and 1986, he was a Member of the Technical Staff in the Indian Hill branch of AT&T Bell Laboratories. During 1996–1997, he spent his sabbatical leave as a visiting faculty at Stanford University, University of California at Berkeley, and Nippon Telephone and Telegraph, Japan. His research interests include VLSI testing, physical design automation, and ultrafast circuit design. He has published over 160 papers on these topics in archival journals and proceedings of the international conferences. He has led his research group's efforts in VLSI testing and built-in self-repair techniques and has developed silicon compilers for RAM, ROM, and PLA with built-in self-repairable capabilities. Two international patents on this research work are pending now. He has also done quite extensive work in the area of VLSI physical design. He has developed a suite of distributed place-and-route tools for VLSI and FPGA chips. He has worked over six years as an integrated circuit designer in semiconductor companies. He is currently leading ultrafast circuit design activities for nano and quantum electronic devices. He has successfully developed CAD tools for high-performance VLSI circuit simulation (NDR-SPICE) and numerous circuit topologies for quantum MOS and other quantum-well devices. Several US and Japanese semiconductor companies including Texas Instruments, Hughes Research Laboratory, Lockheed Martin, NTT and NEC have been collaborating with him on this research work. He is the co-author *Testing and Testable Design of High-Density Random-Access Memories* (Norwell, MA: Kluwer, 1996), *Semiconductor Random-Access Memories: Testing and Reliability* (Rockville, MD: Computer Science), *Genetic Algorithms for VLSI Design, Layout, and Test Automation* (Englewood Cliffs, NJ: Prentice Hall, 1998).

Dr. Mazumder was a recipient of Digital's Incentives for Excellence Award, BF Goodrich National Collegiate Invention Award, National Science Foundation Research Initiation Award and Bell Northern Research Laboratory Faculty Award. He was a Guest Editor of the IEEE DESIGN AND TEST MAGAZINE's Special Issue on multimegabit memory testing, in 1993 and the *Journal of Electronic Testing: Theory and Applications* Special Issue on Memory Testing and Reliability in 1994. He is the Guest Editor of two special issues on emerging nanoelectronic technologies and their applications in IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS (December 1997) and the PROCEEDINGS OF THE IEEE (1998). He is on the Editorial Board of Proceedings of the IEEE, and is also an associate editor of the IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS. He is a member of Sigma Xi, Phi Kappa Phi, and ACM SIGDA.