Pinaki Mazumder's Research Accomplishments

When I started my MS thesis in the field of VLSI in 1984, I was inspired by the local (Edmonton, Canada) hockey legend, Wayne Gretzky whose famous quote ("A good hockey player plays where the puck is. A great hockey player plays where the puck is going to be") had defined the compass of my research activities for the next 33 years as explained below. In *Evolutionary* CMOS research, I solved numerous application-inspired research problems that were 10 to 15 years ahead of their time and eventually Moore's Law has vindicated the practical merits of my research by impacting the memory and FPGA industry as pointed out below. In *Revolutionary* emerging technologies such as quantum tunneling devices, plasmonic devices (in the Terahertz regime), ionic devices (as non-volatile memories), and electron spin current devices (as ultra-low-power memories) I have made sustained impact for the past 20 years by collaborating with multiple leading researchers in universities and companies. In my research career, I have endeavored to emulate the Vannevar Bush model of triad synergy between University, Industry and Government establishments that was conceived at the aftermath of the Second World War to challenge academics to undertake enterprising and leadership role for catalyzing innovations, accelerated economic growth, and sustained US leadership in science and engineering.

I have secured 53 research grants (21 NSF, 18 Department of Defense, 8 Industrial, 2 Korean Govt., and 3 others) amounting to nearly $13 Million (for my share) and over $40 Million (collective) to conduct the above research projects. Diversity, girth, vision, and synergistic problem solving are the hallmark of my group's research that integrates multidimensional knowledge from solid-state devices, circuit theory, numerical analysis, electromagnetic theory, and quantum physics. While such innovative research approach has enabled us to establish the theoretical foundation for solving complex problems in nanoscale VLSI systems, they have also been widely adopted in commercial VLSI systems, thereby providing technology transitioning of our federally and privately funded research work.

I. Evolutionary Research -- Where the Puck is Going to be

My MS thesis described a vision for "multicore parallel processor" (Intel and AMD built multicore chip about 20 years later and on-chip parallel processing is now being widely adopted) by combining VLSI complexity theory, parallel computer architectures, and mathematical theory of chromatic plane ornament[1], which appeared in 3 major computer journals and 3 archival conference proceedings. I extended my MS thesis work to design efficient quad-tree data-structures for 2-dimensional query processing in computer vision, video image processing, and geographical map analysis[2].

1. Conventional Semiconductor Memories

In 1985, when I joined the University of Illinois for my PhD, I was recruited to work in a Semiconductor Research Consortium (SRC) research project to develop new testing methodologies for semiconductor memory chips. At that time, commercial test equipment used simple functional testing methods to detect rudimentary manufacturing defects, and the university research was primarily confined in incremental refinement of functional test algorithms. Since I had worked six years in industrial R&D laboratories after my BS degree, I could envision the need for new way of accelerated memory chip testing with the aggressive increase in density of integration due to scaling. For the first time, I combined the concepts of VLSI process technology, memory layout, circuit design, and theoretical techniques like graph theory and Markov chain modeling to invent "In-line testing" circuitry and comprehensive accelerated test procedures that curtailed "chip testing time" by nearly a thousand times. Please read the

[1] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/MazumderMSThesis.PDF

[2] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/61_Quad-treeDataStructures.pdf

Judgment of European Patent Court in Munich[3], which annulled a Siemens patent on parallel testing of memory cells that used ideas explained in my papers[4].

Also, 10 years after my doctoral work on testable memory design, several semiconductor manufacturers adopted my invention in their products, thereby impacting the DRAM industry. I was hired as Expert Witness to help Samsung, Hyundai, Hynix, Nvidia and Nanya in 10 different major lawsuits. Some of these companies adopted my published papers in their memory products and were later sued by companies who had secured patents based on my research ideas that predated those patents. In 1997, Professor Sudhakar Reddy of University of Iowa, a pioneer in the field of VLSI testing affirmed my fundamental contributions in memory testing: "*Dr. Mazumder was the first to argue that testing of random-access memories will require parallel and built-in testing of RAMs. This is now the practice in both off-line and built-in testing of RAMs*."

My student and I invented an innovative testing method of embedded memories for programming FPGAs through the newly introduced IEEE/JTAG standard for boundary-scan port in 1997. I was hired in 2011 to help Xilinx, Altera, and Lattice Semiconductor who were sued by a test company for infringing on its 2003 patent, which was derived from our previously published papers[5]. Our invention on boundary-scan testing was widely adopted by FPGA industry.

In 1991, for the first time our group developed an efficient *self-healing* methodology for VLSI chips,[6] which was later adapted (in 1997) in our *self-repairable* RAM compiler[7]. In Oct. 1995 by Prof. Kent W. Fuchs who is currently the President of University of Florida at Gainesville recognized my original contributions: "*Dr. Mazumder also initiated the area of built-in self-repair for memories. He was the first to develop designs for embedded repair of memory and computational arrays*." I have coauthored two definitive books on testing and reliability of high-density semiconductor memories that are widely used by VLSI practicing engineers in industry as well as academic researchers. "*Simplicity is the ultimate sophistication*" is the key to numerous design ideas[8] proposed in our books.

2. Emerging Memory Technologies

As conventional static and dynamic random-access memories are confronting multiple formidable challenges with CMOS technology rapidly shrinking to its fundamental limits, our research transcended the realms of conventional memory technologies by pursuing *three* disparate types of emerging memory technologies. We made key inventions that resulted in *five* US patents and several archival journal papers. Our group studied co-integration of quantum tunneling diodes with DRAM and invented key circuit elements for "*tunneling dynamic memory* (TRAM)" technology that eliminated refreshing of DRAM cells and saved energy consumption and soft errors significantly[9]. Our group subsequently invented adaptive programming and erasing techniques for nonvolatile "*resistive memory* (RRAM)" technology[10] that is now poised to replace conventional flash memories due to the superior integration density and lifespan of RRAM memories. Further, to push the frontiers of high-performance and reliable computing by

[3] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/Patent-Annulment.pdf
[4] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/Parametric.pdf;
http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/19_RandomTesting.pdf
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[5] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/30_MarchTests.pdf
[6] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/BISR.pdf
[7] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/BISRAMGEN.pdf
[8] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/ECC.pdf
[9] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/81_RTDMemory.pdf
http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/umera-99.pdf
[10] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/Memristor-Memory1.pdf

developing nonvolatile magnetic memories inside microprocessor chips, my research group has worked on electron spin-based "*straintronics tunneling junction memory* (STJ-RAM)" technology[11]. These memories have life span comparable to conventional SRAM and DRAM, thereby providing a roadmap for magnetic solid-state memories that will slowly replace traditional SRAM-based cache memories as well as the bulk of main memories and solid-state disks that currently employ a combination of DRAM and flash memories.

II. Biology-inspired Disruptive Computing

1. Evolutionary Computing Using Genetic Algorithms

My research group has also done extensive research in biology-inspired computation to develop distributed VLSI chip layout algorithms over networked workstations and desktop computers. Our group developed evolutionary class of algorithms that mimic the Darwinian principle of "survival of the fittest" for biological species by designing multi-dimensional chromosome-encoding schemes to solve various types of VLSI layout automation problems[12][13]. My overall vision in VLSI layout automation was to equip distributed networks of workstations with a specialized hardware accelerator board containing the polymorphic chips developed by my research group to accelerate different styles of VLSI routing algorithms, while Genetic Algorithms would speed up the cell placement algorithms over a cluster of networked workstations. Parallel implementations of the distributed algorithms demonstrated that super-linear speed-ups could be achieved not only for solving VLSI layout problems, but also for a wide variety of engineering problems[14]. In order to promote research in mathematical modeling of the genetic algorithm, I coauthored a book with Dr. Elizabeth Rudnick to illustrate multidimensional genotype encoding schemes and phenotype optimization for different engineering applications[15]. According to Professor Ernest Kuh of UC-Berkeley, who served as the Dean of Engineering and received numerous prestigious awards for his pioneering work in VLSI CAD: "*In physical design he is one of the top leaders especially in developing placement techniques: The genetic algorithms which he is a pioneer in applying to CAD has paid off.*"

2. Biology-inspired Brain-like Neural Computing

Our research in early 1990's to empower VLSI memories and arrays *self-healing* and *self-repairable* by inventing compact neural networks was contemporaneous with Prof. Carver Mead's neuromorphic designs for artificial retina and cochlea on silicon substrates. Inspired by Caltech group's groundbreaking research, we invented hardware-friendly brain-like learning techniques such as spike time-dependent plasticity (STDP), reinforcement learning (Q-learning), and deep learning for real-time in-situ hardware learning. The innovative hardware was implemented on various low-power platforms to significantly accelerate the deployment of emerging Internet-of-Things (IoT) technology. We are presently designing ultra-low-power (ULP) brain-like learning chips with a view to enabling energy-constraint systems to sense, process, organize, and utilize the data more intelligently.

III. Revolutionary Computing using Disruptive Technologies

3. Quantum Tunneling Technology

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[11] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/88_StraintronicsDynStat.pdf
http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/87_TempVariations.pdf
http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/83_StraintronicsRAM.pdf
[12] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/cellplacement.pdf
[13] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/genetic.pdf
[14] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/wolverines.pdf
[15] http://web.eecs.umich.edu/~mazum/Geneti...pdf

In 1992, I started collaborating with my colleague, Prof. George Haddad on a new quantum device, resonant-tunneling diode (RTD) that was originally invented by Dr. Leon Esaki of IBM for which he received Nobel Prize in Physics. The invention of RTD spurred worldwide research for the next-generation digital circuits using quantum-tunneling devices. George's group at Michigan was at that time working on RF circuits using RTDs, but they wanted to develop innovative digital circuits like Dr. Federico Capasso of AT&T Bell Labs, Dr. Gary Frazier of Raytheon, Dr. Gerry Solner of MIT Lincoln Lab, and several Japanese companies like NTT, NEC and Fujitsu. One of the stumbling blocks in the design of digital circuits was that commercial SPICE simulators could not simulate quantum tunneling devices and circuits. Because I had studied quantum physics during my BSc Physics Honors, I started working with Dr. J. P. Sun, who was a postdoctoral fellow in George Haddad's group, to develop the SPICE compatible component models for several types of quantum devices[16], and then my research group made in-depth study of DC and transient analysis mechanisms in Berkeley SPICE simulator. We designed new convergence algorithms and developed Quantum SPICE simulator[17] that attracted several US and Japanese companies to collaborate with my research group in order to accurately simulate their circuits. Our research group received DARPA Research Award for our inventive work on RTD circuits and quantum circuit simulator[18]. Prof. Richard Newton, Dean of Engineering of University of California at Berkeley and a co-inventor of SPICE commented in Oct. 1996: "*I have studied his simulation work for quantum devices (e.g., his extensions to the SPICE program) and found it insightful, solid and practical, a necessary step to extend the research in this area*".

In 1996, DARPA initiated a move to introduce quantum tunneling in commercial VLSI by combining Silicon-based RTDs with CMOS transistors. My research group developed several patented Quantum MOS circuits by working in a consortium of US universities and semiconductor companies. QMOS was our "first" response to the call for discovering Beyond Moore's Law (BML) disruptive technologies that would push the frontier of commercial VLSI industry[19]. At the end, Texas Instruments evaluated the commercial feasibility of QMOS VLSI chips and decided not to introduce QMOS in their production line because of yield and other constraints. Though DARPA ended its premiere Ultra research program in 1999, NSF continued to provide me with research grants to develop QMOS circuit and simulation technology and it may bounce back as commercial CMOS transistors become 3-D. Dr. Alan Seabaugh of Raytheon TI Systems who led the QMOS consortium observed in 1997: "*Dr. Mazumder is unquestionably one of the principal leaders in the design of resonant tunneling circuits, and also unquestionably has simulated the largest systems based on these devices. His designs of RTD/transistor circuits have provided some of the first looks at this technology.*" Dr. Masafumi Yamamoto of NTT Research Laboratories in Japan concurred: "*Dr. Mazumder is regarded as being a leading professional in the field of quantum functional circuit design*."

Subsequently, I undertook more challenging revolutionary computing through fusion of sensing and processing by using self-assembled quantum dots and nanowires. Besides innovations for nanoarchitectures for sensing and in situ data processing, our major contributions entailed solving the Schrodinger equation in three-dimensionally constrained nano-structures and developing suitable transport models for tunneling currents through these structures.[20] But for Hitachi Cambridge Research group in UK, none others had developed such transport models for quantum dots in electronic applications. I also received collaborative grants along with UCLA and Virginia Commonwealth University to fabricate nanocircuits consisting of quantum dots. Further, my research group had

[16] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/RTD-Model.pdf
[17] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/Qspice-TCAD.pdf
[18] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/RTDapp-IEEEP.pdf
[19] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/tvlsi_ntd.pdf
[20] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/quantum%20dot%20modeling.pdf

collaborated with Prof. Leon Chua of UC-Berkeley who invented CNN in 1987[21] and developed several cellular neural networks (CNNs) using quantum dots and quantum tunneling diodes.

4. Terahertz Systems Research – Discoveries and Foundations

The terahertz spectral region, despite significant efforts, is still grossly underdeveloped and underexploited with the main obstacle being an efficient control of the flow of terahertz electromagnetic signals. AFOSR provided me with multi-year funding for developing VLSI applications of plasmonics and invited me to collaborate with Caltech, Stanford and Harvard researchers who received two MURI contracts for developing materials and process technologies for plasmonics devices. We utilized our Quantum SPICE experience to develop for the first time the SPICE-compatible circuit models for plasmonic structures such as nanoparticles and nanowires by developing innovative electrodynamic models[22]. The original intent of this research was to develop an alternative interconnect technology for VLSI chips. However, the signal attenuation in "light on wire" (plasmonics at optical frequencies) interconnect was prohibitively high which led my research group to develop spoof surface plasmon polariton (SSPP) modes that allow terahertz signal to propagate without much attenuation[23]. Terahertz spoof plasmons not only provide solutions to traditional problems such as efficient delivery and control of radiation, but also open new vistas that are unavailable in microwave and too challenging in optical spectral regions.[24] Our work entails three key ingredients of emerging classes of THz applications enabled by SSPP: i) efficient delivery of the THz radiation, ii) precise control over the phase of the THz electromagnetic field, and iii) giant enhancement of the field-matter interaction. My research group has invented several terahertz components such as Boolean switches, interferometer, analog-to-digital converter, and beam-splitter for which we were granted five US patents.

IV. Other Significant Research in CMOS VLSI

Over the course of the last 24 years, my research group has developed many other cross-cutting and synergistic problem solving methodologies for VLSI systems which have been cataloged into 6 different topical areas at my website[25]. Notably, fusion of electromagnetic (EM) theory, VLSI circuit theory, and numerical analysis has led to thermal modeling and failure analysis of electro magnetic radiation effect on integrated circuits[26]. Rigorous VLSI optimization techniques have been developed to maximize the circuit speed, noise, and energy performance metrics[27]. My research group has also designed several types of innovative VLSI chips around new applications such as polymorphic architectures for unified VLSI routing[28], neuromorphic chips for self-repair of VLSI arrays[29], ultra-low-power wireless sensing network (WSN) processor for wearable electronics, and many others as displayed at my website.

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[21] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/Nanoarchitectures.pdf

[22] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/PlasmonicsNanoparticle.pdf
http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/Plasmonics-Nanowire.pdf

[23] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/THz-SSPP1.pdf

[24] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/THz-SSPP2.pdf
http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/tthz-SSPP3.pdf

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[26] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/logtagdouble-4.pdf
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[27] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/CMOStapering.pdf
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[28] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/Routing-layout.pdf

[29] http://web.eecs.umich.edu/~mazum/PAPERS-MAZUM/BISR-mem-layout.pdf