NDR SPICE and QSPICE: Augmented SPICE Simulator Developed by Mazumder's Research Group for RTD and other quantum devices having folded-back I-V.

First augmented circuit simulator version was named NDR SPICE (1994) and was added with simple mechanisms like forced convergence routine to recover from oscillatory (non-convergence) situations in DC simulation. The second version, named QSPICE (1999), was augmented with homotopy-based convergence routine, named RTD-stepping as well as a novel limiting algorithm to overcome the limitations of source stepping and Gmin stepping that are used in commercial SPICE simulators. The component model of NDR and QSPICE were added with a host of quantum tunneling devices, including resonant tunneling diode (RTD), bound state resonant tunneling transistor (BSRTT), resonant tunneling barrier transistor (RTBT), resonant hot electron transistor (RHET), and surface tunneling transistor (STT).

SIMULATION OF QUANTUM ELECTRONIC CIRCUITS

NDR

Personnel

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Introduction

Quantum electronic devices have been widely recognized as future generation devices which will be extensively used in high-performance systems. These devices will be extremely suitable for designing high-speed, low-power nanoelectronic circuits. These devices are gaining increasing importance as the fundamental physical limits of scaling in conventional CMOS technology are becoming apparent. Single and multiple quantum-well devices have been used to experimentally realize a wide variety of high-performance binary as well as multi-valued circuits like arithmetic units, logic gates, multiplexers, counters, A/D converters, etc.

NDR-SPICE

Simulation of circuits containing quantum devices like resonant tunneling bipolar transistors (RTBTs), resonant hot electron transistors (RHETs), surface tunnel transistors (STTs), resonant tunneling HEMTs (RTHEMTs), resonant tunneling diodes (RTDs), etc., present a variety of challenges to simulators like SPICE on a large number of occasions when these devices are modeled using the external voltage controlled current source models. However, it is extremely important to be able to simulate these circuits with accurate device models not only for verifying the circuit ideas, but also for circuit and device optimization, statistical design centering and Monte Carlo analysis.

- accurate, physics-based models
- device-specific DC and transient convergence routines
- no convergence problems
- device code is fined-tuned for optimal performance

NDR-SPICE is an advanced SPICE-based circuit simulator which can handle quantum devices accurately and efficiently without encountering any convergence problems.

Detailed physics-based device model. NDR-SPICE uses physics-based quantum device models derived by self-consistent solution of Poisson and Schrödinger equations. The models are defined by means of ten parameters whose values are supplied by the user. These parameters are easily derived from the I(V) and C(V) characteristics of the devices.

Efficient convergence handling. The NDR devices have extreme non-linearities which can cause SPICE-like simulators to face convergence problems. NDR-SPICE can overcome all such problems. DC operating point and transient analyses are performed with ease.

Minimum simulation time. NDR-SPICE converges to correct solution with minimum number of iterations. This is important for Monte Carlo analysis, statistical design centering, circuit optimization, etc.

Full-Wave Time-Domain Simulation of Quantum Circuits

Fig. 1: Voltage profile for RTD-HBT inverted carry circuit

RTD digital circuits can operate at frequencies close to 100 GHz. At such high speeds TEM and quasi-TEM assumptions are no longer valid. For simulating such circuits, we are developing very accurate full-wave simulation tools. Our current research efforts in circuit simulation are a include full-wave simulation of RTD circuits. By solving Maxwell's curl equations in a finely meshed space containing the circuit and its packaging, we can get very detailed picture of the circuit's behavior at very high speeds of operation. The picture here shows an RTD-HBT inverted Carry circuit layout and its voltage profile generated by our full-wave simulator.

Selected Publications

[1] M. Bhattacharya and P. Mazumder, "SPICE simulation of circuits containing resonant tunneling diodes," *Proceedings of the European Conference on Circuit Theory and Design*, 1999, pp. 663-666.

[2] M. Bhattacharya and P. Mazumder, "Convergence issues in resonant tunneling diode circuit simulation," *13th International Conference on VLSI*, 2000.

[3] S. Mohan, J. P. Sun, P. Mazumder, and G. I. Haddad, "Device and circuit simulation of quantum electronic devices," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 14, no. 6, pp. 653-662, June 1995.

Device and Circuit Simulation of Quantum Electronic Devices

S. Mohan, J. P. Sun, Pinaki Mazumder, *Member, IEEE,* and G. I. Haddad, *Fellow, IEEE*

***Abstract*—Quantum electronic devices such as resonant tunneling diodes and transistors are now beginning to be used in ultrafast and compact circuit designs. These devices exhibit negative differential resistance (NDR) and/or negative transconductance in their I–V characteristics and have active dimensions of a few nanometers. Since the conventional drift-diffusion approximation is not valid for simulation of device behavior at this microscopic scale, quantum simulation models based on the Schrödinger equation are required to accurately predict the behavior of the device. However, these models are too slow for circuit simulation. This paper describes a modeling scheme that maintains the accuracy of the quantum simulation while achieving satisfactory speed for circuit simulation, and is applicable to a wide range of two and three terminal resonant tunneling devices and may also be extended to future scaled-down MOS and bipolar devices. A self-consistent solution of the Poisson and the Schrödinger equations for various bias points is used to build up tables of conductances, capacitances and other parameters. Table-lookup methods are then used during circuit simulation. Convergence techniques have been developed to overcome the problems caused by the NDR characteristics and the lookup-table model in simulation. While implementation details are presented for a resonant tunneling transistor (RTT), models for several other quantum electronic devices have also been implemented in NDR-SPICE.**

I. Introduction

With silicon VLSI technology approaching the limits of scaling and miniaturization, new material systems and device technologies are under investigation for improved speed and circuit compaction. Among the most promising of these are the resonant tunneling devices based on Gallium Arsenide (GaAs), Indium Phosphide (InP), and other III–V semiconductor materials. The electrical performance of these devices is dominated by quantum effects. The devices contain quantum-well structures of nanometer dimensions comparable with the electron wavelength. Consequently, the wave nature of the electrons becomes important in determining the device electrical characteristics and these characteristics are very different from those of larger semiconductor devices such as the conventional MOSFET's or bipolar transistors and the newer devices such as high electron mobility transistors (HEMT's) or heterojunction bipolar transistors (HBT's).

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Quantum electronic devices based on resonant tunneling (RT) through quantum-well/barrier structures exhibit negative differential resistance (NDR) and/or negative transconductance in their *I–V* characteristics [1]. These characteristics have been used to build extremely compact or low-power digital circuits capable of operating at very high frequencies. Capasso *et al.* [1] described extremely compact implementations of multivalued storage elements, frequency multipliers, analog-digital converters, and other applications of resonant tunneling devices. Chang *et al.* [2] describe a low-power logic family similar to I^2L using resonant tunneling diodes (RTD's) and heterojunction bipolar transistors (HBT's). Imamura [3] describes a 1-b full-adder using just 7 resonant tunneling hot electron transistors (RHET's) and a few load resistors. Mohan *et al.* [4] describe a self-latching, picosecond delay logic family using resonant tunneling transistors (RTT's) that provides compact implementations of the majority and latching functions. Seabaugh *et al.* [5] describe a nine-state memory using a single multipeak RTD, while Wei and Lin [6] describe a novel analog to digital converter using RTD's to reduce the number of elements required for a flash type converter from $O(2^n)$ to $O(n)$.

Load lines and approximate equations may be used to design small circuits using passive elements and a few conventional active elements, such as FET's or BJT's. However, the design of more complex circuits and of circuits designed to meet strict specifications on voltage/current levels and fanouts requires the use of a good circuit simulator to accurately analyze the performance of the circuit before it is built. The basis for accurate circuit simulation is the circuit model for the device under consideration. Modeling of RTT's for circuit simulation is a new field; earlier work had focussed primarily on the relatively slower but more accurate modeling for device simulation where the goal is to design a new device with desired properties. This paper presents a device model for resonant tunneling transistors and the incorporation of the device modeling data into a much simpler circuit simulation model. This model has been implemented in SPICE along with new ideas to aid in the convergence of the simulation. The two main contributions of the present work are the incorporation of device modeling data into circuit simulation models and the enhancement of the simulation algorithms to improve convergence in situations where the NDR and piecewise linear characteristics of the devices cause the simulation to oscillate when the actual circuit is perfectly stable. These techniques may also be applied to the simulation of other devices where quantum effects may come into play, such as future scaled-down MOS or bipolar transistors.

A. Device Modeling

The conceptual framework of device modeling can be identified to fall into three levels, i.e., the drift-diffusion models, the Boltzmann transport models, and quantum transport models. If quantum effects are neglected, quantum transport models can reduce to the Boltzmann transport models, while the latter may further reduce to the drift-diffusion models if transient and hot electron effects are neglected. In each of the transport models, the corresponding carrier transport equations are solved within its physical framework and its approximations. Conventional transistors are simulated using the drift-diffusion model, but quantum electronic devices such as the RTD's and RTT's require the self-consistent solution of the Poisson and the Schrödinger equations [7]. These models are computationally expensive and their applicability is usually limited to single-device simulation.

B. A New Modeling Framework for RT Devices

Previous work on circuit modeling for RT devices has been limited to RTD's [8] and quantum modeling has been too complex and slow for circuit simulation. This paper presents a new framework for RT device modeling where a complex quantum model of the device is used to extract circuit parameters such as conductances, transconductances and bias-dependent capacitances, which are then used to build a tabular model for circuit simulation. In addition, the convergence properties of the simulation program are studied and convergence problems caused by the NDR characteristic are identified and resolved by the development and implementation of new convergence algorithms. The following sections describe the quantum modeling of an RTT, the extraction of circuit parameters and the circuit model, the convergence problems caused by the NDR characteristic and the solution, and finally a few sample circuits simulated using the new models. The new modeling framework makes it relatively easy to substitute measured data for the data from quantum simulation. While the RTT model has been implemented based on data from quantum simulation, models for other RT devices such as RTD's and RHET's have been developed based purely on measured values [9].

II. Quantum Modeling of Resonant Tunneling Devices

Various quantum mechanical models have been attempted in modeling quantum devices, such as the kinetic quantum model based on the Wigner function description of electron ensemble, the envelope function model based on the envelope function description of electron states, and more microscopic models based on the empirical tight-binding or pseudopotential calculations.

We now envision a quantum device structure consisting of a quantum barrier/quantum-well region and two or more heavily doped contact regions. The main goal of the modeling calculations is to obtain the device dc *I–V* and small signal *C–V* characteristics by solving the electron transport equations. In the envelope function approach, the transport is initiated by sending *eigenstate* electrons from device contacts into a device structure. The electrons, bearing variable effective mass

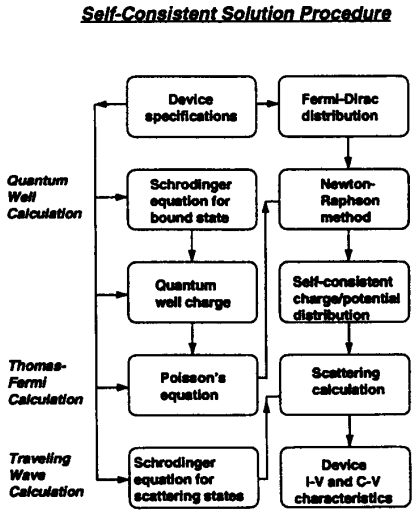


Fig. 1. Self-consistent solution procedure in modeling the quantum devices under study.

in a layered structure, interact with the space-dependent device potential via the Schrödinger equation. Accurate determination of the electron potential profile in a given device structure is therefore critical for the calculation of electron wavefunctions. Once the wavefunctions are obtained, charge, and current densities can be readily calculated.

The Poisson equation relates the electrostatic potential to the charge distribution, in which fixed charge distribution represents ionized impurities (doping profile of the device) and mobile charge distribution represents electron transfer (space charge effects). Since the carrier density responds to the same electrostatic potential it generates, we have a self-consistent problem which entails simultaneous solution of the Schrödinger equation and the Poisson equation. Additional treatment must also be considered for charge in the quantum well(s) to account for the quantized effects, which will be referred to as quantum well calculation. The solution of the Schrödinger equation and the Poisson equation gives self-consistent potential and charge distributions across the device.

When a device is in operation, electrons are injected from the contacts by external electric fields, and the device is driven away from equilibrium. Energy and particle exchanges take place and the device system is open to its environment. This sets up the boundary conditions for the current carrying electron waves in the device model. The incident *eigenstate* electrons traverse through the device while being scattered by the device potential profile. Other scattering processes can also be considered in this calculation. This traveling wave calculation under applied bias voltages requires steady-state solution of the time-independent Schrödinger equation which gives device *I–V* characteristics. The applied bias also modifies the space charge and potential distributions. With the knowledge of these distributions under various bias conditions, the device *C–V* characteristics can be evaluated. Fig. 1 summarizes the general solution procedure outlined above.

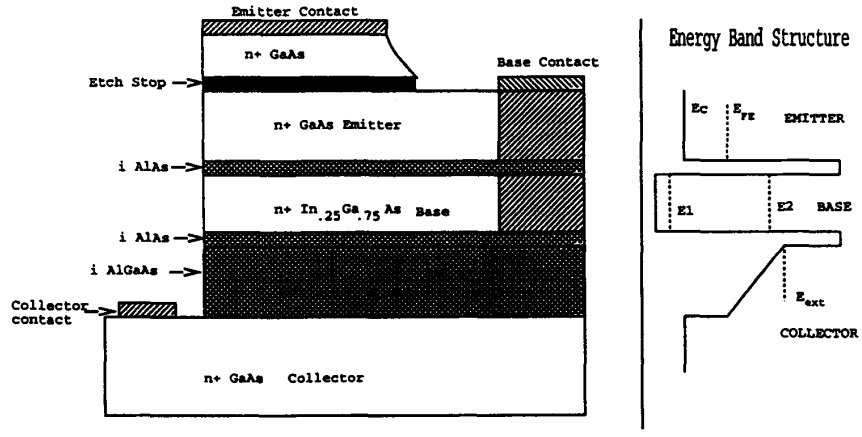


Fig. 2. BSRTT structure and conduction band profile.

The self-consistent calculations for the device models can be divided into three parts and are referred to as the Thomas–Fermi calculation for the self-consistent potential, the quantum-well calculation for space charge in the quantum well(s), and the traveling wave calculation for current density, as shown in Fig. 1. Readers are referred to [10] for more details.

A. Self-Consistent Model of the RTT's

A variety of RTT's, all based on the resonant tunneling mechanism but with different operating principles, has been proposed and demonstrated. Regardless of the particular type of RTT (unipolar, bipolar, field effect, hot electron, or bound state), the transistor action is based on the interaction between the incident electrons and subbands in the quantum well, with the position of the subbands with respect to the emitter Fermi level modulated by the base and/or collector biasing or channel gating. These devices typically present negative differential resistance for a fixed emitter-base bias and negative transconductance for a fixed collector-emitter bias, with multiple current peaks for some RTT variations.

A particular version of the RTT's, also known as the Bound State Resonant Tunneling Transistor (BSRTT), was proposed by Haddad *et al.* [11] at the University of Michigan and Schulman *et al.* [12], independently. A typical BSRTT conduction band structure, which is used for modeling the J_C-V_{CE} characteristics, is shown in Fig. 2. This transistor structure, as proposed by Haddad *et al.*, [11] utilizes a base material with lower band gap than the contact layers. Bound states are created in the narrow quantum-well base. Electrons in these bound states form a low-resistance base region for application of bias to the device. Since these electrons are bound, they will not contribute appreciably to perpendicular base current flow other than for the displacement current between emitter and collector. Current flow is due to tunneling via the second resonant energy level in the well, while the base particle current is due to electron scattering in the quantum-well base. The structure was proposed to alleviate the problem of high base resistance in conventional RTT's. In addition, an extended barrier is placed in the collector region to reduce the leakage current tunneling from the base region to the collector through the base-collector thin barrier in the conventional RTT's. The extended barrier affords additional advantages besides reducing the leakage current. The base-collector capacitance is significantly reduced, so that displacement currents accompanying bias changes across this junction are suppressed. Also, since punch-through from the base to the collector is less likely to occur, the base contact is easier to accomplish. Both theoretical and experimental work on the BSRTT has been conducted [13], [14] and we will, in this section, discuss the self-consistent effect on the device *I–V* characteristics.

The device structure (Fig. 2) to be modeled consists of a double-barrier quantum well (DBQW) and a flat extended barrier of 0.125 eV. The quantum-well base is 80 Å thick and doped at 2×10^{18} cm^{-3}.

To understand the device operation, one needs to study the relative motion of the Fermi level at the emitter, E_{FE}, the bound state levels (especially the second quasibound state E_2) in the quantum-well base, and the top of the extended barrier E_{ext} under various bias conditions. In addition, under sufficient bias thermionic emission and tunneling via the top of the barriers may become dominant in the overall current transport. The resultant current density and the *I–V* characteristics depend on the interplay among these combined effects.

We first examine the J_C-V_{BE} characteristic of the BSRTT structure based on the self-consistent calculation (see Fig. 1). When bias is applied, E_{FE}, the electron Fermi level in the emitter, E_2, the resonant level (bound state) in the base and E_{ext}, the extended barrier level (see Fig. 2) move in accordance with the changes in V_{BE} and V_{CE}. At a fixed V_{CE}, E_{FE} moves upwards and E_2 moves downwards when V_{BE} increases. Keeping track of the positions of the bound states with the bias change indicates that E_2 becomes 36.90 meV, close to E_{FE}, at $V_{BE} = 0.19$ V, and 18.30 meV at 0.26 V. Further increase of V_{BE} will lift E_2 off from the well. This is because the top of the collector barrier at this bias is reduced

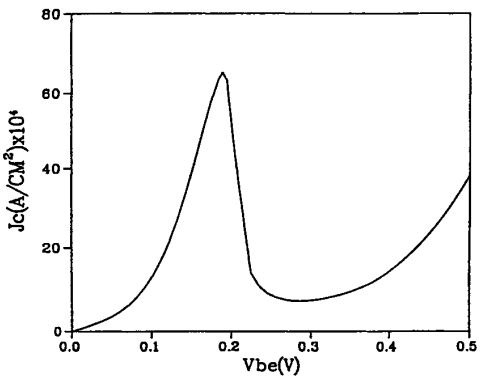


Fig. 3. Collector current density J_C as a function of V_{BE} for the BSRTT structure obtained from self-consistentcalculation.

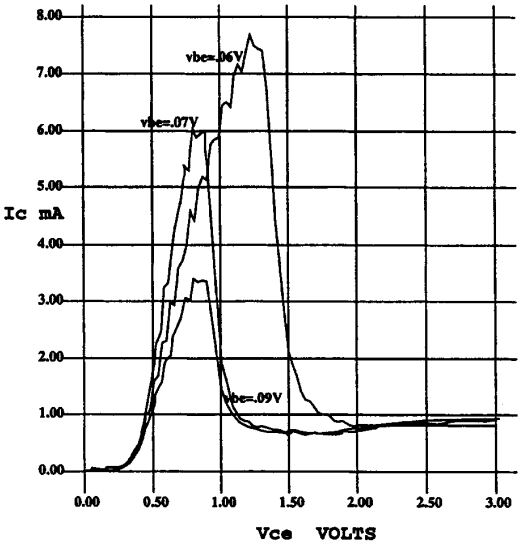


Fig. 4. Collector current I_C as a function of V_{CE} for the BSRTT calculated with self-consistency.

to 0.2184 eV as seen by inspecting the potential profile which is unable to support a second bound state. If we plot the current as a function of V_{BE}, a current peak would be expected corresponding to the alignment between E_{FE} and E_2 at around 0.19 V, and a decrease in current beyond that voltage because there is no resonant state available in the well. The current will increase again with increasing V_{BE} due to the thermionic emission and tunneling via the tops of the barriers. A consistent observation is found in Fig. 3, where the calculated J_C is plotted as a function of V_{BE} for the BSRTT structure.

Next we study the J_C-V_{CE} characteristics of the BSRTT calculated with self-consistency. The inclusion of self-consistency in the device modeling has revealed strong feedback effects in the narrow quantum-well base transistor. In the device model without self-consistency, it was assumed that for a fixed V_{BE}, a change in V_{CE} does not produce any modifications to the emitter-base potential profile, and hence no changes occur for the bound state levels in the base. This assumption is not valid if the bound state charge in the base is not sufficient to keep the base at equilibrium. Since the base does not behave as a perfect shield, at sufficiently large collector bias, further increase in the collector bias will have an appreciable feedback from the output port to the input port, including the base region. The bound states in the quantum well will shift in energy due to the changes in the emitter-base potential profile; the actual emitter-base potential difference may deviate from its nominal value set by V_{BE}. These effects are likely to cause the device to be off resonance and the collector current will drop significantly, leading to the NDR in the BSRTT's.

The calculated I_C versus V_{CE} characteristics of the RTT, with self-consistency, are shown in Fig. 4. These characteristics have also been observed in device measurements [14]. Calculations without self-consistency, on the other hand, would have produced I_C versus V_{CE} characteristics similar to conventional BJT characteristics, contradicting the observed characteristics of this device.

III. Incorporation of the RTT Model in SPICE

In constructing a circuit model for RTT's, it is assumed that the electron transport follows small changes in applied voltage/current in a quasistatic manner, and hence the circuit elements in the model can be approximately evaluated using the model calculation with the time-independent Schrödinger equation. This assumption implies that the circuit model may be valid up to a certain high frequency range. Further increase in frequency may require device simulation in the time domain. As outlined above, the collector current (density) is calculated as a function of both V_{BE} and V_{CE}. Similarly, the charge/capacitance is calculated as a function of the base, emitter and collector voltages, based on the quantum modeling scheme outlined in Fig. 1.

In the present circuit model, the RTT is considered to be a voltage-controlled current source. R_b is the base resistance which accounts for the charging and discharging effects of the capacitance between the emitter and base. The current transport in the circuit model is represented by the voltage-controlled current source $g_m V_{BE}$, and the collector resistance R_C. In the following discussion the collector resistance is represented as an equivalent conductance $g_{ce} = 1/R_C$

$$g_m = \left(\frac{\partial I_C}{\partial V_{BE}}\right)_{V_{CE}} \tag{1}$$

$$g_{ce} = \left(\frac{\partial I_C}{\partial V_{CE}}\right)_{V_{BE}}. \tag{2}$$

As discussed in the above section, since the BSRTT operates based on the bound state charge and second resonant level in the base, g_m may be negative for certain bias ranges. Given a table of current values I_C as a function of the voltages V_{BE} and V_{CE}, the values g_m and g_{ce} are tabulated based on the above definition. For the large signal circuit model, both g_m and g_{ce} are functions of V_{BE} and V_{CE}. Hence the change in collector current for a small change in base and collector voltages may be represented as

$$\delta I_C = g_m \cdot \delta V_{BE} + g_{ce} \cdot \delta V_{CE}. \tag{3}$$

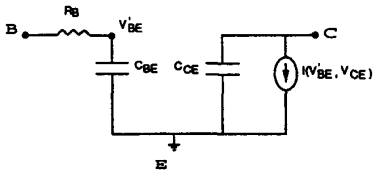


Fig. 5. A large signal circuit model of the BSRTT.

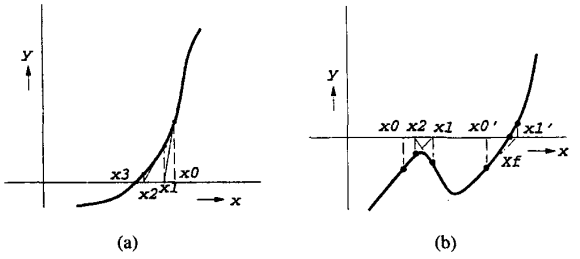


Fig. 6. Convergence of NDR circuits depends on the initial guess. (a) Convergence of Newton–Raphson iterations for general function. (b) Oscillations in Newton–Raphson iterations for NDR circuit with wrong initial guess and convergence with right initial guess.

However, in actual circuit operation, the operating point of a circuit may abruptly shift from one positive differential resistance region of the I_C-V_{CE} curve to the other, corresponding to a large change in V_{CE}. When δV_{CE} is large, the above equation for calculating the current is no longer valid, since the error is large. Hence I_C is calculated directly from the given values of V_{BE} and V_{CE}, this calculation being somewhat more tedious than the quick calculation of δI_C from the above equation. However, the g_m and g_{ce} values are still required in the computation of the Jacobian used in the basic circuit equation solved in each iteration of the simulation algorithm [15]. When abrupt discontinuities in the device current or voltage are seen, special convergence algorithms, described below, are used to force the simulation to converge to the correct state.

The capacitances in the circuit model are defined as

$$C_{BE} = \frac{\partial Q_{BE}}{\partial V_{BE}}, \tag{4}$$

$$C_{BC} = \frac{\partial Q_{BC}}{\partial V_{BC}}. \tag{5}$$

where Q_{BE} and Q_{BC} are the charge between the emitter and base, and the base and collector, respectively. Changes of the charge at both sides of the barriers and the bound state with bias are calculated to give the values of the capacitance. The contact resistances and the electrode resistance are not considered in this device intrinsic model (see Fig. 5). Note that although this circuit model for RTT's resembles the hybrid-π model for BJT's, the circuit elements in the model now represent very different mechanisms of the transistor operation and are calculated based on a quantum model.

Tabulated values for I_C as a function of V_{CE} and V_{BE} are obtained from device simulation, as are values for the capacitances. These tables are read by the initial setup routines of the new NDR model implemented in SPICE. The

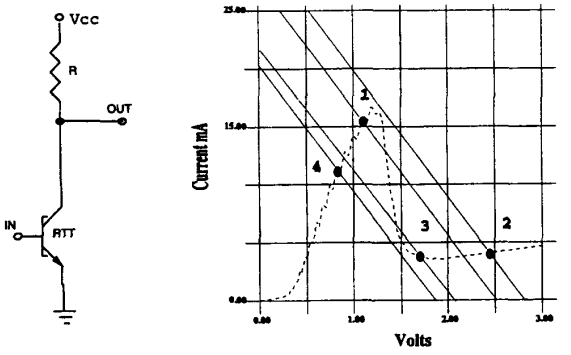


Fig. 7. RTT circuit and load line used in convergence experiment.

conductance and transconductance values are calculated from the current table and stored in separate tables so that they do not have to be recomputed each time during simulation. With the implementation of the table-lookup current source/transconductance model, the complete model described above may be incorporated into the device routines, where the nodal equations for the elements are formulated. The details of nodal equation formulation for passive elements and controlled source, and simulation are described adequately in the literature (see for example [16] and [15]) and will not be discussed here. The new element here is the table driven current source/transconductance. Given the values of V_{BE} and V_{CE}, the values of current, conductance and transconductance are obtained by linear interpolation from the tables and added/subtracted from the corresponding LHS/RHS nodes in the equation formulation step of SPICE [15].

A. Convergence Problems Due to the NDR Characteristic

SPICE uses Newton–Raphson iterations to solve nonlinear circuit equations. Newton–Raphson iterations are guaranteed to converge when the initial guess is close to the actual root of the equation. Consider for example, a simple circuit consisting of a voltage source, a resistor and an RTT in series (see Fig. 7). Let the base voltage of the RTT be held constant so that the current through the RTT is described by $i = g(v)$ where the function g describes the NDR characteristic. Then the nodal equations for the circuit can be written in the form $f(V) = 0$, where $f(V)$ is a nonlinear function of the voltage vector V. In the case of the simple circuit above, the circuit may be described by a single scalar equation $f(v) = 0$, where v is the voltage across the RTT and $f(v)$ has the form shown in Fig. 6(b). When the Newton–Raphson method is used to find the root of the nonlinear equation, the choice of a correct initial guess is crucial in determining the solution obtained by the algorithm. Fig. 6(a) shows a typical function of one variable x and shows the progress of the Newton–Raphson iterations starting from an initial value of $x0$ and converging to the root of the function $g(x)$. Fig. 6(b) shows a typical function $f(x)$ associated with NDR circuits. The function $f(x)$ may, for instance, represent the total collector current through an RTT and a series load resistor. When the initial guess for Newton-Raphson iterations is $x0$, successive iterations produce the

following sequence $x0$, $x1$, $x2$, $x1$, x_2, $\cdots$. This oscillation is a direct consequence of the shape of the function and the initial starting point. If the initial guess were moved to $x0'$ the solution quickly converges to X_f, the root of $f(x)$. Hence the choice of the initial guess is crucial in determining the convergent/oscillatory behavior of the simulator.

For dc simulations using SPICE, a good initial guess can be specified by the user. However, for dc transfer curve or transient simulation, SPICE automatically takes the solution from the previous simulation point (previous bias point for dc transfer curve or previous time point for transient analysis) as the initial guess for the solution at the current point. Referring to the example of the circuit described earlier, the previous simulation point could have had a smaller applied voltage, leading to a solution at $x0$ in Fig. 6. The new simulation point has a larger applied voltage and a single solution point X_f. But the wrong initial guess due to the previous operating point causes the simulation to oscillate.

SPICE employs several techniques to aid convergence [17]. *Gmin stepping* changes the value of the minimum conductance between nodes; *source stepping* reduces all voltage sources to 0 and then slowly steps them up to the actual value; *device limiting* prevents the voltages and currents of devices with exponential characteristics, such as p-n junctions from going out of range. However, none of these techniques is of use in the simple example shown in Fig. 6(b), if the initial guess is $x0$. Changing the value of gmin does nothing to affect this particular problem. Reducing sources to 0 and then stepping them up, still produces the same initial guess $x0$ in some cases. In some other cases involving dc analysis convergence is produced as follows. Assume the RTT in the simple resistive load circuit has two stable points at the previous simulation point and exactly one stable point corresponding to the second positive differential resistance region at the current simulation point. If the previous simulation had found the stable point in the first positive differential resistance region as the solution point, the dc simulation for the current point (obtained by increasing the supply voltage) oscillates, since there is a big jump in the operating point over an NDR region. If the RTT characteristics are such that there is just one stable point for small values of V_{BE} and V_{CE}, corresponding to the second PDR region, this solution point provides a good starting point for future source stepping iterations where both the input and supply voltage are increased simultaneously and the iterations converge to the right solution. Hence source-stepping is not guaranteed to force convergence. Device limiting is not applicable here. The only trick that can force convergence to the right solution is the choice of $x0$' as the initial solution, but there is no existing routine in SPICE to do this. The reason for this limitation in SPICE is that the none of the basic devices such as BJT's, FET's and passive elements which are modeled in SPICE have a folded *I–V* or NDR characteristic.

Hence the following algorithm was implemented to identify oscillatory conditions in simulation (i.e., the simulation does not converge even when the circuit itself is not oscillatory) for the RT elements in the circuit and force convergence. The I_C-V_{CE} characteristic of an RTT for a fixed V_{BE} is split into three regions—the initial region of positive differential resistance, the negative differential resistance region, and the second region of positive differential resistance. Within each region, the characteristic is represented by one or more piecewise linear segments, depending on the number of data points obtained from quantum simulation or device measurements.

```
CONVERGENCE ALGORITHM FOR MULTI-SEGMENT
PIECEWISE LINEAR NDR CURVE
<preprocessing>
    read table of current values
    tabulate conductance and
    transconductance values
<simulation>
    at each time point, for each RTT
        find the direction of change of V_CE
        update LL = (D, L) = direction and
            length of longest monotonic
            run of changes in V_CE
        store LL in the state vector of
            the device
        if (timestep < k*DELMIN) or
        if other convergence routines
            have failed
            CALL force routine
            /* DELMIN is the minimum
            time step and k is a constant.
            The time step is repeatedly
            reduced when there is no
            convergence. If the time step
            equals DELMIN, the simulation
            is aborted. Else, when
            convergence is reached, the
            time step is increased at each
            time point so long as it is
            smaller than the maximum
            time step allowed.
            */
CONVERGENCE ALGORITHM:
THE FORCE ROUTINE
if the device V_CE is oscillating then
    if LL has direction D = INCREASING
      max = highest V_CE in the oscillation
      imax = index of max in the g_ce table
      iforce = smallest index > imax
          such that g_ce[index] >= 0
      use iforce instead of V_CE to calculate
          current, g_ce and g_m
    else if LL has direction D = DECREASING
      min = smallest V_CE in the oscillation
      imin = index of min in the g_ce table
      iforce = biggest index < imin
          such that g_ce[index] >= 0
      use iforce instead of V_CE to calculate
          current, g_ce and g_m
```

Fig. 7 shows the RTT circuit and loadline used to demonstrate the convergence problem and the solution. The base voltage of the RTT is held constant while the supply voltage is first ramped up and then ramped down. As the supply voltage is ramped up, the voltage at the OUT node increases from

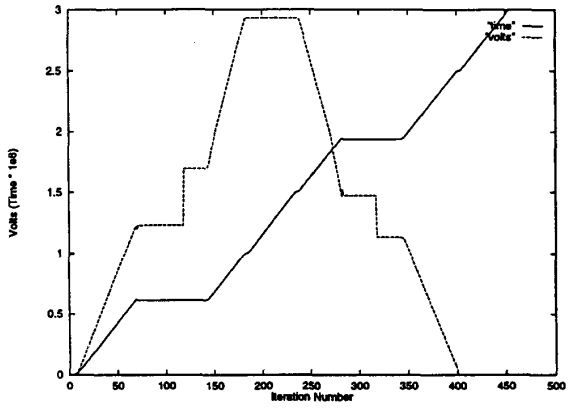


Fig. 8. Output voltage and time as a function of iteration number for RTT/resistor circuit.

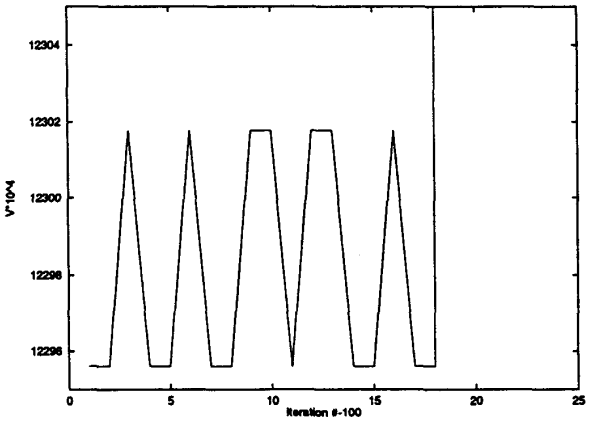
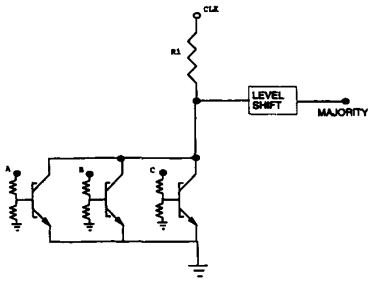
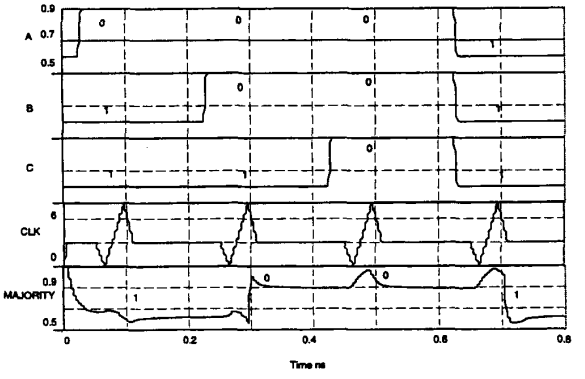


Fig. 9. Closeup of output voltage, showing oscillation.

0 to the point labeled 1 on the RTT characteristic. A slight increase in V_{cc} then causes the operating point to jump to 2. However, when SPICE uses the point 1 as the starting point for Newton–Raphson iterations when the solution is at point 2, the algorithm fails to converge. This is illustrated in Figs. 8 and 9. Fig. 8 shows the output voltage and time as a function of the iteration number. It can be seen that the timestep becomes very small, starting at around iteration 50 and the time hardly increases until almost iteration 150. The output voltage is also constant in this figure, up to iteration 120 or so. When viewed at a higher magnification in 9, it can be seen that the voltage is actually oscillating until iteration 118 when the convergence algorithm forces convergence to point 2. Hence the voltage jumps to approximately 1.7 V and the time step starts increasing. However, until iteration 150, approximately, the time step is still so small that the output voltage and time appear to be almost constant in Fig. 8. A similar pattern of oscillation followed by forced convergence is seen when the supply voltage V_{CC} is ramped down and the output voltage jumps from point 3 to point 4. It may be noted here that the points $1 \cdots 4$ in Fig. 7 are only symbolic and do not represent the actual voltages and currents in Figs. 8 and 9.



(a)



(b)

Fig. 10. Self-latching majority gate. (a) Circuit. (b) Simulation results.

It may be noted here that the new convergence routines apply only to the specific resonant tunneling devices that are causing the simulation algorithm to oscillate. The basic SPICE algorithms for solving nonlinear equations have not been modified. The new convergence routines are analogous to the device limiting/convergence methods applied to specific conventional devices such as diodes or bipolar junction transistors [15], and are part of the device modeling routines rather than the main simulation program. Hence the behavior of the SPICE program when simulating other devices is not adversely affected by the new device model and convergence algorithms.

B. Simulation of Large Circuits Using the RTT Model

The implementation of the large signal RTT model and convergence algorithms has allowed fairly large RTT circuits to be designed and simulated. In particular, a complete set of basic logic gates was designed using RTT's [4] and an adder circuit containing 10 s of RTT's was simulated [18]. Fig. 10(a) shows a circuit containing just 3 RTT's that implements the *Majority* or *Carry* function [4]. Whenever two or more of the inputs are at logic 1, the output is at logic 1; otherwise the output is at logic 0. However the added attraction of this circuit is that it is self-latching and the output does not change until a clock signal is applied, as seen in Fig. 10(b). The self-latching feature of this logic family implies that maximally pipelined circuits with each level of logic corresponding to a pipeline stage, can be designed without incurring the area or

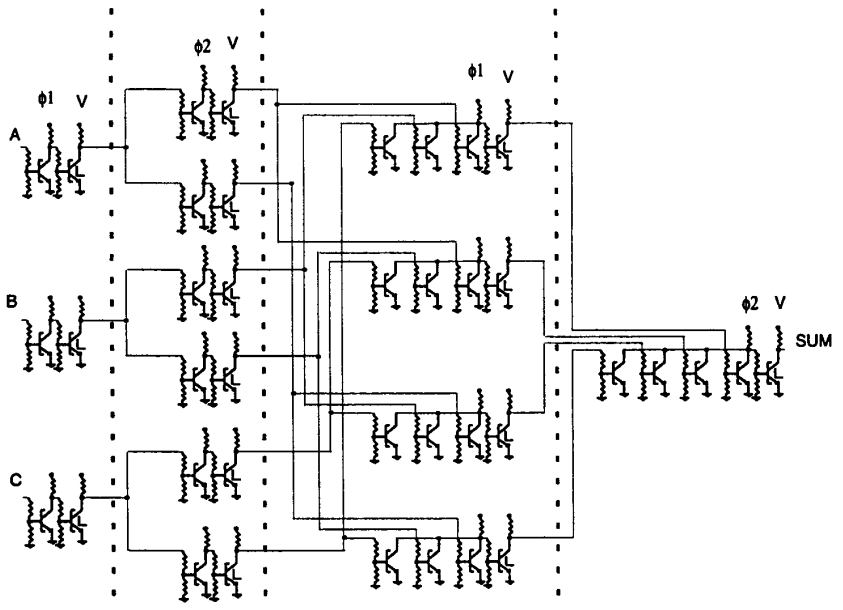


Fig. 11. Pipelined adder circuit using RTT's.

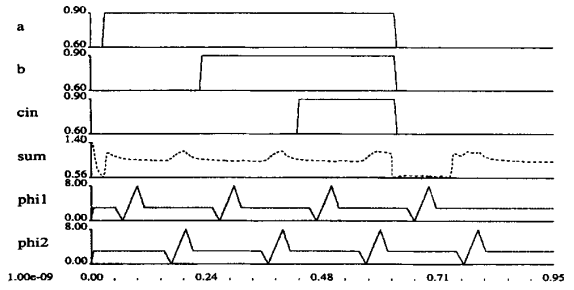


Fig. 12. 1-b adder SPICE output showing inputs a, b, cin, clocks, and sum output; higher voltage level of signals corresponds to logic 0.

TABLE I
SIMULATION TIME AND MEMORY FOR RTT CIRCUITS

Circuit Name	RTTs	Other devices	time pts	datasize	runtime (seconds)
inverterS1	2	15	1862	344064	10.750
or	4	26	1200	352256	13.190
trubist3	4	27	950	360448	9.030
trubist4	5	33	1050	360448	12.240
combN	5	33	950	368640	12.020
2level	12	75	1300	405504	49.890
3level	15	93	500	425984	26.750
and	12	75	200	405504	5.960
sum	22	124	1200	491520	57.090
or3	36	198	600	548864	51.580
comb1N	45	279	1650	888832	298.290

time penalty of extra pipeline latches. This pipelining scheme has been called nanopipelining [18]. Fig. 11, a pipelined adder circuit containing 39 RTT's was designed with the help of the simulator, and Fig. 12 shows the simulation output for this circuit. It was shown in [18] that four such adders, with a ripple carry scheme, along with a buffering and feedback scheme for the carry out of the last bit, could achieve a throughput of 1 32-b addition every 1.5 ns.

Table I shows the simulation time and the data memory required, for several different RTT circuits. All measurements were made with NDR-SPICE running on a Sun SPARCstation 1 machine with 16 Mbytes of memory, with a 20 MHz CPU and FPU, benchmarked at 1.4 M flops [19]. The circuit shown in Fig. 10(a) is called 'trubist3' in the table, and the RTT count includes one RTT in the level shifter. The 'other device' counts for all circuits in the table include the capacitors and resistors from the RTT model. The 'time pts' column in the table is just the simulation time divided by the maximum allowed time step for the simulation algorithm. The time step is dynamically adjusted to ensure accuracy and maintain simulation speed. Hence this is a lower bound on the number of simulation time points. The large circuit shown in Fig. 11 appears as 'comb1N' in the table. The device counts there are somewhat higher due to the addition of some buffer circuitry. The simulation time is a function of the circuit complexity and the number of simulation time points. Sharp discontinuities in node voltage/current waveforms cause the simulator to reduce the time step, i.e., increase the number of time points, in order to maintain accuracy. In all except the last example, the total run-time is less than a minute, for circuits containing as many as 36 RTT's. In contrast, the quantum simulation of a single RTT to obtain the device characteristics takes two days on a similar machine. Hence the table-driven model is orders of magnitude faster than the quantum model, and is fast enough to be used in circuit simulation.

While the technology for fabricating 3-terminal RTT's is still not sufficiently advanced to build the circuits described above, it is possible to verify the operating principles of these circuits using the simpler RTD's in conjunction with bipolar transistors. RTD's are two terminal devices with the

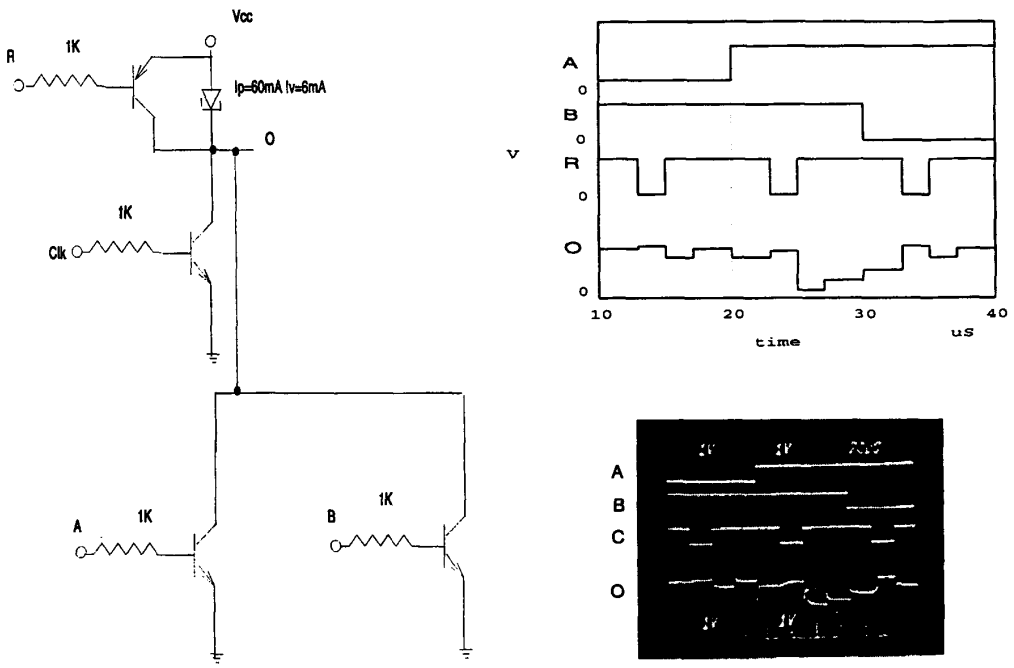


Fig. 13. RTD + bipolar transistor circuit showing simulation results and oscilloscope traces.

same double barrier structure as the RTT's but without the base contact and the collector barrier. The RTD exhibits NDR characteristics corresponding to just one of the curves shown in Fig. 4. Hence the RTD may be simulated using the RTT model, with the base voltage held constant. The same convergence problems associated with the circuit of Fig. 7 are observed when the RTT with the fixed base voltage is replaced by an RTD. Several RTD + bipolar transistor circuits have been successfully simulated and built, verifying the accuracy of the simulation model and the efficacy of the convergence algorithms. An example RTD + bipolar circuit is shown in Fig. 13, along with the simulation results and the oscilloscope traces. Several other examples may be seen in [20].

IV. Conclusion

A modeling scheme for quantum electronic devices that encompasses both quantum modeling results and measured *I–V* characteristics of resonant tunneling devices has been developed. This scheme has been used in developing and implementing models for RTT's, RTD's, RHET's, and MRTD's in NDR-SPICE, an enhanced version of *spice-3e* that contains new convergence routines to force the simulator to converge to the right solution for circuits containing the new NDR devices. NDR-SPICE has been used to simulate circuit designs using RTT's, RTD's and other supported devices. Reference [4] describes two new logic families using RTT's, designed and simulated with the help of the RTT models described above, implemented in NDR-SPICE and [20] describes new multiple-valued logic circuits designed using RTD's, RHET's and RTBT's and simulated with NDR-SPICE.

The quantum device modeling scheme described here has been applied to RTT's and RTD's and is now being applied to RHET's. The table-driven approach using simulated values from the quantum device model has allowed the simulation of circuits using new devices leading to a very short time lag between the fabrication of a new device and the design of circuits using these devices. The link between device simulation and circuit simulation established here, has allowed circuit designers to design circuits with a high degree of confidence even before the device is fabricated and to quickly optimize the design as soon as device measurements are available. This method may readily be extended to the circuit simulation of future scaled down MOS and bipolar transistors, where tables derived from quantum modeling can be augmented with convergence algorithms for fast and accurate circuit simulation.

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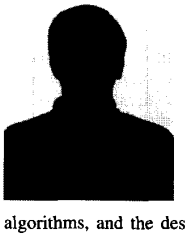

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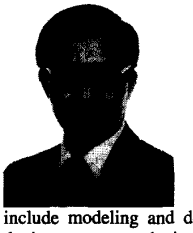

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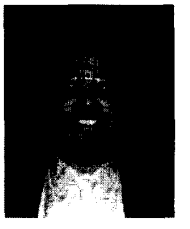

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Augmentation of SPICE for Simulation of Circuits Containing Resonant Tunneling Diodes

Mayukh Bhattacharya and Pinaki Mazumder, *Fellow, IEEE*

***Abstract*—This paper describes the incorporation of an accurate physics-based model of the resonant tunneling diode (RTD) into Berkeley SPICE version 3F5 and addresses the related direct current (dc) and transient convergence problems caused by the negative differential resistance (NDR) and the exponential nature of the device characteristics. To circumvent the dc convergence problems, a new continuation technique using artificial parameter embedding and a current limiting algorithm are proposed. The studies made in this paper have shown that these techniques are superior to the in-built continuation methods of SPICE, such as Gmin-stepping and Source-stepping, for a large number of circuits of varying sizes. To improve transient convergence performance, the following three algorithms are added to SPICE: a modified forced-convergence algorithm, a new time-step adjustment algorithm, and a modified device voltage prediction algorithm.**

***Index Terms*—Circuit simulation, convergence, Newton–Raphson, resonant tunneling diode, SPICE, tunnel diode.**

I. Introduction

RESONANT tunneling diodes (RTDs) are the fastest switching semiconductor devices currently available in the commercial market. RTDs, in conjunction with high-speed three-terminal devices like high electron mobility transistors (HEMTs), heterojunction field effect transistors (HFETs), and heterojunction bipolar transistors (HBTs), etc., can be co-integrated to design a variety of compact and ultrafast digital circuits [1]. The simulation of RTD circuits requires the development of a RTD device model, which will not only accurately represent the input–output characteristics of the RTD, but will also be suitable for implementation in an existing circuit simulator, like SPICE. The main problem with resonant tunneling device models, incorporating quantum transportation of electrons through a double-barrier structure, has been that their current-voltage relationships have involved complex integrals, making them extremely unsuitable for circuit simulation [2]. As a result, NDR-SPICE [3]—one of the few circuit simulators with in-built RTD models—was based on a piecewise-linear RTD characteristic. The recent development of a physics-based analytical current-voltage equation for the RTD [4] has paved the way to the development of a more accurate simulator.

From the similarities between the nature of the I–V curves of tunnel diodes and RTDs, it can be concluded that if the tunnel diode model was part of the device library of Berkeley SPICE, simulating RTD circuits using such a simulator would be quite simple. However, even though the invention of the tunnel diode by Esaki [5] predates the monolithic fabrication of integrated circuits (ICs), the most popular circuit simulation programs did not introduce any tunnel diode model in them. The main reason behind this is that the development of Berkeley SPICE [6] did not commence until the early 1970s, while the tunnel diode, which could not be monolithically fabricated along with other silicon devices, remained primarily a discrete device and was sparingly used in low-noise amplifier circuits [7].

In this paper, we discuss the incorporation of the physics-based model of the RTD into the widely used circuit simulator SPICE 3F5, originally developed at the University of California at Berkeley [8]. We also present a few algorithms that have been demonstrated to substantially reduce the number of convergence problems that the basic circuit simulation procedure of SPICE 3F5 may face when simulating RTD circuits. The contributions of this paper include: 1) a new continuation technique (RTD-stepping); and 2) a modified current iteration method. These dc convergence programs are found to be more effective than the in-built continuation methods used in SPICE, namely Gmin-stepping and Source-stepping. Our contributions also include: 1) a modified forced-convergence technique; 2) a new time-step adjustment algorithm; and 3) a modified device voltage prediction algorithm, which is shown to be effective in minimizing transient convergence problems.

It is widely accepted that leading commercial simulators, such as PSPICE of MicroSim, HSPICE of Avant!, and SPECTRE of Cadence Design Systems, exhibit significantly better convergence performances compared to Berkeley SPICE [9]. Therefore, at the outset we must emphasize that numerous limitations of the SPICE program, some of which we have unraveled in this paper, may not be uniformly attributed to many of these commercial simulators. Unfortunately, due to the inaccessibility of their source codes, we are unable to test the behavior of these simulators with the RTD model as a part of their device libraries. On the other hand, thanks to the generous policy of the developers of Berkeley SPICE, the easy availability of its source code has enabled us to conduct extensive experimental studies with the RTD model using this simulator. It is to be noted that the work presented in this paper does not involve building a completely new circuit simulator for the purpose of simulating RTD circuits. However, we intend to show how to augment a circuit simulator such as Berkeley SPICE 3F5 by incorporating accurate and efficient convergence routines so that highly nonlinear circuits consisting of RTDs can be reliably simulated.

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The organization of the rest of the paper is as follows. In Section II, we present a brief survey of the state of the art in RTD circuit simulation. In Section III, the incorporation of the physics-based model of [4] into SPICE 3F5 is described. In Section IV, the potential dc convergence problems are identified and solutions are proposed. In Section V, the transient convergence problems are explored and ways to minimize them are proposed. In Section VI, the performance of the simulator, with and without the various algorithms proposed in this paper, is studied. Section VII concludes the work summarizing the contributions.

II. RTD Circuit Simulation Status Review

Over the last decade or so, different device models have been adopted for simulating RTD circuits. The various models reported in the literature can be classified under two major categories: the *physics-based models* and the *nonphysics-based models*. The nonphysics-based models can be further classified into *piecewise-linear (PWL) models* and *non-PWL models* to facilitate further discussion.

The nonlinear tunneling characteristic of a RTD can be approximated using the appropriate number of linear pieces. The simplest of the PWL models [3] consists of three linear pieces representing the first positive differential resistance (PDR1), negative differential resistance (NDR), and the second positive differential resistance (PDR2) regions, respectively, as shown in Fig. 1(a). Many real RTDs possess a nonlinear PDR1 region, which cannot be adequately modeled by a single linear I–V relationship. For such cases, a two-piece PDR1 has been used [10]. Also, many tunnel diodes and RTDs exhibit a wide valley region, as shown in Fig. 1(b), which cannot be merged with either the NDR or the PDR2 region and hence needs to be modeled by one or more linear I–V pieces [11]. With the exception of [3], all the other PWL approaches reported were not implemented as part of the internal device library of SPICE. These external device representations involve development of an RTD *macromodel*, combining several of the in-built devices available in the SPICE device library. The usual approach, [10] and [12], is to make use of the *switch* model of SPICE, which can be used to select, based on bias conditions, different current sources (along with resistance and capacitance) representing different linear pieces of the I–V curve of the RTD. Six switches, five resistors, one capacitor, four voltage sources, and one voltage-controlled current source have been used to build a macromodel for a single RTD consisting of four linear I–V pieces [10]. A multicomponent PWL macromodel for tunnel diodes that does not use the switch model was proposed in [11] and can also be used for RTDs. This macromodel makes use of four diodes, five voltage sources, and five resistors to model a five piece I–V characteristic. A similar switchless PWL method was reported around the same time [13], which could be used for modeling multipeak RTDs using a lesser number of circuit elements than the model of [10].

Among the nonphysics-based approaches, several techniques have been reported that model the I–V curve of the RTD using non-PWL methods. A piecewise-nonlinear method using two diodes with different I–V characteristics—one for each PDR region—has been reported in [14]. A switch is utilized to select the diode corresponding to the PDR1 region only when the voltage across the RTD is less than its peak voltage. In [15], a network consisting of two JFETs, one diode, and a current source was used to model a tunnel diode fairly accurately and could also be used to model RTDs. Just as in the case of tunnel diodes in [16] and [17], RTDs have also been modeled using polynomial and trigonometric curve fitting method [18]. Polynomials of order less than five do not provide adequate accuracy for circuit simulation, even though quadratic and cubic functions can satisfactorily model portions of interest of the I–V curve. In this context, a double exponential function of the type $I = AVe^{-aV} + B(e^{bV} - 1)$ was shown to be quite accurate in approximating the I–V curve of a tunnel diode [19] and is in

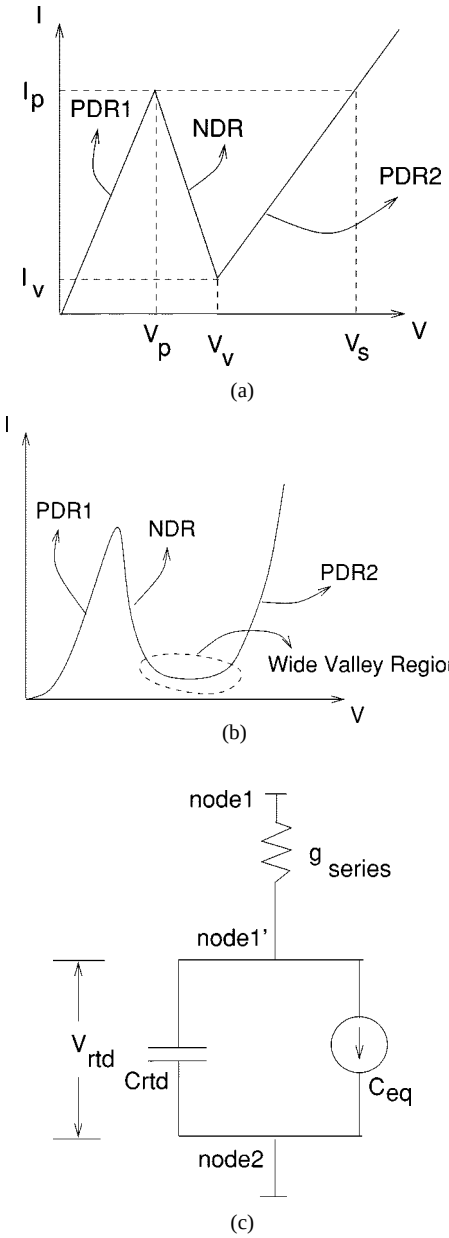


Fig. 1. (a)–(b) I–V characteristics of the RTD. (a) Piecewise-linear I–V. (b) Typical I–V. The characteristics have a negative differential resistance (NDR) between two positive differential resistances (PDR1 and PDR2). (c) Model of the RTD as added to the device library of SPICE 3F5.

essence very similar to the RTD macromodel implementation of [14]. In [20], a combination of Gaussian and exponential functions was proposed as an accurate way to model the I–V curve of the RTD. In [3], look-up table-based resonant tunneling device modeling is discussed. Such models can be very accurate and, at the same time, can save the effort involved in parameter extraction.

In recent times, device technology has matured to a point where a correlation is being sought between the device structure of the RTD and material properties on the one hand, and the performance of digital circuits using these devices on the other. This necessitated the development of a physics-based RTD model [4] and modifications thereof [21], [22].

With the exception of [3], all the above mentioned RTD circuit simulation approaches took advantage of the subcircuit definition option in SPICE to implement a multicomponent RTD model and then instantiated the RTD subcircuit at appropriate places in the main circuit netlist. Such *ad-hoc* implementations are quite cumbersome and can only be adopted while simulating small circuits. That is why the most complex circuit, whose simulation result (using this type of subcircuit approach) has been reported, is an A/D converter [10] consisting of only eight RTDs. Larger circuits have been simulated at the University of Michigan using an internal piecewise-linear model [3]. Models which use unrealistic switch type of devices and/or multiple diodes and resistors unnecessarily increase the number of nodes in the circuit and hence lead to slower simulation with larger memory usage. NDR in I–V characteristic of devices is known to cause convergence problems to circuit simulators employing Newton–Raphson algorithm. Also, exponential characteristics are specially dealt with by a variety of limiting algorithms. When a device is represented externally in the form of a subcircuit, such device-specific convergence aids cannot be easily activated.

As we continue to design larger and more complex RTD circuits, it will become necessary to be able to accurately and efficiently simulate these circuits using SPICE-like simulators. To this end, the physics-based model of the RTD has to be incorporated as an in-built device model and techniques need to be developed to ensure rapid convergence to dc and transient solutions. In this paper, we address these issues by paying attention to the number of iterations needed to solve the circuit nodal equations.

III. Physics-Based Model of the RTD

The detailed derivation of the physics-based model of the RTD used in this paper can be found in [4]. Borrowing the notations from [4], the final simplified model equation can be written as

$$J(V) = J_1(V) + J_2(V) \tag{1}$$

$$J_1(V) = A \ln\left[\frac{1+e^{(B-C+n_1V)q/kT}}{1+e^{(B-C-n_1V)q/kT}}\right] \cdot \left[\frac{\pi}{2} + \arctan\left(\frac{C-n_1V}{D}\right)\right] \tag{2}$$

$$J_2(V) = H\left(e^{n_2qV/kT} - 1\right) \tag{3}$$

where A, B, C, D, n_1, H, and n_2 are the seven device physics-related parameters which define the I–V characteristics of a particular RTD. The capacitance of the RTD is described by

$$C_{\rm RTD} = \frac{C_{j0}}{\left(1+\dfrac{|V|}{V_{bi}}\right)^M} \tag{4}$$

where C_{j0}, V_{bi}, and M are the model parameters.

We modify the basic diode model of SPICE 3F5 to represent an RTD [Fig. 1(c)]. The I–V relation according to (1)–(3) with V is replaced by $|V|$ and $J(V)$, taking negative values when V is negative to account for the symmetric nature of the I–V relationship of the RTD. In order to avoid numerical instabilities, we have to incorporate a limiting algorithm (Section IV-A-2) for which we need to derive the appropriate $V(I)$ relationships, given by (10) and (12), from the I–V equations. The conductance of the RTD is calculated from the I–V relation and found to be

$$g_{\rm rtd}(V) = \frac{Aqn_1}{kT}\left(\frac{\beta}{1+\beta}+\frac{\alpha}{1+\alpha}\right) \cdot \left(\frac{\pi}{2}+\arctan\left(\frac{C-n_1V}{D}\right)\right) + \frac{An_1{}^2\ln\left(\dfrac{1+\beta}{1+\alpha}\right)}{D^2+(C-n_1V)^2} + \frac{qHn_2}{kT}\,e^{(qn_2V/kT)} \tag{5}$$

where

$$\alpha = e^{((B-C-n_1V)q/kT)}$$
$$\beta = e^{((B-C+n_1V)q/kT)}.$$

The first derivative (differential conductance) of the I–V curve of a real RTD is shown in Fig. 2(b). From this figure, we can see that even though the derivative is continuous, it does undergo sharp changes near the peak and in the NDR region. Compared to the conventional devices modeled in SPICE, such as BJT or MOSFET, this characteristic does exhibit significantly less smoothness.

IV. DC Convergence Problems

The basic iterative solution technique employed by SPICE to solve the nonlinear equations is based on the Newton–Raphson algorithm (also known as Newton's method) [23]. This algorithm solves equations of the form $f(\hat{v}) = 0$ for $\hat{v}$ by starting with an initial guess $v^{(0)}$ and repeatedly solving the Newton–Raphson iteration equation

$$\mathcal{J}\left(v^{(k)}\right)\left(v^{(k+1)}-v^{(k)}\right) = -f\left(v^{(k)}\right) \tag{6}$$

or

$$v^{(k+1)} = v^{(k)} - \mathcal{J}^{-1}\left(v^{(k)}\right) f\left(v^{(k)}\right) \tag{7}$$

for $v^{(k+1)}$ [the value of v on the $(k+1)$th iteration] until some convergence criteria are met. $\mathcal{J}(v) = (d/dv)f(v)$ is called the Jacobian of f at v. Since both $f(v)$ and v are N-dimensional vectors, $\mathcal{J}(v)$ is an $N \times N$ matrix. It represents the circuit linearized about v.

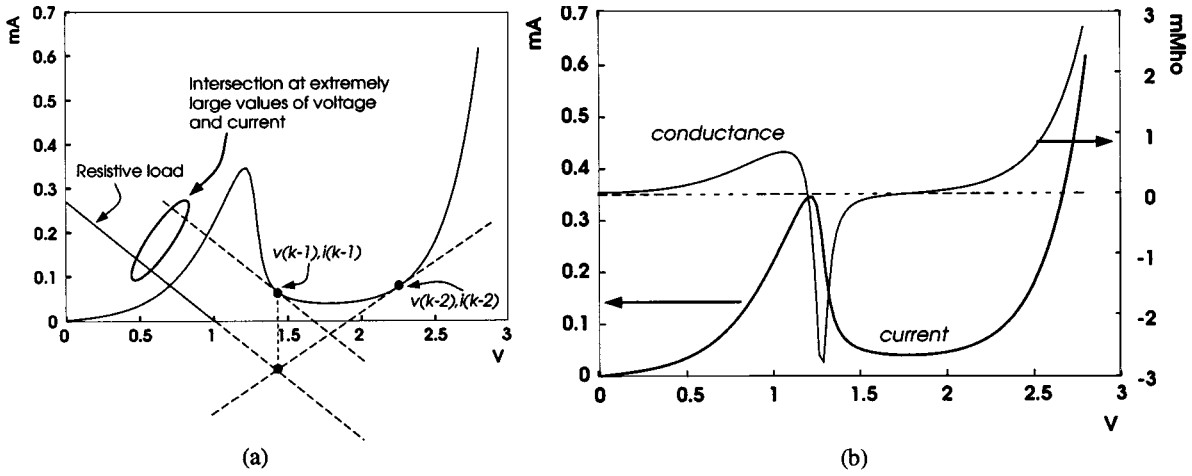


Fig. 2. (a) The numerical instability problem for RTD circuits shown with respect to realistic device characteristics. At any iteration, the solution is given by the intersection of the load lines linearized around the previous solution point. Numerical instability can be caused when the lines intersect at very high current values. (b) Conductance of the RTD as a function of the applied bias.

The popularity of Newton's method stems from the fact that it is simple to implement and is quadratically convergent. However, this type of method is only locally convergent. That is, the iterative process is guaranteed to converge to the correct solution only if the initial guess $v^{(0)}$ is close enough to it. Problems such as oscillations around local minima or maxima of $f(\hat{v})$ and false-convergence to an undesirable solution may occur if $v^{(0)}$ is far from the correct one. In such cases, continuation techniques like Gmin-stepping and Source-stepping may have to be used. During Gmin-stepping, a conductance is added to the diagonal elements of the admittance matrix, which is initially set to a high value, virtually causing all nonlinearities to vanish from the circuit altogether. At each succeeding step, the conductance is reduced (usually by a factor of ten) until it becomes infinitesimally small. During source-stepping, all the voltage and current sources in the circuit are gradually stepped up from zero to their actual time-zero values. For further details on Gmin-stepping and Source-stepping techniques, please refer to [23] and [24]. It is well known that the above mentioned continuation techniques are not without limitations. In the last decade, researchers have sought to find robust methods for dc operating point simulation of nonlinear circuits. Sophisticated artificial parameter homotopy methods have been suggested [25]–[28] and used successfully for dc simulation when Gmin-stepping and Source-stepping have failed to converge. For a comprehensive treatment of the subject of homotopy methods for circuit analysis, please refer to [29] and the references therein.

A. Solving the DC Convergence Problems

To speedup and improve the dc convergence performance of SPICE 3F5 specifically for simulating RTD circuits, we propose a modified limiting algorithm and a new continuation method and compare their performances.

1) Existing Techniques: Devices with exponential I–V characteristics, like diodes, Zener diodes and RTDs, can suffer from numerical instability problems during Newton–Raphson iterations if an intermediate voltage becomes such that the corresponding current through the device becomes unrealistically large. If there are regions of positive and negative conductance values in the device characteristics, the chances of such conductances being close to the slope of the load line become high. If this happens, the solution of (7) will generate voltages and currents that are extremely high. In the case of RTDs, this is a very common problem that can cause Newton's method as well as simple continuation techniques like Gmin-stepping and Source-stepping to fail. By means of extensive simulation of RTD circuits of various sizes, we have observed that the above mentioned in-built continuation techniques of SPICE 3F5 can fail to converge to dc solutions of many RTD circuits even after a reasonably large number of iterations.

While incorporating a Zener diode model into SPICE2 [6], Laha and Smart [30] had proposed a limiting algorithm to facilitate convergence. Here, we propose a modified limiting algorithm suitable for RTD circuit simulation. From a typical RTD characteristic [see Fig. 2(b)], we can see that the RTD curve in the positive quadrant has a wide range of possible conductance values from large negative (NDR region) to large positive (near the peak in PDR1 and for large values of voltages in PDR2) values. As a result, it is very likely that during Newton–Raphson iterations, the conductance of the RTD for a particular value of its voltage may be very close and of opposite sign to that of the load. The solution of the corresponding linearized circuit will be a point having an unrealistically large absolute value of voltage and current, leading to numerical instability and indicated by SPICE as NaN (Not a Number) [Fig. 2(a)].

2) New Techniques: We propose two new techniques for handling the dc convergence problems of RTD circuits: 1) a limiting algorithm and 2) a continuation method which we shall refer to as *RTD-stepping*.

a) Limiting algorithm: Our limiting algorithm is capable of identifying situations that can give rise to numerical instability. By means of using current iterations instead of voltage iterations, it can circumvent the problem. It is similar to Coons' (Laha and Smart [30]) methods but had to be modified to account for the multivalued nature of the I–V curve of the RTD.

Let us consider Fig. 3 in order to understand the mechanism and conditions of application of our limiting algorithm. First of

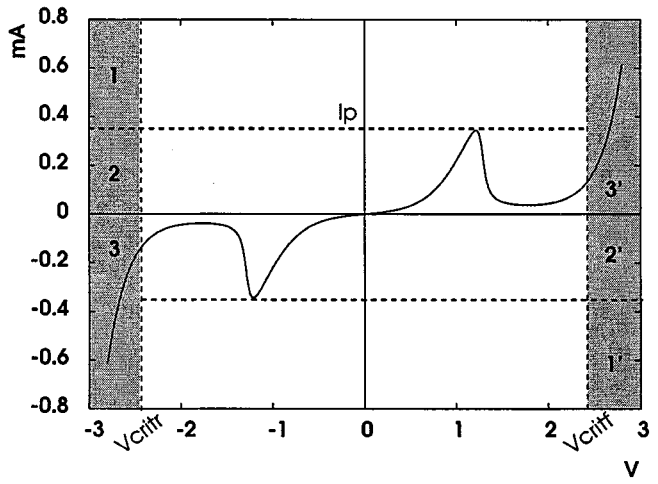


Fig. 3. The limiting algorithm proposed in this paper requires dividing the I–V plane of the RTD into several regions as shown here with respect to a realistic device characteristic. The different regions are explained in Table I.

all, we need to find appropriate values of $V_{\mathrm{crit}r}$ and $V_{\mathrm{crit}f}$ such that when the RTD voltage during Newton–Raphson iterations goes beyond these values, current iteration, instead of voltage iteration, is used. Fig. 4 explains the difference between current and voltage iteration methods. v_{k-1} and i_{k-1} are the RTD voltage and current, respectively, at the $(k-1)$th iteration. The solution of the linearized circuit corresponding to this iteration $(\hat{v}_k, \hat{i}_k)$ are used as the starting point for the kth iteration. In the case of voltage iteration, $\hat{v}_k$ is used as v_k and the device current i_k is computed from I–V relationship. On the other hand, during current iteration, $\hat{i}_k$ is used as i_k and v_k is calculated from $V(I)$ equation. In the case of RTDs, $V(I)$ can be multivalued, so we need to find approximate single-valued functions to facilitate calculations. In the case of diodes, usually $V_{\mathrm{crit}f}$ is taken to be the voltage corresponding to the point having minimum radius of curvature. For a simple exponential diode equation, it is easily calculated. However, if we use the complete RTD equation, it can become quite complex. Since that the PDR2 region is dominated by the diode current $J_2(V)$, $V_{\mathrm{crit}r}$ and $V_{\mathrm{crit}f}$ can be approximately calculated from $J_2(V)$ only. We get the following value:

$$V_{\mathrm{crit}f} = -V_{\mathrm{crit}r} = \frac{kT}{qn_2}\ln\left(\frac{kT}{qn_2H}\right). \tag{8}$$

If, during an iteration, the solution of the linearized circuit is such that the diode voltage-current pair has the value $(\hat{V}_k, \hat{I}_k)$ and $|\hat{V}_k| > V_{\mathrm{crit}f}$, then six different situations can occur depending on the value of $\hat{I}_k$. The corresponding zones in the I–V plane are marked 1, 2, 3, $1'$, $2'$, and $3'$ and the conditions corresponding to each are explained in Table I.

When $|\hat{V}_k| > V_{\mathrm{crit}f}$, we may have to resort to current iterations instead of voltage iterations, but we should also check if there was a substantial change in the voltages V_{k-1} and $\hat{V}_k$. This threshold is taken to be $2kT/qn_2$ [30]. Thus, current iteration is performed if $|\hat{V}_k| > V_{\mathrm{crit}f}$ and $|\hat{V}_k - V_{k-1}| > (2kT/qn_2)$.

Due to the multivalued nature of the $V(I)$ relationship of the RTD

$$V = J^{-1}(I) \tag{9}$$

we have to consider several possible situations depending on the values of $\hat{V}_k$ and $\hat{I}_k$ as compared to I_p, the peak current of the RTD, such that $J^{-1}(I)$ can be made single-valued. For this purpose, we need to manipulate (1) to extract approximately: 1) the peak current of the RTD; 2) the analytical expression for PDR1 only; and 3) the analytical expression for PDR2 only. Now, 3) is easily approximated by $J_2(V)$ given by (3) and we have

$$V = \frac{kT}{qn_2}\ln\left(\frac{I}{H}+1\right). \tag{10}$$

The peak current 1) can be approximated from $J_1(V)$ expression given by (2) as

$$I_p \approx A\arctan\left(\frac{C}{D}+\frac{\pi}{2}\right).$$

The PDR1 region 2) can be extracted from the expression of $J_1(V)$ as:

$$I = I_p \ln\frac{1+e^{(B-C+n_1V)q/kT}}{1+e^{(B-C-n_1V)q/kT}} \tag{11}$$

from which we can derive

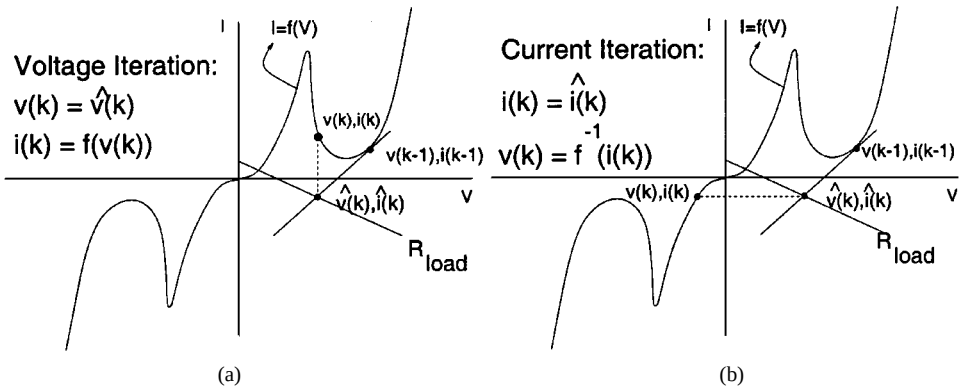
$$V = \frac{kT}{qn_1}\ln\left(\frac{e^{I/I_p}-1}{2e^{(B-C)q/kT}} + \sqrt{\left(\frac{e^{I/I_p}-1}{2e^{(B-C)q/kT}}\right)^2 + e^{I/I_p}}\right) \tag{12}$$

where I is the absolute value of the RTD current. If the RTD current is negative, then the corresponding voltage will also be negative. These equations are not exact but close enough to derive the approximate voltages, which are reasonably low-valued and from which Newton–Raphson can carry on iterations to find the correct dc solution.

Modified Limiting Algorithm

if$(|\hat{v}_k| > v_{critf}$ **and** $|\hat{v}_k - v_{k-1}| > \epsilon)$ {
  $i_k = \hat{i}_k$;
  if ($\hat{v}_k \cdot i_k > 0$ or ($\hat{v}_k \cdot i_k < 0$ and $|i_k| > I_p$)) {
    v_k is given by (10) with I replaced by $|i_k|$;
  } **else** {
    v_k is given by (12) with I replaced by $|i_k|$;
  }
  g_k is given by (5);
  if $(i_k < 0)$ $v_k = -v_k$;
}

b) RTD-stepping: Due to the wide range of conductance values proffered by the neighborhood of the valley region of the RTD along with its exponential I–V, numerical instabilities can occur that can adversely affect dc convergence. Standard continuation techniques like Gmin-stepping and Source-stepping may be able to overcome such problems in some cases. Gmin-stepping effectively linearizes nonlinear devices and hence, during initial Gmin-steps when the NDR region is almost nonexistent, the possibility of having a RTD conductance that is almost parallel to a load line is remote. As Gmin-stepping progresses, the NDR regions of the RTDs in the circuit gradually reappear. Source-stepping can fail for certain RTD characteristics right



(a) (b)

Fig. 4. (a) Voltage and (b) current iteration techniques.

TABLE I
CRITICAL REGIONS OF THE I–V PLANE AS SHOWN IN FIG. 4

	$\hat{V}_k > V_{critf}$	$\hat{V}_k < -V_{critr}$
$\hat{I}_k > I_p$	3′	1
$0 < \hat{I}_k < I_p$	3′	2
$-I_p < \hat{I}_k > 0$	2′	3
$\hat{I}_k < -I_p$	1′	3

in the first step when all sources are zero. When RTD junction voltage is initialized to

$$V_s = \frac{kT}{qn_2} \ln\left(\frac{kT}{\sqrt{2}qn_2H}\right) \tag{13}$$

within the next few iterations, the RTD conductance can be very close to the load for certain RTD curves [for an explanation, please refer to Fig. 2(a)]. We have found that several circuits exist whose particular combination of device parameter values can cause nonconvergence (or convergence after large number of iterations) for both Gmin-stepping and Source-stepping, examples of which can be found in Section IV-A. Having discovered the inadequacies of the existing continuation techniques of SPICE 3F5, we investigated other types of artificial parameter homotopy methods [29] specifically for RTD circuits. Our experiments showed that a particular type of parameter embedding with the RTD current given by

$$J(V) = \lambda J_1(V) + J_2(V) \tag{14}$$

where λ is the continuation parameter, is quite effective and succeeded in finding dc operating points in all the difficult to simulate RTD test circuits. The value of λ is increased in small steps (e.g., 0.1), from zero to one. Basically, this type of embedding converts an RTD circuit to a simpler diode circuit and then gradually introduces the tunneling component into the device characteristics (Fig. 5). We refer to this convergence aid as *RTD-stepping* and, by means of a large number of simulation experiments, we have verified that this type of embedding is more effective than Gmin-stepping and Source-stepping in overcoming dc convergence problems. Unlike Gmin-stepping, RTD-stepping selectively modifies only the RTDs in the circuit. This results in the solution of the converted circuit to be quite close to that of the actual circuit and the solution trajectory (from that of the simplified circuit to that of the actual circuit) is minimized. Thus, chances of nonconvergence are reduced along with the total number of iterations.

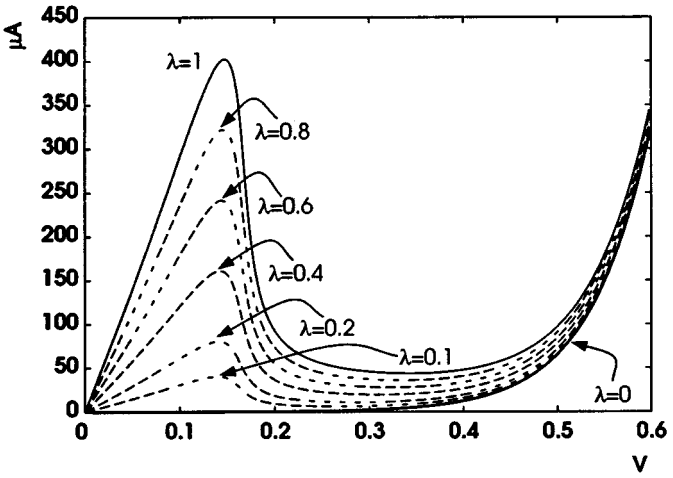


Fig. 5. The RTD-stepping technique. The NDR becomes prominent as continuation parameter (λ) is stepped up from zero to one.

While it can be argued that sophisticated arc-length tracing techniques [28] and [31] can be used to make the continuation technique more robust, we have intentionally kept RTD-stepping to be simple. This is because, first of all, our experiments with a large number of RTD circuits of varying sizes have shown that RTD-stepping is quite effective in dealing with almost all cases (we are yet to find a circuit where it fails to find a dc solution). Secondly, using advanced tracing algorithms, such as the ones in [25] and [31], we can significantly slow down the simulator (possibly by an order of magnitude [27]) or require the usage of additional commercial mathematical software packages, such as MATLAB [32] as suggested in [33]. The beauty and effectiveness of this simple technique lie in the fact that when $\lambda = 0$, the circuit is closer to the actual circuit ($\lambda = 1$) compared to the situation that arises when Gmin-stepping is employed. By selectively modifying only the RTD characteristics, RTD-stepping increases the probability of finding a solution and does not need to invoke complicated solution-trajectory tracing procedures.

We would like to emphasize that RTD-stepping by no means constitutes the first implementation of a continuation or parameter-embedding technique in SPICE. In fact, it is only one in a long line of rich work in this area [29]. The novelty of RTD-stepping lies solely in the fact that it is a simple and effective method for handling dc convergence problems caused by the folded-back I–V characteristic of RTD. Circuits composed

of conventional devices, such as BJTs and MOSFETs (Schmitt trigger circuit or thyristor circuit modeled by back-to-back n-p-n–p-n-p BJTs), may also exhibit NDR in their terminal behavior [34] and can cause convergence problems to circuit simulators. Many of the techniques found in the literature (e.g., [25], [31], and [33]) can be used to solve these problems.

V. Transient Problems

In the case of transient analysis of circuits, SPICE relies on time itself to be the continuation parameter and hence tries to overcome transient convergence problems simply by reducing the time-step until convergence is achieved. This works well for most conventional circuits—the only few known failures (giving the infamous *time-step too small* warning) are due to exceptionally fast switching occurring in the circuit and are very uncommon. As long as the solution waveforms are continuous, it should be possible to achieve convergence by taking a smaller time-step because, with small time-steps, the solution at one time-point becomes closer to the region of convergence for the solution at the next time-point. However, in the case of RTDs, extremely fast switching is very common and hence transient simulation often runs into trouble. We call this problem by its traditional name—the *time-step too small problem*. Unlike the above problem, where SPICE explicitly lets the user know that there is a transient convergence problem, we have discovered a different kind of transient convergence problem unique to RTD circuits. This is due to insufficiently small time-step that results in convergence to an undesirable solution; and there is no definite way of knowing that such a false convergence has occurred. We refer to this type of transient convergence problem as the *coarse time-step problem* and explain it below with a simplified example.

Unlike conventional circuits, the nodal equations of an RTD circuit can have more than one solution and this number can undergo a sudden change with time. Thus, the problem of tracing a single operating point gradually varying with time can often transform itself into one of finding multiple operating points and choosing the right one from them. Unfortunately, there is no known reliable method that can be used with the currently available commercial circuit simulators to find unexpected multiple operating points. In certain NDR circuit topologies, the nodal equations can take such shapes that the simulator can converge to an undesirable solution due to large time-step at critical time-points. We have observed that certain RTD circuits (e.g., monostable bistable transition logic elements (MOBILE) [35]) may exhibit this type of problem.

The circuit shown in Fig. 6(a) is a simplified form of a MOBILE inverter without the control transistors. Even though this circuit will not operate as an inverter, it will help us demonstrate the simulation problems in a simple way. When V_{cc} is ramped up from 0 V, the output should switch from low to high since $D1$ has a higher peak current (I_{p1}). However, for several different combinations of I–V curves of $D1$ and $D2$, with $I_{p1} > I_{p2}$, it has been observed that the simulation results do not show an output switch for a well designed MOBILE circuit. Here, we show what may cause such a problem. The circuit can be described by the simple nodal equation

$$f(v_0) = i_1(v_{\text{bias}} - v_0) - i_2(v_0) = 0. \tag{15}$$

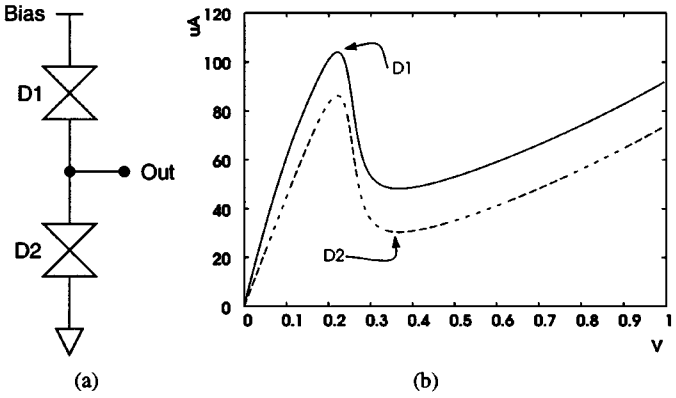


Fig. 6. (a) A series RTD circuit. (b) RTD characteristics corresponding to the devices $D1$ and $D2$.

Fig. 7(b) shows $f(v_0)$ for various values (V_{bias} is being ramped up from zero). Fig. 7(a) is the load-line diagram which explains the operation of the circuit of Fig. 6. The solid line represents the RTD $D2$ while the dashed lines represent the RTD $D1$, whose load-line is gradually moving to the right as the bias voltage is being increased. To demonstrate the switching event, we select three bias voltages—0.35, 0.39, and 0.43 V. Initially, when the bias voltage is 0 V, the only possible solution is at the origin of the plot in Fig. 7(b). With increasing bias, the solution moves such that it remains at the intersection point of the PDR1 regions of $D1$ and $D2$. For example, when the bias voltage is 0.35 V, the solution corresponds to point A in Fig. 7(b). When the bias voltage is 0.39 V, the two PDR1 regions do not intersect anymore, switching has already taken place, and the only possible solution is at B. When the bias is further increased to 0.43 V, it is not difficult to find the desirable solution point C if the starting seed was close to B. However, if it so happens that, due to increased time-step size, the scenario corresponding to bias voltage 0.39 V is skipped, then the simulator may converge to the solution point D instead of the desired point C, since D is closer to the starting solution A.

We can conclude that the sudden increase in the number of solutions for the nodal equations can cause false convergence if the solutions are closely spaced and the time-step is not small enough to detect the change.

A. Solving the Transient Convergence Problems

1) Existing Techniques: For conventional circuits, the *time-step too small* problem is usually attributed to discontinuities in the device model and hence is treated more as a modeling problem than a simulation problem. Since an infinitely fast change of a node voltage is unrealistic for such circuits, usually connecting a small capacitor from the problematic node to the ground can slow down the transition and help the simulator. However, in the case of RTDs, it is not unrealistic to have extremely fast switching [36], primarily because tunneling is a fast mechanism that is not limited by drift transit time and does not have delay associated with minority charge storage [2]. Also, since the devices themselves have very low capacitances, adding an external one, however small, may result in affecting the true response of the circuit.

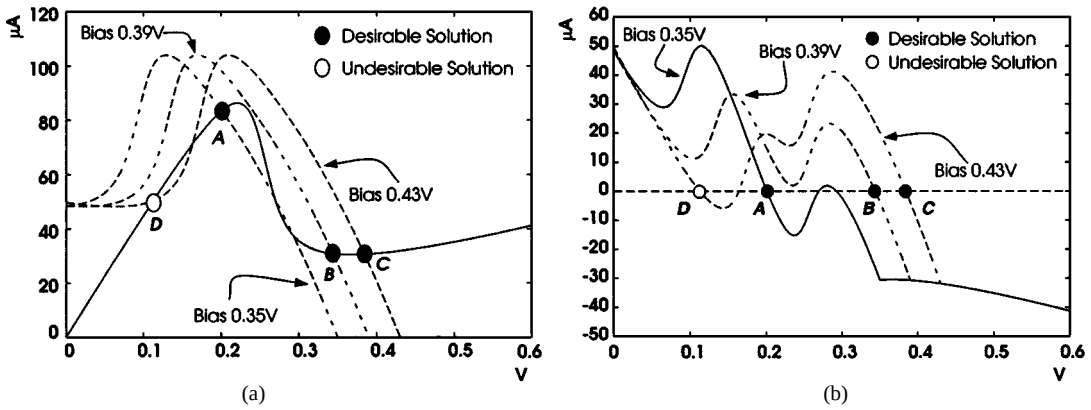


Fig. 7. The coarse time step problem demonstrated using the circuit of Fig. 6. (a) The load lines with varying bias. (b) Plots for (15).

Coarse time-step problems, in the case of conventional circuits, are usually handled by reducing the maximum time-step that the simulator is allowed to take. However, this cannot be a good solution for NDR circuit simulation. This is because, first of all, the simulation is going to become extremely slow. Secondly, the coarse time-step problem is not explicitly observed by the user because the simulator does converge, albeit to an undesirable solution.

2) New Techniques:

a) The time-step too small problem: This problem, in the case of RTD circuit simulation, was first addressed in [3] with respect to a piecewise-linear RTD model. A *forced-convergence* routine was proposed to overcome this problem. For piecewise-linear RTD models, it is very easy to detect this type of convergence problems and also to implement the forced-convergence algorithm since the entire RTD model had only three different conductance values corresponding to the three different linear pieces. Using the knowledge of the three different conductances and well-defined peak and valley voltages, one could easily detect a simulator oscillation between two adjacent pieces of the model and *force* the iterations to move to the third piece. For the physics-based model, implementation of the forced-convergence routine has to be a little different. In this case, the convergence problem is found to occur around the peak only because of its sharp nature, rather than around the valley which is usually wide.

The modified forced-convergence algorithm that we propose here is much the same in concept as the one proposed in [3] but with some modifications. First of all, since there is no well defined peak voltage in the physics-based model and since the oscillation usually occurs around a voltage that is in the NDR region, we need to define a peak *region* rather than a peak voltage. The peak region can be approximated by differentiating the tunneling current portion of the I–V characteristics of the RTD, equating it to zero, and solving for voltage. For the purpose of identifying proximity to the peak region, we use $\pm 20\%$ of this approximate solution given by

$$V_{\text{peak}} \approx \frac{C - 0.577D}{n1}. \tag{16}$$

Once we detect that the operating point is within this region, we can detect a nonconvergence if the simulator's internal time-step comes too close to the minimum possible time-step. If both these conditions are met, we simply force the next iteration to begin from V_s given by (13) in the PDR2, which, as we have seen before, is a good choice for dc convergence—having a conductance approximately equal to $1/\sqrt{2}$.

The Forced-Convergence Algorithm

if (current-step-size $<$ $10\times$ minimum-step-size
and current-operating-point is close to the RTDs peak) {
V_{RTD} = Given by (13);
I_{RTD} = Given by (1) with V replaced by $|V_{RTD}|$;
if ($V_{RTD} < 0$) $I_{RTD} = -I_{RTD}$;
g_{RTD} = Given by (5) with V replaced by $|V_{RTD}|$;
}

During transient analysis, in the case of diodes, SPICE uses a simple linear extrapolation technique to predict the initial seed to make finding the solution of the next time-point faster and easier. The voltage values of previous two time-points and the corresponding time-step sizes are used to determine approximately the voltage value of the current time-step, and then this value is refined iteratively to arrive at the accurate solution. This mechanism is very effective when the voltage changes smoothly. However, in the case of RTD circuits, abrupt switching of voltage across device can cause the linear extrapolation scheme to be a problem rather than an aid to efficient simulation—for it will cause the simulator to iterate for a significantly larger number of steps. This is illustrated in Fig. 8(a). To overcome this problem, we propose the following simple algorithm for voltage prediction. We check the rate of change of the voltage across the RTD for the last two time points and see if the last rate was significantly larger $(10\times)$ than the previous one, in which case, instead of using a linearly extrapolated seed, we use the solution of the previous time point as the seed for the current one [see Fig. 8(b)].

The Voltage Prediction Algorithm

if $\left(\left|\dfrac{V_1 - V_2}{\delta_1}\right| \geq 10 \times \left|\dfrac{V_2 - V_3}{\delta_2}\right|\right)$ {
$V_{RTD} = V_1$;
} **else** {
$V_{RTD} = \left(1 + \dfrac{\delta}{\delta_1}\right) V_1 - \left(\dfrac{\delta}{\delta_1}\right) V_2$;
}

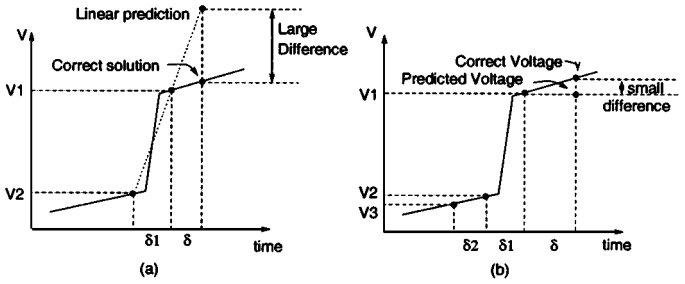


Fig. 8. (a) Ordinary linear voltage prediction method. (b) The modified voltage prediction scheme.

It is to be noted that the linear prediction scheme can also fail during the time-step $\delta 1$ [see Fig. 8(a)] since the predicted voltage would be close to V_2 and the correct value will be V_1, which may result in a large error value as well. Obviously, the modified voltage prediction technique described above will not be of any help in this case. However, as will be discussed later in this section, we have implemented a mechanism to cut down the time-step when we detect that the voltage across a RTD is approaching its peak to minimize *the coarse time-step problem*. This has a secondary effect of minimizing the convergence problem that can occur during time-step $\delta 1$.

By default, SPICE chooses its time-steps by means of local truncation error (LTE) of its numerical integration routines. The time-step at time instance $t+1$ is calculated based on the LTE values at time instance t and certain tolerance parameters which can be controlled by the user [9]. If the LTE at one time instance is large, the time-step for the next time instance is appropriately reduced. However, since RTDs can switch in picoseconds [36], LTE-based time-step calculation may not be able to adjust time-steps, particularly when the desired total transient simulation time is much longer than the device switching time. Purely LTE-based time-step calculation is known to be inadequate in certain cases since the time-steps are allowed to increase to a maximum value of 1/50th of the total simulation time (e.g., [9]), which may lead to undersampling. To avoid this problem, if the upper-limit of this maximum time-step is intentionally set to a small value by the user, simulation can become slow.

b) The coarse time-step problem: The coarse time-step problem can be handled by simply reducing the allowable time-step size in the .TRAN line of the SPICE input file. However, this can only be done if the user *knows* that such a problem can occur while simulating the circuit since the simulator will not be able to identify and report such a problem. Also, reducing time-step leads to increasing the simulation time since the circuit will now be simulated at a larger number of time-points.

To solve this problem, we propose an algorithm by which the simulator can automatically adjust the time-step only when necessary. Our simple technique is as follows: we simply detect if the voltage across a RTD is approaching its peak or not. If it is approaching the peak, then we reduce the time-step. The customary time-step reduction factor used in SPICE is 1/8, which has been found to be sufficient for this purpose as well. This simple method has been found to be very effective in avoiding false-convergence problems at the cost of only a few extra time-steps. For instance, in the case of a particular

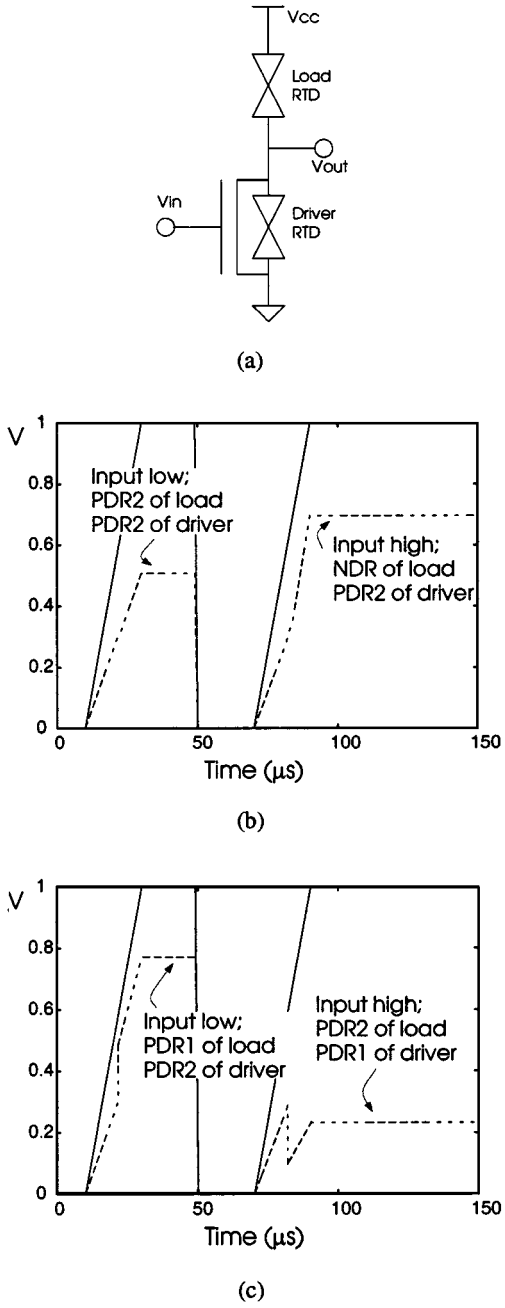


Fig. 9. (a) A MOBILE-type circuit. (b) Simulator fails to detect switch from high to low (without time-step adjustment). (c) Modified time-step adjustment method detects switch from high to low (with time-step adjustment). Solid lines represent V_{cc} while dashed lines represent the output voltage. Input changes from 0 to 5 V at 60 μs.

circuit which consisted of two RTDs connected in a series [as in Fig. 9(a)], when the bias voltage is slowly ramped up from zero, the voltage at the common node of the two RTDs may exhibit convergence to an undesirable value [see Fig. 9(b)] if the user-defined time-step is larger than $0.4\,\mu$s. When the time-step is set to $0.4\,\mu$s, the simulator converges to the expected solution [see Fig. 9(c)] but does so using 406 time-steps. On the other hand, when the time-step adjustment scheme is employed, the user-defined time-step could be as coarse as $1.8\,\mu$s (resulting in 139 time-steps) with no false convergence problems [see Fig. 9(c)].

TABLE II
NONLINEAR DEPENDENT CURRENT SOURCE CIRCUITS, WHICH SPICE 3F5 FAILS TO SIMULATE

R_{load}	V_{su}	D	Iterations before failing
5050	4.6	0.0055	509
2080	1	0.0064	459
5050	4.6	0.0058	474
5050	4.6	0.0064	503
6040	5.5	0.0052	504
7030	6.4	0.0058	464
8020	7.3	0.0049	433

VI. RESULTS

A. DC Operating Point Results

SPICE 3F5 fails to simulate a large number of RTD circuits in which the RTD models are nonlinear voltage dependent current sources defined externally as subcircuits. Here we present examples of such circuits for which the basic topology is the same—a voltage divider circuit consisting of a series-connected RTD and a resistor. We could find a large number of combinations of values of the supply voltage, load resistance, and the value of the parameter D of the RTD, which SPICE could not simulate using Newton's method combined with Gmin-stepping and Source-stepping techniques. All these circuits could be easily simulated using the in-built RTD model within 10–15 Newton's iterations. However, since the in-built model uses a different initial voltage, we cannot really compare the performances of the two implementations. These examples only help demonstrate the weakness of the externally represented nonlinear voltage dependent current source model. For the results presented in Table II, the basic RTD parameters were: $A = 1 \times 10^{-4}$, $B = 0.0456$, $C = 0.0689$, $D =$ variable, $n_1 = 0.430$, $n_2 = 0.4373$, and $H = 1.43 \times 10^{-8}$. The series resistance of the RTD was taken to be $20\,\Omega$.

In order to test our in-built RTD model of SPICE 3F5, we used a simple circuit consisting of a BJT driver and a series combination of two RTDs as the load. The two RTDs had area factors of 0.1 and 0.11, respectively, and had the following model parameter values: $R_{\text{series}} =$ variable, $A =$ variable, $B = 0.035$, $C = 0.1472$, $D =$ variable, $n_1 = 0.115$, $H =$ variable, and $n_2 = 0.1201$. The transistor used is the default npn BJT model of SPICE 3F5. When the four parameters (R_{series}, A, D, and H) were perturbed, we observed that in some cases, ordinary SPICE 3F5 had problems in finding the dc operating point. We found that simply applying RTD-stepping can improve the performance in many such cases. However, the limiting algorithm proved to be the most effective. The results are presented in Table III.

B. DC Convergence for Larger Circuits

We have applied the dc convergence methods proposed in this paper—RTD-stepping and the limiting algorithm—to a large number of RTD circuits and have obtained satisfactory results. For instance, while simulating the quantum-MOS (QMOS or RTD/CMOS) circuits of varying sizes, we have observed that in-built continuation techniques in SPICE, like Gmin-stepping and Source-stepping, fail in a number of cases while our continuation method, RTD-stepping, succeeds in finding a dc solution in each of these cases. Some of these examples are presented in Table IV.

TABLE III
COMPARISON OF PERFORMANCE OF DC CONVERGENCE ALGORITHMS (NUMBER OF ITERATIONS BEFORE CONVERGENCE OR FAILURE). P = PLAIN NEWTON'S METHOD; G = GMIN-STEPPING; S = SOURCE-STEPPING; R = RTD-STEPPING; PL = PLAIN NEWTON'S METHOD WITH LIMITING ALGORITHM

R_{series}	A	D	H	SPICE 3F5	RTD-stepping	Limiting Algo.
0	8e-05	0.0055	1.011e-09	P 93	P 93	PL 35
0	8e-05	0.0046	2.211e-09	P 87	P 87	PL 42
0	8e-05	0.0043	4.110e-10	PG 159	PR 147	PL 26
2	9.2e-05	0.0043	6.110e-10	PG 159	PR 151	PL 37
4	1.12e-04	0.004	4.110e-10	PG 158	PR 152	PL 39
0	1.12e-04	0.0067	1.411e-09	PGS 368	PR 145	PL 50
0	1.16e-04	0.0052	2.211e-09	PGS 368	PR 145	PL 19
2	8e-05	0.0058	1.211e-09	PGS 386	PR 152	PL 26
2	8e-05	0.0064	1.211e-09	PGS 434	PR 152	PL 32
4	8.8e-05	0.0064	8.110e-10	PGS 369	PR 152	PL 42
4	1.08e-04	0.0043	1.211e-09	PGS 380	PR 152	PL 36
4	1.12e-04	0.0064	1.211e-09	PGS 368	PR 152	PL 28
2	1e-04	0.0061	2.211e-09	Fail, 428	PR 152	PL 20
4	1.04e-04	0.0046	1.011e-09	Fail, 434	PR 152	PL 26
6	1e-04	0.0055	1.411e-09	Fail, 427	PR 152	PL 25
10	1.04e-04	0.0046	1.211e-09	Fail, 436	PR 152	PL 53
16	9.6e-05	0.0052	1.411e-09	Fail, 429	PR 152	PL 28
18	8.8e-05	0.0055	1.011e-09	Fail, 437	PR 152	PL 44
18	8.8e-05	0.0058	1.011e-09	Fail, 429	PR 152	PL 31
18	9.2e-05	0.0061	1.211e-09	Fail, 429	PR 152	PL 21
18	1.12e-04	0.0046	1.011e-09	Fail, 429	PR 152	PL 24
18	1.12e-04	0.0058	2.211e-09	Fail, 429	PR 152	PL 30

C. Transient Analysis Results

In order to demonstrate the necessity as well as the performance of the modified forced-convergence and the voltage prediction algorithms, we simulated a simple RTD-resistor series pair circuit with the resistor as the load and with the voltage across the pair being swept from 0 to 2 V. We simulated the circuit for various values of the load resistor and different RTD curves. The RTD curves were generated from the following basic model values, with A and D being perturbed: $R_{\text{series}} = 20$, $A =$ variable, $B = 0.0456$, $C = 0.0689$, $D =$ variable, $n_1 = 0.43$, $H = 1.43 \times 10^{-8}$, and $n_2 = 0.4373$. The results of the transient simulation of the RTD-resistor circuit are presented in Table V. The results show that the circuits, which cannot be simulated by simple SPICE 3F5 transient analysis procedure, can be simulated with the help of the forced-convergence (FC) routine and that the performance of the FC method can be improved by the modified Voltage Prediction Algorithm (Section V-A-2). It can also be seen that the circuits, which can be simulated ordinarily, can also be simulated by FC at no extra iteration cost. The default options settings of the simulator were used in each of the simulations.

In order to verify the utility of the VPRED algorithm, we simulated a large number of RTD circuits, which exhibit switching, with and without VPRED and plotted the total number iterations required in the transient simulation in both the cases. Fig. 10 shows this plot from which it is clear that VPRED helps reduce the number of iterations on an average and hence makes the simulator more efficient.

TABLE IV
RTD CIRCUITS THAT COULD BE SIMULATED BY RTD-STEPPING BUT NOT BY GMIN/SOURCE-STEPPING. SIMULATIONS RUN ON A SUN ULTRA-2 WORKSTATION

Circuit	No. of devices	Type of Simulation	Iterations	CPU time
QMOS inverter chain	90 RTDs, 90 MOSFETs	Operating point	169	0.49 s
RTD-HBT inverter chain	3 RTDs, 3 HBTs	Operating point	135	0.15 s
QMOS bistable Carry chain	3 RTDs, 21 MOSFETs	Operating point	143	0.23 s
QMOS bistable Adder	10 RTDs, 30 MOSFETs	Operating point	147	0.23 s
QMOS static Carry	3 RTDs, 7 MOSFETs	DC sweep (500 points)	1361	0.97 s

TABLE V
PERFORMANCE OF THE FORCED-CONVERGENCE (FC) AND THE VOLTAGE PREDICTION (VPRED) ALGORITHMS (NUMBER OF ITERATIONS BEFORE SUCCESS OR FAILURE)

R_{load}	A	D	Without FC	With FC	With FC & VPRED
2000	8.40e-05	6.1e-03	535	535	513
2000	8.80e-05	6.7e-03	409	409	387
2000	9.20e-05	6.7e-03	423	423	402
2000	9.60e-05	6.7e-03	409	409	391
2000	8.00e-05	4.0e-03	Fail, 539	763	692
2000	8.00e-05	5.5e-03	Fail, 576	792	661
2400	8.00e-05	5.8e-03	Fail, 595	742	701
2400	1.04e-04	4.9e-03	Fail, 545	735	708
2800	8.80e-05	5.5e-03	Fail, 552	705	667
2800	1.04e-04	5.8e-03	Fail, 707	779	736
3200	8.40e-05	4.9e-03	Fail, 717	913	742
3200	8.40e-05	6.4e-03	Fail, 672	786	737
3200	1.04e-04	6.1e-03	Fail, 818	898	766
3200	1.12e-04	5.8e-03	Fail, 757	841	709

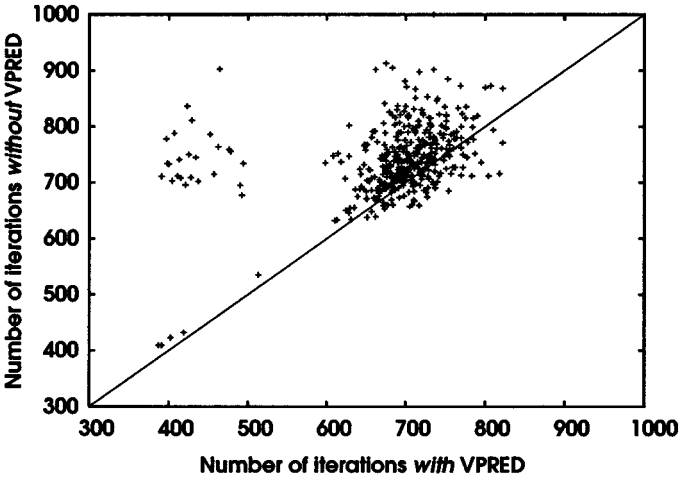


Fig. 10. Effect of applying Voltage Prediction Algorithm (Forced-Convergence Algorithm is used in both cases).

VII. CONCLUSION

RTDs are at the forefront of emerging technologies that are expected to play a significant role in continuing IC performance improvements beyond what may be possible by scaling alone [37]. Published results indicate that usage of RTDs in conjunction with HBTs or HEMTs in III–V compound materials like Gallium Arsenide (GaAs) or Indium Phosphide (InP) [1], [35], and [38] can lead to the realization of very compact high-performance circuits and systems. The inherent bistability of the device and its picosecond switching speed can be exploited to conceive novel circuit ideas that may find use in future-generation communication systems.

In order to design high-performance RTD circuits, the development of an accurate simulator for such circuits is of central importance. In this paper, we have presented a study of the convergence problems that SPICE-like simulators may face while simulating RTD circuits. We have also presented a suite of techniques that, when added to Berkeley SPICE, can lead to efficient simulation of these circuits. From the results obtained, we can draw several conclusions. First of all, the wide range of negative conductance values of the NDR region of the physics-based RTD curve increases the probability of causing numerical instabilities for the simulator. Second, the in-built continuation techniques of SPICE 3F5, namely Gmin-stepping and Source-stepping, may fail to simulate many RTD circuits. Third, an effective approach for dc convergence seems to be the application of the limiting algorithm of Section IV-A-2 backed up by the RTD-stepping technique. Fourth, during transient analysis, the *time-step too small* problem can be dealt with by a combination of a modified forced-convergence algorithm and a voltage prediction scheme (Section V-A-2). Fifth, a time-step adjustment (Section V-A-2) algorithm may prevent convergence to undesirable solutions during transient simulation of certain types of RTD circuits.

The contributions of this paper include: 1) a survey of the various methods that have been employed to simulate RTD or tunnel diode circuits as of this work; 2) incorporation of a physics-based model of the RTD into Berkeley SPICE 3F5; 3) identification of the sources of dc convergence problems for RTD circuits; 4) a new continuation technique (RTD-stepping) and a modified current iteration method for improving dc convergence; 5) identification of different scenarios for transient convergence problems for high-speed RTD circuits; and 6) a modified forced-convergence technique, a new time-step adjustment algorithm, and a modified device voltage prediction algorithm for handling transient convergence problems.

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