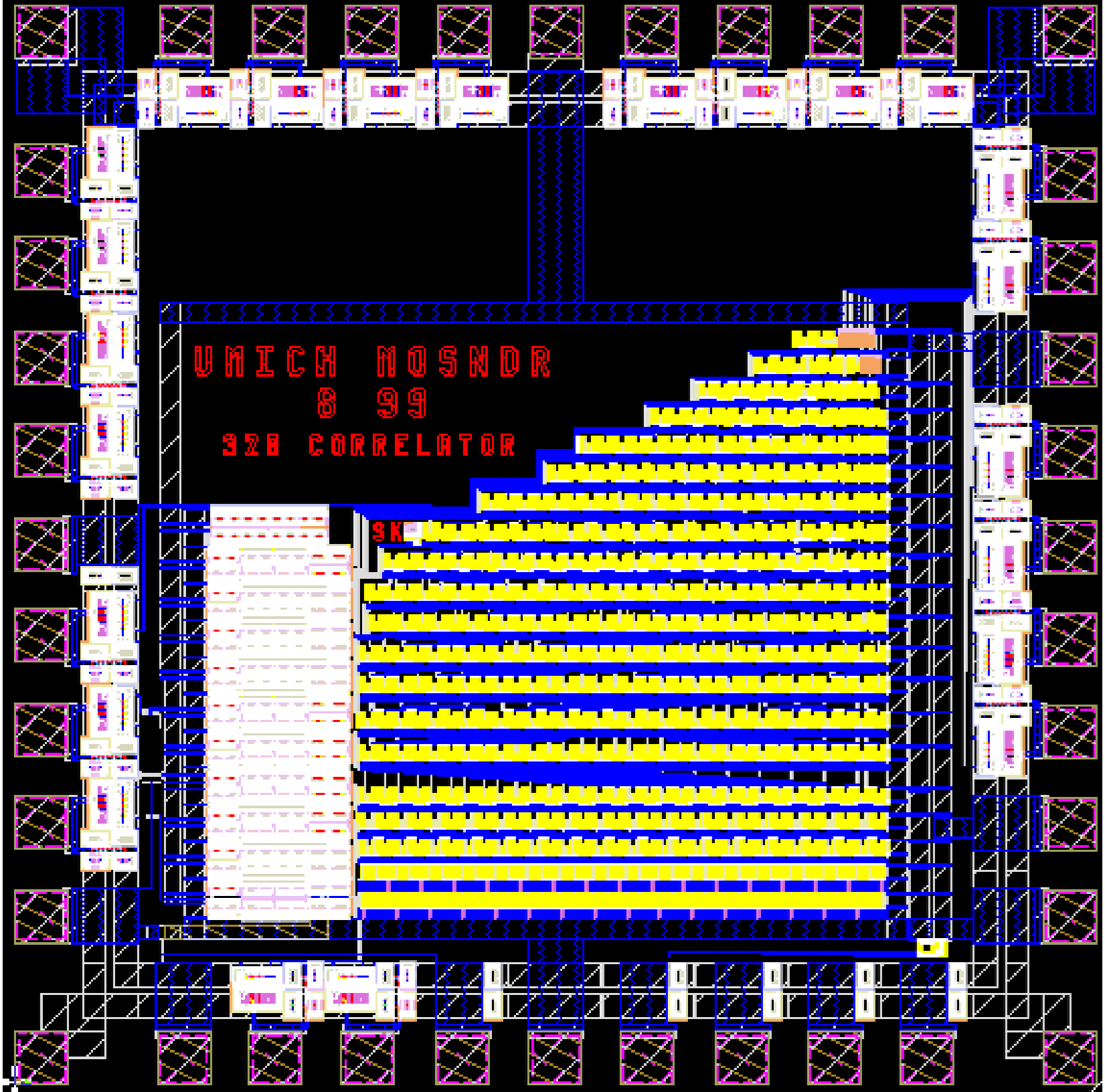
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32B CORRELATOR

A 250-MHZ, 32-BIT QUANTUM MOS CORRELATOR PROTOTYPE

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ABSTRACT

Simulation results of Quantum MOS circuits comprising resonant-tunneling diodes (RTDs) and MOSFETs indicate greater than twofold improvement in power-delay product over CMOS. However, the challenges of co-integrating RTDs and CMOS devices have not been completely overcome yet, leaving the testing of RTD-CMOS circuit ideas to be accomplished by either simulation, or by electrically connecting discrete RTDs to CMOS chips, or by grafting and bonding RTDs to CMOS chips via a complicated hybrid integration process. While research in RTD-CMOS co-integration is ongoing, we present a 250-MHz, 32-bit QMOS correlator prototype that uses only MOS devices to emulate RTDs.

1. INTRODUCTION

Over the past few years, the negative differential-resistance (NDR) characteristics of resonant-tunneling diodes (RTDs) have been exploited to design extremely fast, compact, and inherently bistable circuits in conjunction with III-V transistors [1]. These circuits demonstrate reduced complexity for implementing a given function and superior power-delay performance as compared to conventional circuits. Recent reports of the possibility of achieving resonant tunneling using, for example, a Silicon/Silicon-dioxide heterostructure [2] make it attractive to envision these compact, high-performance circuits implemented in a technology such as CMOS that offers low power dissipation and very high integration levels. While research in RTD-CMOS co-integration, referred to as Quantum MOS (QMOS), is ongoing, we have developed a method for emulating I-V characteristics of RTDs using only MOS devices [3]. This method overcomes the following disadvantages of hybrid RTD-MOS integration [4] currently available for QMOS circuit prototyping: 1) large area overhead, 2) inability to integrate large scale NDR circuits, 3) poor switching speeds, 4) increased design turnaround time, 5) increased process complexity, and 6) increased cost. This new prototyping method for QMOS circuits has made possible the implementation of the 32-bit parallel correlator which is the first known LSI circuit that uses NDR logic.

2. QMOS OPERATING PRINCIPLE

The possibility of two stable RTD operating points at the same current level, due to NDR characteristics, makes bistable RTD-CMOS logic feasible [5]. Fig. 1(a) illustrates a bistable QMOS gate. An RTD forms the active load in the circuit, the n-type pull-down network determines the circuit function, a clock transistor controls the evaluation of the gate, and a bias transistor maintains the quiescent current through the RTD while also controlling the precharging of the gate output. Fig. 1(b) shows the load lines for the bistable logic gate. Using a two-phase clocking scheme, multiple bistable QMOS logic gates can be cascaded to implement any given function, pipelined at the gate level without necessity for separate latches. This eliminates area, delay, and power overhead of discrete latches. Simulation results of a 0.35-micron QMOS bistable inverter indicate a power-delay product of 5.4 fJ at 1.5 V supply as compared to 11 fJ for a dynamic CMOS circuit. Advantages of QMOS stem from the high switching speed and bistability of the RTD, the elimination of p-type devices that limit CMOS circuit performance, the reduction of charge-sharing susceptibility that affects dynamic CMOS, and the possibility of lower voltage operation due to elimination of PMOS

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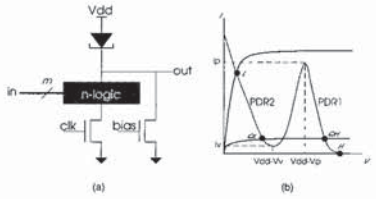


Figure 1: (a) Bistable-mode QMOS logic gate (b) Load lines for bistable QMOS gate operating point

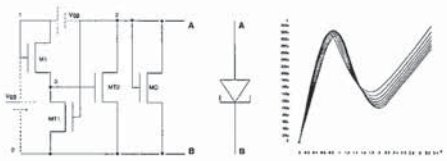
device threshold voltage drop.

3. ENHANCEMENT-MODE NMOS NEGATIVE DIFFERENTIAL-RESISTANCE CIRCUITS

The MOSFET circuit used as an RTD emulator [3] is illustrated in Fig. 2(a). The simulated I-V characteristics of this circuit under variable source-bulk bias are presented in Fig. 2(b). This circuit was derived from a Λ-type circuit (implying that the I-V characteristic of the circuit resembles the letter Λ of the Greek alphabet) described in [6]. The transistor MD has been added to model the PDR2 region of the RTD characteristics. As in most NDR-producing FET circuits, the transistor MT2 needs to be taken from cutoff to saturation and then back to cutoff as the voltage between nodes A and B is ramped up from zero. To achieve this, the voltage at the gate of MT2 has to decrease as the applied voltage increases, which is made possible by connecting the gate of MT2 to the output of an inverter circuit formed by M1 and MT1. M1 is a saturation-mode active load of this inverter circuit whose input is node A.

3.1. Emulating a given RTD characteristic

Even though we derived analytical equations for designing the NMOS circuits to match a given RTD characteristic, the hand-calculated results are very crude and the resulting errors are particularly large with respect to deep submicron MOSFET models like the BSIM3v3 model [7]. The particular methodology we have adopted to precisely design the RTD-emulating NMOS circuits is as follows. First we perform hand calculations to derive approximate transistor sizes for achieving the peak region specifications. Based on



(a) (b)

Figure 2: (a) Four transistor RTD emulator showing two possible positions of V_{gg}. (b) I-V characteristics of MOSFET NDR circuit.

SPICE simulation, we verify if the resulting circuit produces approximately an RTD-like characteristic with a visible NDR region. This usually takes a couple of iterations. Next, starting from these hand-calculated sizes, we use a circuit optimization tool to find the optimal values of the transistor sizes that would give us the best possible fit for the target current and voltage values. The tool we have used for this purpose is CUMIN [8], which is a SPICE-based, flexible direct-search optimization software in which any arbitrary cost-function can be defined very easily. The particular cost function we have found to be adequate for our purposes is given by:

$$\text{Cost} = \left|\frac{\hat{I}_p - I_p}{I_p}\right| + \left|\frac{\hat{I}_v - I_v}{I_v}\right| + \left|\frac{\hat{V}_p - V_p}{V_p}\right| + \left|\frac{\hat{V}_v - V_v}{V_v}\right| + \left|\frac{\hat{I}_s - I_p}{I_p}\right| \quad (1)$$

where variables with a caret represent the values corresponding to a particular circuit. $\hat{I}_s$ represents the current through the device when the voltage across it is V_s (the desired value of this current is, of course, I_p).

The RTD emulator is used to implement a MOSFET NDR shift register whose simulation results depicted in Fig. 3 indicate more than twofold improvement in switching speed over a hybrid integrated NDR shift register.

4. SYSTEM LEVEL DESIGN: 32-BIT CORRELATOR

Communication systems and signal processing systems represent two application areas where deeply pipelined systems are effective because of the volume and similarity of computational requirements at each

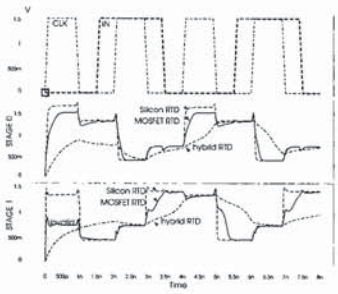


Figure 3: Simulation traces of NDR shift register.

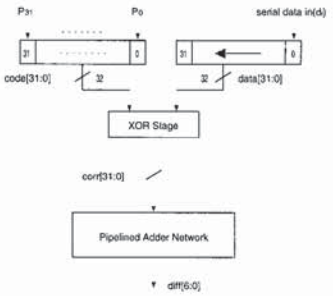


Figure 4: Block diagram of a 32-bit parallel correlator.

clock cycle. These systems have minimal data dependence between active computations in pipeline stages and hence are ideal candidates for implementation using gate-level pipelined QMOS logic. Typically, in spread spectrum systems, a parallel correlator computes the correlation of the incoming data stream with a predetermined pseudonoise (PN) sequence of fixed length to estimate the output data. For secure and noise-free communication, a long PN sequence length is desirable, resulting in reduced symbol transmission rate. To maintain high transmission rates, it is therefore necessary to employ high-speed circuits in the receiver. A QMOS gate-level pipelined correlator can fulfill these requirements. The pipelined correlator illustrated in Fig. 4 uses a 32-bit register to hold the PN sequence. The input serial bit stream is fed to a 32-bit shift register. The 32-bit registers are each composed of 64 bistable QMOS inverters. A pair of cascaded bistable inverters, each operating on separate phases of a two-phase clock, form a master-slave flip-flop.

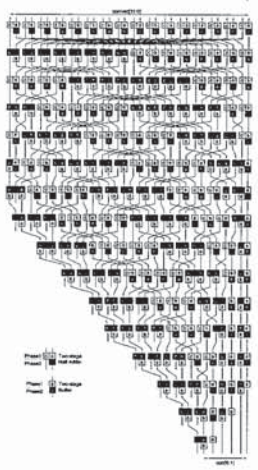


Figure 5: 32-bit pipelined adder network.

A 32-bit correlation vector generated by performing a self-latched bit-wise XOR on the PN sequence and the most recent 32 bits of the input data forms the input to a pipelined adder network that determines the correlation value at each cycle. The pipelined adder network, illustrated in Fig. 5, is the computational core of the parallel correlator. The circuit performs 14 stages of addition to generate a 7-bit correlation result at each clock cycle.

5. RESULTS

The correlator, illustrated in Fig. 6, has been fabricated using a Hewlett-Packard 3-metal, 1-poly process with MOSIS 0.6-micron scalable CMOS design rules. The pad-limited die of 1.94 mm $\times$ 1.94 mm includes 16,000 MOSFETs, and 1110 RTDs are emulated. The correlator is clocked at 250 MHz resulting in one 32-bit correlation every 4 ns. The clock generation circuitry uses phase splitters at the output of the final clock drivers to generate the necessary two-phase clocks. As far as possible, the clock and data flow are in opposite directions to minimize effect of clock skew. Due to the low voltage (2-V) operation, and given the 0.6-V threshold voltage of NMOS devices, half adders are used in the pipelined adder network to limit the number of series transistors in the pulldown network. Level-shifting circuitry drives the I/O pads operating at

Figure 6: Layout plot of 32-bit QMOS prototype currently under fabrication.

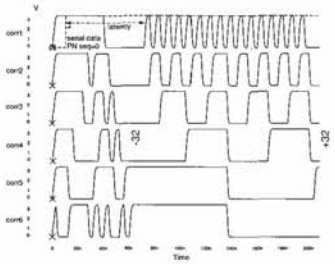


Figure 7: Simulation result showing correlation value changing from -32 to $+32$ in response to serial data input change.

the process recommended 3.3 V. It should be noted that the RTD emulation circuitry uses weak MOSFETs and hence the prototype circuit cannot match the projected speed of QMOS circuits using RTDs. Fig. 7 illustrates the simulation results of the 32-bit correlator with a PN sequence value of 0 which results in the correlation output changing from -32 to $+32$ when the input data signal changes from 0 to 1. The estimated data is the complement of the sign bit when the correlation threshold is met.

6. CONCLUSIONS

In this paper we have presented the first large-scale integrated circuit that uses NDR logic. The CMOS prototype of a quantum MOS circuit allows system-level verification of RTD-CMOS circuit ideas till such time when Silicon-based RTDs are fabricated with ease. The correlator circuit exploits the gate-level pipelining feature of QMOS logic to achieve high-throughput operation. This fine-grained pipelining scheme benefits communication system components that have minimal data dependence among a large volume of similar computations at each clock cycle. The fewer number of devices used in the QMOS correlator also imply a reduction in wiring lengths, translating to smaller parasitics and hence lower interconnect delays at the system level as compared to a conventional implementation.

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