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Straintronics

A leap toward ultimate energy efficiency of magnetic random access memories.

AGGRESSIVE SCALING OF COMplementary metal–oxide–semiconductor (CMOS) technologies in the past decade has left circuit engineers with a plethora of design challenges. As the feature size in CMOS scales below 22 nm, static power dissipation due to multiple sources of leakage (weak inversion current, drain induced barrier lowering, gate induced drain leakage, gate tunneling, etc.) becomes significantly large in digital circuits. The supply voltage, on the other hand, does not scale down equally. Therefore, the shorter channel length along with a high supply voltage leads to a high leakage power dissipation. Integrated systems are facing an increasing leakage to active power ratio [1]. Leakage is more pronounced in low-speed applications, such as biomedical devices, where the performance is limited to a few megahertz [2]. Another obstacle, which is mainly a concern for high-speed applications, is the increasing energy density [3], which requires complicated cooling schemes and packaging. Furthermore, battery technologies are not growing as fast as CMOS technology, leaving large portable systems with a few microwatts of power to live on. The obstacles facing circuit designers call for novel solutions to enable the industry to push the integration density as prophesized by Moore's law [4]. Alternative technologies need to be combined with CMOS to overcome the shortcomings of CMOS technologies.

The magnetic tunneling junction (MTJ) has been proposed as an energy-efficient nonvolatile device that can be combined with CMOS elements to create energy-efficient memories and systems. Magnetic logic has an inherent energy advantage over charge-based logic. Theoretically, the energy required to switch the state of a charge-based logic is $E_{\min-\text{charge}} = NkTln(1/p)$, where N is the number of charge carriers, k is the Boltzmann constant, T is the temperature,

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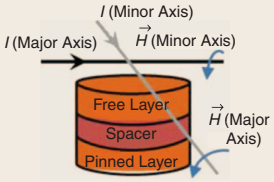
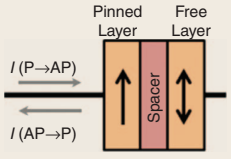
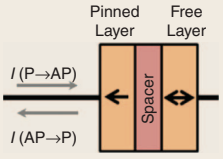
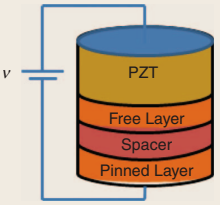
TABLE 1 A comparison of FIMS, STT, and straintronics magnetization switching approaches.

	FIMS	IN-PLANE STT	PERPENDICULAR-TO-PLANE STT	STRAINTRONICS
Methodology	V→I→H→M	V→I→M	V→I→M	V→S→M
View of the cell				
Switching energy (kT)	~10^{11}	~10^{8}	~10^{7}	~10^{3}
Switching delay (ns)	10–50 ns	5–20 ns	Several nanoseconds	Hundreds of picoseconds to 2 ns
Scalable with CMOS?	No	Yes	Down to ~20 nm tech	Yes
Operating voltage?	1 V and up	0.5 V and up	0.3 V and up	0.01 V and up
Possibility of read disturbance?	No	No	Low	No

V: voltage; I: current; H: magnetic field; M: magnetization; S: strain; P: parallel; AP: antiparallel.

> Straintronics can provide a much more energy-efficient approach for Bennett clocking, leading to a much more energy-efficient neuron model.

and p is the error probability [5]. For magnetic logic, this energy limit reduces to $E_{\min-\mathrm{mag}} = kTln(1/p)$ since the magnetic domains align with each other. This inherent advantage, however, is not leveraged in magnetic memories, as most of them use the flow of current (electric changes) to achieve the write operation into the magnetic memory cell [6], [7]. Hence, efforts to minimize the write power of the magnetic logic to leverage the inherent energy and data retention advantages of such devices continue unabated.

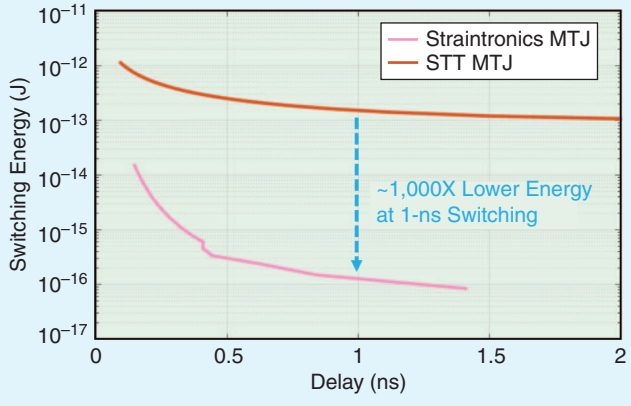


FIGURE 1 A comparison between an STT and a straintronics MTJ in terms of energy–delay tradeoff.

The conventional field-induced magnetization switching (FIMS) uses the flow of current in a neighboring wire to switch the magnetization state of the MTJ device. This method is energy inefficient, and the possibility of half-select errors makes this scheme area inefficient. Spin-transfer-torque (STT) switching, which employs a spin-polarized current to assist with switching, is highly area and energy efficient. This method has demonstrated promising features comparable with pure-CMOS systems. However, like FIMS, STT still employs the flow of static current for the write operation, which eventually nullifies the inherent energy advantage of the MTJ. To maximize the energy efficiency, the amount of charge required to switch the state of the MTJ should be minimized. To this end, straintronics, as an alternative energy-efficient method to switch the state of the MTJ, was recently proposed [8], [9].

In this article, we provide a review of straintronics magnetic data storage and its advantages over FIMS and STT technologies. Furthermore, we discuss a recently proposed nonvolatile straintronics-based random access memory (RAM) [10] that combines piezoelectricity and

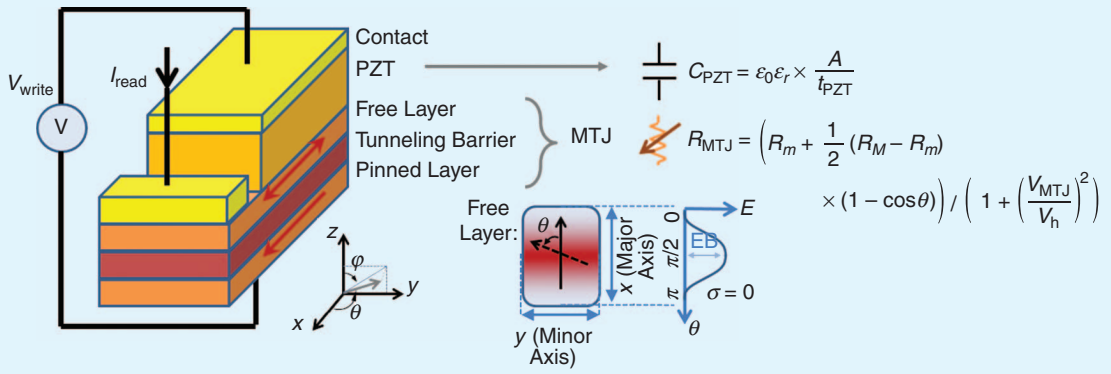


FIGURE 2 The straintronics MTJ and its electrical model and the demonstration of the intrinsic EB.

the Villari effect to assist with MTJ switching to build an energy-efficient nonvolatile magnetic memory. We will discuss the use of straintronics devices for application-specific systems by introducing straintronics-based random number generation and artificial neuron implementation. The use of voltage pulses instead of static current makes the straintronics device highly energy efficient, as demonstrated in Table 1.

> The magnetic tunneling junction has been proposed as an energy-efficient nonvolatile device that can be combined with CMOS elements to create energy-efficient memories and systems.

It is worthwhile to observe the energy–speed tradeoff of the straintronics MTJ (STJ) and its STT peer. The MTJ switching delay t_{sw} in an STT MTJ is expressed using the current-delay equation [11] $t_{sw} = \tau_0 \ln(\pi/2\theta_i)/(I/I_C - 1)$, where I is the current passing through the device, I_C is the critical switching current, τ_0 is the natural time constant, and θ_i is the initial magnetization angle due to thermal fluctuations. Given the high requirements

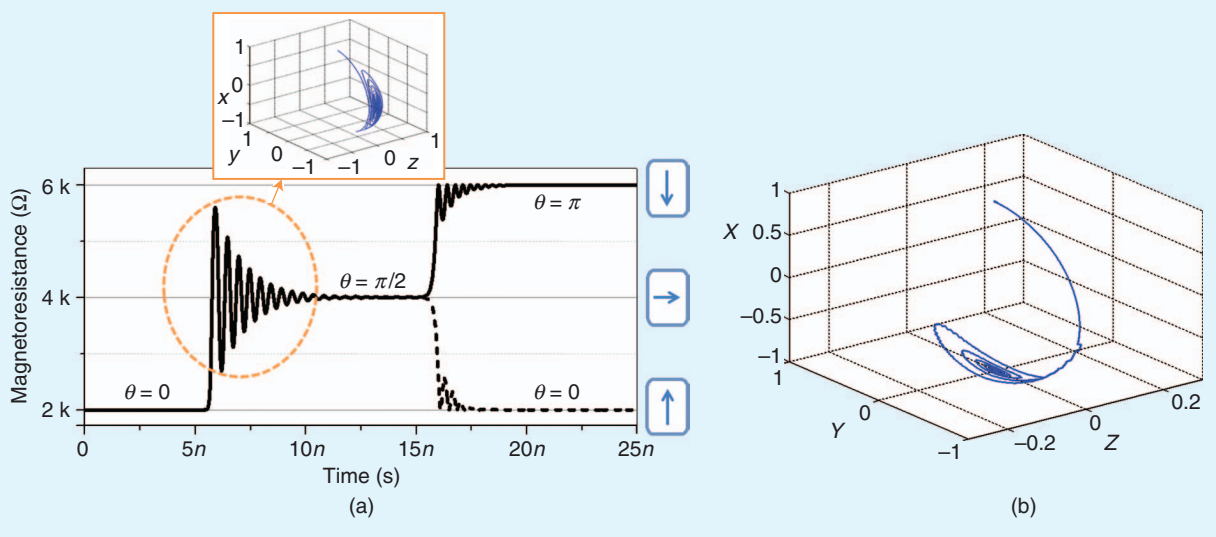


FIGURE 3 (a) By applying a voltage pulse, the magnetization vector settles at $\theta = \pi/2$. If the voltage is retained, the magnetization vector settles at the metastable state, where, upon removing the voltage, the magnetization can settle at either P or AP orientation. (b) If the pulse is tailored carefully, the magnetization vector will continue rotating and will settle at the opposite state.

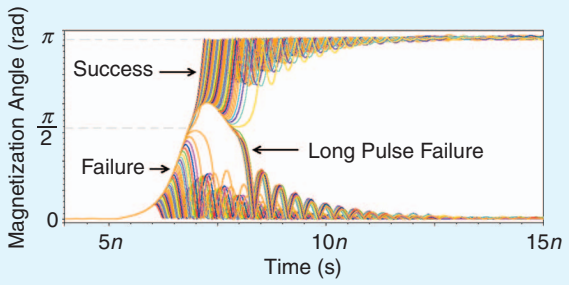


FIGURE 4 A demonstration of successful flipping when the applied pulse is tailored properly; if the pulse is removed too quickly or too late, the magnetization will bounce back and settle at the original state.

> Efforts to minimize the write power of the magnetic logic to leverage the inherent energy and data retention advantages of such devices continue unabated.

of current for STT switching (on the order of a few hundred microamperes for an in-plane MTJ and a few tens of microamperes for a perpendicular-to-plane MTJ), fast switching will require high energy investments, as demonstrated in Figure 1. This tradeoff is much less severe for straintronics devices with the same thermal stability, where the application of a voltage slightly higher than the critical voltage switches the magnetization state. Switching delays, as fast as a few hundred picoseconds, can be accomplished by merely investing below-femtojoule energies.

The energy efficiency that the STJ brings to the table, along with the inherent data retention, data endurance, and small size of the MTJ, makes the straintronics memory a good candidate to fulfill the requirements of a universal memory [12], a storage hierarchy that digital designers envision to improve the overall performance of the system in terms of energy per operation, speed, and reliability.

STJ AS DATA STORAGE UNIT

A view of the STJ and its equivalent electrical model is demonstrated in Figure 2. The device is made by placing a piezoelectric layer (PZT) on top of the free layer of an MTJ. The thickness of the PZT is selected to be four times larger than the free layer while keeping a large plane interface between the PZT and the MTJ. This will ensure that the majority of stress will transfer from the PZT to the free layer [8], [13].

In the absence of an external stress, the free layer's magnetization vector settles along the major axis in parallel (P, $\theta = 0$) or antiparallel (AP, $\theta = \pi$) orientations because of the intrinsic magnetic energy barrier (EB), as demonstrated in Figure 2. The principle of straintronics expresses that the state of the MTJ can switch from P to AP and vice versa through the following steps:

1) An applied voltage across the STJ creates an electric field in the PZT.
2) The electric field modifies the shape of the PZT due to the modified Hooke's law for piezoelectricity.
3) The physical deformation transfers a strain to the free layer of the MTJ.
4) If the applied voltage is high enough, due to the inverse magnetostriction (Villari effect), the magnetization vector of the device

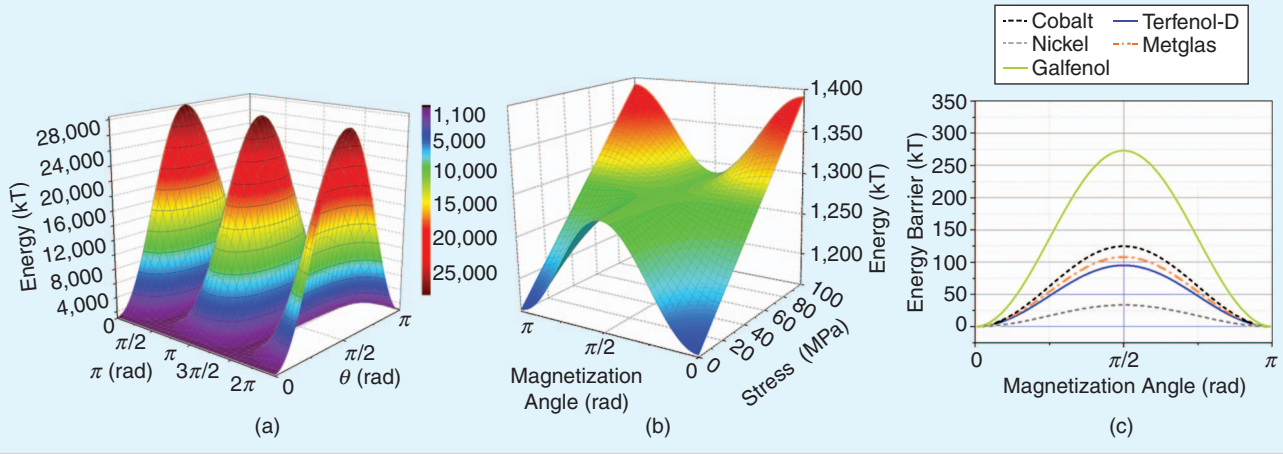


FIGURE 5 (a) The magnetic energy of the free layer as a function of the magnetization vector's orientation, (b) the EB and its elimination under an applied stress, and (c) different materials used as the free layer demonstrate different EBs.

will be forced to align along the minor axis, as demonstrated in Figure 3(a). The polarity of the voltage is selected to ensure a tensile stress that will make the minor axis the energy minimum in the presence of high stress.

5) If the duration of the applied pulse signal is selected properly [14], the magnetization vector will continue rotating after removal of the pulse signal and will settle in the opposite orientation, as demonstrated in Figure 3(b).

The proper selection of the pulsewidth is critical to achieve successful switching of the free layer in the STJ. As illustrated in Figure 4, removing the voltage pulse too soon will not give enough time for the magnetization vector to flip. However, removing the voltage pulse too late will also make the magnetization vector bounce back into the original magnetization state. The applied pulse should be tailored carefully to ensure successful flipping.

In the absence of stress, the intrinsic magnetic energy of the device is mainly dominated by shape anisotropy and uniaxial anisotropy. The total intrinsic magnetic energy of the free layer is given by

$$E_{\text{int-mag}}(\theta,\varphi) = \frac{\mu_0}{2} M_s^2 N_{\text{sh}}(\theta,\varphi) + K_u \sin^2\theta, \quad (1)$$

where the first term indicates shape anisotropy energy, and the second term is the uniaxial anisotropy energy. In (1), μ_0 is the permeability of vacuum, M_s is the saturation magnetization of the magnet, and K_u is the uniaxial anisotropy coefficient. $N_{\text{sh}}(\theta,\varphi)$ is the demagnetization factor, which assumes its maximum and minimum along the z-axis and x-axis, respectively, and has a saddle point along the y-axis. The free layer's magnetic energy level is, therefore, a function of the magnetization orientation, which is simulated and visually demonstrated in Figure 5(a). The shape anisotropy will force the magnetization to stay mainly in the $x-y$ plane. Furthermore, within this plane, there is an EB between the minor axis and the major axis of the device, as demonstrated in Figure 5(b) (at stress = 0). This makes the P and AP orientations the preferred orientations of the free layer's magnetization vector in the absence of an external stress. It should be noted that the EB is material dependent,

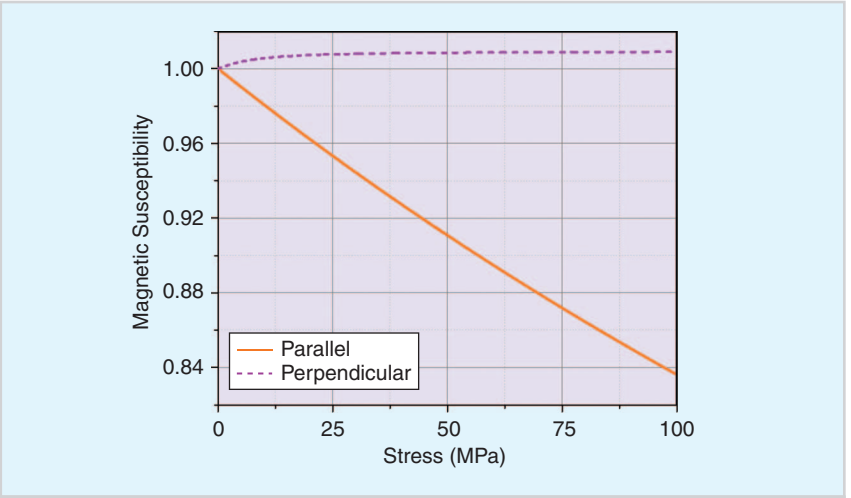


FIGURE 6 The effect of applied stress on the directional susceptibility of the free layer; the parallel component will be reduced, while the perpendicular component will increase slightly.

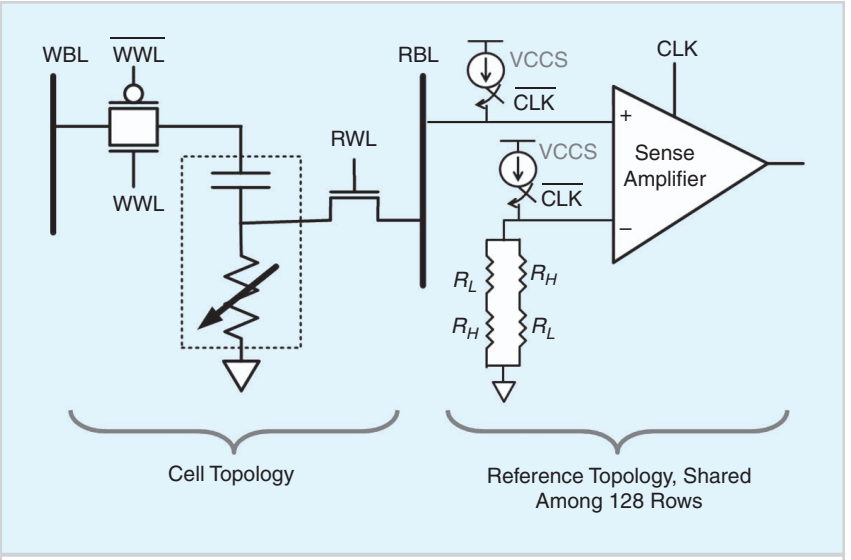


FIGURE 7 The memory cell architecture, the reference cell, and the detection circuitry. CLK: clock; WBL: write bit line; WWL: write word line; RWL: read word line; RBL: read bit line; VCCS: voltage-controlled current source.

The polarity of the voltage is selected to ensure a tensile stress, which will make the minor axis the energy minimum in the presence of a high stress.

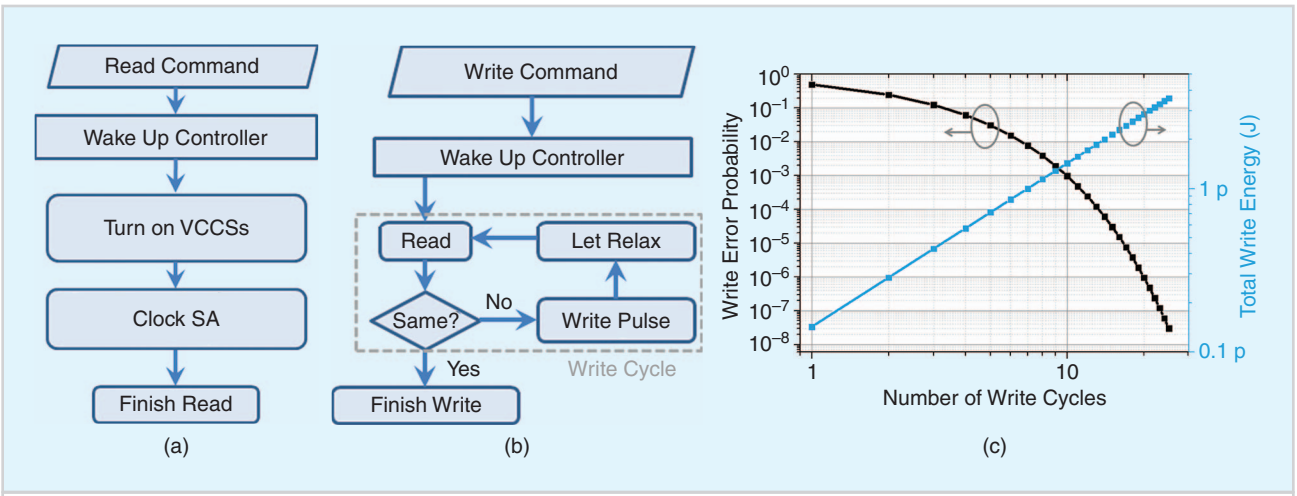


FIGURE 8 (a) The read algorithm, (b) the write algorithm with the write cycle shown, and (c) the WEP and total write energy as a function of the number of write cycles.

> STT still employs the flow of static current for the write operation, which eventually nullifies the inherent energy advantage of the MTJ.

and among the five simulated materials in Figure 5(c), nickel shows the lowest EB due to its low M_s value, while Galfenol has the highest level of EB mainly because of its high M_s.

An applied stress σ on the free layer of the MTJ leads to stress anisotropy energy [$E_\sigma = (3/2)\lambda_s \sigma \sin^2\theta_\sigma$, with λ_s being the magnetostriction coefficient and θ_σ being the magnetization vector's angle with the minor axis], which will eliminate the EB of the free layer, as demonstrated in Figure 5(b). The required stress for eliminating the EB, called the critical stress, is shape and material dependent [9].

The elimination of the EB in a straintronics device is due to the magnetostrictive response of the free layer to the applied stress. A uniaxial stress σ will manipulate the directional magnetic susceptibilities of the free layer [and, therefore, manipulate $N_{sh}(\theta, \varphi)$], reducing its parallel magnetic susceptibility $\chi^{\parallel}$ while slightly increasing the perpendicular susceptibility $\chi^{\perp}$, as predicted by [9], [15]

$$\chi^{\parallel}(\sigma) = \frac{\chi_0}{1+\beta\sigma}, \tag{2}$$

$$\chi^{\perp}(\sigma) = \frac{\chi_0}{1+\sqrt{k^2+\frac{1}{4}\beta^2\sigma^2}-\left(k+\frac{1}{2}\beta\sigma\right)}, \tag{3}$$

where χ_0 is the intrinsic susceptibility under no-stress conditions, and β and k are materially dependent parameters. The manipulation of the directional susceptibilities is highlighted in Figure 6 for the STJ with cobalt as the free layer. When the stress is high enough [9], the directional susceptibilities will favor the magnetization vector's settlement along the minor axis.

The STJ has a rectangular shape, as shown in Figure 2. The PZT material is chosen to be lead–zirconate–titanate since it has a high piezoelectric coefficient and a high dielectric constant. Cobalt is selected as the free-layer material since it has a moderate critical switching voltage and a fast response time because of its low damping factor. The major and minor axes are selected to be 205 and 195 nm, respectively, and the thickness of the free layer is 10 nm. The PZT is four-times thicker than the free layer. This, along with the large plane interface between the PZT and the free layer, ensures that the majority of strain will transfer from the PZT to the free layer.

The MTJ is modeled as a variable resistor. The value of the resistance is a function of the relative orientation of the free layer and the pinned layer. A parallel orientation leads to the minimum resistance, while an antiparallel orientation will lead to a maximum resistance value. These two states are the basis of binary data storage in an MTJ. The PZT is modeled as a parallel plate capacitance, which makes the equivalent electrical model of the device an RC circuit, as demonstrated in Figure 2.

MEMORY CELL TOPOLOGY AND READ/WRITE ALGORITHMS

The straintronics memory cell architecture comprising an STJ with CMOS access transistors is demonstrated in Figure 7. The read operation is performed through an n-channel MOSFET (NMOS) switch by sending a small current through the MTJ and sensing its state. The current level is retained within a few microamperes to avoid any STT

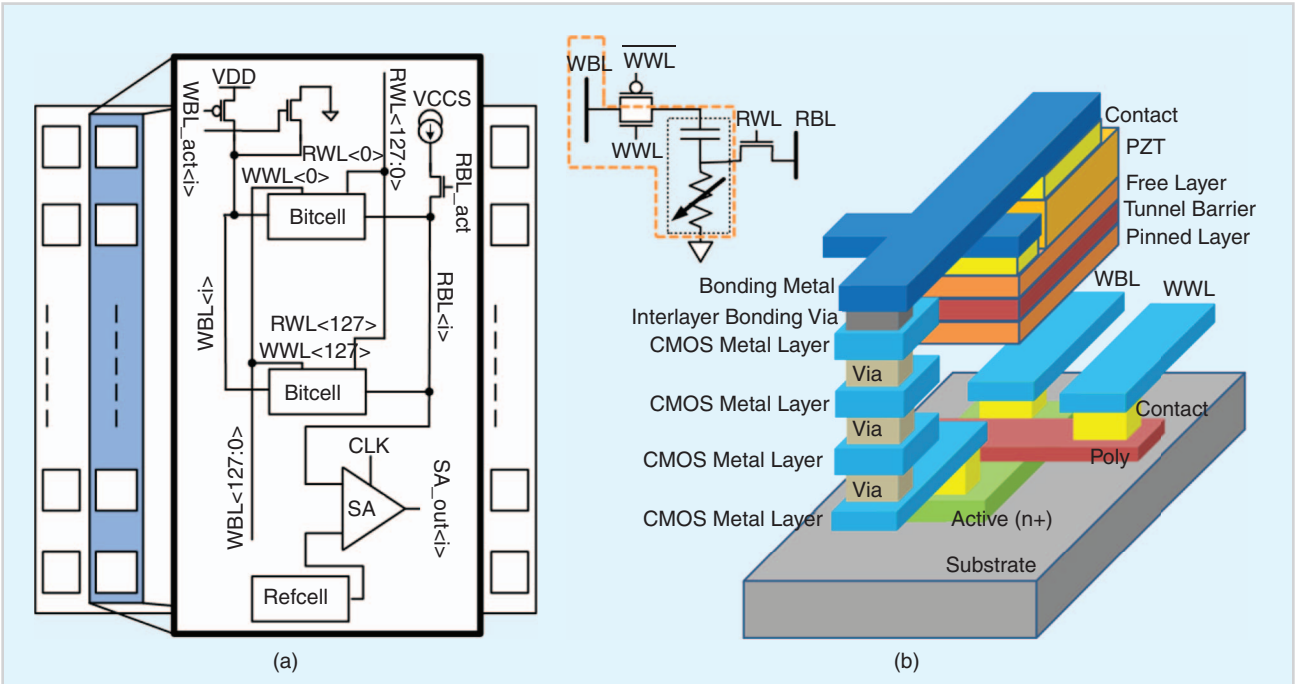


FIGURE 9 (a) The proposed 2-kb memory architecture and (b) a demonstration of the physical connection of the STJ to the NMOS access transistor as part of the bitcell layout.

read disturbances. A voltage-controlled current source (VCCS) is used to generate such current. Since the read voltage stays well below the technology's power supply (VDD) levels, an NMOS would suffice for the read operation.

When it's not performing read or write operations, the memory switches to sleep mode by disconnecting from the power supply. Because of nonvolatility, the stored data will remain unchanged. The sleep mode can significantly save power in low-speed battery-operated applications such as sensor nodes and biomedical implants.

The write operation is performed by applying a pulse signal across the STJ. Since the applied pulse can swing between high and low voltages, a transmission gate is chosen as a switch to relax the voltage-dependent resistance behavior of the access devices. Dynamics in the Landau–Lifshitz–Gilbert equation promise a certain pulsewidth that ensures successful flipping of the MTJ state, as discussed in the "STJ as Data Storage Unit" section. However, when the device is combined with CMOS circuitry, because of circuit fluctuations, skews, rise, and fall time limitations, the success is no longer guaranteed. Our simulations indicate a 65% success rate when a 75-mV pulse is applied across the STJ for 1.8–2.6 ns. The pulse amplitude can be increased to speed up the settling of the magnetization vector along the minor axis, which, in turn, reduces the success rate to values close to 50%. A 1-V pulse can switch the state of the device within 1 ns with a 50% success rate.

The 1-V pulse (instead of 75 mV) is more compatible with CMOS operating voltages and leads to a less complicated design. Therefore, it is more convenient to adopt this approach. It should be noted that regardless of the pulse amplitude, since the success is not fully guaranteed, the memory is always required to perform a read after writing to ensure a successful write operation. The write algorithm is demonstrated in Figure 8(b). The entire cycle of attempting to write into the STJ and reading the MTJ's state afterward is named a write cycle. There will be a trade-off between the number of write cycles M, the write error probability (WEP), and the total write energy E_{write}, as demonstrated in Figure 8(c). We have

$$E_{\text{write}} = E_{\text{write-cycle}} \times M,$$
$$E_{\text{write-cycle}} = E_{\text{write-pulse}} + E_{\text{read}}, \quad (4)$$

where $E_{\text{write-cycle}}$ is the energy consumed in one write cycle. As Figure 8(c) indicates, within 20 write cycles (equivalent to 80 ns of total write time, with each write cycle taking ~4 ns), a WEP less than 10^{-6} is achieved. This is much more efficient than the nonvolatile charge-based flash memory, taking only a few microseconds for writing. For example, the flash memory presented in [16] takes 20 μs for the write operation.

TABLE 2 A 2-kb straintronics memory specifications.

	MEMORY SPECS
Volatility	Nonvolatile
Technology	65 nm
Operating VDD	1
Cell area	0.2 μm^2
Read frequency	562 MHz
Write frequency at 10^{-6} WEP	12.5 MHz
E_{read}/b	0.049 pJ
E_{write}/b at 10^{-6} WEP	2.9 pJ

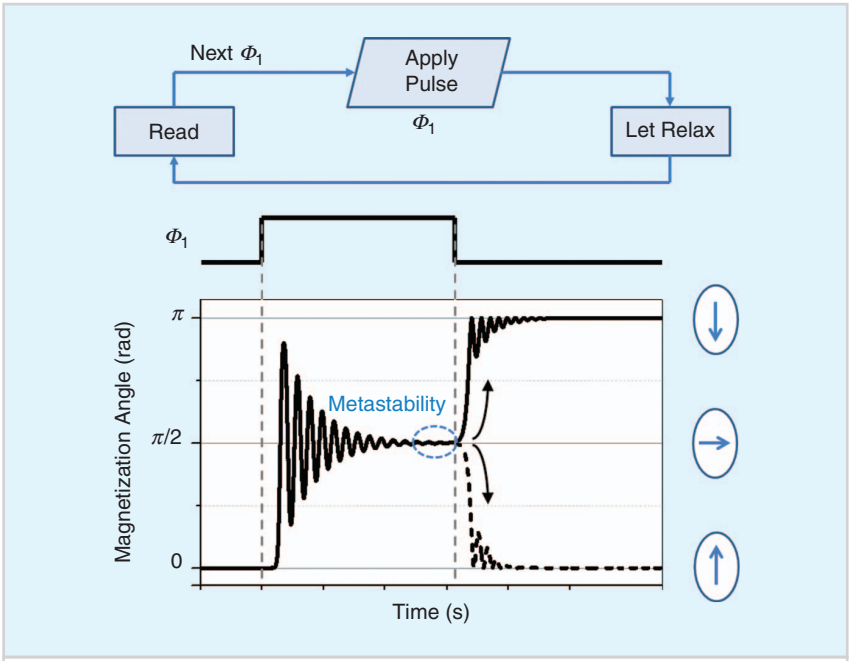


FIGURE 10 The algorithm for random number generation using STJ with the waveforms demonstrated.

From the graphs in Figure 8(c), it should be noted that while the write energy increases linearly with M, the WEP decreases exponentially. For example, increasing the number of write-cycles from $M = 10$ to $M = 11$ will halve the WEP at the expense of merely a 10% increase in the write energy. Therefore, a higher M is desirable for low-speed error-intolerant applications.

2-KB MEMORY AND ITS SPECIFICATIONS

The architecture of the straintronics memory is demonstrated in Figure 9(a). The 2-kb memory, designed and simulated in 65-nm CMOS technology, consists of 16 columns and 128 rows with 16-b simultaneous read/write input/output capability. CMOS controllers and address sequencers are used to generate the control and access signals. Because of the low operating voltage of the STJ, the entire system can operate in the deep subthreshold regime. The full compatibility with deep subthreshold operation plus immunity to CMOS noise and fluctuations (due to the EB) is one of the salient features of the straintronics device, which is not easy to achieve with FIMS and STT because of their high critical current values.

It has been practically demonstrated that MTJs can be fabricated on top of the CMOS circuitry to achieve higher design density [17]. Following the same design architecture, we demonstrated the proposed physical connection of the STJ and the NMOS access device in Figure 9(b). For simplicity and ease of demonstration, the figure does not contain the entire layout of the memory cell and only includes the memory cell's NMOS access device connected to the STJ's PZT.

The performance and energy specifications of the straintronics memory are demonstrated in Table 2. Since the STJ can be fabricated on top of the CMOS access devices, the bitcell size is estimated to be as

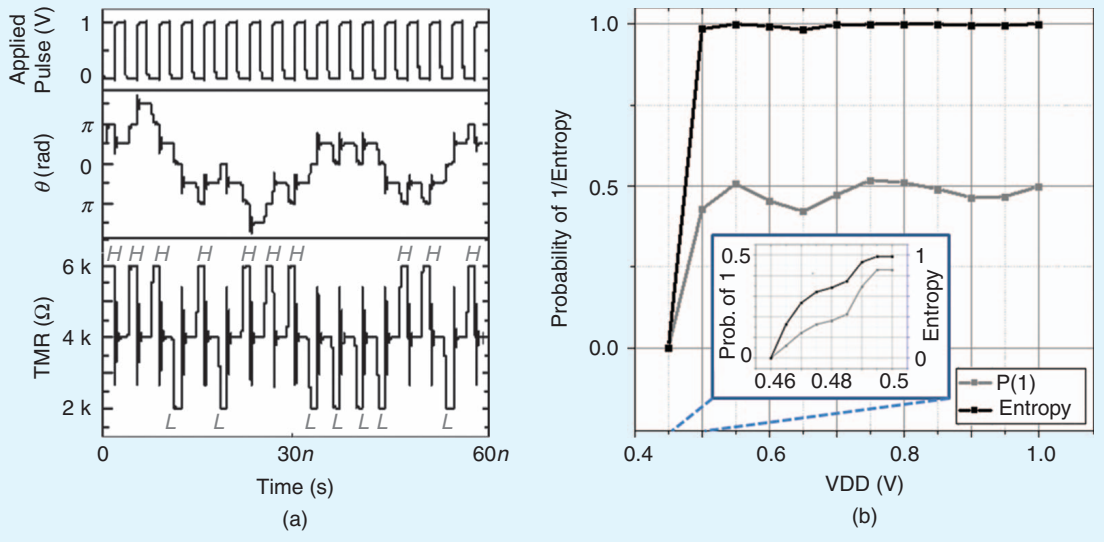


FIGURE 11 (a) The dynamic waveforms demonstrating random final state of the STJ and (b) the dependency of entropy on the system's operating voltage.

small as 0.2 μm^2. The memory can read as fast as 562 MHz. The write speed is adjustable based on the system's error tolerance, as discussed earlier. A write speed of 10 MHz leads to WEP $< 10^{-7}$. At 1-V operating voltage, the read access energy is merely 49 fJ/b for the entire system, while a write cycle consumes 143 fJ/b. The energies include the active and leakage power dissipations in the CMOS controllers.

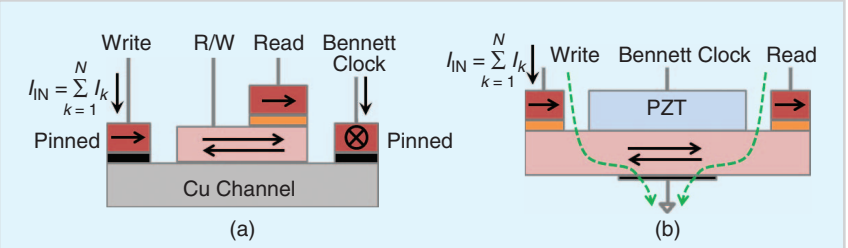


FIGURE 12 (a) The conventional Bennett clocking using STT. (b) The proposed neuron topology that uses the straintronics principle for Bennett clocking.

STRAINTRONICS FOR APPLICATION-SPECIFIC SYSTEMS

Straintronics, as described earlier and with its unique dynamic and static behavior, can have applications beyond memory design. In this section, we will take a step forward and propose the use of the straintronics principle in two application-specific systems: a true random number generator (TRNG) hardware and a neural network design. In both of these applications, the use of straintronics helps reduce the complexity of the conventional designs and reduces the required area and overall energy of the system compared to the works presented in the literature.

TRUE RANDOM NUMBER GENERATOR

When the voltage on top of the PZT is retained for a long time, the STJ will enter a metastable state, where successful flipping of the magnetization vector is no longer guaranteed [10]. This feature, however, is handy when we consider the random number generation procedure. Conventional TRNGs use the metastable state in CMOS back-to-back inverter loop [18], [19] or they combine a fast clock with a slow jittery clock [20]. Both of these approaches, however, are vulnerable to process variations and mismatch. Therefore, power- and area-hungry calibration circuitries are required to ensure that the generated numbers are truly random.

The proposed method for the generation of random numbers using the STJ is shown in Figure 10. First, a Φ_1 pulse is applied across the device and is retained until the magnetization vector settles into a metastable point. Then, the pulse is removed abruptly, which suddenly leaves the magnetization at a metastable state. Because of the thermal noise, the STJ will randomly settle down to either a P or an AP state. The STJ will be much less vulnerable to mismatch effects compared to the conventional CMOS since, as long as $x > y$ in Figure 2, a random final state is guaranteed.

The dynamic simulation results on the STJ's random flipping is demonstrated in Figure 11(a). The speed of the TRNG depends highly on how long it takes for the STJ to settle into the metastable state (material and voltage dependent) and how long it takes to relax back into the major axis. Our simulation indicates that if the voltage is reduced to values below 0.5 V, the STJ will not fully settle into the metastable state, leading to the loss of entropy, as demonstrated in Figure 11(b).

The use of STJ for true random number generation is highly energy efficient. The device, on its own, consumes the totally energy per operation of

$$E_{tot} = E_{cap} + E_d = CV^2 + E_d. \quad (5)$$

The first term is due to charging and discharging of the PZT capacitance and E_d is the energy due to Gilbert damping [21]. Our simulations indicate that the device can generate random states at 460 MHz with less than a 1-fJ energy requirement. It should be noted that the simulated energy is solely the STJ's energy dissipation. If placed in an entire TRNG system, CMOS controllers and sensing circuitry will increase the system's overall energy.

STRAINTRONICS FOR NEURON DESIGN

The use of STT devices and the domain wall motion systems have been proposed recently as an energy-efficient approach for neural network design. The work in [22] uses a STT-based device with three magnetic ports to create a neuron model, as demonstrated in Figure 12(a). The pinned magnet on the right side is solely used for the purpose of Bennett clocking. A current is flowed through this magnet to rotate the free layer's magnetization vector into the minor axis, and then the write current is applied. Much lower write current values are required since the device is already settled close to the minor axis.

Straintronics can provide a much more energy-efficient approach for Bennett clocking, leading to a much more energy-efficient neuron model. The proposed structure is shown in Figure 12(b). When performing a write operation (neuron sensing), a pulse is applied to the PZT to assist with Bennett clocking. The total current is then flowed through the write port. The neuron can send signals out to the other synapses through the read port. It should be noted that the proposed topology allows an unlimited number of neurons to be connected together in a neural network, something that is missing in some of the STT-based neural networks [23], [24].

The energy requirement for straintronics Bennett clocking of a 60 nm × 20 nm × 1 nm free-layer magnet in [22] can be as low as 3×10^3 kT, depending on the material choice. This is much lower than the STT Bennett clocking energy, where more than 10^6 kT (150-μA fast spike preset current) is required [22] to send the free layer's magnetization into the minor axis. This shows the inherent advantage of the straintronics principle for energy-efficient neuron design.

CONCLUSION

The straintronics device as a candidate for the design of nonvolatile energy-efficient RAM was demonstrated, analyzed,

and simulated, and the incorporation of the device in a memory cell architecture along with the specifications of the straintronics memory was highlighted. The topology of the memory cell comprising an STJ and CMOS access devices was introduced, and the read and write algorithms were discussed. The use of STJs for application-specific systems was investigated by introducing straintronics-based random number generation and artificial neuron design. The ultralow energy and fast response of the straintronics devices make them good candidates for energy-limited and energy-harvesting applications.

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