Brief Papers

Performance Modeling of Resonant Tunneling-Based Random-Access Memories

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***Abstract*—Resonant tunneling-based random-access memories (TRAMs) have recently garnered a great amount of interest among memory designers due to their intrinsic merits such as reduced power consumption by elimination of refreshing operation, faster read and write cycles, and improved reliability in comparison to conventional silicon dynamic random access memories (DRAMs). In order to understand the precise principle of operation of TRAM memories, an in-depth circuit analysis has been attempted in this paper and analytical models for memory cycle time, soft error rate, and power consumption have been derived. The analytical results are then validated by simulation experiments performed with HSPICE. These results are then compared with conventional DRAMs to establish the claim of superiority of TRAM performance to DRAM performance.**

***Index Terms*—Critical charge, dynamic random access memory (DRAM), power consumption, soft error rate (SER), tunneling-based random-access memory (TRAM).**

I. Introduction

SILICON dynamic random-access memories (DRAMs) are currently the dominant commercial commodity in the semiconductor memory market due to their lowest cost per bit, as well as giant integration scale that allows DRAM manufacturers to monolithically fabricate over 256 million cells per chip. However, these megasize DRAM chips are encountering several formidable problems due to a host of reasons, some of which are listed below.

First, DRAMs are becoming increasingly prone to soft errors due to aggressive shrinking of storage capacitor size. Soft error, also known as single event upset, is caused by extra charge collection in the storage node of memories, generally induced by external charged particles and neutrons. The chance of loss of a stored bit depends on the amount of critical charge of the storage node. Critical charge (Q_c) of a memory cell is defined as the minimum amount of single event induced charge at the sensitive circuit node necessary to cause the circuit state change. Technology scaling that achieves lowered capacitance, reduced power supply voltage, and tinier transistor geometries is generally deployed to increase the density and performance of the DRAMs; however, the scaling also concomitantly reduces the critical charge of the DRAM cell, thus increasing the soft error rate (SER).

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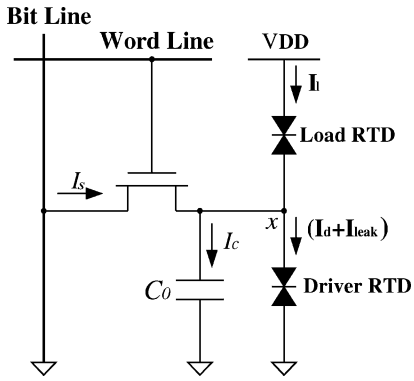

Fig. 1. Schematic diagram of 1T RTD-based RAM.

Second, a DRAM's power consumption largely depends on periodic refreshing of memory cells deemed necessary due to excessive leakage currents such as dark current, weak-inversion current through access transistor, and field current between storage nodes. The continuous downscaling of the transistor threshold voltage, as well as packing of memory cells more densely aggravates leakage currents, thereby significantly increasing the power consumption of DRAM chips.

With the objective to solving these problems, memory manufacturers are continuously pursuing circuit and technology innovations. Tunneling-based random-access memories (TRAMs) proposed in [1] are of interest because of their potential in increasing critical charge, while reducing power consumption due to dispensing with mandatory refreshing of cells in DRAMs. Nikolic and Forshaw [2] have made a preliminary simulation of a TRAM-based system and compared its performance with that of semiconductor CMOS, single electron tunneling (SET), and the electronic quantum cellular automata (EQCA) systems. Their simulation results show that the operation frequency of TRAM is approximately ten times faster than that of the CMOS system, 10^3 times faster than that of the EQCA system, and 10^5 times faster than that of the SET system.

A TRAM cell is composed of a conventional DRAM cell, being augmented by co-integrating a pair of series connected resonant tunneling diodes (RTDs) [3] near the cell capacitor, as shown in Fig. 1. The RTD is a heterostructure device consisting of a quantum well of low bandgap material, sandwiched between two barriers of high bandgap material. The RTD provides a folded-back *I–V* characteristic, as shown in Fig. 2. Instead of having a monotonic *I–V* characteristic like in MOSFETs and

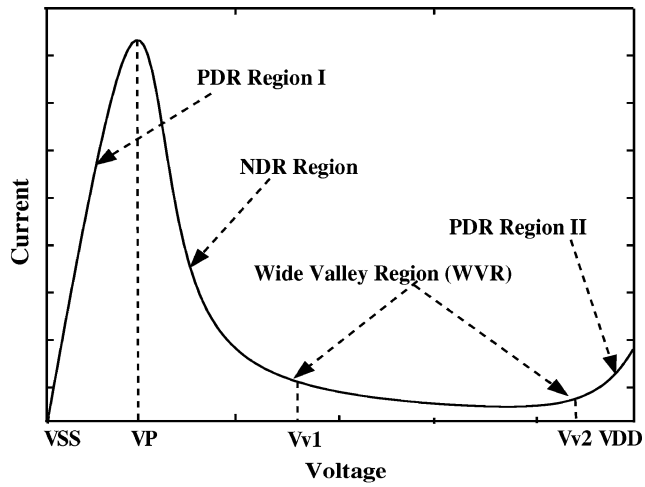

Fig. 2. Typical *I–V* characteristic of RTD.

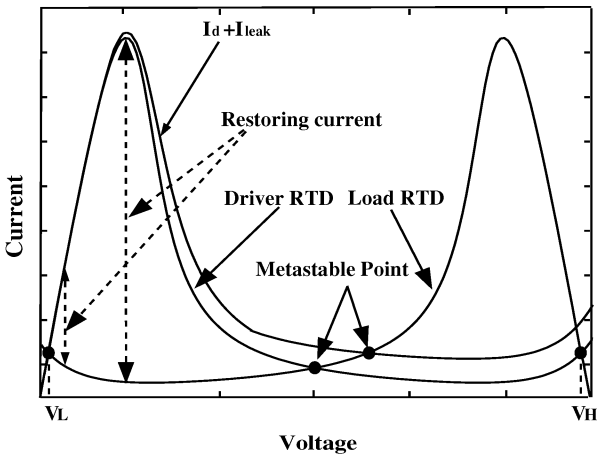

Fig. 3. Bistable property of an RTD pair.

bipolar junction transistors (BJTs) consisting of linear and saturated regions, the RTD has three distinct regions: two positive differential resistance (PDR) regions interspersed by a negative differential resistance (NDR) region. This nonlinear characteristic renders the RTD into a very promising device for a wide class of circuit applications, as described in [4], namely, multivalued logic, nanopipelined high-speed circuits, radiation-hardened reliable circuits, and circuits with low power-delay products. Two figures-of-merit commonly used for characterizing the RTD are the peak-to-valley current ratio (PVCR) and the speed index that is defined as a ratio of the device current and the device intrinsic capacitance.

Two series connected RTDs have the self-latching or bistable property, as shown in Fig. 3. The RTD pair can latch at either V_H or V_L, corresponding to logic "1" or logic "0," respectively. This bistable property of the RTD pair in the TRAM can be exploited to improve the soft error immunity, standby power consumption, and speed of memories. From a circuit design point-of-view, however, a detailed analytical study of the impact of augmentation of a conventional DRAM cell by an RTD pair is necessary.

In this paper, a thorough analysis of speed, SER, and power consumption in a TRAM cell is presented. The organization of this paper is as follows. In Section II, an analytical study of READ and WRITE speeds are given and the formulas are validated by HSPICE simulation. In Section III, the analytical model of the critical charge, usually used as one of the most important parameters in SER analysis, is derived. A comparison between the critical charge of TRAM and that DRAM is also presented. Finally, the power consumption of TRAM is analyzed in Section IV.

II. READ AND WRITE OPERATIONS ANALYSIS

In conventional DRAM, since charge sharing occurs between the storage capacitor of a DRAM cell (C_0) and the bit-line capacitor $(C_{\rm bit})$, the READ operation is destructive due to loss of cell charge during the READ operation. Therefore, a refreshing operation is needed to restore the logic value of the DRAM cell. Besides, the operational speed of the cell is also lowered due to the rapidly decreasing voltage between the drain and source of the access transistor. However, in the case of TRAM, these two problems can be completely solved under certain circumstances. As shown in Fig. 3, the restoring current is the current difference between the load RTD and driver RTD. The RTD pair indeed helps the storage node hold on to the stable point, and simultaneously helps drive the bit-line capacitance. For example, during the READ "0" operation, the current of the driver RTD is larger than that of the load RTD, the restoring current thus helps discharge $C_{\rm bit}$ and latch the storage node at V_L. The same advantage in TRAM is also preserved for the READ "1" operation. Therefore, the READ access time in TRAM is potentially shorter than that of the conventional DRAM. Also, if the bit-line precharge voltage is set properly, the refreshing operation will be eliminated, which will be discussed in more detail in Section II-A. For a WRITE operation, however, the restoring current plays two critical roles. Initially, it opposes the transition between V_L and V_H. However, once the storage voltage reaches the metastable point, as shown in Fig. 3, the restoring current begins to help the switch over. The advantage of TRAM, for the WRITE operation, is that the storage node only needs to be driven to the metastable point. After that, the RTD pair will self-latch to the stable logic value even after the access transistor turns off. Therefore, the RTD pair should be sized carefully to allow the storage node being driven to the metastable point in order to obtain a fast WRITE operation. Here, we first analytically study the READ and WRITE operations. The results are then validated with HSPICE and compared with that of conventional DRAMs.

A. Analytical Study

It may be observed that, in the standby mode, the TRAM is stable either at V_L or V_H. These stable values are not exactly V_{SS} or V_{DD} and are determined by the *I–V* characteristic of the RTD pair. Assuming both the RTDs have identical *I–V* characteristics, for simplicity and accuracy, we use the modified piecewise linear model [5] for the RTD pair given as follows:

$$I=\begin{cases}\dfrac{1}{R_1}\cdot V, & 0\le V<V_p \quad \text{(PDRI)}\\ I_p+\dfrac{1}{R_n}\cdot(V-V_p), & V_p\le V<V_{v1} \quad \text{(NDR)}\\ I_{v1}+\dfrac{1}{R_v}\cdot(V-V_{v1}), & V_{v1}\le V<V_{v2} \quad \text{(WVR)}\\ I_q+\dfrac{1}{R_2}\cdot(V-V_{DD}), & V_{v2}\le V\le V_{DD} \quad \text{(PDRII)}\end{cases} \tag{1}$$

where

$$R_1 = V_p/I_p$$
$$R_n = (V_p - V_{v1})/(I_p - I_{v1})$$
$$R_v = (V_{v2} - V_{v1})/(I_{v2} - I_{v1})$$
$$R_2 = (V_{DD} - V_{v2})/(I_q - I_{v2})$$

where I_p and V_p represent the peak current and peak voltage, respectively. I_{v1}, V_{v1}, I_{v2}, and V_{v2} are valley current and corresponding valley voltage, respectively. I_q is used to model the second peak current at $V = V_{DD}$. R_1 is the resistance of the positive differential resistance I (PDRI) region. R_n is the resistance of the NDR region. R_v is the resistance of the wide valley region (WVR), and R_2 is the resistance of the positive differential resistance II (PDRII) region. To simplify the complex expression of the equations, we also define

$$R_{12} = R_1R_2/(R_1 + R_2)$$
$$R_{1v} = R_1R_v/(R_1 + R_v)$$
$$R_{1n} = R_1R_n/(R_1 + R_n).$$

Let x denote the storage voltage of the TRAM and x_0, x_1 represent the stored logic value "0" and "1," respectively. When the TRAM is stable at "0," the driver RTD operates in the PDRI region and the load RTD operates in the PDRII region. When the TRAM is stable at "1," the driver RTD operates in the PDRII region and the load RTD operates in the PDRI region. To balance the performance of READ "0" operation and READ "1" operation, we choose the two RTD sizes to be equal. We use κ to denote the size of the RTDs in the following analysis. At a stable point, there is $I_d = I_l$, where I_d and I_l represent the currents of the driver RTD and load RTD, respectively. From (1), the stored logic value x_0 and x_1 are derived as

$$x_0 = I_q \cdot R_{12} \tag{2}$$
$$x_1 = V_{DD} - I_q \cdot R_{12}. \tag{3}$$

Equations (2) and (3) indicate that, in TRAM, x_0 and x_1 are not exactly V_{SS} and V_{DD}, and they are determined by the RTD's characteristic.

1) Analysis of the READ Operation: We have mentioned that a successful READ of a DRAM cell will lose part of the stored charge and, thus, data retention is needed to restore the logic value. However, in TRAM, the READ operation is destructive only when the metastable point is reached. In our case, since the two RTDs are identical, the metastable voltage is $V_{DD}/2$. That means the voltage swing of the storage node should be larger than $V_{DD}/2 - x_0$ for a destructive READ "0" operation and should be larger than $x_1 - V_{DD}/2$ for a destructive READ "1" operation. The precharged bit-line voltage plays an important role in determining whether the READ operation in TRAM is destructive or not. If the bit line is precharged to $V_{DD}/2$ during a READ operation, the storage node voltage swing is always smaller than the required voltage to result a destructive READ operation. However, if the bit line is precharged to a value other than $V_{DD}/2$, a destructive READ "0" or a destructive READ "1" may occur depending on the strength of the RTD pair. The speed of the TRAM is also strongly dependent on the strength of the RTD pair. If the RTD pair is too weak, the storage node can be charged/discharged to the voltage level very close to the metastable point and the restoring current in this scenario is very small, as shown in Fig. 3. The self-restoration of a TRAM cell logic value will take longer time. Therefore, to guarantee a nondestructive READ, as well as to obtain a fast access speed, κ should satisfy $|I_{sr}| > \kappa \cdot (I_p - I_{(V_{DD}-V_p)})$, where I_{sr} is the read access current. κ has a minimum value $\kappa_{\min}$

$$\kappa_{\min} = \frac{|I_{sr}|}{I_p - I_{(V_{DD}-V_p)}}. \tag{4}$$

In READ "0" operation, the TRAM latches at $V_L = x_0$. The driver RTD operates in the PDRI, NDR, or WVR regions and the load RTD operates in the WVR or PDRII regions depending on the strength of the RTD pair. Since the operation region for the access transistor is small, we can use linear model $I_{sr} = A + B \cdot (V_{\text{bit}} - x)$ to model the access transistor current. Let the charge (discharge) current of the storage node be I_c. I_c has the following relation with the storage node voltage x:

$$I_c = C_0 \cdot \frac{dx}{dt}. \tag{5}$$

By using Kirchoff's Current Law (KCL)

$$I_c = I_{sr} + \kappa \cdot (I_l - I_d) \tag{6}$$

where I_d and I_l are given by (1). We obtain the storage node voltage waveform expression for READ "0" operation as follows:

$$x = \frac{A^*}{B^*} + \left(x_0 - \frac{A^*}{B^*}\right) \cdot e^{-\lambda_r t} \tag{7}$$

where $\lambda_r = B^*/C_0$. For different regions, A^* and B^* are derived as

$$A^* = A + \kappa \cdot I_q + B \cdot V_{\text{bit0}}$$
$$B^* = B + \frac{\kappa}{R_{12}}$$
$$(0 \le x < V_{DD} - V_{v2})$$

$$A^* = A + \kappa \cdot \left(I_{v1} + \frac{V_{DD} - V_{v1}}{R_v}\right) + B \cdot V_{\text{bit0}}$$
$$B^* = B + \frac{\kappa}{R_{1v}}$$
$$(V_{DD} - V_{v2} \le x < V_p)$$

$$A^* = A + \kappa \cdot \left(I_{v1} - I_p + \frac{V_p}{R_n} + \frac{V_{DD} - V_{v1}}{R_v}\right) + B \cdot V_{\text{bit0}}$$
$$B^* = B + \frac{\kappa}{R_{nv}}$$
$$(V_p \le x < V_{v1})$$

$$A^* = A + \kappa \cdot \frac{V_{DD}}{R_v} + B \cdot V_{\text{bit0}}$$
$$B^* = B + 2\frac{\kappa}{R_v}$$
$$(V_{v1} \le x < V_{DD}/2). \tag{8}$$

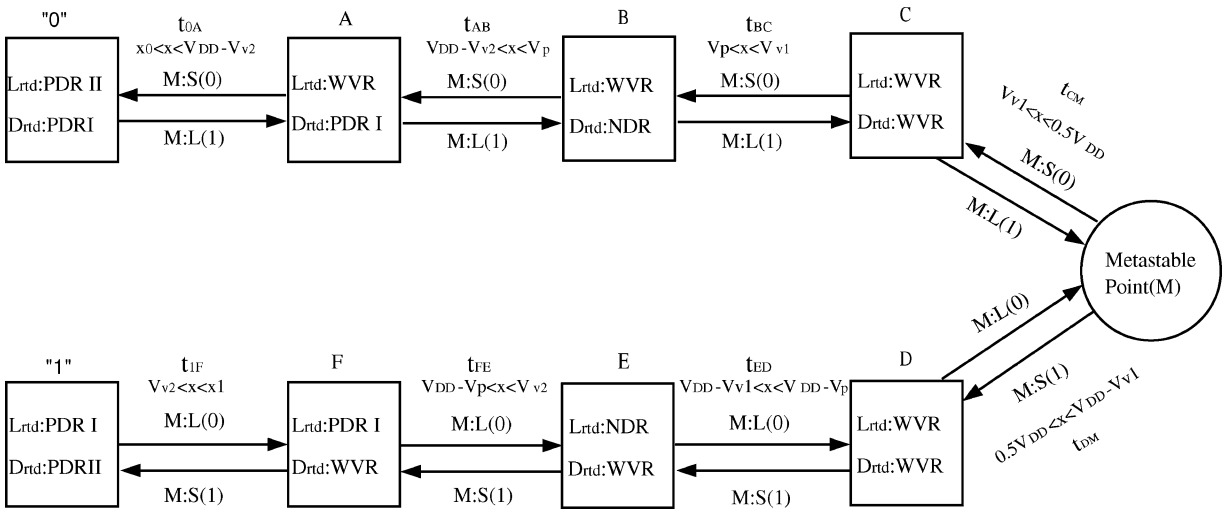

Fig. 4. TRAM WRITE operation microstate diagram. $L_{\rm rtd}$ and $D_{\rm rtd}$ represent the load RTD and driver RTD, respectively. $M:S(1), M:S(0), M:L(1)$, and $M:L(0)$ represent the saturation (S) and linear (L) operation region of the access transistor. (1) denotes WRITE "1" operation and (0) denotes WRITE "0" operation.

Bit-line voltage swing satisfies

$$C_{\rm bit}\frac{dV_{\rm bit}}{dt} = I_{sr} \tag{9}$$

and the bit-line waveform can be solved as

$$\Delta V_{\rm bit}(t) = a_1 e^{-\lambda_1 t} + a_2 e^{-\lambda_2 t} + d \tag{10}$$

where

$$\lambda_1 = \frac{-B}{C_{\rm bit}} \quad \lambda_2 = \lambda_r = \frac{B^*}{C_0} \quad d = \frac{A^*B - AB^*}{BB^*}. \tag{11}$$

The parameters a_1 and a_2 can be calculated from the initial conditions

$$a_1 = V_{\rm bit0} - d - a_2 \tag{12}$$

$$a_2 = -\frac{A/B + d - x_0}{1 + \dfrac{B^* C_{\rm bit}}{BC_0}} \tag{13}$$

where $V_{\rm bit0}$ is the precharged bit-line voltage.

Similarly, we can obtain the bit-line waveform for READ "1" operation, which is identical to that for READ "0" operation, except for the values of parameters A^* and B^*, which are

$$A^* = \kappa \cdot \left(\frac{V_{DD}}{R_{12}} - I_q\right) - B \cdot V_{\rm bit0} - A$$
$$B^* = \frac{\kappa}{R_{12}} - B$$
$$(V_{v2} \le x < V_{DD})$$

$$A^* = \kappa \cdot \left(\frac{V_{DD}}{R_1} - I_{v1} + \frac{V_{v1}}{R_v}\right) - B \cdot V_{\rm bit0} - A$$
$$B^* = \frac{\kappa}{R_{1v}} - B$$
$$(V_{DD} - V_p \le x < V_{v2})$$

$$A^* = \kappa \cdot \left(I_p - I_{v1} + \frac{V_{DD} - V_p}{R_n} + \frac{V_{v1}}{R_v}\right) - B \cdot V_{\rm bit0} - A$$
$$B^* = \frac{\kappa}{R_{nv}} - B$$
$$(V_{DD} - V_{v1} \le x < V_{DD} - V_p)$$

$$A^* = \kappa \cdot \frac{V_{DD}}{R_v} - B \cdot V_{\rm bit0} - A$$
$$B^* = 2\frac{\kappa}{R_v} - B.$$
$$(V_{DD}/2 \le x < V_{DD} - V_{v1}). \tag{14}$$

2) Analysis of the WRITE Operation: The phase change of a WRITE operation is shown in Fig. 4. Since the restoring current of the RTD pair is against the state transition at first and then it helps to flip the state, the WRITE operation is only successful when $|I_{sw}| > \kappa(I_p - I_{(V_{DD}-V_p)})$, where I_{sw} is the access transistor current for WRITE operation. Therefore, κ should be smaller than $\kappa_{\max}$

$$\kappa_{\max} = \frac{|I_{sw}|}{I_p - I_{(V_{DD}-V_p)}}. \tag{15}$$

For WRITE "1" operation, the WRITE access time is the transition time from state "0" to the metastable point, as shown in the microstate diagram. In the first phase, i.e., from state "0" to state "A," the drive RTD operates in the PDRI region and the load RTD operates in the PDRII region

$$I_c = I_{sw} + \kappa \cdot (I_l - I_d) \tag{16}$$

where $I_l = I_q - x/R_2$ and $I_d = x/R_1$. By using a linear access transistor current model

$$I_{sw} = A + B \cdot (V_{\rm bit} - x). \tag{17}$$

TABLE I
PARAMETERS FOR WRITE "1" OPERATION

	State Transition			
	'0'→'A'	'A'→'B'	'B'→'C'	'C'→ 'M'
a^*	$A+\kappa I_q$ $+BV_{bit0}$	$A+\kappa I_{v1}+BV_{bit0}$ $+\kappa(\frac{V_{DD}-V_{v1}}{R_v})$	$A+BV_{bit0}+\kappa(I_{v1}-I_p)$ $+\kappa(\frac{V_p}{R_n}+\frac{V_{DD}-V_{v1}}{R_v})$	$A+BV_{bit0}+\frac{\kappa V_{DD}}{R_v}$
b^*	$B+\frac{\kappa}{R_{12}}$	$B+\frac{\kappa}{R_1 v}$	$B+\frac{\kappa}{R_n v}$	$B+\frac{2\kappa}{R_v}$

The WRITE access time t_{0A} for this phase has the following expression:

$$t_{0A}=\frac{1}{\lambda_w}\ln\frac{a^*-b^*x_{t0}}{a^*-b^*x}+t_0 \tag{18}$$

where $\lambda_w = b^*/C_0$. a^* and b^* are determined by A, B, and RTD electrical parameters. Similarly, we get the expression of t_{AB}, t_{BC}, and t_{CM}, which are identical to t_{0A}, except for different a^* and b^* values. Therefore, the WRITE "1" access time is obtained as

$$T_{w1}=t_{0A}+t_{AB}+t_{BC}+t_{CM}. \tag{19}$$

For WRITE "0" operation, the access time is the transition time from state "1" to the metastable point, as shown in Fig. 4. By using a similar analysis procedure, WRITE "0" access time is derived as

$$T_{w0}=t_{1F}+t_{FE}+t_{ED}+t_{DM} \tag{20}$$

where t_{1F}, t_{FE}, t_{ED}, and t_{DM} have an identical expression as t_{0A} with different a^* and b^*. The parameters a^* and b^* for a different time region are listed in Tables I and II.

B. Equation Validation and Performance Comparison With Conventional DRAM

Fig. 5 shows the bit-line waveform of the READ operation for TRAM and DRAM. For TRAM, the bit-line waveform is obtained from both the derived equation and HSPICE simulation. We have used the physical RTD model [12] implemented by using a voltage controlled current source (VCCS) in HSPICE to process the validation. The simulation environment was set to $V_{DD}=1.6$ V, $C_0=30$ fF, and $C_{\rm bit}=180$ fF, and the access transistor was set to a minimum feature size. Bit-line voltage was precharged to $(V_{DD}-V_{\rm th})/2$. Under this condition, the TRAM READ "0" operation is always nondestructive. However, this desirable property does not hold for the READ "1" operation. A minimum size of the RTD pair $\kappa_{\rm min}$ should be satisfied to obtain a nondestructive READ "1." Experimental and validation results for TRAM READ "0" operation are shown in Fig. 5(a) and an experimental study for DRAM was also done to make the performance comparison. As is shown, for a small $\kappa=0.1$, the performance of TRAM is comparable to that of DRAM. However, since the restoration of TRAM, under this scenario, may be slower than the refreshing operation of a DRAM cell due to the small retention current, TRAM lost its advantage in improving the access speed. As we have analyzed, a larger κ value will result in a larger retention current, which helps a faster TRAM READ "0" operation. Fig. 5(a) also shows that for READ "0," the bit-line swing of DRAM is faster than that of TRAM initially. This is because the initial stored voltage of DRAM is V_{SS}, which is stronger than that of $\mathrm{TRAM}(x_0)$, resulting in a faster bit-line voltage drop. For READ "1" operation, we obtain the $\kappa_{\rm min}=0.4$ for the RTD pair to guarantee a nondestructive READ. As shown in Fig. 5(b), we only chose one κ value to compare with conventional DRAM because the variation of the κ value does not affect the speed too much as long as κ is greater than $\kappa_{\rm min}$. This fact is determined by the property of the access transistor. Since the body effect in READ "1" operation limits the variation of the access current I_{sr}, changing the size of the RTD pair will not have much effect on bit-line voltage swing variation. Since I_{sr} is the perturbation to latched state, small I_{sr} also leads to a fact that the two RTDs always work in certain regions for READ "1" operation even if we increase the κ value. Fig. 5(b) also shows that a weak "1" $(V_{DD}-V_{\rm th})$ is stored by a DRAM cell due to a threshold voltage drop across the access transistor. This problem can be solved in the TRAM. Since the RTD pair can self-latch at x_1, a strong "1" can be obtained by properly designing the RTD *I–V* characteristic. In this case, the TRAM bit-line voltage drop is always faster than that of the DRAM. By choosing $\kappa=0.5$ for both READ "0" operation and READ "1" operation, the speed improvement compared with DRAM is 62.2% and 49.6%, assuming a bit-line voltage swing of 70 mV. Fig. 5 also shows that $\Delta V_{\rm bit}$ of the TRAM keeps increasing when $\Delta V_{\rm bit}$ of the DRAM saturates. For a sense amplifier design that may have larger sensing voltage, but smaller propagation delay, the performance of the TRAM is much better than that of the DRAM. For example, for READ "0" operation, if $\Delta V_{\rm bit}=70$ mV, the DRAM delay is 250 ps, while the TRAM delay is 120 ps, which is approximately 52% faster. For a sense amplifier design that requires small sensing voltage, the performance of the DRAM and that of the TRAM are likely to be comparable. However, higher sensitivity of the sense amplifier often increases the circuit complexity and leads to the increase of the circuit propagation delay. Therefore, the TRAM does not require stringent sensitivity of the sense amplifier and can afford to work correctly with a simple sense amplifier. From Fig. 5, we can also see that the derived result matches with the result of HSPICE simulation very well.

Fig. 6 shows the storage node waveform from the stable point to the metastable point for a WRITE operation. As we have analyzed, when the storage node voltage reaches the metastable point, the RTD pair will flip to another state as long as there is a small positive disturbance (in our case, the small disturbance is the access transistor current). As we can see, the WRITE access time increases with the increase of the κ value. As indicated in Fig. 6(a), $\kappa_{\rm max}$ for a successful TRAM WRITE "0" operation is 1.0, and DRAM has a much faster initial WRITE. This phenomenon happens because of the following reasons. First, the RTD pair initially prevents the state transition, which slows down the operational speed; second, the initial voltage in DRAM is a weak "1" due to threshold voltage drop, whereas it is a strong "1" in TRAM. Given the RTD size to be $\kappa_{\rm max}$, which is the worst case scenario, we measured the WRITE "0" access time for both TRAM and DRAM. Even in this worst case, TRAM has a better WRITE performance. The speed improvement of the TRAM is 9.38% compared with that of the DRAM. For WRITE "1" operation, due to the body effect, the access transistor current is much smaller than

TABLE II
PARAMETERS FOR WRITE "0" OPERATION

	State Transition			
	'1'→ 'F'	'F'→'E'	'E'→'D'	'D'→'M'
a^*	$A-\kappa I_q+BV_{bit0}+\kappa\frac{V_{DD}}{R_{12}}$	$A-\kappa I_{v1}+BV_{bit0}+\kappa(\frac{V_{DD}}{R_1}+\frac{V_{v1}}{R_v})$	$A+\kappa(I_p-I_{v1})+BV_{bit0}+\kappa(\frac{V_{DD}-V_p}{R_n}+\frac{V_{v1}}{R_v})$	$A+BV_{bit0}+\kappa\frac{V_{DD}}{R_v}$
b^*	$B+\frac{\kappa}{R_{12}}$	$B+\frac{\kappa}{R_{1v}}$	$B+\frac{\kappa}{R_{nv}}$	$B+\frac{2\kappa}{R_v}$

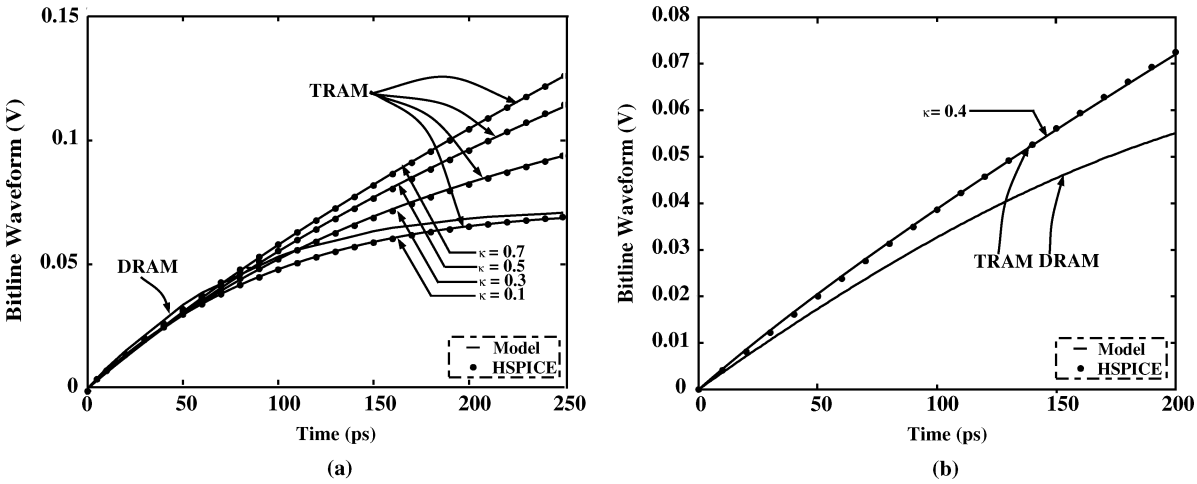

Fig. 5. Bit-line waveforms during READ operations. (a) Read "0" operation. (b) Read "1" operation.

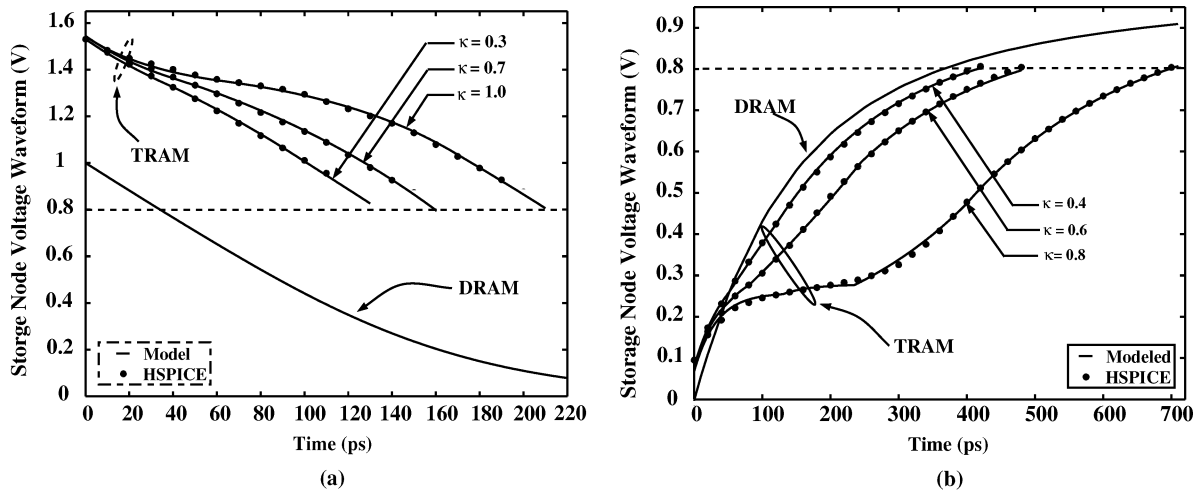

Fig. 6. Storage node waveforms during WRITE operation (a) Write "0" operation. (b) Write "1" operation.

WRITE "0," which results in a smaller $\kappa_{\max}$ of 0.8, as shown in Fig. 6(b). The speed improvement of the TRAM at $\kappa_{\max}$ is 35.9%, which is larger than WRITE "0" operation because both DRAM and TRAM store a strong "1" at the beginning of WRITE operation. Fig. 6 also shows that the derived WRITE results agree with experimental results very well.

III. ANALYSIS OF CRITICAL CHARGE FOR TRAM

Soft error is becoming a critical circuit reliability issue for very deep submicrometer very large scale integration (VLSI) technology applying device and interconnect shrinking methods. Recent studies [6], [7] have addressed the effect of technology scaling on soft errors. Soft error occurs in both terrestrial and space radiation environment. In the terrestrial environment, alpha particles are the leading cause of soft errors. Alpha particles are produced from the radioactive decay of impurities in the metal, passive layer, and the surrounding package materials in memories. When alpha particles penetrate the device, electron–hole pairs are generated along the track of the particles. These generated carriers are then collected due to various charge collection mechanisms, such as drifting, diffusion, and funneling [8]. Once the amount of the collected charge at the sensitive node of the memory cell is larger than a critical charge, it results in logic errors, such as flip of bits in SRAM and false READ in DRAM. Therefore, the critical charge is one of the most important parameters for estimating the SER in memories. Here, we analytically study the critical charge of TRAM and compare it with conventional DRAM technology.

Soft error can occur at both READ operation mode and standby mode. For DRAM, the worst case occurs at standby mode. Soft error occurs only when the logic "1" is stored.

The charge sharing between the bit-line capacitor and storage capacitor leads to the following equation [9]:

$$(C_{\rm bit}+C_0)\cdot V'_{\rm bit}=C_{\rm bit}\cdot V_{\rm bit}+C_0\cdot V_s-Q_M \tag{21}$$

where $V'_{\rm bit}$ is the bit-line voltage after charge sharing. V_s is the original storage node voltage. Q_M is the collected charge in the storage node due to injection of the external particles. Therefore, the bit-line voltage swing can be calculated as

$$\Delta V_{\rm bit}=V'_{\rm bit}-V_{\rm bit}=\frac{1}{2}\cdot\frac{C_0}{C_{\rm bit}+C_0}V_s-\frac{Q_M}{C_{\rm bit}+C_0}. \tag{22}$$

If the collected charge Q_M is less than the critical charge Q_c, the bit-line voltage swing $\Delta V_{\rm bit}$ will be less than $\Delta V_{\rm sen}$, the minimum voltage swing that the sense amplifier can detect. By replacing Q_M by Q_c and $\Delta V_{\rm bit}$ by $\Delta V_{\rm sen}$, we have

$$Q_c=\frac{1}{2}C_0V_s-(C_{\rm bit}+C_s)\cdot\Delta V_{\rm sen}. \tag{23}$$

For TRAM, soft error also occurs in both the standby mode and READ operation mode. The stored state flips when the metastable point is reached. Let x_m represent the metastable point voltage. At the standby mode, the critical charge values for logic "0" and logic "1" are

$$Q_{sc0}=C_0\cdot(x_m-x_0) \tag{24}$$
$$Q_{sc1}=C_0\cdot(x_1-x_m) \tag{25}$$

respectively. Assuming the two RTDs are identical, x_m is $V_{DD}/2$. Q_{sc0} and Q_{sc1} are calculated to have the same value

$$Q_{sc0}=Q_{sc1}=C_0\cdot\left(\frac{1}{2}V_{DD}-I_qR_{12}\right). \tag{26}$$

The worst case for TRAM occurs at the READ operation mode instead of the standby mode. The reason is that the storage node voltage will deviate from its nominal value due to charging/discharging of the storage capacitance through the access transistor. The largest voltage deviation occurs when $I_c=0$. Therefore, the storage voltage x satisfies $I_{sr}+\kappa(I_l-I_d)=0$. For the READ "1" operation, the critical charge Q_{r1} is obtained as

$$Q_{r1}=Q_{sc1}-C_0\cdot(x_1-x). \tag{27}$$

When the RTD pair is strong, the driver RTD operates in the PDRII or WVR region and the load RTD operates in the PDRI region. When the RTD pair is weak, the driver RTD operates in the WVR region and the load RTD may work in the NDR or WVR region. The storage node voltage is

$$x=\begin{cases}\dfrac{\kappa\cdot\left(\dfrac{V_{DD}}{R_{12}}-I_q\right)-A-B\cdot V_b}{\dfrac{\kappa}{R_{12}}-B}, & V_{v2}\le x<x_1\\[2ex] \dfrac{\kappa\cdot\left(\dfrac{V_{DD}}{R_1}+\dfrac{V_{v1}}{R_v}-I_{v1}\right)-A-B\cdot V_b}{\dfrac{\kappa}{R_{1v}}-B}, & V_{DD}-V_p\le x<V_{v2}\\[2ex] \dfrac{\kappa\cdot\left(I_p-I_{v1}+\dfrac{V_{DD}-V_p}{R_n}+\dfrac{V_{v1}}{R_v}\right)-A-B\cdot V_b}{\dfrac{\kappa}{R_{nv}}-B}, & V_{DD}-V_{v1}\le x<V_{DD}-V_p\\[2ex] \dfrac{\kappa\cdot\dfrac{V_{DD}}{R_v}-A-B\cdot V_b}{\dfrac{2\kappa}{R_v}-B}, & V_{DD}/2\le x<V_{DD}-V_{v1}.\end{cases} \tag{28}$$

For the READ "0" operation, the critical charge Q_{r0} can be similarly derived as

$$Q_{r0}=Q_{sc1}-C_0\cdot(x-x_0) \tag{29}$$

where

$$x=\begin{cases}\dfrac{\kappa\cdot I_q+A+B\cdot V_b}{\dfrac{\kappa}{R_{12}}+B}, & x_0\le x<V_{DD}-V_{v2}\\[2ex] \dfrac{\kappa\cdot\left(I_{v1}+\dfrac{V_{DD}-V_{v1}}{R_v}+\dfrac{V_p}{R_n}\right)+A+B\cdot V_b}{\dfrac{\kappa}{R_{1v}}+B}, & V_{DD}-V_{v2}\le x<V_p\\[2ex] \dfrac{\kappa\cdot\left(I_{v1}-I_p+\dfrac{V_{DD}-V_{v1}}{R_v}\right)+A+B\cdot V_b}{\dfrac{\kappa}{R_{nv}}+B}, & V_p\le x<V_{v1}\\[2ex] \dfrac{\kappa\cdot\dfrac{V_{DD}}{R_v}+A+B\cdot V_b}{\dfrac{2\kappa}{R_v}+B}, & V_{v1}\le x<V_{DD}/2.\end{cases} \tag{30}$$

In DRAM design, the access transistor is usually minimal-sized nMOS transistor in order to obtain high density. At a given supply voltage, the critical charge is determined by the electrical characteristic of the RTD device and the RTD sizing parameter κ, as shown in (26), (27), and (29). The relation between $Q_{r0}(Q_{r1})$ and κ is shown in Fig. 7 for both nondestructive READ "0" operation and nondestructive READ "1" operation. For READ "0," the critical charge is initially of small value when κ is small. With the increase of κ, the critical charge then jumps to large values and becomes saturated. The reason for this phenomenon is that, in the READ mode, the storage node has a larger voltage swing with small κ values and the maximum voltage swing occurs when the storage node is charged to a voltage level close to

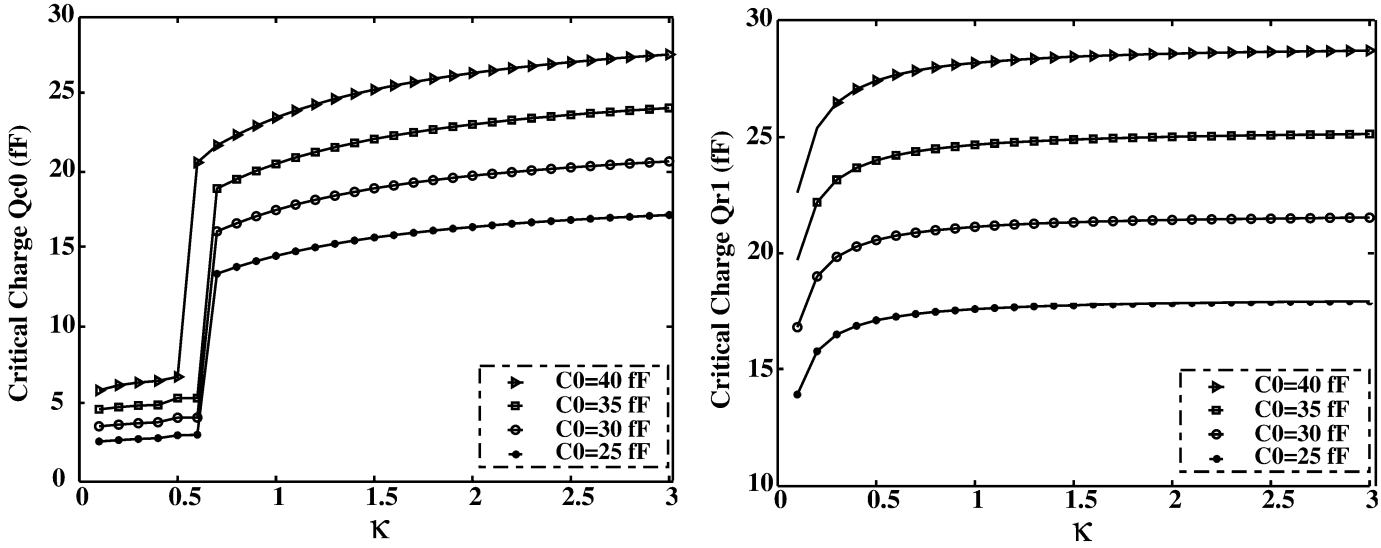

Fig. 7. Critical charge of READ operation with respect to κ. (*left*) READ "0" operation. (*right*) READ "1" operation.

TABLE III
CRITICAL CHARGE COMPARISON OF TRAM AND CONVENTIONAL DRAM.

	DRAM Q_C (fC)									TRAM Q_C (fC)						
$C_{bit}(fF)$	150			200			250			Q_{r1} (fC)			Q_{r0} (fC)			Q_{sc}
C_0	$\Delta V_{sen}(mV)$			$\Delta V_{sen}(mV)$			$\Delta V_{sen}(mV)$			$\Delta V_{sen}(mV)$			ΔV_{sen} (mV)			(fC)
(fF)	50	60	70	50	60	70	50	60	70	50	60	70	50	60	70	
25	11.3	9.5	7.8	8.8	6.5	4.3	6.3	3.5	0.8	17.1	17.0	17.0	14.4	14.4	14.5	17.8
30	15.0	13.2	11.4	12.5	10.2	7.9	10.0	7.2	4.4	20.5	20.5	20.4	17.2	17.3	17.3	21.4
35	18.8	16.9	15.1	16.3	13.9	11.6	13.8	10.9	8.1	24.0	23.9	23.8	20.1	20.1	20.2	24.9
40	22.5	20.6	18.7	20.0	17.6	15.2	17.5	14.6	11.7	27.4	27.3	27.2	22.9	23.0	23.1	28.5

the metastable point. Therefore, the critical charge at this scenario is very small. With the increase of the κ value, the RTD pair helps to suppress the storage node voltage swing. The maximum voltage variation occurs at the voltage level close to the nominal value x_0, resulting in a larger critical charge value. For READ "1" operation, since the access current is small due to body effect, the maximum storage node voltage swing always occurs at the point near the nominal voltage x_1. Therefore, the critical charge for READ "1" operation does not change much with the increase of the κ value and always keeps a relatively large value. In order to get large critical charge for both READ "1" and READ "0" operations with small area penalty, κ should be chosen properly. Table III shows the critical charge comparison between TRAM and DRAM. In the comparison, we choose $V_{DD} = 1.6$ V and $\kappa = 0.7$. Parameters A and B are extracted from a 0.18-μ CMOS technology by means of curve fitting of the *I–V* characteristic generated by the HSPICE level-49 model. The result shows that, even in the worst case, which is READ operation mode, TRAM still has larger critical charge than conventional DRAM.

IV. POWER CONSUMPTION ANALYSIS

TRAMs potentially have lower power consumption than conventional DRAMs because of the following reasons. First of all, the bistable property eliminates the requirement of refreshing operation. The storage node always latches at logic "0" or logic "1" by self-restoration and leakage currents are replenished by restoring current of the RTD pair. Second, in DRAM, due to the leakage current variation of the cell, the worst case leakage current has to be accounted for at each cell when performing the refreshing of cells. However, the ratio of the worst case cell leakage current to the average leakage current can be as high as 50 [10], meaning that, on average, power consumption for the refreshing operation is much more than what is actually required. In case of TRAM, the restoring current of the RTD pair is always equal to the actual leakage current of each single cell, as shown in Fig. 3. Therefore, the power consumption is reduced further. Here, we derive the analytical model for power consumption of TRAMs and then compare it with that of conventional DRAMs.

Static power consumption in a TRAM cell is determined by the leakage current of the cell and the direct current through the RTD pair [11]. Assuming the average leakage current of a cell is I_{leak}, in order to guarantee bi-stability of a TRAM cell, the following condition should be satisfied:

$$I_P > I_{\text{leak}} + I_v. \tag{31}$$

Let δ be the ratio of the maximum leakage current $I_{\text{leak}}^{\max}$ and the average leakage current I_{leak} in a DRAM chip. As (28) must satisfy for all cells, the valley current I_v should be larger than a minimum valley current $I_v^{\min}$, which is given by

$$I_v^{\min} = \delta \cdot \frac{I_{\text{leak}}}{\text{PVCR} - 1}. \tag{32}$$

Therefore, for the worst case that the maximum leakage current is assumed for all the cells, the standby power is obtained as

$$P_{\mathrm{TRAM}} = I_{\mathrm{leak}} V_{DD} \cdot \left(1 + \frac{\delta}{\mathrm{PVCR} - 1}\right). \tag{33}$$

Due to the dynamic compensation of the leakage current, the standby power is then given by

$$P_{\mathrm{TRAM}}^{\mathrm{Avg}} = I_{\mathrm{leak}} V_{DD} \cdot \left(\frac{1}{\delta} + \frac{1}{\mathrm{PVCR} - 1}\right). \tag{34}$$

As described earlier, the most significant improvement of the TRAM is its low power consumption in comparison with the conventional one-transistor (1T) DRAM cell, which requires refreshing periodically. The power consumption of the DRAM due to the refresh operation is given by [11]

$$P_{\mathrm{DRAM}} = \delta I_{\mathrm{leak}} V_{DD} \cdot \left(1 + \frac{C_{\mathrm{bit}}}{C_0}\right) \cdot \frac{1}{1 - \dfrac{C_{\mathrm{bit}}}{C_0} \dfrac{1}{\dfrac{V_{DD}}{2V_r} - 1}} \tag{35}$$

where V_r is the minimum voltage a sense amplifier can detect. Therefore, the power consumption of TRAM versus that of DRAM is derived as

$$\eta = \frac{P_{\mathrm{TRAM}}^{\mathrm{Avg}}}{P_{\mathrm{DRAM}}} = \frac{\left(\dfrac{1}{\delta} + \dfrac{1}{\mathrm{PVCR} - 1}\right)}{\delta \cdot \left(1 + \dfrac{C_{\mathrm{bit}}}{C_0}\right) \cdot \dfrac{1}{1 - \dfrac{C_{\mathrm{bit}}}{C_0} \dfrac{2V_r}{V_{DD} - 2V_r}}}. \tag{36}$$

For an ideal sense amplifier with $V_r = 0$, by choosing $\delta = 50, \mathrm{PVCR} = 10, C_{\mathrm{bit}}/C_0 = 10$, we obtain the power consumption ratio $\eta \simeq 10^{-2}$. This means that the TRAM standby power consumption can be two orders of magnitude less than that of DRAM. With increase of the DRAM density, C_{bit}/C_0 becomes larger, and the power consumption ratio η still tends to decrease.

V. Conclusion

In this paper, we have analytically modeled the READ and WRITE operations, critical charge for soft errors, and power consumption of single-transistor TRAM. The results are validated by HSPICE simulation. In READ and WRITE operations, the size ratio of the RTD pair to the access transistor (κ) plays an important role in determining the memory access speed. Experimental results show that suitable κ will give a greater flexibility in sense amplifier design. From the soft-error point-of-view, analytical results show that the critical charge of TRAM is not as sensitive to ΔV_{sen}, as in DRAM, due to its self-latching property. The relationship between Q_c and κ shows that Q_c is saturated with an increase of κ. The analytical study of power consumption shows that the dynamic compensation to the leakage current by the restoring current of the RTD pair will reduce the power consumption by one or two orders of magnitude. Considering the area penalty, κ should not be chosen large because the access time and critical charge of TRAM do not improve much further with larger κ value, and the power consumption increases due to the larger standby dc current. In a nutshell, TRAM indeed has a promising potential in future high-density, low-power, fast, and highly reliable memory design. This paper has analytically established the above claim through in-depth analysis.

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