For instance, the equivalent inductor circuit for the example of Fig. 1 is shown in Fig. 5.

It should be noted that in the above equations, an "effective cross section" is used which is based on the skin depth of the signal line at the specified frequency. Skin depths for copper interconnects at a few sample frequencies are shown in Table II. When the skin depth is smaller than one of the cross section dimensions, the interconnect is considered to be a set of four separate interconnects (Fig. 4) that carry the current. In that case, separate inductive loops are considered for each one of the four interconnects.

V. Test Cases

A number of test cases that are from actual chips used to validate the extractor are examined in this section. The extracted results were compared to those obtained from the HFSS tool and are tabulated in Table III.

The results from HFSS are used as the benchmark and the percent error is defined as the difference between the results obtained from this approach (static) versus those of the HFSS.

Test cases 1 and 2 are clock trees with only interconnects between the driver and the sinks using differential clock signaling. Test cases 3–5 are clock distribution trees, which include buffers to balance the clock tree [12]. In order to preserve the signal integrity, differential clock signaling is used with ground shields on either sides of the clock signal. Percentage error for test cases 3–5 is calculated as the worst case piece-wise difference between the static results and those obtained from HFSS.

VI. Conclusion

This paper underlines the need for a more accurate interconnect extraction algorithm that models inductance as well as capacitance and resistance for VLSI circuits. The results obtained from this analysis combined with the extracted *RC*s were used to analyze propagation times. This analysis has resulted in savings of hundreds of thousands of dollars in mask-set costs that would have been required if only *RC* analysis were used.

More accurate modeling of interconnects based on the technology [13] is the next area of improvement. The proper modeling of interconnects remains as one of the most challenging areas of the VLSI design as the industry moves toward smaller devices.

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Simultaneous Switching Noise Analysis Using Application Specific Device Modeling

Li Ding and Pinaki Mazumder

***Abstract*—In this paper, we introduce an application-specific device modeling methodology to develop simple device model that accurately tracks the actual device *I–V* characteristics in relevant but bounded operating regions. We have specifically used a simple MOSFET model to precisely analyze the switching noises generated on a chip due to simultaneous driving of chip output pads by bulky buffer gates. Previous works in analytical modeling of simultaneous switching noises employed long-channel and α-power law transistor models; however, these models led to complex circuit equations that on truncation caused poor matching between manual analysis and actual simulation results. Also, in order to retain the simplicity of manual analysis, previous researchers ignored the parasitic capacitances of the bonding pads. This paper demonstrates that by using a simple application-specific transistor model, circuit equations can be solved precisely without requiring any gross approximations or model truncations, even when the inductance effects of bonding wires are simultaneously considered along with parasitic capacitances of the output pads. The analytical results derived in this paper tally with HSPICE simulation values within 3% deviations.**

***Index Terms*—Alpha-power law model, device modeling, digital system noise, noise modeling, simultaneous switching noise.**

I. Introduction

Simultaneous switching noise (SSN) [1]–[6], also referred in the literature as ΔI noise or ground bounce, primarily occurs due to very large instantaneous power supply and ground currents propagating within a chip when a large number of transistors are simultaneously switched between on and off states. The magnitude of SSN is found to be proportional to the parasitic inductor L associated with power and ground networks along with the bonding wires that connect pads to pins, and also the rate of change of the current through the inductor dI/dt. SSN noise often leads to serious degradation of signal integrity and overall performance of a chip. It generates glitches on the ground and the power-supply network, it decreases the effective driving strength of the gates, it causes output signal distortion impairing signal

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The authors are with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109 USA (e-mail: lding@eecs.umich.edu; mazum@eecs.umich.edu).

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integrity, and it reduces the overall noise margin of a system. The effect of SSN is becoming more prominent as a result of the continuous increase in both chip integration level and system operating speed. Therefore, it is extremely important to accurately model the SSN and develop SSN-aware design methodologies to ensure high performance and reliable operation of VLSI chips.

The effects of SSN are prominently noticed near the output pads of a chip owning to the following reasons. First, the output drivers are usually very large in size, drawing significant amount of instantaneous currents when they switch to change the output binary states on pads. Second, in clock synchronized chips the output drivers tend to switch simultaneously, which is especially true for output bus drivers. Third, the parasitic inductance of the bonding wire and the package is usually in the range of nano-Henries. Therefore, in this paper we will study the SSN at output pad drivers. Furthermore, we will primarily model the SSN on the ground network since the mathematical treatment can similarly be extended to the power network.

Simultaneous switching noises at chip output drivers have been studied extensively in the literature by various researchers [7]–[13]. As a result of these studies, many elegant circuit designs have been proposed for pad drivers after duly taking into account of the SSN effects [14]–[18]. Two central components in any SSN modeling include the transistor model used in circuit equations of the pad driver circuits, and the pad parasitics that significantly influence the accuracy of the resulting SSN modeling, as it has been demonstrated in this paper.

Previous attempts in SSN modeling [9]–[11] have used the α-power law model [19] for short channel devices. However, because of the use of the αth power function in the α-power law model, frequently approximation techniques have to be used to obtain the closed-form solution involving transcendental functions in the SSN models. Vemuru [9] assumed that the time derivative of the drain current was a constant for deep submicron processes. Jou *et al.* in [10] applied Taylor series expansion on the drain current and simplified the expression by truncating the second and higher order terms in the series. Song *et al.* in [11] made two assumptions in their SSN model: constant derivative of the drain current and linear time dependent SSN voltage. In this paper, we introduce an application-specific device modeling (ASDM) methodology for SSN modeling. In contrast to conventional short-channel device models like the commonly used α-power law model that attempts to track the transistor *I–V* characteristics as closely as possible over the entire domain of transistor operation, the proposed ASDM methodology tightly matches the characteristics of a MOSFET device at the transistor operating region of interest in a specific application, and hence the name ASDM. By sacrificing the flexibility of a full-scale MOSFET model, ASDM approach gives a more accurate modeling in the relevant region of MOSFET operation and leads to a simpler mathematical formulation for the pad driver circuits. Using the proposed ASDM approach, we have developed a new SSN modeling technique that does not require any series truncations and model approximations, hence improves the overall accuracy in comparison to previous methods.

For the purpose of SSN modeling at output drivers, previous models only considered the parasitic inductance of the bonding wire while the parasitic capacitance and resistance of the wires and pads were neglected. For a pin grid array (PGA) package, the values of the parasitic inductance, capacitance and resistance are typically 5 nH, 1 pF, and 1 mΩ, respectively [15]. While it is reasonable approximation to neglect the effects of the small resistance because its accompanying *IR* voltage drop is typically less than 1 mV, the effect of the package parasitic capacitance has not been quantitatively evaluated. In this paper, we derive a complete SSN model which considers both the parasitic inductance and capacitance of pads and bonding wires. We specifically show that the maximum SSN voltage can be obtained using four closed-form formulas depending on the operating modes of the system. Through HSPICE simulation, it is observed that the SSN model without the pad capacitance values is adequate when the system is in the over-damped mode. The paper also demonstrated that the proposed new SSN model including pad parasitic capacitances should be used when the system is in the under-damped mode with small number of pad drivers.

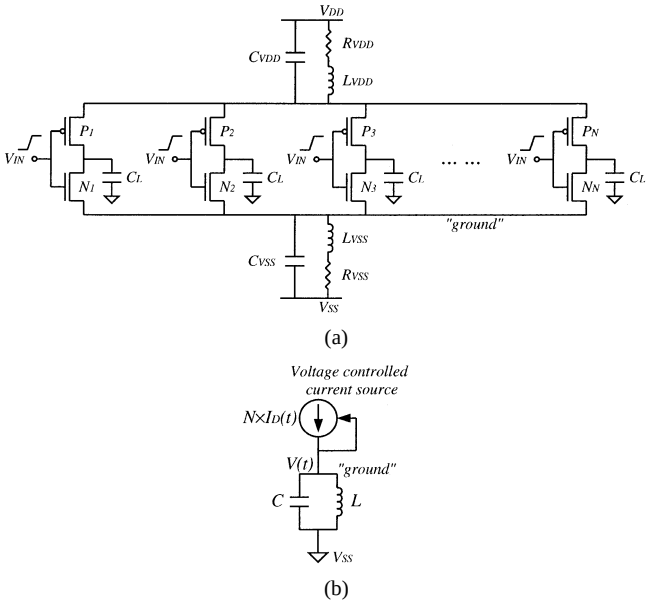

Fig. 1. (a) Equivalent circuit for simultaneous switching noise modeling. (b) Simplified circuit for ground bounce modeling.

The rest of this paper is organized as follows. In Section II, we propose the application-specific MOSFET model for estimating the simultaneous switching noise. In Section III, a simple SSN formulation is presented on the basis of the simple model and is compared to previously published results. Section IV includes the parasitic capacitance of the package in the model. We derive the maximum SSN voltages for four different cases depending on the value of the parasitic capacitance and the slope of the input signal. Finally, we present our conclusions in Section V.

II. MOSFET Modeling for SSN Estimation

In this paper, we study the simultaneous switching noise caused by the switching of N identical output drivers. For simplicity of presentation, only the noise at the ground network is discussed. The SSN at the power-supply grid can be analyzed similarly. The main purpose of this paper, similar to that of [7], [9], and [11], is to calculate the worse case SSN voltage in a chip when the following are given: i) the deep submicron process technology to derive the ASDM model; ii) the values of parasitic inductance and capacitance; and iii) the number of simultaneous switching drivers. It may be noted that the worst case SSN occurs under the following conditions: 1) the load capacitance is infinitely large so that an output node stays high during the entire period of time when the input switches; 2) all drivers switch at the same time and in the same direction; and 3) there is no decoupling capacitance. The equivalent circuit for SSN modeling is shown in Fig. 1(a).

The simplified circuit for ground bounce modeling is illustrated in Fig. 1(b), where the small parasitic ground resistance is neglected. From here onwards to maintain simplicity of notations, we omit the subscripts of the capacitance and the inductance. The pull-down transistors are modeled as a voltage controlled current source. In the worst case load condition, one can reasonably assume that the output nodes stay high during the input rising period and the transistors are in

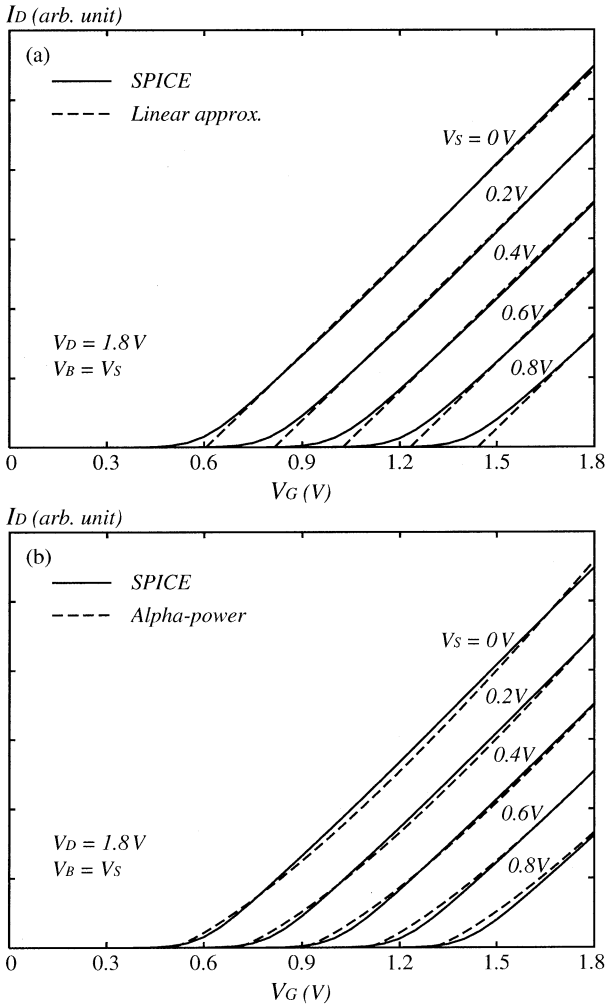

Fig. 2. MOSFET **I–V** characteristic modeling. (a) Linear approximation. (b) $\boldsymbol{\alpha}$-power law model.

the saturation region [7]. According to Sakurai and Newton's α-power law model [19], the drain current of a MOSFET device when in the saturation region can be modeled as

$$I_D = K(V_{GS} - V_T)^{\alpha} \tag{1}$$

where V_T is transistor threshold voltage and α is a fitting parameter which is close to 2 for long channel FET's and is close to 1 for short channel devices. Directly applying (1) for analytical study of the SSN, however, turns out to be impossible to obtain closed-form formulas because of the αth power function. Therefore, various approximation techniques have been used in the literature, each of which leads to inaccuracy in addition to the error introduced in device modeling.

On the other hand, we are only interested in certain specific operating region of a transistor for the SSN application. More specifically, we are interested in the scenario that the drain terminal of the FET stays high during the input rising period and the source and bulk terminals of the FET have the same voltage. Therefore, the drain current of the FET can be written as a function of two variables, the gate voltage and the source voltage

$$I_D = f(V_G, V_S). \tag{2}$$

In Fig. 2, we plot the drain current of a 0.18-μm process n-type transistor with respect to the gate voltage at different source voltage values. The solid curves are obtained through HSPICE simulation using Level 49 MOSFET model (BSIM3). It is observed that, 1) for any given value of V_S, I_D is approximately a linear function of V_G, and 2) the group of I_D versus V_G curves are equally spaced with different V_S values, which suggests a linear dependence of I_D on V_S. Therefore, the transistor drain current can be formulated as

$$I_D = K(V_G - V_0 - \gamma V_S), \quad \text{when } V_G \geq V_0 + \gamma V_S \tag{3}$$

and $I_D = 0$, otherwise, where V_0 measures the voltage displacement and $\gamma - 1$ models the channel length modulation effect.

TABLE I
EXTRACTED MODEL PARAMETERS FOR MOSIS TSMC PROCESSES

Process	V_{DD} (V)	Type	K (mA/V)	V_0 (V)	γ
0.18 μm	1.8	NFET	0.455	0.606	1.044
		PFET	0.258	0.759	1.090
0.25 μm	2.5	NFET	0.299	0.722	1.046
		PFET	0.217	0.907	1.039
0.35 μm	3.3	NFET	0.209	0.877	1.050
		PFET	0.175	1.034	1.062

As illustrated in Fig. 2(a), the simple linear model matches the drain current curves extremely well when the current values are not very small. The small discrepancy near the transistor threshold region is not important for the SSN modeling purpose because the current, as well as the change in current, in this region is insignificant. As a comparison, in Fig. 2(b) we have plotted the drain current curves calculated by the α-power law model. The simple linear model actually matches the BSIM3 curves slightly better than the α-power law model in the relevant region. The model parameters are extracted by least square error fitting of the MOSFET *I-V* characteristic. We have assumed that the transistors have the minimum channel length for the given technology. Only the portion of operating points with a drain current greater than 20% of the saturated drain current is considered in the curve-fitting procedure. Extracted model parameters for three recent TSMC processes, which are available through MOSIS, are shown in Table I. The value of K is per micrometer transistor width assuming minimal channel length.

The proposed SSN-specific device model may look similar to the α-power law model if α is set to 1. However, the proposed ASDM linear model is conceptually different from this special case of α-power law model. First, α-power law model does not account for the effect of channel length modulation while the ASDM model captures this effect through the parameter γ. Second, V_T in the α-power law model is the actual transistor threshold voltage; in contrast, V_0 in the ASDM linear model is an arbitrary fitting number. For example, for the n-type transistor in the TSMC 0.18-μm process, V_T is 0.50 V while the extracted V_0 is 0.606 V. Third, in the parameter extraction process, the α-power law model, being a general-purpose device model, is designed to model the entire MOSFET *I–V* characteristic while the linear model only tries to match the portion of the characteristic that is of interest to the specific application, therefore it offers better matching with the measured characteristics in the regions of interest. A general-purpose device model, like the α-power law model, tries to achieve good overall matching quality with respect to all possible combinations of voltages at four terminals of a MOSFET device. In this specific task for modeling of SSN, only limited regions that pertain to the linear region of the MOSFET are considered. Paradoxically, ASDM employs simpler and incomplete formulation of the FET devices, nevertheless this anomalous modeling indirectly leads to more accurate estimation of SSN.

III. SIMULTANEOUS SWITCHING NOISE CALCULATION

Previous analytical models for simultaneous switching noises at output drivers only consider the parasitic inductance [9]–[11]. To make a fair comparison among the models, in this section, we first assume that the effect of the parasitic package capacitance can be neglected.

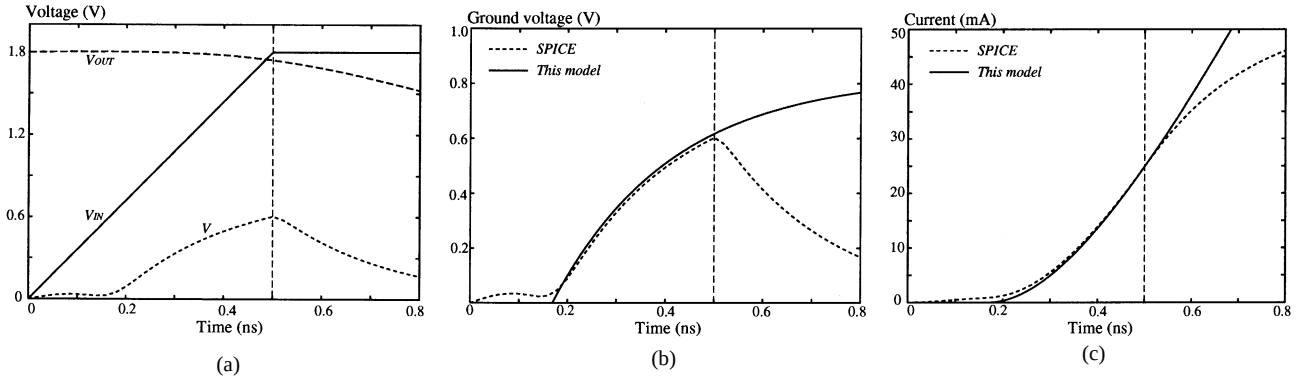

Fig. 3. Comparison of SPICE simulation and model results. (a) Simulated waveforms of ground node and I/O nodes. (b) Simulated and calculated simultaneous switching noise voltage. (c) Simulated and calculated current through the inductor.

The condition when this assumption is valid will be discussed in the next section.

Referring to Fig. 1(b), when the parasitic inductance is the only device connecting between the voltage-controlled current source and the true ground, the simultaneous switching noise due to the discharging current of N identical drivers through the inductor can be formulated as

$$V(t) = NL\,\frac{dI_D(t)}{dt}. \tag{4}$$

Inserting (3) into the right side of the above equation and noting that in this application V_G and V_S should be replaced by V_{IN} and V, respectively, one obtains

$$V(t) = NLK\left(\frac{dV_{\rm IN}(t)}{dt} - \gamma\,\frac{dV(t)}{dt}\right), \quad \text{when } V_{IN}(t) \geq V_0 \tag{5}$$

and the ground voltage $V(t)$ stays at zero before the input voltage $V_{IN}(t)$ reaches V_0. Equation (5) can be simplified to the following equation assuming the input signal is a ramp input with a rising slope of s_r:

$$\frac{dV(t)}{dt} + \frac{V(t)}{NLK\gamma} = \frac{s_r}{\gamma}, \qquad t \geq t_0. \tag{6}$$

This is a first-order ordinary differential equation. And the initial condition is that the ground node voltage is zero at the time $t = t_0$. Therefore, we can solve the differential equation to obtain the following time-dependent formula for simultaneous switching noise voltage at the ground node

$$V(t) = NLs_rK\left(1 - e^{-(s_r(t-t_0)/\gamma NLs_rK)}\right), \qquad t_0 \leq t \leq t_r \tag{7}$$

where t_r is the rise time of the input signal. The maximum noise voltage is achieved at the time the input signal reaches V_{DD}, which, after simplification, reads

$$V_m = NLs_rK\left(1 - e^{-(V_{DD}-V_0)/\gamma NLs_rK)}\right). \tag{8}$$

The time-dependent current through the transistor can then be calculated using (3) and (7)

$$I_D(t) = K\left(s_rt - V_0 - \gamma NLs_rK\left(1 - e^{-(s_r(t-t_0)/\gamma NLs_rK)}\right)\right) \qquad t_0 \leq t \leq t_r. \tag{9}$$

Fig. 3 compares the time-dependent ground voltage and current calculated using the proposed formulas with SPICE simulation results using typical parameters. Note that the formulas are valid only in the range that the input signal rises, in this case, from 0–0.5 ns. It is observed that both the SSN voltage formula and the current formula match the SPICE simulation results very well.

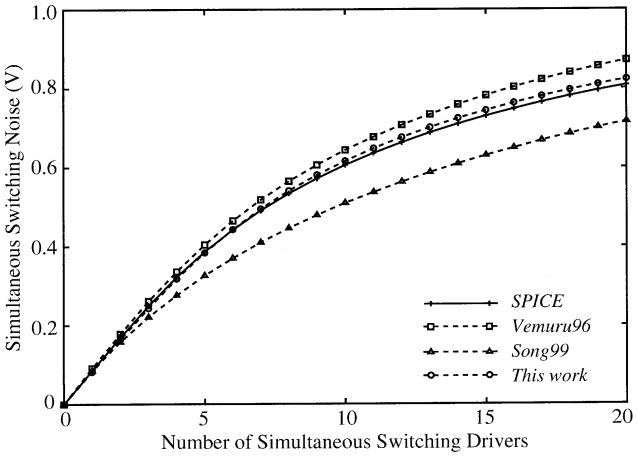

Fig. 4. Comparison with SPICE simulation and with previous works.

Fig. 4 plots the calculated maximum SSN voltage with respect to the number of simultaneously switching drivers together with two previous model calculation results [9], [11] for the TSMC 0.18-μm process. The proposed model is shown to be the most accurate among the three. We have also compared the models based on drivers designed using the TSMC 0.25-μm and 0.35-μm process technologies and the proposed model has similar advantage in accuracy.

Besides being accurate, the formulation of the maximum SSN voltage is very simple. Now let us further look into (8). Define a circuit-related figure H

$$H = NLs_r. \tag{10}$$

Then (8) can be rewritten as

$$V_m = HK\left(1 - e^{-(V_{DD}-V_0)/\gamma HK)}\right). \tag{11}$$

First, it is observed that the maximum simultaneous switching noise is a function of the circuit-related figure H and process-related parameters K, V_{DD}, V_0 and γ. The design implication of this observation is that, given a process technology, H is the only variable that we can use in circuit design to control the simultaneous switching noise. Second, H is a simple multiplication of three factors: N, L, and s_r. This means that changes in each of those three factors will have the *same* effect on SSN. This observation is helpful in optimizing the bonding pad driver design.

TABLE II
FORMULAS FOR MAXIMUM SSN VOLTAGE CONSIDERING BOTH PARASITIC INDUCTANCE AND CAPACITANCE

Case	Condition	Description	Maximum SSN voltage formula
1	$\Delta > 0$	over damped	$NLKs_r\left(1 - \frac{\lambda_2}{\lambda_2-\lambda_1}e^{-\lambda_1 t_{r,0}} + \frac{\lambda_1}{\lambda_2-\lambda_1}e^{-\lambda_2 t_{r,0}}\right)$,
2	$\Delta = 0$	critically damped	$NLKs_r\left(1 - (1+\lambda t_{r,0})e^{-\lambda t_{r,0}}\right)$,
3a	$\Delta < 0$, $t_{r,0} \le \pi/\omega$	under damped (fast input)	$NLKs_r\left(1 - e^{-\lambda t_{r,0}}(cos\omega t_{r,0} + \frac{\lambda}{\omega} sin\omega t_{r,0})\right)$,
3b	$\Delta < 0$, $t_{r,0} > \pi/\omega$	under damped (slow input)	$NLKs_r\left(1 + e^{-\frac{\lambda}{\omega}\pi}\right)$,

where $t_{r,0} = t_r(1 - V_0/V_{DD})$, $\lambda = NK\gamma/(2C)$, $\omega = \sqrt{4C/L - N^2K^2\gamma^2}/(2C)$,
$\lambda_1 = (NK\gamma - \sqrt{N^2K^2\gamma^2 - 4C/L})/(2C)$, $\lambda_2 = (NK\gamma + \sqrt{N^2K^2\gamma^2 - 4C/L})/(2C)$.

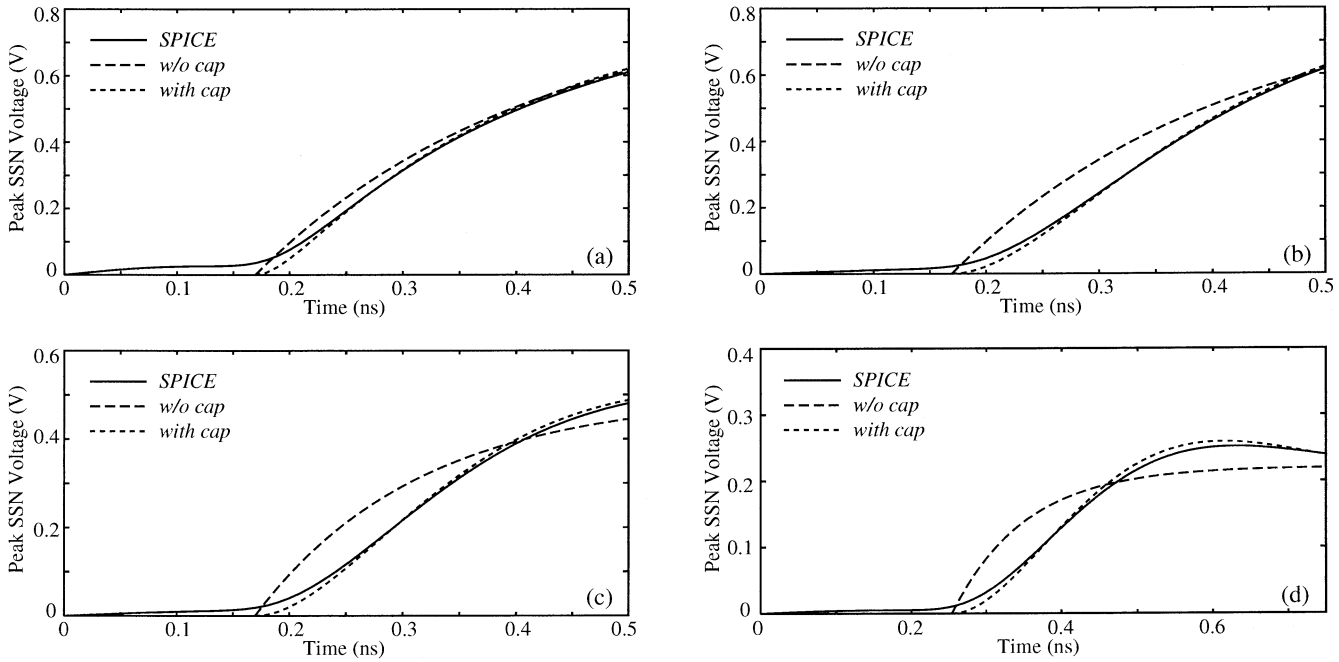

Fig. 5. Comparisons of simulated and calculated SSN waveforms. (a) Case 1: over damped, $\boldsymbol{L = 5.0}$ nH, $\boldsymbol{C = 1.0}$ nF, $\boldsymbol{t_r = 0.50}$ ns, $\boldsymbol{N = 10}$. (b) Case 2: critically damped, $\boldsymbol{L = 5.0}$ nH, $\boldsymbol{C = 3.0}$ nF, $\boldsymbol{t_r = 0.50}$ ns, $\boldsymbol{N = 10}$. (c) Case 3a: under damped, $\boldsymbol{L = 5.0}$ nH, $\boldsymbol{C = 2.0}$ nF, $\boldsymbol{t_r = 0.50}$ ns, $\boldsymbol{N = 6}$. (d) Case 3b: under damped, $\boldsymbol{L = 5.0}$ nH, $\boldsymbol{C = 2.0}$ nF, $\boldsymbol{t_r = 0.75}$ ns, $\boldsymbol{N = 4}$.

IV. SSN MODELING WITH PARASITIC CAPACITANCE

In this section, we study the simultaneous switching noise problem considering both parasitic inductance and capacitance. The problem can be formulated as follows:

$$V(t) = L\,\frac{dI_L(t)}{dt} \tag{12}$$

$$I_L(t) = NK(s_r t - V_0 - \gamma V(t)) - C\,\frac{dV(t)}{dt} \tag{13}$$

where $I_L(t)$ is the current through the inductor. Inserting (13) into the right side of (12), one gets the following

$$C\,\frac{d^2V(t)}{dt^2} + NK\gamma\,\frac{dV(t)}{dt} + \frac{1}{L}\,V(t) = NKs_r. \tag{14}$$

Denoting

$$\Delta = N^2K^2\gamma^2 - 4C/L \tag{15}$$

the system is in one of the three operating modes depending on the value of Δ.

Case 1): $\Delta > 0$, (Over Damped): In this case, the time dependent SSN voltage can be derived as

$$V(t) = NLKs_r\left(1 - \frac{\lambda_2}{\lambda_2-\lambda_1}\,e^{-\lambda_1 t'} + \frac{\lambda_1}{\lambda_2-\lambda_1}\,e^{-\lambda_2 t'}\right) \tag{16}$$

where

$$\lambda_1 = \frac{NK\gamma - \sqrt{\Delta}}{2C}, \quad \lambda_2 = \frac{NK\gamma + \sqrt{\Delta}}{2C}$$

and $t' = t - t_0$. It can be shown that the derivative of the SSN voltage with respect to time is positive definite during the period $t_0 < t \le t_r$. Therefore, the maximum SSN voltage is obtained at time t_r.

Case 2): $\Delta = 0$, (Critically Damped): In this case, the SSN voltage waveform can be derived as

$$V(t) = NLKs_r\left(1 - (1+\lambda t')e^{-\lambda t'}\right) \tag{17}$$

where

$$\lambda = \frac{NK\gamma}{2C}.$$

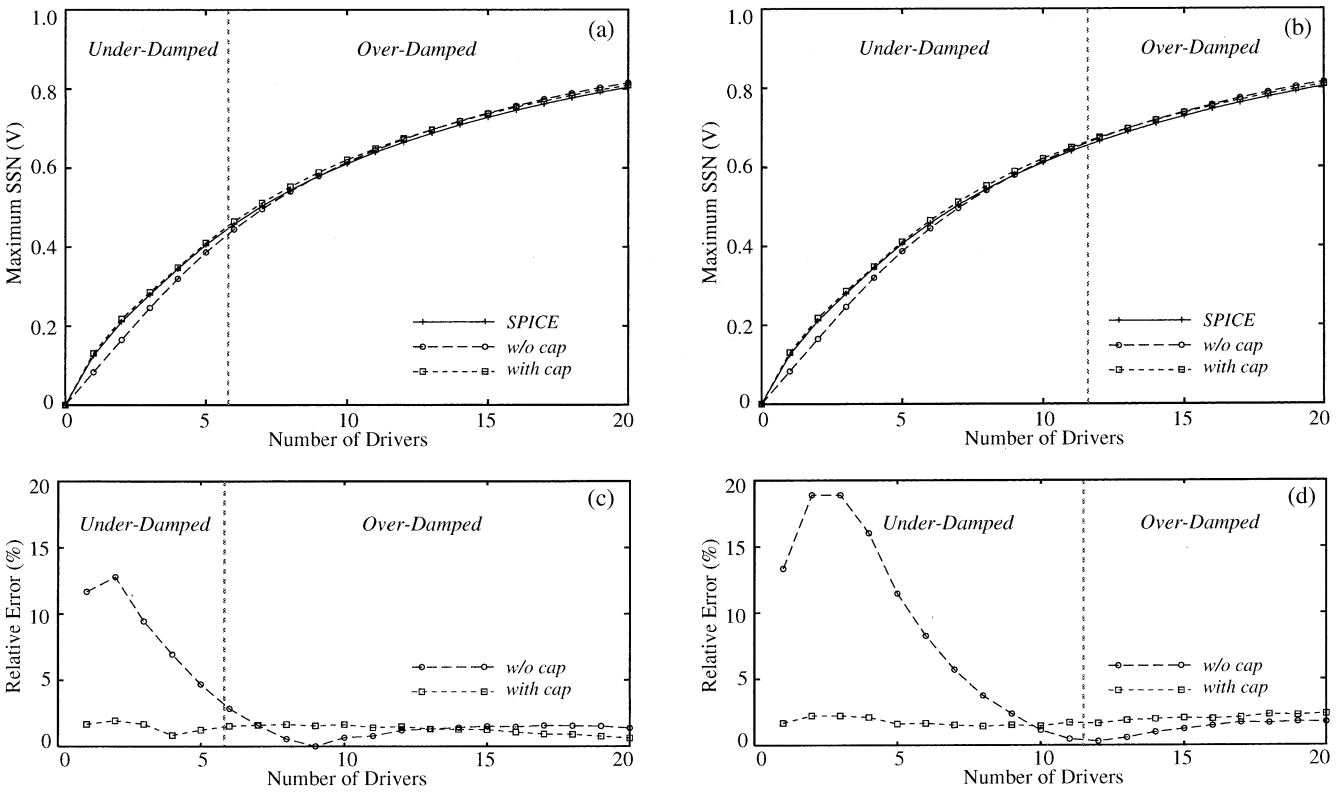

Fig. 6. Comparisons of simulated and calculated maximum SSN voltages. (a) $\boldsymbol{L = 5.0}$ nH, $\boldsymbol{C = 1.0}$ pF and $\boldsymbol{t_r = 0.50}$ ns. (b) $\boldsymbol{L = 2.5}$ nH, $\boldsymbol{C = 2.0}$ pF and $\boldsymbol{t_r = 0.25}$ ns. (c) Relative error of (a). (d) Relative error of (b).

Similarly, it can be shown that the derivative of the noise waveform with respect to time is positive definite during the period $t_0 < t \leq t_r$. Therefore, the maximum SSN voltage is also obtained at time t_r.

Case 3): $\Delta < 0$, *(Under Damped):* In this case, the time dependent simultaneous switching noise voltage is calculated as

$$V(t) = NLKs_r \left(1 - e^{-\lambda t'} \left(\cos \omega t' + \frac{\lambda}{\omega} \sin \omega t'\right)\right) \tag{18}$$

where

$$\lambda = \frac{NK\gamma}{2C}, \quad \omega = \frac{\sqrt{4C/L - N^2K^2\gamma^2}}{2C}.$$

The derivative of the above noise voltage formula is

$$V'(t) = NLKs_r \frac{\lambda^2 + \omega^2}{\omega} e^{-\lambda t'} \sin \omega t' \tag{19}$$

meaning that the simultaneous switching noise voltage reaches local maxima/minima when the term $\sin \omega t'$ is zero. It is derived that as long as the input signal rise time is greater than the time for the ground noise voltage to reach its first peak

$$t_r > t_0 + \pi/\omega \tag{20}$$

the maximum SSN voltage occurs at the first noise peak

$$V_m = NLKs_r \left(1 + e^{-(\lambda/\omega)\pi}\right). \tag{21}$$

If, on the contrary, the inequality shown in (20) does not hold, the maximum SSN voltage is obtained at time t_r.

There are four possible cases on the whole: over damped, critically damped, under damped with fast input signal, and under damped with slow input signal. Each has a different formulation for the maximum SSN voltage. A complete list of the formulas for maximum simultaneous switching noises is shown in Table II.

In Fig. 5, we compare the noise waveforms obtained by HSPICE simulation with those calculated using the manually derived equations with or without considering the parasitic capacitance. Fig. 5(a) shows the case that the system operates in the over-damped mode. The model without considering the capacitance predicts slightly faster transient response in the beginning but is still able to approximately characterize the transient response of the noise glitch. The critically damped case is shown in Fig. 5(b). Despite the apparent difference in noise waveforms, the peak noise voltage that the simple model predicts is still very close to the actual simulated value. In Fig. 5(c), we illustrate the case that the system is in the under-damped region and the input signal rise time is relatively small. Here, the maximum noise voltage is reached at time t_r. The simple model that neglects parasitic capacitance starts to show its inadequacy in terms of modeling peak noise voltage. Finally, Fig. 5(d) shows the case that the simple model clearly fails to predict a meaningful maximum SSN voltage value. This is the case that the system is under damped and the input signal is slow. As shown in Fig. 5, the simple model predicts that the noise reaches its maximum at time t_r (0.75 ns), whereas the actual noise peaks at around $t = 0.6$ ns. On the other hand, it is also observed that the improved model that takes into account both parasitic capacitance and inductance is able to match the simulation waveforms very well in all four cases.

Fig. 6 compares the derived formulas with HSPICE simulation results in terms of maximum simultaneous switching noise voltage. Fig. 6(a) shows a typical case where $L = 5.0$ nH and $C = 1.0$ pF while Fig. 6(b) assumes that the number of ground pads is doubled, therefore, the parasitic inductance is halved and the parasitic

capacitance is doubled. The relative model errors of the two cases are shown in Fig. 6(c) and (d), respectively. We have used the following to calculate the relative error values:

$$\text{R.E.} = \frac{|V_{\text{sim}} - V_{\text{eqn}}|}{\max(V_{\text{sim}},\, 0.2V_{DD})}$$

where V_{sim} and V_{eqn} are the maximum SSN voltages obtained by SPICE simulation and by our formulations, respectively. We have used the larger of V_{sim} and $0.2V_{DD}$ as the denominator to avoid the problem of producing extremely large relative error values when V_{sim} is very small. In both cases, it is observed that the simple model without considering the parasitic package capacitance performs well in the over-damped region. But the error is significant in the under-damped region. On the other hand, the relative error of the improved model considering both parasitic inductance and capacitance is always less than 3%.

Since the effect of parasitic capacitance is significant only when the system is in the under-damped region, the critical capacitance, C_{crit}, which is defined as the capacitance that makes the system operate in the critically damped region, can be used as a guideline to determine if the parasitic capacitance effect is needed to be modeled in design practice. Based on the definition of Δ, the critical capacitance value is derived as

$$C_{\text{crit}} = \frac{N^2K^2\gamma^2L}{4}. \tag{22}$$

When the effective ground parasitic capacitance is greater than C_{crit}, the system is in the under-damped region. Therefore, one should use the more accurate SSN formulas shown in Table II. Note that C_{crit} depends quadratically on N, the number of drivers that switch at the same time. Therefore, the system is very likely in the under-damped region when N is relatively small and in the over-damped region when N is large.

V. Conclusion

This paper presents an accurate modeling scheme for simultaneous switching noises generated at the periphery of a chip due to simultaneous switching of output pad drivers. The paper has introduced a SSN-specific MOSFET modeling methodology which strictly models the operating region of FET that is relevant for accurately modeling SSN. The paper has demonstrated that the proposed simple model that predicts a linear dependency of the transistor current on both the gate voltage and the source voltage, is superior to the α-power law model in terms of both accuracy and simplicity for estimation of simultaneous switching noise. The paper has, also for the first time, analytically studied the effects of the parasitic package capacitance on the simultaneous switching noise. It shows that the effect of the package capacitance cannot be neglected when the system is in the under-damped region. Further, the paper postulates a simple criterion [note (22)] to determine when parasitic capacitance of wires and pads must be included in the SSN calculations. The paper also has derived SSN formulas including the effects of both parasitic inductance and capacitance, and the analytical results are shown to tally within 3% of SPICE simulation results.

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