Compact Multiple-Valued Multiplexers Using Negative Differential Resistance Devices

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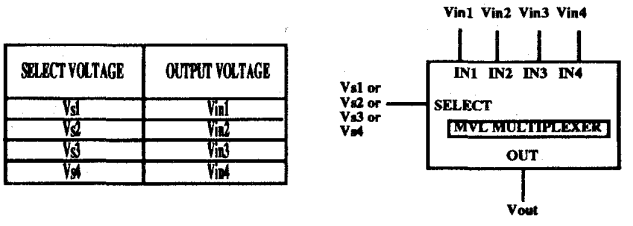
Abstract—**Quantum electronic devices with negative differential resistance (NDR) characteristics have been used to design compact multiplexers. These multiplexers may be used either as analog multiplexers where the signal on a single select line selects one out of four analog inputs, or as four-valued logic multiplexers where the select line and the input lines represent one of four quantized signal values and the output line corresponds to the selected input. Any four-valued logic function can be implemented using only four-valued multiplexers (also known as T-gates), and this T-gate uses just 13 devices (transistors) as compared to 44 devices in CMOS. The design of the T-gate was done using a combination of resonant tunneling diodes (RTD's) and heterojunction bipolar transistors (HBT's) with the folded I-V characteristic (NDR characteristic) of the RTD's providing the compact logic implementation and the HBT's providing the gain and isolation. The application of the same design principles to the design of T-gates using other NDR devices such as resonant tunneling hot electron transistors (RHET's) and resonant tunneling bipolar transistors (RTBT's) is also demonstrated.**

I. Introduction

IT is well known that negative differential resistance (NDR) or folded I-V characteristics of devices can be exploited to create extremely fast and compact circuits [1]. While the properties of resonant tunneling diodes (RTD's) were predicted almost 20 years ago [2], recent developments in growth techniques such as molecular beam epitaxy (MBE) have made it possible to actually build and use these devices. One of the main application areas of the new devices is in multiple-valued logic.

Multiple-valued logic seeks to improve the information processing efficiency of a circuit by transmitting more information on each signal line than simple binary logic and by implementing complex functions of the inputs in a single gate [3]. However, the use of multiple-valued logic has been hampered by the fact that compact and stable multiple-valued logic circuits are hard to build, the noise margins on multiple-valued lines are reduced, and most important of all, there is a need to perform conversions to and from a predominantly binary world. The folded I-V characteristic of RTD's and other quantum electronic devices makes it possible to have multiple stable states with good margins in a simple circuit consisting of just a few devices. This fact was recognized by several researchers and several compact multiple-valued storage functions have been described in the literature. For example, [4] and [5] describe a three-state memory cell using NDR devices, and a more recent work [6] describes a multivalued SRAM cell constructed with RTD's. The basic idea in these designs is that a simple series connection of a resistor, transistor, or any other load with a NDR device that has folded I-V characteristics produces a circuit with multiple stable states. While the storage functions realized by these circuits are very important, not much research has been done on the implementation of multivalued logic gates.



(a) (b)

Fig. 1. Schematic and truth table of four-valued T-Gate or multiplexer.

Reference [7] describes a design methodology for generating multiple-valued functions of a single multiple-valued input, using RTD's. Given a function f: $M \rightarrow M$ where $M = \{0, 1, 2, \cdots, m-1\}$ is a set of input/output values, the design methodology of [7] can be used to build a gate consisting of m RTD's and many transistors and resistors to implement the function f. However, the general multiple-valued logic gate with n inputs and one output, all of which can take on values from the set M, cannot be implemented efficiently using this method. Nor is it possible to simply combine the basic single input gates to implement the general function F: $M^n \rightarrow M$.

Just as any binary logic circuit can be implemented using just two-input NAND's or NOR's or two-input binary multiplexers or a combination of AND-OR-NOT gates, it is possible to implement any multiple-valued function F using just a small set of gate types [8]. While the generalized multiple-valued NAND/NOR gates cannot by themselves implement any generalized function F, T-gates, or generalized m-valued multiplexers with n m-valued inputs and one m-valued se-

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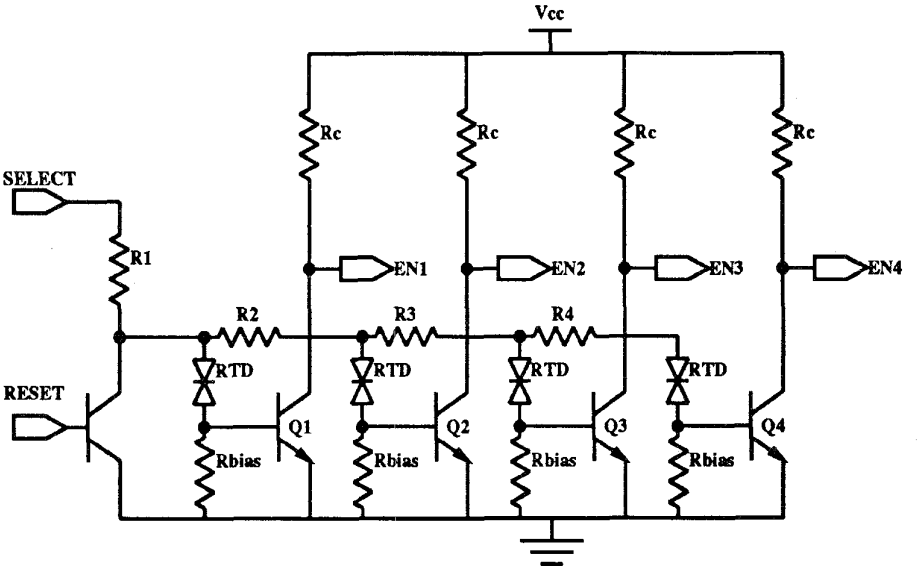

Fig. 2. The RTD decoder.

lect line, can by themselves implement any other m-valued function of n inputs.

This paper describes a multiple-valued logic T-gate using NDR devices. This gate not only achieves significant savings in area over implementations using conventional devices, but also achieves savings in area when compared with MOS implementations of binary logic with equivalent information processing capacity. A quaternary logic T-gate is described here, but the design principles apply to any m-valued logic, ($m > 2$). The quaternary logic T-gate described here can also be used to build simple and efficient binary-quaternary and quaternary-binary converters. Any quaternary logic function can be efficiently implemented using these T-gates alone, just as any binary logic function can be implemented using binary multiplexers alone. A detailed description of the T-gate designed with RTD's is presented next, followed by an alternate design with RTBT's or RHET's. All the designs were simulated using NDR-SPICE [9], an enhanced version of the standard SPICE simulator that has models for the new quantum electronic devices and has improved convergence routines. The designs using RTD's and HBT's (or BJT's) were assembled and tested using discrete devices.

II. T-Gate Using RTD's

The quaternary T-Gate or multiplexer is a circuit with four data inputs, one data output, and one control(select) input. All the inputs and the output are four-valued, taking on one of the logical values from the set $M = \{0, 1, 2, 3\}$. Fig. 1 shows the schematic outline and truth table of the T-Gate. The *select* line is input to a decoder circuit made up of RTD's; the output of the decoder is in the form of four *enable* lines, each of which is *HIGH* for exactly one of the four possible values on the *select* line. The *enable* lines control four independent current switch stages, each of which receives one of the four data inputs to the T-gate. The output of each current-switch is proportional to its input data when the current-switch *enable* line is *HIGH* and zero when the *enable* line is low. The output stage sums the current-switch outputs and performs suitable level-shifting and scaling of the output levels. Each of the above three components is described in detail below.

A. The RTD Decoder

The *select* input of the multiplexer is connected to a π network consisting of RTD's and resistors (see Fig. 2). The series resistors R1, R2, R3, and R4 form a chain terminated in an RTD branch. The other RTD branches are tapped off from the resistor chain. Each RTD branch consisting of an RTD in series with a resistor, is in itself a bistable circuit that switches from one state to another at a precise value of the applied voltage, as the applied voltage is increased from 0 V. The resistor chain causes a progressively smaller voltage to be applied across each RTD branch in the π-network, causing each RTD branch to switch states at different (increasing) applied voltages.

The RTD Branch: The operation of the selector circuit may be understood by considering the operation of a single RTD branch consisting of an RTD connected to the base of a transistor and a resistor R_{bias}. The voltage at the base of the HBT is determined from the load line shown in Fig. 3(a). The base-emitter junction of the HBT is assumed to behave as an ideal diode. As the input voltage V_{node} is increased, the idealized RTD characteristic slides to the right as shown in Fig. 3(a). The voltage V_{base} is plotted as a function of V_{node} in Fig. 3(b). Initially, V_{base} is small and the HBT is OFF. When V_{base} reaches the cut-in voltage of the ideal diode, the HBT is ON (saturation). As the input voltage is increased further, the folded I-V characteristic of the RTD causes the operating point to jump to the second positive differential resistance region in the RTD curve and the voltage V_{base} is consequently well below cut-in so that the HBT gets turned OFF. Further increasing the applied voltage will cause the HBT to eventually turn ON again. However, the resistance

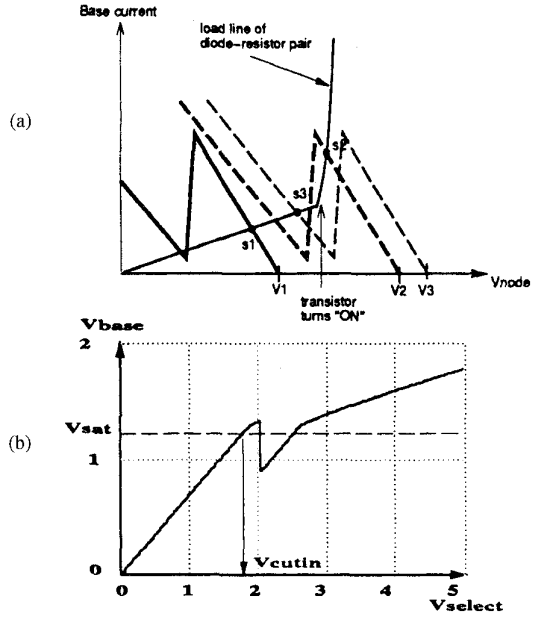

Fig. 3. Load lines and voltages in the RTD branch circuit. (a) RTD load line. (b) Base voltage of HBT.

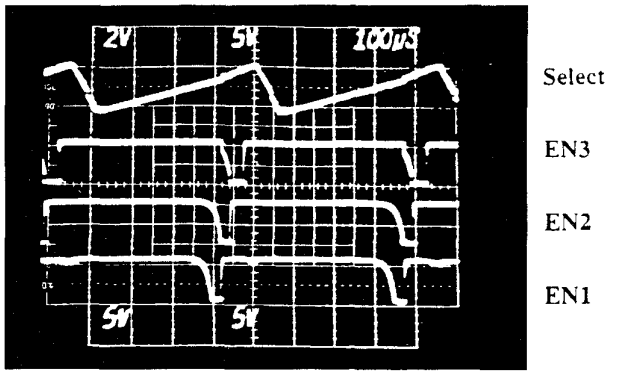

Fig. 4. Oscilloscope traces for the select line and three of four enable voltages of the decoder (Y-axis: 5 V/div for EN1-EN3 and 2 V/div for Select; X-axis: 100 μs/div).

values and the applied voltages are chosen so that the voltage never gets high enough to turn on the HBT a second time. The RTD-branches further down the chain see smaller input voltages (V_{node}) and consequently the associated HBT's turn on at higher applied voltages (higher *select* voltages). The collector voltage of the HBT is low whenever the HBT is ON and high whenever the HBT is OFF.

The explanation above is based on simple linear models and neglects higher order effects (observed/simulated) and also the fact that the switching of the stable state of an RTD branch abruptly decreases the current through the branch, causing voltage changes across the entire π network. A four-valued decoder has been breadboarded with npn transistors (2N2222) and RTD's (UMA-1174) fabricated and packaged in the University of Michigan. Oscilloscope traces of the enable outputs corresponding to a sawtooth select voltage are shown in Fig. 4. It can be observed that the enable lines go low at

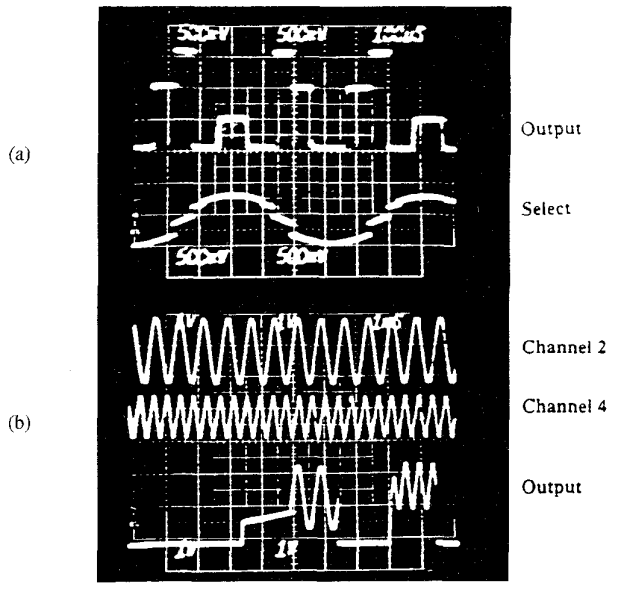

Fig. 5. Experimental results of a breadboarded RTD multiplexer. (a) Used as multiple-valued logic circuit (X-axis: 500 mV/div; Y-axis: 100 μs/div). (b) Used as an analog channel selector (X-axis: 1 V/div; Y-axis: 1 ms/div).

their corresponding select voltages and are nonoverlapping, which is desirable in a decoder.

B. Current Switches and the Output Stage

The *enable* outputs of the RTD decoder stage are compared with a fixed voltage to set four current switches ON or OFF. The multiplexer-data inputs are used to set up the tail current in the current switch through a simple current mirror configuration. Considering for the moment a single current-switch, the entire tail current $((V_{\text{in}} - V_{\text{cut-in}})/R_{\text{in}})$ flows through R_{out} if the *enable* voltage is low, causing the output voltage to be $V_{\text{out}} = V_{\text{cc}} - (V_{\text{in}} - V_{\text{cut-in}}) \cdot (R_{\text{out}}/R_{\text{in}})$. If the *enable* voltage is high, the output voltage is V_{cc} since all the current is diverted to the other branch. Hence the output voltage is a linear function of the input voltage when the *enable* line is low. All the branch currents from the four current switches are connected together, but one and only one of the *enable* lines is low at any time so the output is always a linear function of the selected input voltage. The output stage inverts and level shifts this voltage to produce a voltage compatible with the input levels. The *reset* input accepts a pulse that triggers the low-to-high transformation of the select voltage. This is necessary to eliminate hysteresis effects inherent in any circuit using the folded I-V characteristics [9].

The multiplexer circuit can also be modified to make a 1 : 4 demultiplexer. The tail current in all the switch branches is set by the input voltage or current while the *enable* lines make each output equal to either V_{cc} (if not selected) or a linear function of the input (if selected). An output stage is again required to invert and shift the output levels.

Experimental results for a breadboarded multiplexer are shown in Fig. 5(a). Channels 1–4 are connected to 1.5 V, 2.0 V, 0.5 V, and 1.0 V, respectively; these voltages represent logic levels of 2, 3, 0, and 1. The select input is a sine

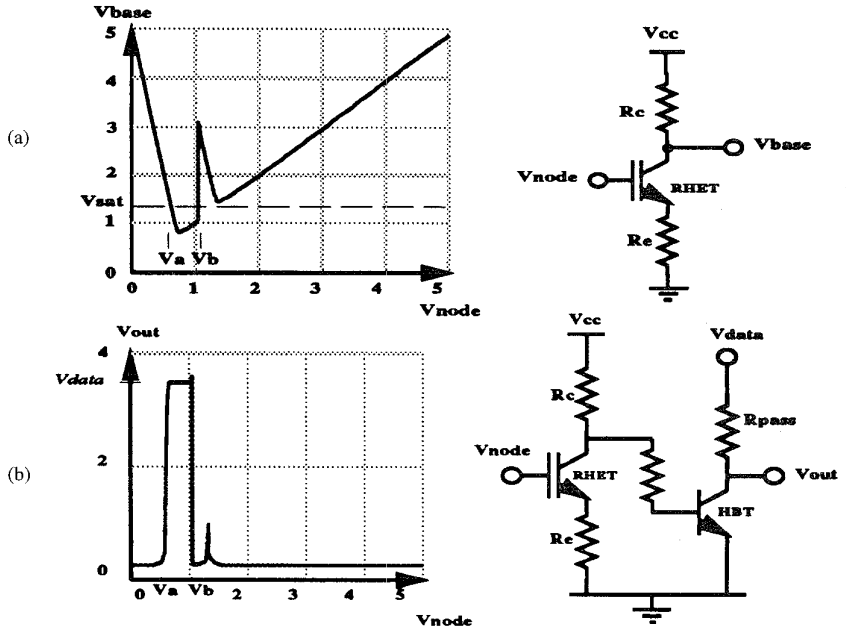

Fig. 6. (a) RHET/RTBT in inverter circuit configuration. (b) A literal-pass gate.

wave with a 0.95 V offset and 0.825 V amplitude; this allows repeated selection of the four different channels together with a period where no channel is selected (V_{select} is out of range). One can clearly see that the output (0, 2, 3, 0, 1, 0, 3, 2, 0, $\cdots$) shown corresponds exactly to the input of the channel being selected; it also shows that if no channel is selected, the output will assume a zero value. Note that a fast asynchronous pulse (not shown) is also being applied to the reset input in order to eliminate hysteresis.

The same multiplexer has also been used for analog multiplexing [see Fig. 5(b)]. Channel 1 of the multiplexer is connected to a ramping up signal, Channel 2 is connected to a sinusoidal wave (top trace), Channel 3 is connected to ground, and Channel 4 is connected to a triangular wave (middle trace). The select input is given a ramping up signal that cuts through all the select voltages. One can see that the output of the multiplexer (bottom trace) outputs the correct channel input waveform as that particular channel is selected.

III. T-Gate Using RHET's and RTBT's

Resonant tunneling bipolar transistors (RTBT's) [10] and resonant tunneling hot electron transistors (RHET's) [11] are three terminal devices with negative differential resistance in the base-emitter I-V characteristics and negative transconductance in the common-emitter characteristics. An advantage of the RHET and RTBT over the RTD is that the three terminal devices allow the input and output signals to be decoupled without having to insert extra buffer stages.

When the RHET or RTBT is connected in a simple common-emitter or inverter configuration as shown in Fig. 6, the resultant dc transfer curve shows a small, sharply defined region where the output voltage falls below a voltage marked V_{sat}. This is similar to the RTD branch circuit of the RTD-HBT multiplexer, where the HBT base voltage is high enough to turn on the HBT for a small, sharply defined range of input voltages. When the output of the RHET/RTBT inverter is inverted again, the output is low for all except a small range of input voltages. If the supply voltage of the second inverter stage is connected to some other voltage V_{data} instead of V_{cc}, the *HIGH* output voltage is equal to V_{data} and the low output voltage is close to zero, ignoring the loading effects of subsequent stages. Such a gate is called a *literal-pass gate*. When a resistor chain is used to supply progressively smaller fractions of a *select* voltage to four literal-pass gates, the resistor values can be chosen so that the ranges (V_{ai}, V_{bi}) for the four literal-pass gates correspond to ranges $(V_i - \delta, V_i + \delta)$ where V_i is the voltage corresponding to logic level i, $i = 0, 1, 2, 3$, and δ is a margin. Since at most one of the output voltages is nonzero for any input (select) voltage, they can be connected to the control inputs of a bank of current switches to produce a multiplexed output. Simulation results for this circuit are shown in Fig. 7.

IV. Summary

Two quaternary T-Gates or multiplexers and one demultiplexer have been described. These gates use the folded I-V characteristics of NDR devices to obtain compact implementations of multiple-valued logic functions. The RHET/RTBT multiplexer uses 13 transistors (RHET's/RTBT's and HBT's) and 16 resistors while a CMOS circuit with equivalent functionality (binary, 2-b 4 : 1 mux) would require 44 transistors (MOSFET's). The savings in area increase with higher-valued logics. For an eight-valued T-Gate (8 : 1 mux), the multiplexer design described above can be extended by using eight literal-pass gates with tighter margins on input voltages. Such a multiplexer would use 25 transistors and 32 resistors as against 118 MOSFET's for an equivalent CMOS implementation (binary, 3-b 8 : 1 mux).

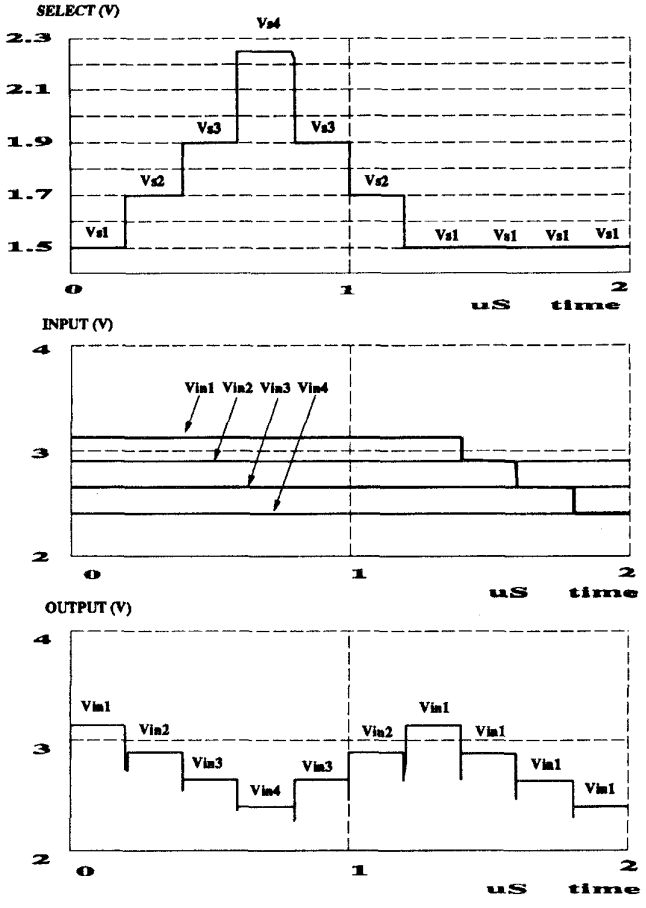

Fig. 7. Simulation results for RHET 4 : 1 four-valued multiplexer.

The operating speed of the RTD and RTBT/RHET circuits is expected to be much higher than CMOS operating speeds, since the switching speeds of both HBT's and RTD's are known to be in the range of a few picoseconds [12], [13]. Since interconnect delay is likely to be a major factor in the total delay, the shorter interconnect length in RTD or RTBT/RHET circuits (due to the compact nature of the circuit and the use of multiple-valued signals to reduce interconnect) gives these circuits one more advantage over CMOS in terms of speed.

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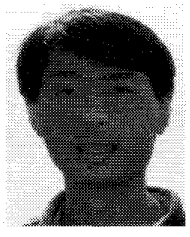

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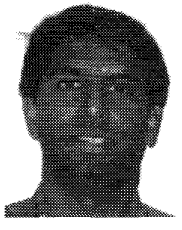

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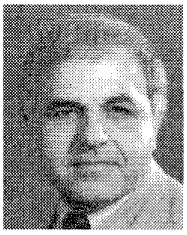

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