Transactions Briefs

Noise Margins of Threshold Logic Gates Containing Resonant Tunneling Diodes

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***Abstract*—Threshold gates consisting of resonant tunneling diodes (RTDs) in conjunction with HBTs or CHFETs or MOSFETs can form extremely compact, ultrafast, digital logic alternatives, and may be used for digital signal processing applications in the near future. The resonant tunneling phenomenon causes these circuits to exhibit super-high-speed switching capabilities. Additionally, by virtue of being threshold logic gates, they are guaranteed to be more compact than traditional digital logic circuits, while achieving the same functionality. However, reliable logic design with these gates will need a thorough understanding of their noise performance and power dissipation among other things. In this brief, we present an analytical study of the noise performance of these threshold gates supplemented by computer simulation results, with the objective of obtaining reliable circuit design guidelines.**

***Index Terms*—Emerging technologies, noise margins, resonant tunneling diode, threshold logic.**

I. Introduction

Nanoelectronic devices based on the resonant tunneling phenomenon are poised to make a major impact on integrated circuit technology [1]. Over the years, a wide variety of circuits consisting of resonant tunneling devices have been proposed in the literature [2]–[8], which have given us the reason to believe that compact ultra-high-speed integrated circuits based on these types of devices will be physically realized in the near future. More recently, several researchers have reported the development of multi-gigahertz digital circuits [9], [10]. From their projected performance, logic circuits composed of resonant tunneling diodes (RTDs) in conjunction with HBTs or MODFETs compare favorably with gates belonging to various other logic families (Table I).

Circuits containing resonant tunneling devices, such as threshold gates, literals [11], multiplexers [3], counters and MOBILE gates [12], [13], are not only faster than the conventional circuits, but they also use far less number of devices to achieve the same functionality (Table II).

Compared to the large number of published research papers dealing with the demonstration of RTD-based circuit operation and circuit ideas, work related to the analysis of such circuits seems to be very limited. This brief is a part of our continuing effort to fill that void.

II. RTD-HBT Threshold Logic Gate

In this brief, we present a study of the noise immunity of a certain kind of RTD threshold gate whose circuit topology is shown in Fig. 1. This kind of circuit, proposed by Mohan *et al.* [6], can be tailored to function as an n-input m-threshold gate (m-threshold $\Rightarrow$ output is low, if and only if m or more inputs are high). The number n is related to the number of transistors $(n+1)$ and m is determined by the input signal levels. For example, for $n=3$ and $m=2$, we can have a 3-input inverted-MAJORITY (or, MINORITY) gate. Simulation results of such a gate working at 10-GHz clock speed is shown in Fig. 2. The layout diagram of this circuit is shown in Fig. 3. By virtue of the generic nature of this gate, it is our opinion that this type of RTD-HBT circuit may find wide application in the near future [14]. If the current drawn by each of the transistors $Q_1, \ldots, Q_n$ in their ON states be I (assuming no transistor mismatch) and the current drawn by Q_{clk} be I_H (when Clock is HIGH) and I_Q (when Clock is QUIESCENT), then for an m-threshold gate function, the following basic necessary conditions have to be satisfied:

$$(m-1)I + I_{clkH} < I_p \tag{1}$$

$$I_v < mI + I_{clkL} < I_p \tag{2}$$

$$mI + I_{clkH} > I_p. \tag{3}$$

TABLE I
Comparison of Process Technologies

Parameter	0.5 μm CMOS	GaAs CHFET	RTD+HBT	RTD+MODFET
Power/gate	0.2 mW	0.1 mW	0.5 mW	0.3 mW
Delay/gate	500 ps	250 ps	40 ps	200 ps
Device count per function	Large due to regular I-V characteristics	Large due to regular I-V characteristics	Small due to NDR I-V characteristics	Small due to NDR I-V characteristics

TABLE II
Device Counts for Function Implementation in Various Technologies

Circuit	TTL	CMOS	ECL	NDR
XOR	33	16	11	4
Majority	36	18	29	4
Muller C-element	45	8	44	4
9-state memory	24	24	24	5
NOR2+flipflop	14	12	33	3
NAND2+flipflop	14	12	33	3

III. Margin of Noise on the Signal Lines

The noise margin measurement technique adopted in this work is based on the simple but accurate method of fitting a maximum area rectangle between the normal and mirrored transfer characteristics of an RTD-HBT inverter. This method has been shown to be by far the most general and precise method for characterizing noise margins [15].

If we consider the normal transfer characteristic of the RTD-HBT inverter [Fig. 4(a)], we see that Regions 1 and 3 are monotonically decreasing functions of V_{in}, while Region 2 is an almost vertical drop. Region 2 is unique to the folded $I-V$ characteristic of resonant tunneling devices which causes almost instantaneous switching of the output voltage, when the operating point skips over the unstable NDR region.

Important adjustments, however, are necessary in order to apply the above noise margin measurement philosophy to our circuit, simply because of the fact that this method is easy to apply to static digital gates, but is not applicable to clocked logic gates of the type we are currently concerned with. In RTD-HBT threshold gates, the clock voltage levels play an important role. While evaluating the inputs to a gate, the level

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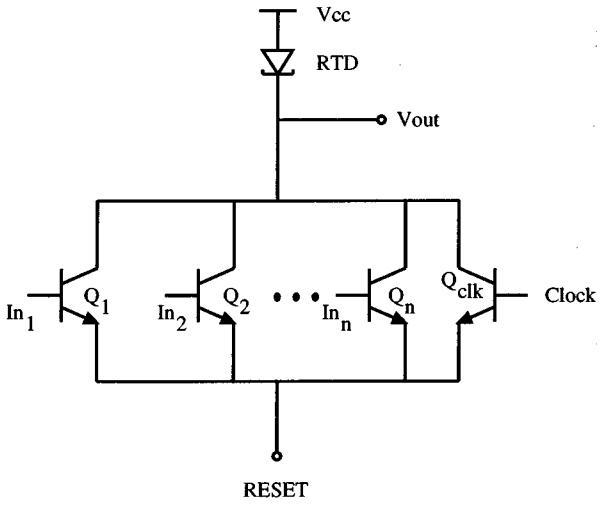
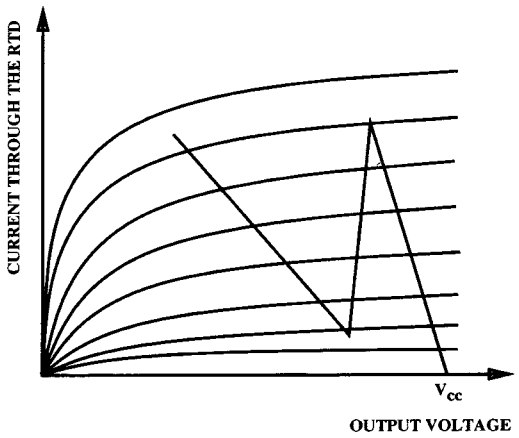


(a)



(b)

Fig. 1. (a) Circuit topology. (b) Load line.

of the clock typically increases to V_H and after evaluation, this level decreases to a quiescent value of V_Q. If we consider two such RTD-HBT inverters connected in series, for proper operation, the clocks to the two inverters have to be out of phase. That is, when the second gate is being evaluated by a high clock pulse, the clock to the previous gate has to be quiescent. Simply stated, the transfer characteristic should reflect the fact that the second inverter *sees* the output of the first inverter with the clock at V_Q and not at V_H.

The folded $I-V$ characteristic produces a sharp switching which can be regarded as a perfect vertical drop, for all practical purposes. Referring to Fig. 4(b), the maximum rectangle within the loop formed between the normal and the mirrored transfer characteristics will be $A'BCD$. If one tries to fit a rectangle of the type of $PQRS$, one can very soon realize that such a rectangle will almost always be smaller than $A'BCD$ and in a special case, if $PQRS > A'BCD$, $PQRS \approx A'BCD$, since Regions 1 and 3 are almost horizontal. Thus $A'BCD$ can be regarded as a good approximation of the maximum rectangle, in a general sense, within an area of the type $ABCD$. If the coordinates of the point B be $(x,\ y)$ and that of point E be $(x,\ y')$, then the coordinates of the point D will be $(y',\ x)$. Thus, the noise margins are simply expressed as

$$\text{NM}_H = y - x \tag{4}$$

$$\text{NM}_L = x - y'. \tag{5}$$

Therefore

$$\text{NM}_H + \text{NM}_L = y - y'. \tag{6}$$

It is easily seen that

$$x = V_T \ln\left(\frac{I_p - I_H}{I_s\left(1 - e^{-((V_{cc}-V_p)/V_T))}\right)}\right) \tag{7}$$

where $V_T = kT/q$,

$$y = (V_{cc} - V_p) + (I_H - I_Q)R_{p1} \tag{8}$$

$$y' = (V_{cc} - V_f) + (I_H - I_Q)R_{p2}. \tag{9}$$

The symbols R_{p1}, R_{p2}, V_p, V_f, etc., are explained with respect to the RTD's $I-V$ characteristics in Fig. 5. Equation (7) is based on the simple exponential relationship between a BJT's collector current and its base voltage

$$I_c = I_s\left(e^{V_{BE}/V_T} - e^{V_{BC}/V_T}\right). \tag{10}$$

This relationship is not very accurate, and hence, provides approximate results. For computer simulation, we shall use a more accurate relationship based on the Gummel–Poon model of the bipolar transistor, but for the sake of deriving simple analytical noise margins, let us, for the moment, assume this relation. Equation (6) shows us that the sum of the two noise margins is independent of x, and can be simply written as

$$\text{NM}_H + \text{NM}_L = (V_f - V_p) + (I_H - I_Q)(R_{p1} - R_{p2}). \tag{11}$$

Since

$$R_{p2} = \frac{V_f - V_v}{I_p - I_v} \tag{12}$$

and

$$|R_n| = \frac{V_v - V_p}{I_p - I_v}. \tag{13}$$

Equation (11) can be rewritten as

$$\begin{aligned}\text{NM}_H + \text{NM}_L = &\left(R_{p2} + |R_n|\right)\left(I_p - I_v\right)\\ &+ \left(I_H - I_Q\right)\left(R_{p1} - R_{p2}\right).\end{aligned} \tag{14}$$

For proper operation of the gate, $I_H < I_p$ and $I_Q > I_v$, implying, $I_H - I_Q < I_p - I_v$. Therefore, if $R_{p1} \geq R_{p2}$

$$\text{NM}_H + \text{NM}_L < \left(R_{p1} + |R_n|\right)\left(I_p - I_v\right)$$

or

$$\text{NM}_H + \text{NM}_L < V_v\left(1 - \frac{\text{PVVR}}{\text{PVCR}}\right) \tag{15}$$

where PVVR = Peak to Valley Voltage Ratio $= ((V_p)/(V_v))$ and PVCR = Peak to Valley Current Ratio $= ((I_p)/(I_v))$.

On the other hand, if $R_{p2} \geq R_{p1}$

$$\text{NM}_H + \text{NM}_L < \left(R_{p2} + |R_n|\right)\left(I_p - I_v\right)$$

or

$$\text{NM}_H + \text{NM}_L < V_f - V_p. \tag{16}$$

In (15) and (16), we are given important upper bounds for the sum of the two noise margins (when $R_{p1} = R_{p2}$, they are identical). On the one hand, they provide us with a simple way to estimate the maximum

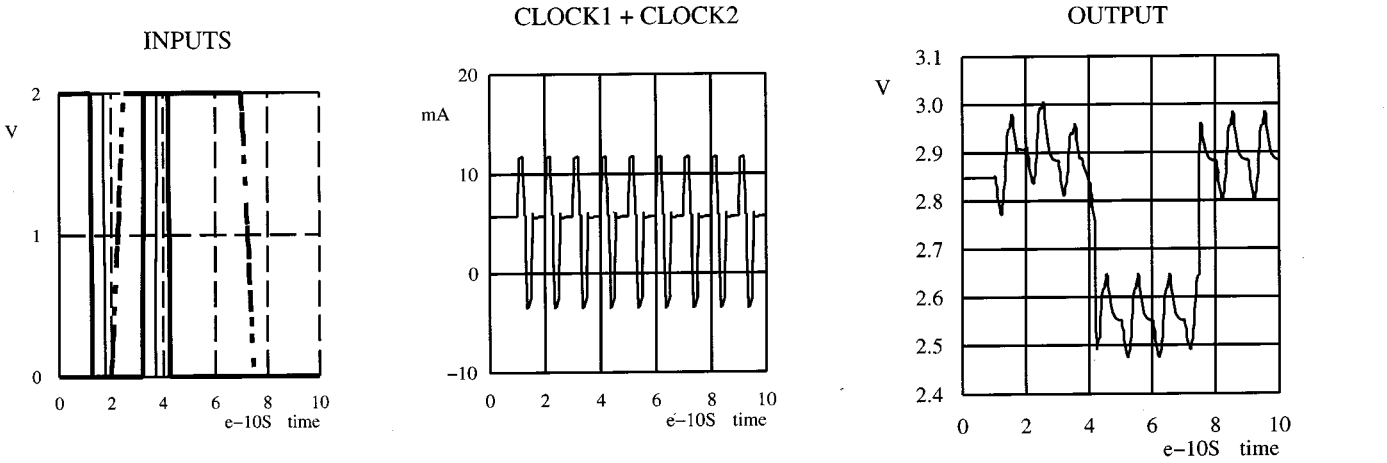


Fig. 2. Simulation results at 10-GHz clock speed of 3-input inverted-MAJORITY gate.

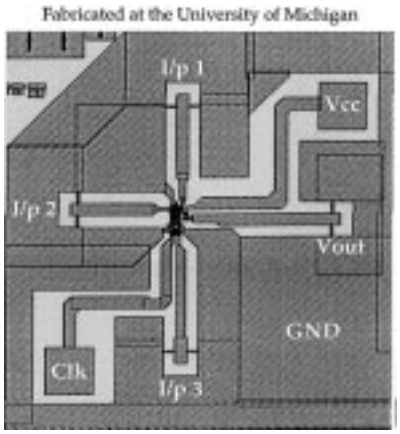


Fig. 3. Layout diagram of 3-input inverted-MAJORITY gate.

noise margin that can be harnessed from a given RTD, while on the other hand, they can be used by the device engineers as a guideline for designing RTDs for digital logic applications. Diamond *et al.* [16] had shown that *PVCR* is not a crucial factor in determining RTD circuit switching speed. Their analysis had shown that C/I_p (where C is the RTD's capacitance) is a much more important figure that can be directly related to switching time. However, (15) re-establishes, to a certain extent, the importance of *PVCR* so far as clocked RTD switching circuits are concerned. Furthermore, lower static power dissipation of such circuits is possible only when I_v is low. Thus, ultimately, PVCR remains an important figure of merit for the RTD beyond merely indicating the quality of epitaxial growth. For RTDs with *PVCR* in the range of 10 to 20 and above, (15) reduces to

$$\text{NM}_H + \text{NM}_L < V_v. \tag{17}$$

Using (10), we can write

$$x = V_T \ln\left(\frac{I_p - I_H}{I_s\left(1 - e^{-((V_{cc}-V_p)/V_T)}\right)}\right).$$

Therefore, the individual noise margins are given by

$$\text{NM}_H = (V_{cc} - V_p) + (I_H - I_Q)R_{p1} - V_T \ln\left(\frac{I_p - I_H}{I_s\left(1 - e^{-((V_{cc}-V_p)/V_T)}\right)}\right) \tag{18}$$

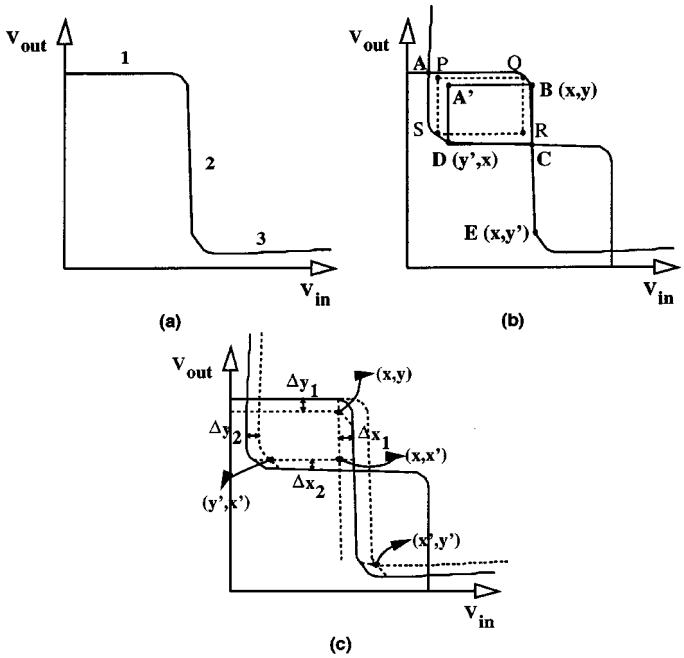


Fig. 4. The transfer characteristic at: (a) constant clock; (b) finding the maximum area rectangle; and (c) the effect of clock-current fluctuation.

$$\text{NM}_L = V_T \ln\left(\frac{I_p - I_H}{I_s\left(1 - e^{-((V_{cc}-V_p)/V_T)}\right)}\right) - (V_{cc} - V_f) - (I_H - I_Q)R_{p2}. \tag{19}$$

Therefore, in order to have $\text{NM}_L = \text{NM}_H$, we should have

$$2V_T \ln\left(\frac{I_p - I_H}{I_s\left(1 - e^{-((V_{cc}-V_p)/V_T)}\right)}\right) = 2V_{cc} - (V_p + V_f) + (I_H - I_Q)(R_{p1} + R_{p2}). \tag{20}$$

The accuracy of (19) will be a subject of discussion in Section V.

IV. Noise Margin With Noise on the Clock Signal

So far, we have dealt with the noise margin estimates on the signal line without considering any noise on the clock inputs. Noise on the clocks will definitely lower the previously estimated signal noise margins. In order to study the worst-case noise margins on the signal lines

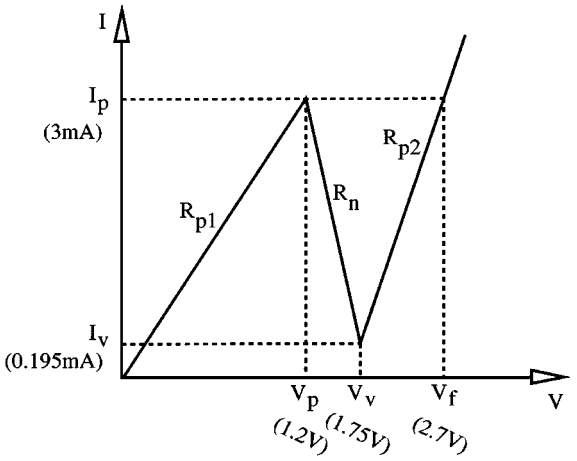


Fig. 5. RTD used for computer simulations (not to scale).

by introducing noise on the clock lines, we shall follow the following procedure.

We shall assume that noise on the clock lines can cause $\pm\delta_I$ fluctuations in the quiescent and high clock currents. That is, instead of a steady value of I_Q, the quiescent clock can vary from $I_Q-\delta_I$ to $I_Q+\delta_I$. Similarly, the high clock current can vary from $I_H-\delta_I$ to $I_H+\delta_I$. We have to understand now how the three regions of the transfer characteristic will fluctuate with variations in the clock levels. Fig. 4(c) and Table III together provide the worst-case situations that will adversely affect the noise margins. Based on them, the shrinkage of the noise margins can be approximately characterized by (21)–(24) as follows:

$$\Delta x_1 = V_T \ln\left(1+\frac{\delta_I}{I_p-I_H-\delta_I}\right) \tag{21}$$

$$\Delta x_2 = V_T \ln\left(1+\frac{\delta_I}{I_p-I_H}\right) \tag{22}$$

$$\Delta y_1 = \delta_I R_{p1} \tag{23}$$

$$\Delta y_2 = \delta_I R_{p2}. \tag{24}$$

Therefore, the modified noise margins are

$$\begin{aligned}\mathrm{NM}_H &= (V_{cc}-V_p)+(I_H-I_Q-\delta_I)R_{p1} \\ &\quad - V_T \ln\left(\frac{I_p-I_H+\delta_I}{I_s\left(1-e^{-((V_{cc}-V_p)/V_T)}\right)}\right)\end{aligned} \tag{25}$$

$$\begin{aligned}\mathrm{NM}_L &= V_T \ln\left(\frac{I_p-I_H-\delta_I}{I_s\left(1-e^{-((V_{cc}-V_p)/V_T)}\right)}\right) \\ &\quad - (V_{cc}-V_f)-(I_H-I_Q+\delta_I)R_{p2}.\end{aligned} \tag{26}$$

V. Computer Simulation Results

For the purpose of obtaining a general idea about the effect of various RTD and transistor parameters and the choice of current values $(I_H \& I_Q)$, the above equations should be sufficient. However, for accurate calculation of noise margins for a particular circuit, computer simulation seems to be the best approach. A computer simulation can handle the complex equations arising out of a detailed device model. For the RTD-HBT gate, we use the simple piecewise linear RTD model, but resort to the modified Gummel–Poon model of the bipolar transistor that is used in SPICE. Using an accurate model of the transistor is very essential, since the transistor plays a crucial role in determining the transfer function of these gates.

TABLE III
Fluctuations in I_H & I_Q and the Resultant Change in Noise Margins

Fluctuation	I_H	I_Q
Δy_1	Increase	Increase
Δx_1	Increase	Don't Care
Δx_2	Decrease	Don't Care
Δy_2	Decrease	Decrease

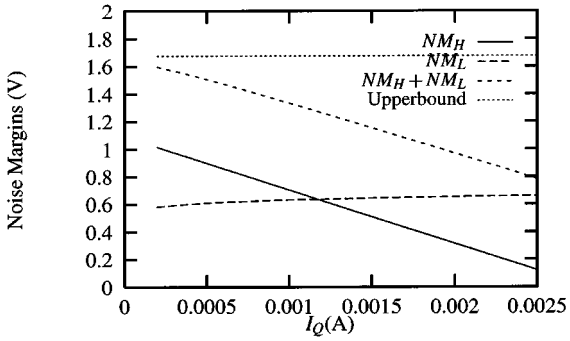


Fig. 6. Noise margins versus quiescent clock current $(V_{cc}=2\,\mathrm{V})$.

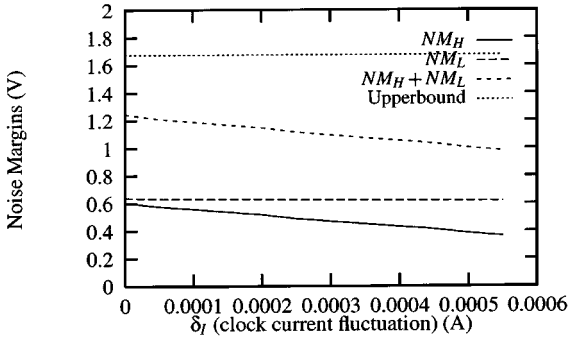


Fig. 7. Noise margins versus δ_I.

The collector current of a bipolar transistor, expressed in terms of the modified Gummel–Poon model parameters, is given by (27) as follows:

$$\begin{aligned}I_c &= \frac{I_s}{Q_B}\left[\left(e^{V_{B'E'}/N_F V_T}-1\right)-\left(e^{V_{B'C'}/N_R V_T}-1\right)\right] \\ &\quad - \frac{I_s}{\beta_R}\left(e^{V_{B'C'}/N_R V_T}-1\right)-I_{SC}\left(e^{V_{B'C'}/N_C V_T}-1\right).\end{aligned} \tag{27}$$

The noise margin calculations are carried out based on the methodology discussed in the previous section, by replacing (10) by (27). The piecewise linear RTD characteristic used is shown in Fig. 5.

Fig. 6 shows the variation of an RTD-HBT inverter's noise margins as a function of the quiescent clock current I_Q. As we have seen before, the upper-bound of the sum of the noise margins that can be extracted from an RTD is given by (15) and (16). Practically, this upper bound can never be reached because I_H has to be less than I_p and I_Q has to be greater than I_v for proper operation. We see in Fig. 6, for a constant-clock high current of 2.5 mA ($I_p=3.08$ mA) as I_Q is increased from I_v to I_H, NM_H decreases fast while NM_L increases by a very small amount. While the behavior of NM_H is corroborated by (18), the behavior of NM_L deviates considerably from (19) at higher values of I_Q. This should not come as a surprise, since the derivation of (19) assumes $(V_{cc}-V_f)$ to be positive, while results presented in Fig. 6 were obtained using $V_{cc}=2$ V, making $V_{cc}-V_f=-0.7$ V. Load

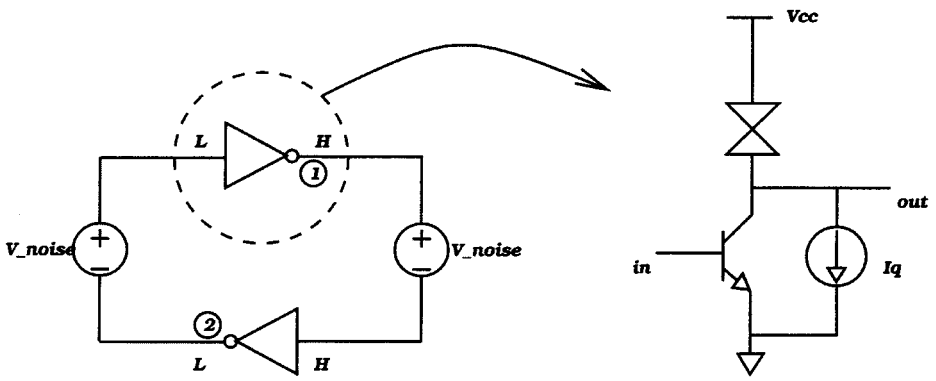


Fig. 8. Circuit for evaluating quiescent noise margin.

lines drawn with $V_{cc} < V_f$ will show us that the operating point after switching (from 1 to 0) has to be such that the transistor will be in saturation. From the above observation, it is clear that (19) cannot be used when $V_{cc} < V_f$.

Next, we present computer simulation results by taking into account the noise on the clock signal as described in Section IV. For this purpose, we use (27) to calculate the collector current of the transistor. In order to get accurate numerical results, we compute the coordinates $(x,\ y)$ using $I_H + \delta_I$ in place of I_H and $I_Q + \delta_I$ in place of I_Q and $(x',\ y')$ using $I_H - \delta_I$ in place of I_H and $I_Q - \delta_I$ in place of I_Q [Fig. 4(c)] in accordance with Table III. Thereafter, we calculate the noise margins as

$$\mathrm{NM}_H = y - x' \tag{28}$$

$$\mathrm{NM}_L = x - y'. \tag{29}$$

[It should be noted that (25) and (26) are approximate forms of the above two equations.]

Obviously, the noise on the clock line will have an effect of reducing the overall noise margin on the signal lines. Fig. 7 shows this effect. Interestingly, NM_L does not seem to be affected at all by the clock noise. This, in conjunction with the fact that NM_H decreases with increasing δ_I, tells us that the choice of I_H and I_Q should not be such that $\mathrm{NM}_H = \mathrm{NM}_L$. In fact, a robust design that can tolerate a larger amount of noise in the clock line, should have I_H and I_Q that make $\mathrm{NM}_H > \mathrm{NM}_L$.

VI. Noise Margins in the Quiescent State

The analysis presented in the previous sections are valid during the evaluation phase of the clock cycle. It was noted that the noise margins during gate switching can be increased by choosing the level of I_Q to be closer to the RTD's peak current (when $R_{p1} < R_{p2}$) or to its valley current (when $R_{p1} > R_{p2}$). However, it may seem that this type of biasing may be counter-productive in the quiescent phase of the clock cycle. During this phase, the gate is supposed to latch its state and not switch even if the inputs change. If we consider the case where $R_{p1} < R_{p2}$, it may seem that when I_Q is set close to I_p a small amount of signal noise can cause the gate whose output is high to flip to the low state. Thus, a study of the quiescent noise margins of the gate becomes important.

The best and the most accurate method of finding the noise margins of these types of gates would be to observe the behavior of a flip-flop circuit obtained by connecting two of these gates back to back. Lohstroh [17] has pointed out that in order to make accurate estimations of voltage noise margins for a gate whose input resistance is lower than its output resistance, it would be best to attach noise sources of appropriate polarities in the feedback paths of a flip-flop and increase their values till the flip-flop changes its state. In this section, we make an accurate evaluation of the quiescent state voltage noise margins of the RTD-HBT inverter using this technique. Fig. 8 shows the flip-flop circuit arrangement used for this purpose. Node 1 is at a high voltage while node 2 is low. The noise sources are initially at 0 V. They are gradually increased together till node 1 or node 2 changes state. The value of the noise sources at this point corresponds to the noise margin of the gate. Fig. 9 shows the load-line and voltage waveform for one such simulation.

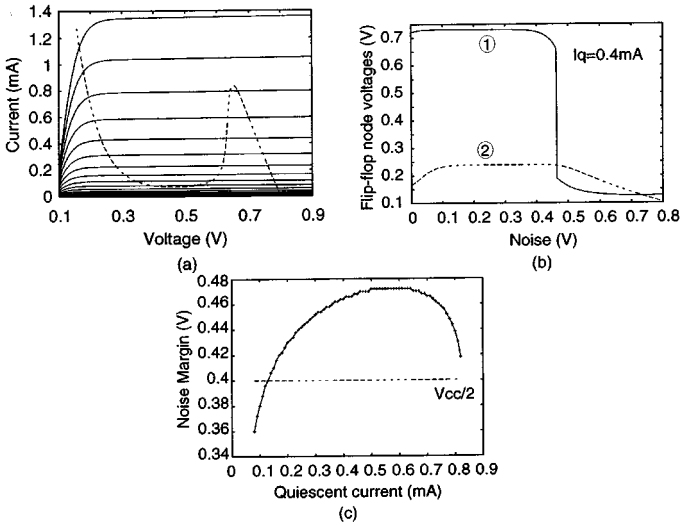


Fig. 9. (a) Load line of the inverter. (b) Noise induced node voltage flipping. (c) Noise margin as a function of I_q.

For simulating this circuit using SPICE, we used a very accurate physics-based RTD model [18] along with an HBT model. The noise margins were calculated for various values of I_Q for a particular RTD characteristic and then the peak current (I_p) of the RTD characteristic was also varied. The results are presented in Fig. 10.

Interestingly, we find that the noise margin increases as I_Q is increased and attains a maximum at a point close to the peak, before falling off again.

We see that the noise margins attained are quite high for a wide range of values of I_Q and the noise margins increase with higher peak current densities. The reason behind such high noise margins is the hysteretic nature of the RTD's current–voltage characteristics. To this extent, the RTD-HBT inverter is very similar to a Schmitt Trigger in its functionality. We know that the sum of the noise margins of a Schmit Trigger

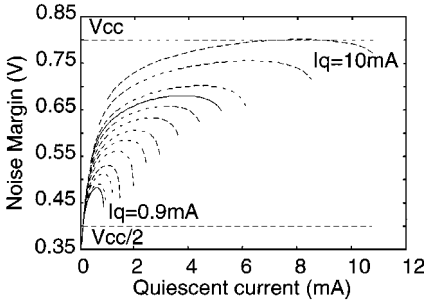


Fig. 10. Noise margins for different values of I_p and I_q.

can be more than its supply voltage [19]. In Fig. 10, we see that this property is true for RTD-HBT gates, and in fact, by designing RTDs with high peak currents, we can achieve very high individual quiescent noise margins (definitely more than $V_{cc}/2$).

VII. Conclusion

The noise margin evaluation procedure presented in this brief can be useful in the design of threshold gates using RTD. We have shown that an upper-bound on the sum of the noise margins $(\mathrm{NM}_H + \mathrm{NM}_L)$ that can be extracted from a given RTD, irrespective of the type of transistors used, can be obtained by using (15) and (16). Our analysis shows that the choice of the clock currents I_Q and I_H should be guided by (18), (19), (25), and (26), but the final choice should be made after computer simulations of the form presented in Section V. This is because, when the output is LOW, the transistors are in saturation and (27) is definitely superior to (10), which tends to overestimate NM_L. The analysis presented in this brief is for RTD threshold gate circuits with bipolar transistors as pull-down devices. Analysis of threshold gates for other types of transistors should be similarly performed. Since RTD circuits are meant to be used at ultra-high speeds, the sharp rising and falling edges of the clock and signal lines, coupled with the inductances associated with the interconnects will produce what is known as ΔI-noise. The analysis presented above should be adequate in taking these ringing effects into account.

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