Transactions Briefs

Noise Margins of Threshold Logic Gates Containing Resonant Tunneling Diodes

M. Bhattacharya and P. Mazumder

Abstract—Threshold gates consisting of resonant tunneling diodes (RTDs) in conjunction with HBTs or CHFETs or MOSFETs can form extremely compact, ultrafast, digital logic alternatives, and may be used for digital signal processing applications in the near future. The resonant tunneling phenomenon causes these circuits to exhibit super-high-speed switching capabilities. Additionally, by virtue of being threshold logic gates, they are guaranteed to be more compact than traditional digital logic circuits, while achieving the same functionality. However, reliable logic design with these gates will need a thorough understanding of their noise performance and power dissipation among other things. In this brief, we present an analytical study of the noise performance of these threshold gates supplemented by computer simulation results, with the objective of obtaining reliable circuit design guidelines.

Index Terms—Emerging technologies, noise margins, resonant tunneling diode, threshold logic.

I. INTRODUCTION

Nanoelectronic devices based on the resonant tunneling phenomenon are poised to make a major impact on integrated circuit technology [1]. Over the years, a wide variety of circuits consisting of resonant tunneling devices have been proposed in the literature [2]–[8], which have given us the reason to believe that compact ultra-high-speed integrated circuits based on these types of devices will be physically realized in the near future. More recently, several researchers have reported the development of multi-gigahertz digital circuits [9], [10]. From their projected performance, logic circuits composed of resonant tunneling diodes (RTDs) in conjunction with HBTs or MODFETs compare favorably with gates belonging to various other logic families (Table I).

Circuits containing resonant tunneling devices, such as threshold gates, literals [11], multiplexers [3], counters and MOBILE gates [12], [13], are not only faster than the conventional circuits, but they also use far less number of devices to achieve the same functionality (Table II).

Compared to the large number of published research papers dealing with the demonstration of RTD-based circuit operation and circuit ideas, work related to the analysis of such circuits seems to be very limited. This brief is a part of our continuing effort to fill that void.

II. RTD-HBT THRESHOLD LOGIC GATE

In this brief, we present a study of the noise immunity of a certain kind of RTD threshold gate whose circuit topology is shown in Fig. 1. This kind of circuit, proposed by Mohan et al. [6], can be tailored to function as an \( n \)-input \( m \)-threshold gate (\( m \)-threshold \( \Rightarrow \) output is low, if and only if \( m \) or more inputs are high). The number \( n \) is related to the number of transistors \( (n+1) \) and \( m \) is determined by the input signal levels. For example, for \( n = 3 \) and \( m = 2 \), we can have a 3-input inverted-MAJORITY (or, MINORITY) gate. Simulation results of such a gate working at 10-GHz clock speed is shown in Fig. 2. The layout diagram of this circuit is shown in Fig. 3. By virtue of the generic nature of this gate, it is our opinion that this type of RTD-HBT circuit may find wide application in the circuit in near future [14]. If the current drawn by each of the transistors \( Q_{1}, \ldots, Q_{n} \) in their ON states be \( I \) (assuming no transistor mismatch) and the current drawn by \( Q_{c,ih} \) be \( I_{II} \) (when Clock is HIGH) and \( I_{E} \) (when Clock is QUIESCENT), then for an \( m \)-threshold gate function, the following basic necessary conditions have to be satisfied:

\[
(m - 1)I + I_{E} < I_{P} \tag{1}
\]

\[
I_{E} < mI + I_{E,sh} < I_{P} \tag{2}
\]

\[
mI + I_{E,sh} > I_{P} \tag{3}
\]

III. MARGIN OF NOISE ON THE SIGNAL LINES

The noise margin measurement technique adopted in this work is based on the simple but accurate method of fitting a maximum area rectangle between the normal and mirrored transfer characteristics of an RTD-HBT inverter. This method has been shown to be by far the most general and precise method for characterizing noise margins [15],

If we consider the normal transfer characteristic of the RTD-HBT inverter [Fig. 4(a)], we see that Regions 1 and 3 are monotonically decreasing functions of \( V_{in} \), while Region 2 is an almost vertical drop. Region 2 is unique to the folded \( I - V \) characteristic of resonant tunneling devices which causes almost instantaneous switching of the output voltage, when the operating point skips over the unstable NDR region.

Important adjustments, however, are necessary in order to apply the above noise margin measurement philosophy to our circuit, simply because of the fact that this method is easy to apply to static digital gates, but is not applicable to clocked logic gates of the type we are currently concerned with. In RTD-HBT threshold gates, the clock voltage levels play an important role. While evaluating the inputs to a gate, the level

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The authors are with Department of Electrical Engineering and Computer Science, The University of Michigan, 2215 EECS, Ann Arbor, MI 48109-2122 USA (e-mail: mayukh@eecs.umich.edu). Publisher Item Identifier S 1057-7130(00)09327-7.
of the clock typically increases to \( V_{\text{H}} \) and after evaluation, this level decreases to a quiescent value of \( V_Q \). If we consider two such RTD-HBT inverters connected in series, for proper operation, the clocks to the two inverters have to be out of phase. That is, when the second gate is being evaluated by a high clock pulse, the clock to the previous gate has to be quiescent. Simply stated, the transfer characteristic should reflect the fact that the second inverter sees the output of the first inverter with the clock at \( V_Q \) and not at \( V_{\text{H}} \).

The folded \( I - V \) characteristic produces a sharp switching which can be regarded as a perfect vertical drop, for all practical purposes. Referring to Fig. 4(b), the maximum rectangle within the loop formed between the normal and the mirrored transfer characteristics will be \( A'B'C'D \). If one tries to fit a rectangle of the type of \( PQRS \), one can very soon realize that such a rectangle will almost always be smaller than \( A'B'C'D \) and in a special case, if \( PQRS > A'B'C'D \), \( PQRS \approx A'B'C'D \), since Regions 1 and 3 are almost horizontal. Thus \( A'B'C'D \) can be regarded as a good approximation of the maximum rectangle, in a general sense, within an area of the type \( ABCD \). If the coordinates of the point \( B \) be \((x, y)\) and that of point \( E \) be \((x', y')\), then the coordinates of the point \( D \) will be \( (y', x)\). Thus, the noise margins are simply expressed as

\[
\begin{align*}
NM_H &= y - x \\
NM_L &= x - y'.
\end{align*}
\]  

Therefore

\[
NM_H + NM_L = y - y'.
\]  

It is easily seen that

\[
x = V_T \ln \left( \frac{I_p - I_{\text{H}}}{I_p \left( 1 - e^{-\frac{(V_{\text{ce}} - V_p)/V_T}{}} \right)} \right)
\]

where \( V_T = kT/q \),

\[
y = (V_{\text{ce}} - V_p) + (I_{\text{H}} - I_Q)R_{p1}
\]

\[
y' = (V_{\text{ce}} - V_p) + (I_{\text{H}} - I_Q)R_{p2}.
\]

The symbols \( R_{p1}, R_{p2}, V_p, V_J \), etc., are explained with respect to the RTD’s \( I - V \) characteristics in Fig. 5. Equation (7) is based on the simple exponential relationship between a BJT’s collector current and its base voltage

\[
I_p = I_s \left( e^{\frac{V_{\text{BE}}}{V_T}} - e^{\frac{V_{\text{BC}}}{V_T}} \right).
\]

This relationship is not very accurate, and hence, provides approximate results. For computer simulation, we shall use a more accurate relationship based on the Gummel–Poon model of the bipolar transistor, but for the sake of deriving simple analytical noise margins, let us, for the moment, assume this relation. Equation (6) shows us that the sum of the two noise margins is independent of \( x \), and can be simply written as

\[
NM_H + NM_L = (V_J - V_p) + (I_{\text{H}} - I_Q)(R_{p1} - R_{p2}).
\]

Since

\[
R_{p2} = \frac{V_p - V_v}{I_p - I_v}
\]

and

\[
|R_{p1}| = \frac{V_p - V_v}{I_p - I_v}.
\]

Equation (11) can be rewritten as

\[
NM_H + NM_L = (R_{p2} + |R_{p1}|)(I_p - I_{\text{v}}) + (I_{\text{H}} - I_Q)(R_{p1} - R_{p2}).
\]

For proper operation of the gate, \( I_{\text{H}} < I_p \) and \( I_Q > I_v \), implying, \( I_{\text{H}} - I_Q < I_p - I_v \). Therefore, if \( R_{p1} \geq R_{p2} \)

\[
NM_H + NM_L < (R_{p2} + |R_{p1}|)(I_p - I_{\text{v}})
\]

or

\[
NM_H + NM_L < V_v \left( 1 - \frac{\text{PVVR}}{\text{PVCR}} \right)
\]

where PVVR = Peak to Valley Voltage Ratio = \( \frac{(V_{\text{v}})/(V_{\text{p}})}{1} \) and

\[
\text{PVCR} = \text{Peak to Valley Current Ratio} = \left( \frac{(I_p)}{(I_{\text{v}})} \right).
\]

On the other hand, if \( R_{p2} \geq R_{p1} \)

\[
NM_H + NM_L < (R_{p2} + |R_{p1}|)(I_p - I_{\text{v}})
\]

or

\[
NM_H + NM_L < V_p - V_{\text{v}}.
\]
noise margin that can be harnessed from a given RTD, while on the other hand, they can be used by the device engineers as a guideline for designing RTDs for digital logic applications. Diamond et al. [16] had shown that PVCR is not a crucial factor in determining RTD circuit switching speed. Their analysis had shown that $C/I_p$ (where $C$ is the RTD’s capacitance) is a much more important figure that can be directly related to switching time. However, (15) re-establishes, to a certain extent, the importance of PVCR so far as clocked RTD switching circuits are concerned. Furthermore, lower static power dissipation of such circuits is possible only when $I_p$ is low. Thus, ultimately, PVCR remains an important figure of merit for the RTD beyond merely indicating the quality of epitaxial growth. For RTDs with PVCR in the range of 10 to 20 and above, (15) reduces to

$$\text{NM}_{\text{in}} + \text{NM}_{\text{in}} < V_c.$$  

(17)

Using (10), we can write

$$\Delta V = V_T \ln \left( \frac{I_p - I_H}{I_p \left( 1 - e^{-\left( (V_{cc} - V_{pl}) / V_T \right)} \right)} \right).$$

Therefore, the individual noise margins are given by

$$\text{NM}_{\text{in}} = (V_{cc} - V_p) + (I_H - I_Q) R_{p1}$$

$$- V_T \ln \left( \frac{I_p - I_H}{I_p \left( 1 - e^{-\left( (V_{cc} - V_{pl}) / V_T \right)} \right)} \right).$$

(18)

Therefore, in order to have $\text{NM}_{\text{in}} = \text{NM}_{\text{in}}$, we should have

$$2V_T \ln \left( \frac{I_p - I_H}{I_p \left( 1 - e^{-\left( (V_{cc} - V_{pl}) / V_T \right)} \right)} \right)$$

$$= 2V_{cc} - (V_p + V_f) + (I_H - I_Q) (R_{p1} + R_{p2}).$$

(20)

The accuracy of (19) will be a subject of discussion in Section V.

IV. NOISE MARGIN WITH NOISE ON THE CLOCK SIGNAL

So far, we have dealt with the noise margin estimates on the signal line without considering any noise on the clock inputs. Noise on the clocks will definitely lower the previously estimated signal noise margins. In order to study the worst-case noise margins on the signal lines
by introducing noise on the clock lines, we shall follow the following procedure.

We shall assume that noise on the clock lines can cause \( \pm \delta_I \) fluctuations in the quiescent and high clock currents. That is, instead of a steady value of \( I_Q \), the quiescent clock can vary from \( I_Q - \delta_I \) to \( I_Q + \delta_I \). Similarly, the high clock current can vary from \( I_H - \delta_I \) to \( I_H + \delta_I \). We have to understand now how the three regions of the transfer characteristic will fluctuate with variations in the clock levels. Fig. 4(c) and Table III together provide the worst-case situations that will adversely affect the noise margins. Based on them, the shrinkage of the noise margins can be approximately characterized by (21)–(24) as follows:

\[
\Delta x_1 = V_T \ln \left( 1 + \frac{\delta_I}{I_p - I_H - \delta_I} \right) 
\]

\[
\Delta x_2 = V_T \ln \left( 1 + \frac{\delta_I}{I_p - I_H} \right) 
\]

\[
\Delta y_1 = \delta_I R_{p1} 
\]

\[
\Delta y_2 = \delta_I R_{p2} 
\]

Therefore, the modified noise margins are

\[
NM_H = (V_{cc} - V_p) + (I_H - I_Q - \delta_I) R_{p1} 
\]

\[
- V_T \ln \left( \frac{I_p - I_H + \delta_I}{I_p \left( 1 - e^{-(V_{cc} - V_p)/V_T} \right)} \right) 
\]

\[
NM_L = V_T \ln \left( \frac{I_p - I_H - \delta_I}{I_p \left( 1 - e^{-(V_{cc} - V_p)/V_T} \right)} \right) 
\]

\[
- (V_{cc} - V_f) - (I_H - I_Q + \delta_I) R_{p2} 
\]

V. COMPUTER SIMULATION RESULTS

For the purpose of obtaining a general idea about the effect of various RTD and transistor parameters and the choice of current values \( I_{H} \& I_{Q} \), the above equations should be sufficient. However, for accurate calculation of noise margins for a particular circuit, computer simulations seem to be the best approach. A computer simulation can handle the complex equations arising out of a detailed device model. For the RTD-HBT gate, we use the simple piecewise linear RTD model, but resort to the modified Gummel–Poon model of the bipolar transistor that is used in SPICE. Using an accurate model of the transistor is very essential, since the transistor plays a crucial role in determining the transfer function of these gates.
lines drawn with $V_{cc} < V_T$ will show us that the operating point after switching (from 1 to 0) has to be such that the transistor will be in saturation. From the above observation, it is clear that (19) cannot be used when $V_{cc} < V_T$.

Next, we present computer simulation results by taking into account the noise on the clock signal as described in Section IV. For this purpose, we use (27) to calculate the collector current of the transistor. In order to get accurate numerical results, we compute the coordinates $(x, y)$ using $I_{H1} + \delta_1$ in place of $I_{H1}$ and $I_{Q} + \delta_1$ in place of $I_{Q}$ and $(x', y')$ using $I_{H1} - \delta_1$ in place of $I_{H1}$ and $I_{Q} - \delta_1$ in place of $I_{Q}$ [Fig. 4(c)] in accordance with Table III. Thereafter, we calculate the noise margins as

$$\text{NM}_{H1} = y - x'$$
$$\text{NM}_{L} = x - y'. \tag{28}$$

[It should be noted that (25) and (26) are approximate forms of the above two equations.]

Obviously, the noise on the clock line will have an effect of reducing the overall noise margin on the signal lines. Fig. 7 shows this effect. Interestingly, $\text{NM}_{L}$ does not seem to be affected at all by the clock noise. This, in conjunction with the fact that $\text{NM}_{H1}$ decreases with increasing $\delta_1$, tells us that the choice of $I_{H1}$ and $I_{Q}$ should not be such that $\text{NM}_{H1} = \text{NM}_{L}$. In fact, a robust design that can tolerate a larger amount of noise in the clock line, should have $I_{H1}$ and $I_{Q}$ that make $\text{NM}_{H1} > \text{NM}_{L}$.

VI. NOISE MARGINS IN THE QUIESCENT STATE

The analysis presented in the previous sections are valid during the evaluation phase of the clock cycle. It was noted that the noise margins during gate switching can be increased by choosing the level of $I_{Q}$ to be closer to the RTD’s peak current (when $R_{v1} < R_{v2}$) or to its valley current (when $R_{v1} > R_{v2}$). However, it may seem that this type of biasing may be counter-productive in the quiescent phase of the clock cycle. During this phase, the gate is supposed to latch its state and not switch even if the inputs change. If we consider the case where $R_{v1} < R_{v2}$, it may seem that when $I_{Q}$ is set close to $I_{v}$ a small amount of signal noise can cause the gate whose output is high to flip to the low state. Thus, a study of the quiescent noise margins of the gate becomes important.

The best and the most accurate method of finding the noise margins of these types of gates would be to observe the behavior of a flip-flop circuit obtained by connecting two of these gates back to back. Lohstroh [17] has pointed out that in order to make accurate estimations of voltage noise margins for a gate whose input resistance is lower than its output resistance, it would be best to attach noise sources of appropriate polarities in the feedback paths of a flip-flop and increase their values till the flip-flop changes its state. In this section, we make an accurate evaluation of the quiescent state voltage noise margins of the RTD-HBT inverter using this technique. Fig. 8 shows the flip-flop circuit arrangement used for this purpose. Node 1 is at a high voltage while node 2 is low. The noise sources are initially at 0 V. They are gradually increased together till node 1 or node 2 changes state. The value of the noise sources at this point corresponds to the noise margin of the gate.

Fig. 9 shows the load-line and voltage waveform for one such simulation.

For simulating this circuit using SPICE, we used a very accurate physics-based RTD model [18] along with an HBT model. The noise margins were calculated for various values of $I_{Q}$ for a particular RTD characteristic and then the peak current ($I_{p}$) of the RTD characteristic was also varied. The results are presented in Fig. 10.

Interestingly, we find that the noise margin increases as $I_{Q}$ is increased and attains a maximum at a point close to the peak, before falling off again.

We see that the noise margins attained are quite high for a wide range of values of $I_{Q}$ and the noise margins increase with higher peak current densities. The reason behind such high noise margins is the hysteretic nature of the RTD’s current–voltage characteristics. To this extent, the RTD-HBT inverter is very similar to a Schmitt Trigger in its functionality. We know that the sum of the noise margins of a Schmit Trigger...
can be more than its supply voltage [19]. In Fig. 10, we see that this property is true for RTD-HBT gates, and in fact, by designing RTDs with high peak currents, we can achieve very high individual quiescent noise margins (definitely more than $V_{cc}/2$).

VII. CONCLUSION

The noise margin evaluation procedure presented in this brief can be useful in the design of threshold gates using RTD. We have shown that an upper-bound on the sum of the noise margins ($NM_{I_H} + NM_{I_L}$) that can be extracted from a given RTD, irrespective of the type of transistors used, can be obtained by using (15) and (16). Our analysis shows that the choice of the clock currents $I_{C2}$ and $I_{C1}$ should be guided by (18), (19), (25), and (26), but the final choice should be made after computer simulations of the form presented in Section V. This is because, when the output is LOW, the transistors are in saturation and (27) is definitely superior to (10), which tends to overestimate $NM_{I_L}$. The analysis presented in this brief is for RTD threshold gate circuits with bipolar transistors as pull-down devices. Analysis of threshold gates for other types of transistors should be similarly performed. Since RTD circuits are meant to be used at ultra-high speeds, the sharp rising and falling edges of the clock and signal lines, coupled with the inductances associated with the interconnects will produce what is known as $\Delta I$-noise. The analysis presented above should be adequate in taking these ringing effects into account.

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