CMOS Implementation of a Multiple-Valued Logic Signed-Digit Full Adder Based on Negative-Differential-Resistance Devices

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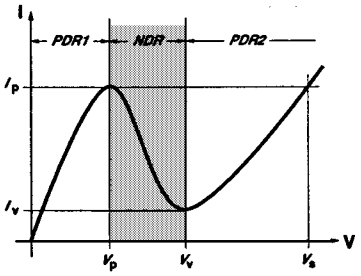
***Abstract*—This paper presents a fully integrated implementation of a multivalued-logic signed-digit full adder (SDFA) circuit using a standard 0.6-μm CMOS process. The radix-2 SDFA circuit, based on two-peak negative-differential-resistance (NDR) devices, has been implemented using MOS-NDR, a new prototyping technique for circuits that combine MOS transistors and NDR devices. In MOS-NDR, the folded current–voltage characteristics of NDR devices such as resonant-tunneling diodes (RTDs) are emulated using only nMOS transistors. The SDFA prototype has been fabricated and correct function has been verified. With an area of 123.75 by 38.7 μm^2 and a simulated propagation delay of 17 ns, the MOS-NDR prototype is more than 15 times smaller and slightly faster than the equivalent hybrid RTD–CMOS implementation.**

***Index Terms*—CMOS, multiple-valued logic, negative differential resistance, negative resistance, quantum electronics, resonant-tunneling diode, RTD.**

I. Introduction

THE signed-digit number system [1] can be used in adder circuits to eliminate carry propagation by removing the dependency of the carry output function on the carry input signal. To restrict carry propagation, these number systems employ redundant representation, in which a number different from zero can be expressed in more than one way. In signed-digit adders, it is possible to perform addition of two arbitrary size numbers in constant time. Redundant algorithms can therefore help to significantly improve arithmetic circuit performance in applications with large operand sizes. In contrast, conventional ripple-carry adders have worst-case propagation delays which are proportional to the number n of digits involved in the operation. Even though alternative approaches such as carry look-ahead can reduce the propagation delay to $O(\log n)$ time, the improvement is achieved at the expense of additional circuits that cause irregularity in chip layout and make the adder circuit less amenable to comprehensive testing. Signed-digit systems have been adopted in the development of experimental high-performance arithmetic circuits [2]–[5], but signed-digit adders are difficult to implement in compact circuits with conventional device technologies due to the multivalued nature of signed digits.



Symbol	Parameter
V_p	Peak Voltage
I_p	Peak Current
V_v	Valley Voltage
I_v	Valley Current
V_s	Second Voltage

Fig. 1. I–V characteristic of an RTD.

Scaling provides diminishing returns in performance improvement of field-effect devices as dimensions in integrated circuits shrink to deep-submicron levels. At the same time, quantum effects such as resonant tunneling arise which result in interesting new device characteristics that can be exploited in the creation of extremely fast and compact circuits [6]. Among the host of quantum technologies, resonant-tunneling diodes (RTDs) [7] are the most promising and appear to be imminently viable for commercial introduction. A typical current–voltage curve of an RTD is shown in Fig. 1. This curve is described by its peak and valley voltages, $V_{\rm p}$ and $V_{\rm v}$, by the peak and valley currents, $I_{\rm p}$ and $I_{\rm v}$, and by the second voltage $V_{\rm s}$. Two positive-differential-resistance regions, PDR1 and PDR2, and a negative-differential-resistance region, NDR, are distinguished in the RTD I–V curve. Two or more RTDs can be stacked in series to obtain a multipeak current–voltage characteristic. Since one stable operating point can be associated with each PDR region, multipeak RTDs are extremely useful in the implementation of multiple-valued logic circuits. Multivalued logic (MVL) can help alleviate critically limiting problems of interconnect complexity that are arising in VLSI and ULSI chips. This is possible because multivalued signals convey more information than binary signals, thus requiring fewer interconnects to transmit similar bandwidth of information [8], [9].

It is very attractive to envision circuits which combine the advantages of resonant-tunneling diodes with the features of a technology like CMOS, which offers low power dissipation and very large integration levels. Recently, it has been reported [10]–[12] that it may be possible to achieve resonant tunneling

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TABLE I
COMPARISON OF ADDITION TECHNIQUES

	QMOS (from [14])	Binary Full Adder (generic)
Area (μm^2)	297×92	132×92
Delay (ns)	3.5	S:3.23, C_o:1.85

using, for example, a Si/SiO_2 heterostructure. Thus far, however, silicon-based RTD technology has not matured to the level at which RTD–CMOS circuits can be reliably fabricated to validate these circuit ideas.

This paper presents a multiple-valued logic signed-digit full adder (SDFA) circuit based on NDR devices such as resonant-tunneling diodes [13]. The operating principle of the proposed SDFA circuit has been presented in [14]. In Table I, the SDFA full adder is compared to a conventional binary full adder in terms of speed and circuit area. The *QMOS* column gives the area and simulated delay of a quantum-MOS implementation of the SDFA cell. In quantum-MOS, the efficient cointegration of resonant-tunneling diodes and MOS transistors is assumed to be possible. The delay of the QMOS implementation was reported in [14], and it was obtained using parameters of a 2-μm CMOS process. The column labeled *Binary Full Adder* includes information for a generic full adder cell, also designed in the same 2-μm CMOS process used for the SDFA implementation of [14]. The figures included in Table I indicate that it will take an operand size of just two digits to produce similar worst-case propagation delay values for a QMOS parallel adder based on SDFA cells and a CMOS ripple-carry adder built with binary full adder cells. This indicates that the SDFA can provide significant speedup of addition for multibit adders since addition of operands of any length can be accomplished in the time required for a 2-bit binary addition.

The novelty of this work is in the application of a new prototyping technique [15] that has been proposed recently. This new technique, which is based on the idea of reproducing the I–V characteristics of RTDs using only MOS devices, is simple and inexpensive, and can lead to the prototyping of RTD–CMOS circuits without the severe limitations of other methods such as:

1) large area overhead;
2) inability to integrate large-scale NDR circuits;
3) poor switching speeds;
4) increased design turnaround time;
5) increased process complexity;
6) increased cost.

The advantages of this prototyping technique in implementing multiple-valued logic circuits is demonstrated via the development of a fully integrated SDFA circuit prototype [13]. In [14], the CMOS portion of the RTD-based SDFA circuit was fabricated using a standard process and discrete external resonant-tunneling diodes were electrically connected to the chip. This approach inserts parasitic circuit elements of such significance that useful measurements of performance parameters, such as speed or power consumption, are completely impeded. A second, and perhaps more sophisticated, approach reported in the literature [16], [17] involves fabricating the RTDs on a III–V substrate and then, by means of a thin-film transfer and bonding procedure, grafting the RTDs onto a silicon substrate where the CMOS portion of the circuit has been prefabricated. However, as is justified in Section V, the hybrid RTD–CMOS integration process is disadvantageous for prototyping NDR circuits.

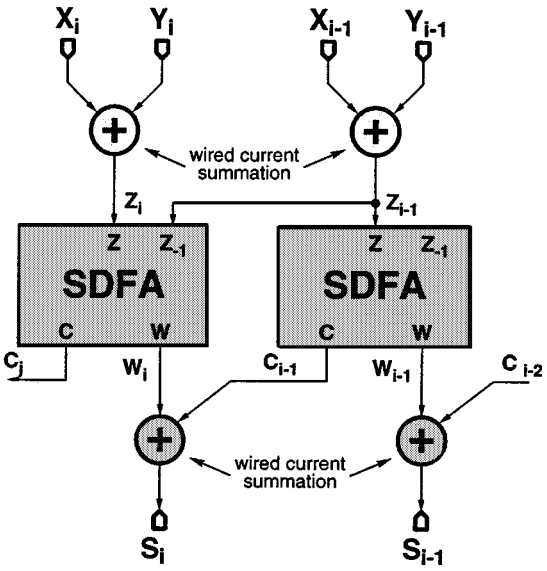


Fig. 2. Scheme for parallel addition using the signed-digit full adder (SDFA) cell.

The rest of this paper is organized as follows. Section II describes the principle of operation of the proposed signed-digit adder circuit. In Section III, the nMOS-based NDR circuit is described. The adder prototype implementation is discussed in Section IV. Finally, Sections V and VI present results and conclusions, respectively.

II. SIGNED-DIGIT ADDER OPERATION

This section presents a brief description of the SDFA circuit operating principle. For a detailed description, the reader is referred to [14].

Fig. 2 shows the connection of the SDFA cell as a building block in a parallel adder. Signals x_i, y_i, c_i, w_i, and s_i are three-valued current signals. The addition $z_i = x_i + y_i$ is obtained by simple wired summation of currents. The SDFA block generates a two-digit representation (w, c) of input signal z such that $rc + w = z$, where $r = 2$ is the radix of the number system. The final sum output $s_i = w_i + c_I$ is also generated through wired current summation. This scheme implements a *modified signed-digit* arithmetic [1]. It is observed in Fig. 2 that the SDFA block has an input z_{-1} that is connected to the wired summation result z of the adjacent less significant digit slice. The use of input z_{-1} is explained below.

For correct operation, output functions w and c must be defined so that they always represent the arithmetic value $z = x + y$ as defined in the preceding paragraph. A definition of the SDFA output functions which meets this requirement is shown in Fig. 3. Notice that there are two pairs of output functions. The active pair is determined by the value of z_{-1}. Each SDFA cell in the parallel system must determine if the adjacent cell is generating a carry output $c = -1$ or $c = 1$ in order to know

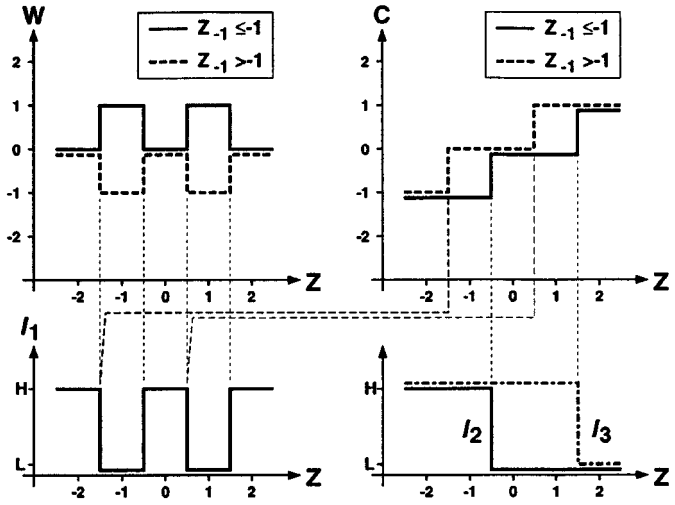


Fig. 3. SDFA block output functions and their description by means of three literal signals l_1, l_2, and l_3.

the range of values it is allowed to generate for its interim sum output, w. Since the sum result s_i is generated by the wired current summation $w_i + c_{i-1}$ and $s, w, c \in \{-1, 0, 1\}$, w_i must not be equal to -1 or 1 when c_{i-1} is equal to -1 or 1, respectively. This scheme is enabled by the redundancy of the number system, and it eliminates carry propagation by making c_i independent of c_{i-1}.

Consider the following example of an addition performed by the system shown in Fig. 2. The allowed values for the digits represented in the diagram are

$$x_i, y_i, w_i, c_i, s_i \in \{\overline{1}, 0, 1\}$$
$$z_i \in \{\overline{2}, \overline{1}, 0, 1, 2\}.$$

Digits with negative values are identified with a bar above the integer. Assume that the inputs applied to the system have the values $[x_i, x_{i-1}] = \overline{1}1$, $[y_i, y_{i-1}] = \overline{1}0$. The algebraic values of the applied inputs then are $X = -1, Y = -2$. From Figs. 2 and 3, the addition procedure is

augend x:	$\overline{1}\ \ 1$
addend y:	$\overline{1}\ \ 0$
wired sum z:	$\overline{2}\ \ 1$
interim sum w:	$0\ \ 1$
carry c:	$\overline{1}\ \ 0\ \ 0$
wired sum s:	$0\ \ 1.$

The resulting sum is $[c_i, s_i, s_{i-1}] = \overline{1}01$, which has the algebraic value $S = -4 + 1 = -3 = X + Y$.

As seen in Fig. 3, literals l_1, l_2, and l_3 include all the multivalued logic switching thresholds contained in functions w and c. This set of literal signals can thus be used to control switched current sources to synthesize the SDFA output functions, as is explained in Section IV. Generating literals l_2 and l_3 is relatively easy, since each of them contains only one threshold point. Literal l_1, on the other hand, contains four threshold points, which makes its implementation the task of greatest complexity in the adder cell. It is possible, however, to generate function l_1 with a compact circuit based on resonant-tunneling diodes. The proposed design, shown in Fig. 4, consists of the series connection of a resistor, R_s, and a two-peak RTD . Two single-peak RTDs are connected in series to generate the required two-peak I–V characteristics. The input of the circuit is voltage V_z, which is proportional to the current sum $z = x + y$. The voltage comparator senses and digitizes V_A, the voltage at node A, and isolates node A from the rest of the adder cell.

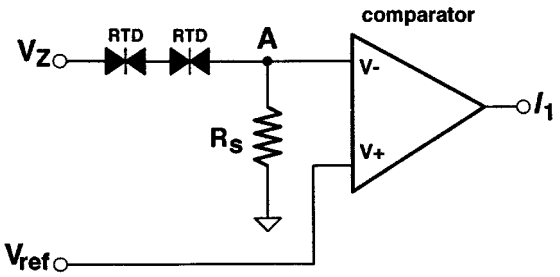


Fig. 4. Compact circuit for implementing literal l_1.

The behavior of V_A with respect to V_z can be described using the load-line method. In Fig. 5(a), the RTD and resistor currents are plotted with respect to V_A. In the figure, the RTD characteristics are represented by a piecewise linear model. Since the voltage applied across the RTD is $V_z - V_A$, the RTD current curve is mirrored along the I axis and its position along the V axis is determined by the value of V_z. The bias current is always found at the intersection of the two I–V curves. Assuming that most of the bias current flows through resistor R_s, V_A is proportional to this current and its transfer characteristic with respect to V_z is as shown in Fig. 5(b). Given an adequate value for the reference voltage $V_{\rm ref}$, the voltage comparator generates literal l_1 by digitizing V_A as shown in the figure.

To select the value of resistance R_s, the I–V characteristics of the NDR elements have to be taken into account. It was proven in [14] that R_S should be as close as possible to the absolute value of the negative differential resistance of the NDR element, $R_n = (V_v - V_p)/(I_p - I_v)$, in order to maximize the swing of voltage V_A. Other aspects that play a role in the tradeoff for selecting R_s are the delay of signal V_A with respect to input V_Z and the desired input resistance of the adder circuit [14].

III. NMOS-Based NDR Circuits

In the signed-digit adder implementation presented in this work, RTDs are emulated by a configuration of four nMOS transistors which exhibits negative differential resistance. This configuration, which is studied in detail in [15], is referred to as *MOS-NDR circuit* in the rest of this paper. The following paragraphs give an overview of the MOS-NDR circuit operation and the corresponding transistor sizing for the intended SDFA design.

The MOS-NDR circuit used in this work is shown in Fig. 6. This circuit was derived from a Λ-type topology described in [18]. Transistor MD has been added to model the PDR2 region of the RTD characteristics. As in other NDR-producing FET circuits, Transistor $MT2$ needs to be taken from cutoff to saturation and then back to cutoff as the voltage applied between

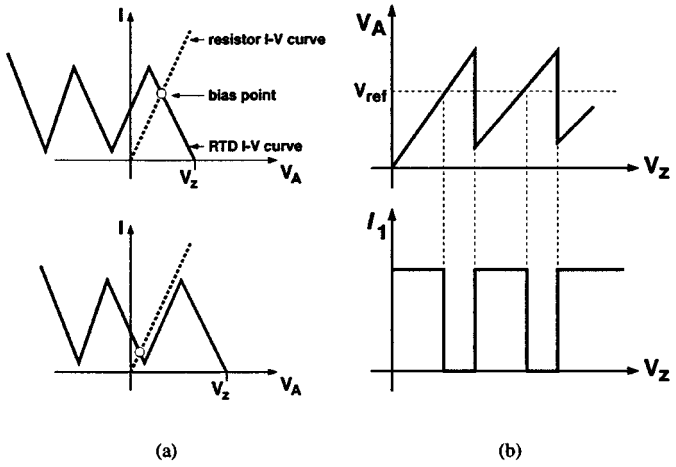


Fig. 5. (a) The load-line method is used to describe the behavior of the voltage at node A. (b) Generation of literal l_1 by comparison of voltage V_A to reference voltage $V_{\rm ref}$.

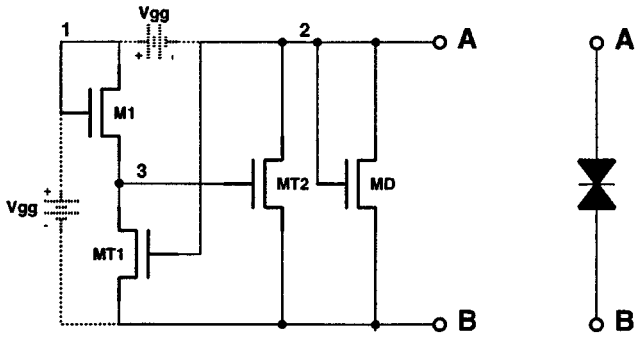


Fig. 6. The four-transistor MOS-NDR circuit emulates the RTD I–V characteristics. Two possible ways of applying V_{gg} are shown.

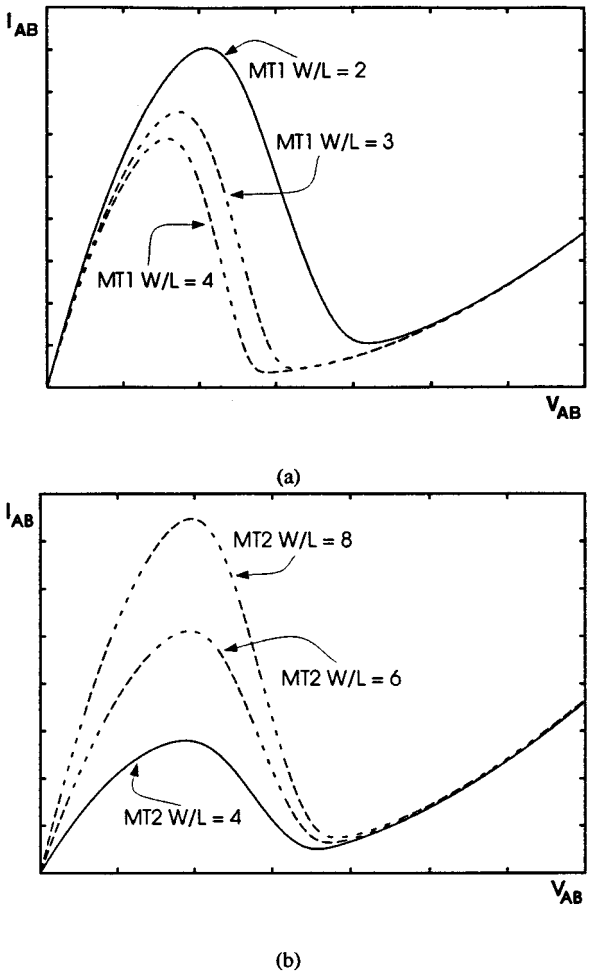


Fig. 7. Simulation results showing the effect of varying W/L of (a) $MT1$ and (b) $MT2$ while holding V_{gg} constant.

nodes A and B increases. To achieve this, the voltage at the gate of $MT2$ has to decrease as the applied voltage increases, which is made possible by connecting the gate of $MT2$ to the output of the inverter formed by $M1$ and $MT1$. It is to be noted that the bias voltage for the inverter can be applied at any one of the two positions shown in Fig. 6.

Fig. 7 shows the simulated variation in the current–voltage characteristics between terminals A and B of the MOS-NDR circuit as the sizes of Transistors $MT1$ and $MT2$ are changed. If the W/L ratio of $MT1$ is increased, V_2 decreases faster as V_1 rises, and hence the NDR region occurs at a lower voltage reducing both $V_{\rm p}$ and $I_{\rm p}$. This is shown in Fig. 7(a). When $MT2$ is made wider, the drawn current increases, causing $I_{\rm p}$ to increase while $V_{\rm p}$ remains the same, as shown in Fig. 7(b).

Even though device and process engineers describe an RTD by means of its peak-to-valley current ratio (PVCR) and peak current density (PCD), circuit designers are usually concerned with the five parameters $V_{\rm p}$, $I_{\rm p}$, $V_{\rm v}$, $I_{\rm v}$, and $V_{\rm s}$ when it comes to designing an RTD-based digital circuit. It is therefore important that the MOS-NDR circuit can be sized to generate an I–V curve which has the same, or approximately the same, five parameter values.

To find the best transistor sizing in the MOS-NDR circuit such that a given RTD characteristic is emulated, the following methodology is used. First, hand calculations are performed to derive approximate transistor sizes for achieving the peak region specifications. Using SPICE simulation, it is then verified if the resulting circuit produces approximately an RTD-like characteristic with a significant NDR region. Next, starting from the hand-calculated sizes, a circuit optimization tool is used to find the optimal values of the transistor sizes that would give the best possible fit for the target current and voltage values. The tool that has been used for this purpose is CUMIN [19], which is a SPICE-based flexible direct-search optimization software in which any arbitrary cost-function can be defined very easily. The following cost function has been defined and used in sizing the MOS-NDR circuit:

$$\text{Cost} = \left|\frac{\widehat{I_{\rm p}} - I_{\rm p}}{I_{\rm p}}\right| + \left|\frac{\widehat{I_{\rm v}} - I_{\rm v}}{I_{\rm v}}\right| + \left|\frac{\widehat{V_{\rm p}} - V_{\rm p}}{V_{\rm p}}\right| + \left|\frac{\widehat{V_{\rm v}} - V_{\rm v}}{V_{\rm v}}\right| + \left|\frac{\widehat{I_{\rm s}} - I_{\rm p}}{I_{\rm p}}\right|$$

where variables with a caret represent the values corresponding to a particular circuit.

Using the method described above and the current–voltage characteristics required for the SDFA circuit, an optimal sizing for the MOS-NDR circuit was obtained. The optimization was carried out using the 0.6-μm MOSIS CMOS process parameters, where the specified zero-bias threshold voltages for N and

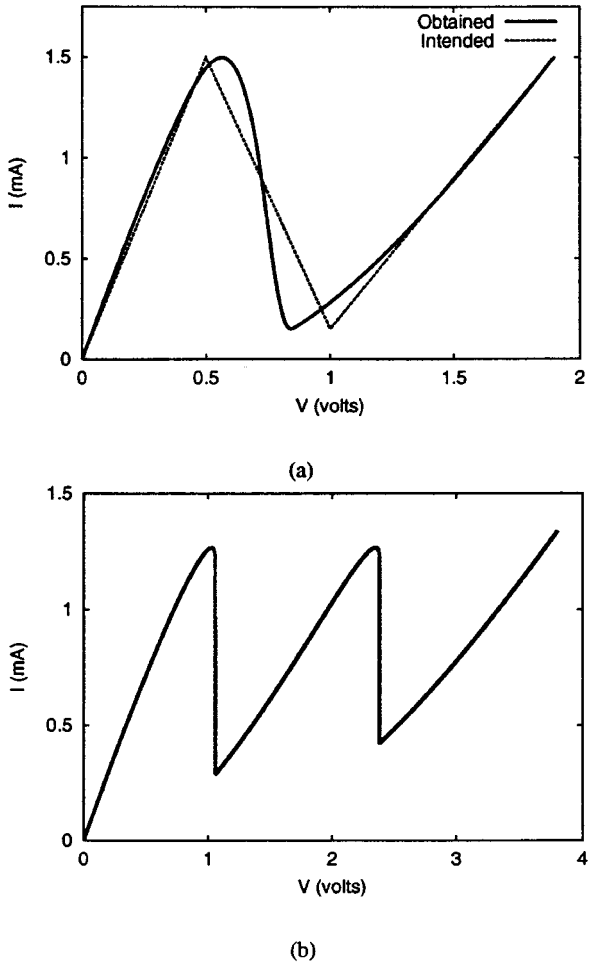


Fig. 8. (a) Simulated I–V characteristics of the sized NDR circuit. (b) Two-peak current–voltage characteristics of two MOS-NDR circuits connected in series with applied V_{gg} of 4 and 4.25 V.

P devices are, respectively, $V_{TN0} = 0.5$ V and $V_{TP0} = -0.5$ V. The resulting sizes are presented in Table II, and Fig. 8(a) shows the simulated I–V characteristics of the optimized circuit with $V_{gg} = 5.71$ V. Notice that the obtained current–voltage characteristics (solid line) and the intended characteristics (dotted line) are very similar. Since a two-peak I–V curve is required in the SDFA cell, two instances of the MOS-NDR circuit are connected in series, as is done with actual RTDs when a multipeak characteristic is needed. The ability of the MOS-NDR circuit to produce multipeak characteristics was verified, as shown in Fig. 8(b).

The fast switching speeds of the RTDs in conjunction with their bistable nature can be utilized to design several types of logic styles [20]. Such logic styles could potentially lead to compact high-performance digital circuits and systems. For instance, binary logic styles using RTD–CMOS combination have been explored and system application of such building blocks has been evaluated [21]. The MOS-NDR prototyping method used in the research presented in this paper has recently been successfully applied to the emulation of such binary QMOS logic gates [15]. Other types of logic styles using RTDs could similarly be redesigned using the method presented here. Incidentally, digital logic circuits are not the only beneficiaries of the NDR characteristics of devices such as RTDs. It has been shown that NDR circuits can be useful in low-loss inductor design. Such techniques are common in CMOS RF circuit design (for example, [22]). The applicability of our current method to such cases is beyond the scope of this paper.

TABLE II
MOS-NDR OPTIMIZATION RESULTS

Transistor	Gate Width (microns)	Gate Length (microns)
MT1	5.93	0.6
MT2	9.23	0.6
M1	0.9	5.45
M2	10.45	0.6

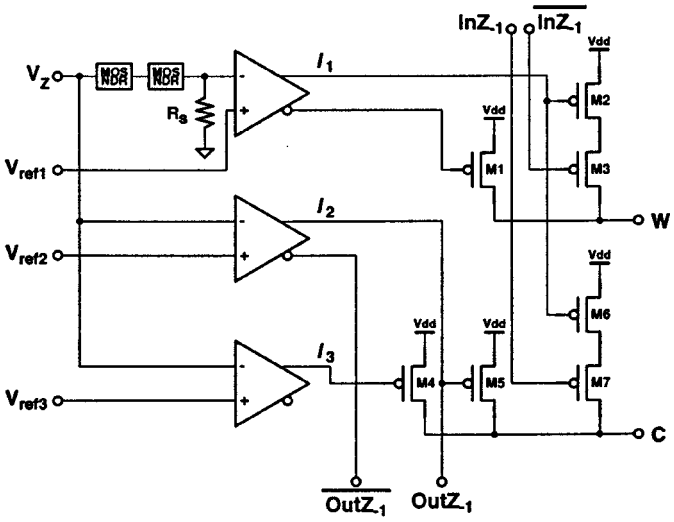


Fig. 9. SDFA cell circuit schematic diagram.

IV. CIRCUIT IMPLEMENTATION

If literals l_1, l_2, and l_3, shown in Fig. 3, are available, it is relatively easy to generate the w and c SDFA output functions by means of switched current sources. This idea is used in the signed-digit adder cell circuit shown in Fig. 9.

Three voltage comparators, one for each literal, are used in the circuit. The generation of l_1 by means of two NDR circuits, a resistor, and a voltage comparator has been discussed in Section II. Literals l_2 and l_3 can be implemented by threshold detection circuits using voltage comparators. The threshold levels of these circuits match the switching points of output function c when $z_{-1} \leq -1$. The reference voltages for the comparators are primary inputs of the chip for greater prototype flexibility, but it will not be difficult to generate the threshold levels internally once the technology is fully developed.

The voltage comparator used in this prototype consists of a simple source-coupled differential pair, a current-mirror pull-up configuration, and three static CMOS inverters in the output stage. The purpose of the output inverters is to provide signal buffering and to generate the complements of the literals as well as their true values. Availability of the literal signals and their complements allows the use of a single type of transistors in the circuitry which generates current output signals w and c.

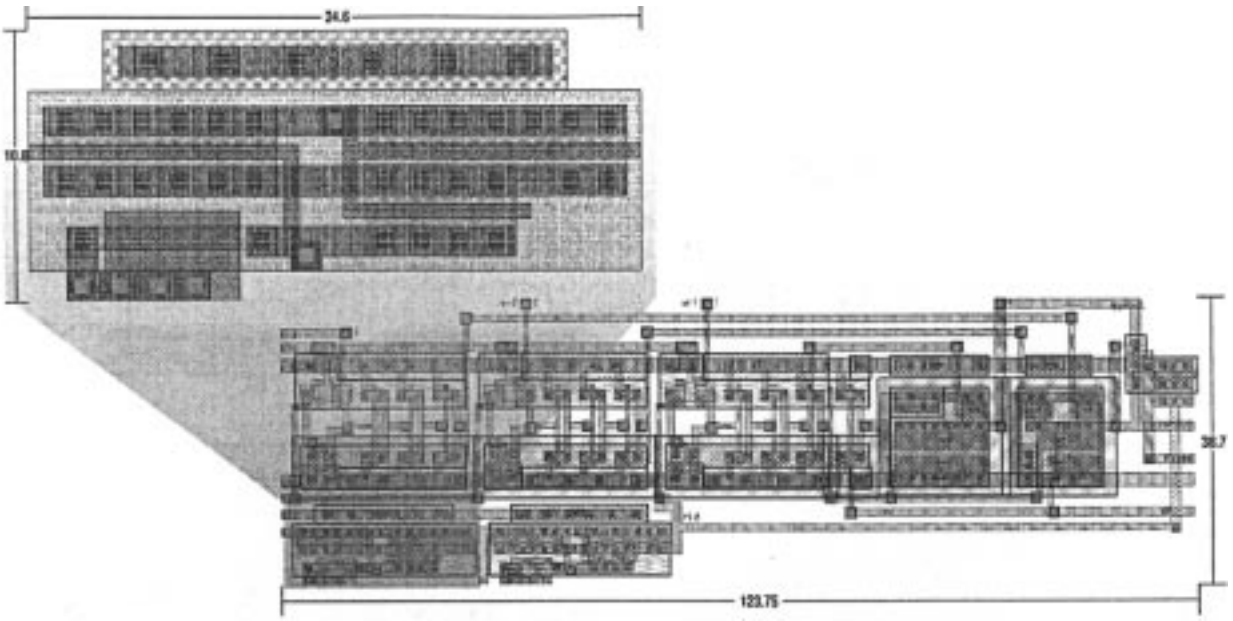


Fig. 10. SDFA cell layout for a 0.6-μm process. The expanded block corresponds to the MOS-NDR subcircuit. Dimensions are noted in micrometers.

Output currents w and c are generated by means of transistors $M1$ through $M7$, seen in Fig. 9, as follows. Output function w requires only three MOS transistors. This part of the circuit is simple due to the similarity between function w and literal l_1. Transistor $M1$ injects a current equivalent to one logic level when l_1 is high. These states correspond to $z \in \{-2, 0, 2\}$ in the transfer function shown in Fig. 3. States $z \in \{-1, 1\}$ are handled by transistors $M2$ and $M3$, which inject a current equivalent to two logic levels or no current at all, depending upon the value of z_{-1}. In the portion of the circuit corresponding to output c, transistors $M4$ and $M5$ produce the basic stairway form of the carry function for $z_{-1} \leq -1$. Transistors $M6$ and $M7$ ensure that the correct output current levels for signal c are produced when $z_{-1} > -1$. This is achieved by injecting a current equivalent to one logic level at the operating points where output c is affected by the value of z_{-1}, that is, at $z \in \{-1, 1\}$. In the circuit diagram of Fig. 9, $\mathrm{In}Z_{-1}$ is a binary signal which indicates if $z_{-1} < -1$. To our advantage, the behavior of $\mathrm{In}Z_{-1}$ is identical to that of literal l_2, as seen in Fig. 3. For this reason, output $\mathrm{Out}Z_{-1}$ is taken directly from the second comparator of the SDFA circuit. In a parallel signed-digit adder, ports $\mathrm{Out}Z_{-1}$ and $\mathrm{In}Z_{-1}$ of contiguous stages are connected together. Notice, however, that a carry propagation chain is not formed, since at each stage $\mathrm{Out}Z_{-1}$ is not a function of $\mathrm{In}Z_{-1}$.

Layout for the circuit shown in Fig. 9 has been designed and fabricated using a standard 0.6-μm CMOS process technology. The resulting layout is presented in Fig. 10, which also shows an expanded closeup view of the MOS-NDR subcircuit. Fig. 11 shows a chip microphotograph of the fabricated circuit. The SDFA layout occupies an area of 4789.125 μm^2. Of this area, only 531.36 μm^2 (11.1%) is used by the two MOS-NDR subcircuits. The layout shown in Fig. 10 includes the resistor R_s and two output load resistors implemented by MOS transistors biased as active load elements. The two output load resistors act as transducers which permit easy observation of output currents w and c by means of simple voltage measurements.

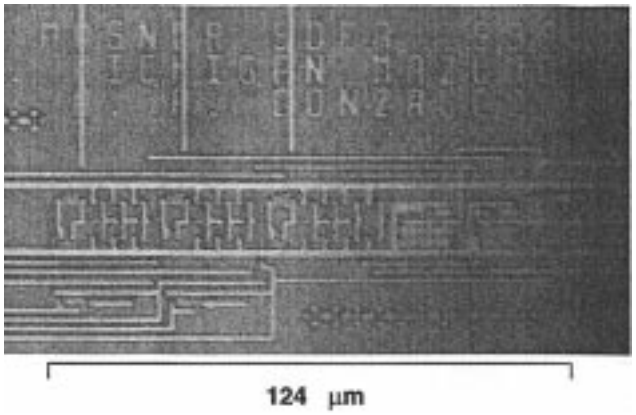


Fig. 11. Chip microphotograph of fabricated signed-digit adder prototype.

V. Results and Discussion

Functionality of the signed-digit adder prototype has been verified through experimental measurements. Fig. 12 presents oscilloscope traces which confirm correct operation of the SDFA cell. As seen in the figure, measurements were made for the two possible values of the condition z_{-1} versus -1. The measured dc transfer characteristics are in good agreement with the intended output functions, seen in Fig. 3. However, there exists a noticeable difference in the logic levels of the measured output signals and the desired functions. For example, while the difference between levels -1 and 0 of voltage V_w is around 300 mV, the swing between levels 0 and $+1$ is 450 mV. This peculiarity arises because the output signal is measured in the prototype by converting the output currents into voltages by means of on-chip active loads. It is necessary to point out that the x axis of the signal traces shown in Fig. 12 describes input voltage V_z, but in oscilloscope traces the x axis usually corresponds to time. To carry out this measurement, the input signal had to be ramped with an extremely low slow rate. It was possible, in this way, to confidently arrange the traces as

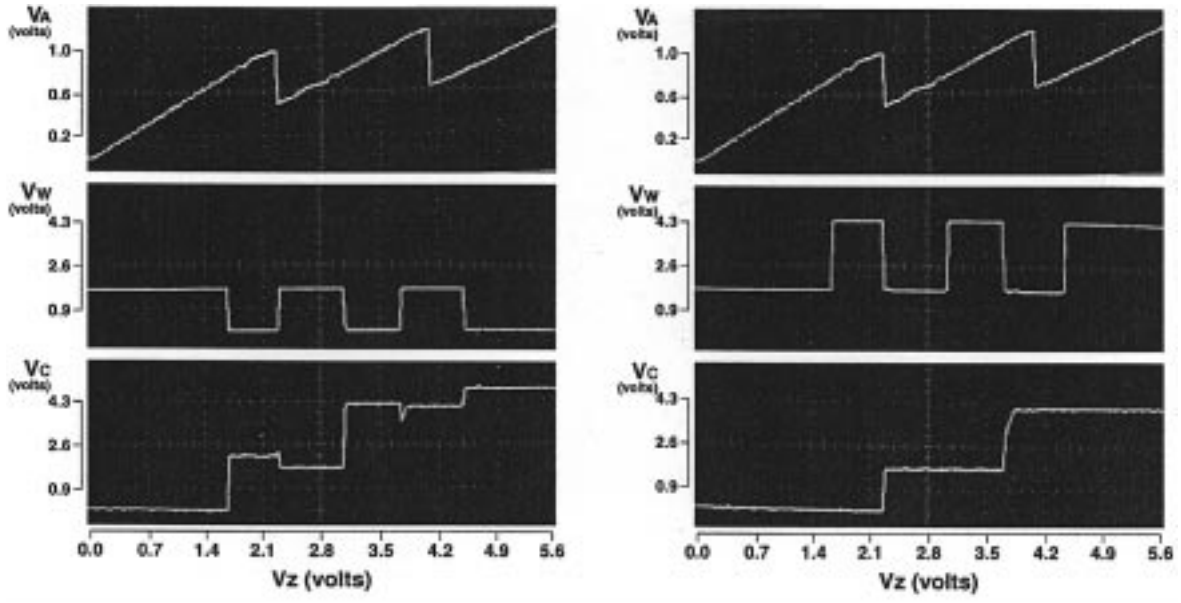


Fig. 12. Measured results at low speed showing the transfer characteristics of the SDFA cell. (a) $InZ_1 = L$. (b) $InZ_1 = H$.

dc transfer curves. This measurement is useful in determining the voltage levels, 1.3, 2.0, 2.7, 3.4, and 4.1 V, of input signal V_z which correspond to logic levels "−2" through "+2," respectively.

A good estimate of speed performance for the adder circuit can be obtained from computer-aided circuit simulation. In order to make this estimate as accurate as possible, the simulation model includes parasitic elements introduced by the interconnecting wires. The estimated worst-case delay for the circuit is 17 ns, and it is for the transition of input V_z from logic level "+1" to level "+2", that is, from 3.4 to 4.1 V. Note that this delay corresponds to the intrinsic circuit performance, since in the experiment the circuit drives no additional output load besides the layout parasitic capacitances and the capacitances of the circuit transistors. Fig. 13 shows oscilloscope traces corresponding to an experiment which was carried out to measure the propagation delay of the SDFA prototype circuit. The experimentally measured delay—1.4 μs—is much higher than the delay estimated by simulation. This large delay is caused by the fact that the SDFA circuits produce weak multivalued voltage signals since the output currents are converted to voltages by means of active loads working as transducers. These weak signals, in turn, have to drive the large chip output pads and the load presented by the inputs of the measurement instrument (oscilloscope). Moreover, the experimental setup was not designed for precise measurements of high-speed parameters and, hence, additional parasitics and delays that cannot be included in the simulation model may be present.

Table III presents a comparison of three implementations of identical SDFA circuits. The first column includes the layout, circuit area, and worst-case delay of a hybrid RTD–CMOS prototype, the second column contains similar information for the MOS-NDR implementation, and the third column presents a QMOS SDFA that assumes viable RTD-MOS cointegration. The worst-case delay in all columns was obtained by computer-aided simulation of circuits extracted from the layout geometries, including parasitic capacitances. In the table, the circuit layout images are drawn to scale and all implementations are based on the same 0.6-μm process technology. As was explained earlier in the paper, the hybrid RTD–CMOS technique consists of fabricating the RTDs on a III–V substrate and then grafting the RTDs onto the Silicon substrate containing the prefabricated CMOS portion of the circuit. As shown in Table III, the circuit area of the hybrid RTD–CMOS prototype is more than 15 times that of the MOS-NDR implementation due to the enormous size of the RTD landing area and its bonding pads as compared to the area of the CMOS circuitry. Also shown in Table III is the fact that the worst-case propagation delay of the MOS-NDR SDFA is comparable to that of the hybrid RTD–CMOS prototype while it uses a significantly smaller area.

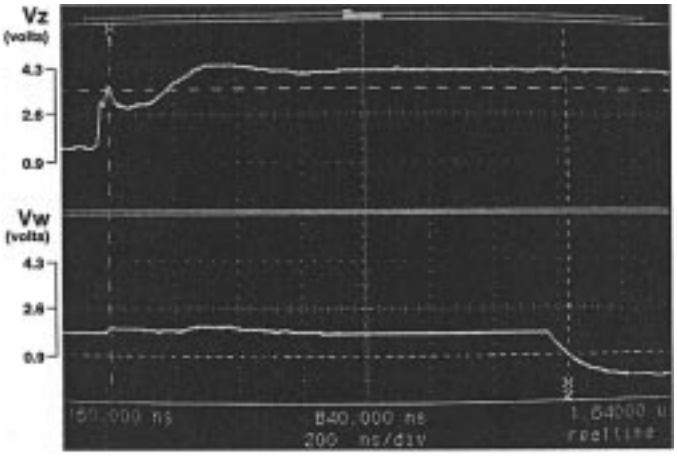
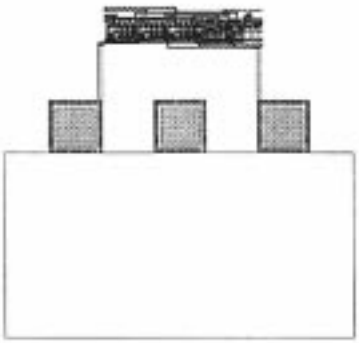


Fig. 13. Measurement of worst case gate delay, including delay of the chip pads.

The MOS-NDR approach is a prototyping technique that allows efficient verification of circuit concepts based on NDR

TABLE III
SDFA PROTOTYPE COMPARISON

	Hybrid RTD-CMOS	MOS-NDR	QMOS
Layout			
Area (μm^2)	282 × 267.15	123.75 × 38.7	123.75 × 30.6
Delay (ns)	19	17	4

devices. MOS-NDR is not intended as the final realization of a given design. Instead, projected figures for the intended RTD-MOS circuit more accurately reflect the potential of NDR circuits assuming a viable process technology. It should be noted that as compared to the result presented in Table I, the delay value of the QMOS SDFA reported in Table III is larger since the circuits compared in Table III utilize voltage comparators for literal generation instead of the faster threshold-modified inverters used in [14]. Comparators are used in this design to allow for variations in the post-fabrication I–V characteristics of the MOS-NDR circuits. These variations may occur because of nonavailability, at the time of design, of binned SPICE device models that can very accurately model transistors with widely varying W/L-ratios such as those used in the MOS-NDR circuits.

VI. CONCLUSION

The implementation of a signed-digit full adder circuit based on NDR devices has been presented. The SDFA circuit prototype takes advantage of MOS-NDR, a new prototyping technique proposed in [15]. The MOS-NDR technique enabled the design and fabrication of a fully integrated version of the adder circuit using a standard 0.6-μm CMOS process technology. The new SDFA implementation provides a 15:1 reduction in circuit area, as compared to the area of a hybrid RTD–CMOS version of the same circuit. At the same time, the worst-case propagation delay of the MOS-NDR prototype is similar to that of the hybrid RTD–CMOS SDFA implementation. A disadvantage of the MOS-NDR implementation technique is that the RTD-emulating circuit requires a bias voltage. In our design, since two RTDs are connected in series, two separate bias voltages are necessary.

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