

Circuit Behavior Modeling and Compact Testing Performance Evaluation

Jih-Shyr Yih and Pinaki Mazumder

Abstract—This study suggests a realistic modeling of circuit output error patterns with random test inputs. The model can then be used as the basis for accurate evaluation of the probability of aliasing in compact testing. For several example compression techniques, the following aspects are investigated: 1) identification of the error patterns which cause aliasing, 2) asymptotic effectiveness analysis, and 3) comparative simulation study with a limited amount of random test vectors applied.

I. INTRODUCTION

DATA compression techniques have been introduced to reduce long test responses into short pieces of information called *signatures*. Fault detection is done by comparing the compressed signature produced by the circuit under test to the predetermined fault-free signature. Testing of this kind is usually referred to as *compact testing*. But due to the information lost through data compression, some error responses may be mapped to the fault-free signature, thus causing faulty circuits to escape detection. This problem is called *aliasing*.

With known deterministic test sets, Hayes [1] and Fujiwara and Kinoshita [2] have proposed several methods to arrange test sequences by which the compact testing fault coverage can be as good as the conventional test methods. That is, the ordering of the test inputs will make it impossible for output error patterns to be compressed into the fault-free signature. As for the nondeterministic counterpart, it is understood that not all detectable faults may be covered by the random test patterns in the first place, not to mention the further degradation caused by the data compression. Therefore, the quality of the fault detection achieved by a compression method is of practical interest.

Recently most research interests regarding compact testing have been directed toward testing by feedback shift registers. Frohwerk first performed probabilistic analysis based on the assumption of total randomness in circuit test outputs [3]. If the shift register length is m -bit long, this assumption suggests that, regardless of the polynomial divider used, the chance of not detecting a fault is always 2^{-m} . David constructed a proof for the polynomial divider of the form $x^m + 1$, showing that, when the number of test patterns applied is much greater than the length of the shift register m , the probability for failing to detect a fault is 2^{-m} , even if all the test output patterns are not equally likely [4]. Smith presented two special types of error patterns, burst errors and errors due to repeated-use faults [5]. However, the same result was obtained for these two types of error patterns.

Manuscript received June 29, 1989; revised June 20, 1990.

The authors are with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109.
IEEE Log Number 9038974.

In this study, we have performed a more realistic analysis based on two probability numbers, p_1 and p_2 , as characterization factors which take care of both the circuit's functional and faulty behaviors. p_1 is the probability for a combinational circuit to have a 1 output each time a random input is applied, and p_2 is the probability for an output bit to be in error. The p_1 characteristic is a constant associated with the circuit's functional definition, and is generally known as the *syndrome* [6], while a circuit may have different p_2 characteristics depending on the fault conditions. In fact, for any n -input combinational circuit, p_1 can be calculated once the function is known. Let the test set of a fault be defined as $\{x|x \text{ is a test pattern which can cause an error in output}\}$. If the fault is associated with a test set of size m , then $p_2 = m/2^n$. Thus, p_2 can also serve as a measure of difficulty to detect the fault f . Note that the existence rather than the calculation of these two characteristics is emphasized. We are interested in observing the effectiveness of a compression technique over a wide range of faulty circuits having different characteristics. The two factors can be used in asymptotic analysis to find out the achievable rate of fault detection by a particular technique with an infinite amount of random test vectors applied. Moreover, they can be used to generate a spectrum of error test output patterns of practical length to examine the effectiveness of a particular compression technique.

II. DATA COMPRESSION BY CHECK SUM FUNCTIONS

Some early developed data compression techniques include *ones counting*, which uses the number of ones in an output stream as the signature, and *transition counting*, which keeps track of the number of bit value transitions, i.e., if the next bit is different from the current one, a transition is counted [1].

A. Ones Counting

Let a test response R with length k be represented by $R = r_1 r_2 \cdots r_k$, where $r_i \in \{0, 1, D, \bar{D}\}$. For ones counting, each error bit in the test outputs is capable of affecting the count by 1, i.e., a \bar{D} bit will increase the count by 1 and a D bit will decrease the count by 1. An error response with as many \bar{D} 's and D 's will not be detected.

In terms of p_1 and p_2 , the probability for an output bit to be \bar{D} is $(1 - p_1) p_2$ and the probability for an output bit to be D is $p_1 p_2$. Let k be the length of the test response, and P_a the probability of aliasing. We found

$$P_a = \sum_{\forall \text{ even } m's, 0 \leq m \leq k} C_{m/2}^k C_{m/2}^{k-m/2} \cdot [(1 - p_1) p_1]^{m/2} p_2^m [1 - p_2]^{k-m}.$$

TABLE I
THE RELATION BETWEEN ERROR BIT STREAMS
AND THE TRANSITION COUNT

left neighbor	starting error bit	ending error bit	right neighbor	effect to the count
0	\bar{D}	\bar{D}	0	+2
0	\bar{D}	D	0	0
0	D	\bar{D}	0	0
0	D	D	0	-2
0	\bar{D}	\bar{D}	1	0
0	\bar{D}	D	1	+2
0	D	\bar{D}	1	-2
0	D	D	1	0
1	\bar{D}	\bar{D}	0	0
1	\bar{D}	D	0	-2
1	D	\bar{D}	0	+2
1	D	D	0	0
1	\bar{D}	\bar{D}	1	-2
1	\bar{D}	D	1	0
1	D	\bar{D}	1	0
1	D	D	1	+2

Since the factor $[(1-p_1)p_1]^{m/2}$ is maximized at $p_1=1/2$, we claim that ones counting has a maximum probability of aliasing when $p_1=1/2$.

Since the number of error bits occurring in the error response follows a binomial distribution with the probability of success being p_2 , the expected number of error bits n_e will increase as p_2 gets larger, i.e., $n_e = kp_2$. With n_e error bits expected and the fact that $(1-p_1)p_1 < 1$, the conditional probability of having $n_e/2$ D 's and $n_e/2$ \bar{D} 's is $[(1-p_1)p_1]^{k p_2/2}$. Thus, we claim that P_a in ones counting decreases as the circuit output characteristic p_2 increases.

B. Transition Counting

Let us consider a 9-b fault-free output stream, 101011101, which has six transitions in bit value. If, for some fault, every output bit is inverted to become 010100010, one can find that the number of transitions shown by the new output stream remains six. In fact it is found that, in an output stream, the transition count can only be affected by the relation between the starting/ending bits and their neighboring error-free bits. The entire 16 possible combinations are listed in Table I.

For the special case that a period of error bits is happening at the beginning or the end of the total response, the count will only be affected by ± 1 , like a single error bit. By now it should be clear that the transition count is affected by runs of error bits instead of individual error bits as in the ones counting case. Thus if an error response is to go undetected, the output stream must satisfy the following conditions: 1) the output stream must have both the starting and ending bits being fault-free or in error at the same time. Moreover, if the initial and last parts of the stream are runs of error bits, the net effect of these two runs to the transition count must be zero. 2) The output stream contains as many error periods that increase the count as there are error periods that decrease the count. According to Table I, most of the error periods have zero effect on the transition count. Transition counting not only takes more error bits to affect the signature, but is also likely to have useless error periods for fault detection.

We claim that transition counting has the minimum P_a when $p_2=1/2$. To prove this, let x be the length of an error period. x follows a geometric distribution with the probability of success being $1-p_2$. Thus, we have the expected value of x , $E(x) = p_2/(1-p_2)$. Likewise, if y is the length of an error-free period, we have the expected value of y , $E(y) = (1-p_2)/p_2$. Based on the fact that P_a decreases in ones counting as the number of error bits increases, similarly P_a in transition counting also decreases as the number of expected error periods in the output stream increases. Since the error periods are interleaved with error-free periods, the number of error periods is maximized when $E(x)+E(y)$ is minimized. It is not hard to find that the minimum of $E(x)+E(y)$ happens at $p_2=1/2$, i.e., P_a is minimized at $p_2=1/2$.

C. Data Compression by Polynomial Divisions

Let the fault-free circuit test output stream Z be composed of k bits, $Z = z_1z_2 \dots z_k$. A binary polynomial $Z(x)$ can be constructed to represent Z by using z_i as the coefficient of the term x^{k-i} , i.e., $Z(x) = z_1x^{k-1} + z_2x^{k-2} + \dots + z_k$. Now let the bit stream E_f be defined as an output error pattern when some fault f is present during the test. $E_f = e_1e_2 \dots e_k$, where e_i is 1 if z_i is in error, otherwise e_i is 0. Then $Z(x)+E_f(x)$ corresponds to the faulty test output stream.

The essential idea of compaction is to choose a binary polynomial $P(x)$ as the divider and use the remainder $R(x)$ of $Z(x)/P(x)$ as the signature. The detection of fault f is done by comparing the remainders of $Z(x)/P(x)$ and $[Z(x)+E_f(x)]/P(x)$. $Z(x)/P(x)$ and $[Z(x)+E_f(x)]/P(x)$ have the same remainder if and only if $E_f(x)$ is a multiple of $P(x)$. Consequently, fault detection using the polynomial division compression technique is independent of p_1 .

In order to study the relation between p_2 and $E_f(x)$ as a multiple of $P(x)$, let us begin with the implementation of polynomial divisions. Let $P(x) = a_0x^d + a_1x^{d-1} + \dots + a_d$, where the a_i 's are binary numbers and $a_0=1$. The divider $P(x)$ can be implemented as a shift register depicted in Fig. 1. The memory cells of the shift register are all set to zero initially. The dividend stream is shifted in serially as the input, and the quotient stream will be shifted out serially as the output. The coefficients of the remainder polynomial $R(x)$, $R(x) = r_1x^{d-1} + r_2x^{d-2} + \dots + r_d$, will be left in the corresponding memory cells after the dividend stream is exhausted.

Let us start with a feedback shift register of the simplest kind for analysis, $P(x) = x^d + 1$, which is shown in Fig. 2(a). Let the value of memory cell i after k shifts be $C_i(k)$. The logic expression which determines $C_i(k)$ is described recursively as below:

$$C_i(k) = \begin{cases} z_{k-i+1} \oplus C_i(k-d), & \text{if } k > d \\ z_{k-i+1}, & \text{if } i \leq k \leq d \\ 0, & \text{otherwise.} \end{cases}$$

In other words,

$$\begin{aligned} C_1(k) &= z_k \oplus z_{k-d} \oplus \dots \\ C_2(k) &= z_{k-1} \oplus z_{k-d-1} \oplus \dots \\ &\dots \\ C_d(k) &= z_{k-d+1} \oplus z_{k-2d+1} \oplus \dots \end{aligned}$$

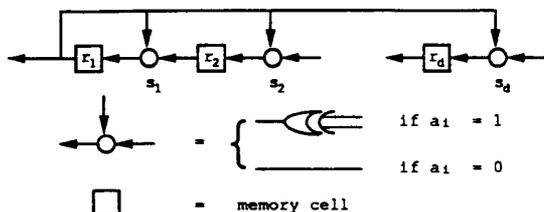


Fig. 1. Shift-register implementation of polynomial division.

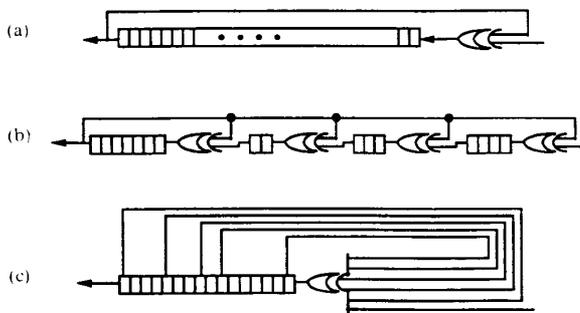


Fig. 2. Feedback shift registers as signature generators.

Note that for any two different memory cells i and j , $C_i(k)$ and $C_j(k)$ are determined by two different sets of z 's, i.e., there is no common variable z between any two logic expressions. Therefore $C_i(k)$ and $C_j(k)$ are independent of each other. Let $y = x_1 \oplus x_2 \oplus \dots \oplus x_n \oplus \dots$, where y and x_i 's are Boolean variables. Let $P_c(k)$ denote the probability of y failing to keep the original value with k -input x variables. Then we have $P_c(k) = P_c(k-1)(1-p_2) + [1-P_c(k-1)]p_2$ and $P_c(1) = p_2$, i.e., $P_c(k) = [1-2p_2]P_c(k-1) + p_2$. We can solve the difference equations, and get $P_c(k) = -1/2(1-2p_2)^k + 1/2$. Since $|1-2p_2| < 1$, $P_c(k)$ approaches $1/2$ exponentially as k gets larger. Consequently, the probability of aliasing for the feedback shift register with $P(x) = x^d + 1$ approaches 2^{-d} asymptotically.

Finally, let us examine a more complicated polynomial divider used by signature analysis [3], $P(x) = x^{16} + x^9 + x^7 + x^4 + 1$, which is shown in Fig. 2(b). Since it is undesirable to insert EXCLUSIVE-OR gates between memory cells, a variation of the implementation is shown in Fig. 2(c). The resulting signature generator performs the polynomial division in a slightly different way, i.e., it would produce the same quotient but a wrong remainder. But, as has been pointed out in [5], it is still true that $Z(x)$ and $[Z(x) + E_f(x)]$ will have the same remainder if and only if $E_f(x)$ is a multiple of $P(x)$. Each new value to be shifted into the register is the result of an EXCLUSIVE OR of the current test output and the values of the memory cells 16, 12, 9, 7, and 1.

Let $C_i(k)$ be the logic value of the i th memory cell in the shift register after k shifts, and $Z_i(k)$ be the set of test output variables effectively involved in the calculation of $C_i(k)$. For any two different memory cells i and j , we can express $C_i(k)$ and $C_j(k)$ as: $C_i(k) = P_{ij}(k) \oplus S_{ij}(k)$ and $C_j(k) = P_{ji}(k) \oplus S_{ji}(k)$, where $P_{ij}(k)$ is the EXCLUSIVE OR of all the elements in $Z_i(k) \setminus Z_j(k)$ and $S_{ij}(k)$ is the EXCLUSIVE OR of all the elements in $Z_i(k) \cap Z_j(k)$. Note that as k approaches infinity, the sizes of $Z_i(k) \setminus Z_j(k)$, $Z_j(k) \setminus Z_i(k)$, and $Z_i(k) \cap$

$Z_j(k)$ are also approaching infinity. Similar to the result obtained for the $x^d + 1$ shift register, with possible inverted test outputs, $P_{ij}(k)$, $P_{ji}(k)$, and $S_{ij}(k)$ will all have a probability of $1/2$ to remain unchanged.

If $C_j(k)$ is in error, then exclusively either $P_{ji}(k)$ or $S_{ij}(k)$ must be different from the expected value. In the case of $S_{ij}(k)$ being changed (unchanged), the probability of $C_i(k)$ being in error is equal to the probability of $P_{ij}(k)$ being unchanged (changed), which is $1/2$ for a large k . In other words, $\Pr\{C_i(k) \text{ in error} | C_j(k) \text{ in error}\} = \Pr\{C_i(k) \text{ in error}\}$. We can claim that, for any two different memory cells, their error conditions are mutually independent when a long test sequence has been applied. Thus, we have shown that, under the new circuit error output patterns model, the probability of aliasing for signature analysis approaches 2^{-16} .

III. SIMULATION STUDIES

In order to examine the effectiveness of compact testing methods with a limited number of random test patterns applied, 2000 circuit output patterns ranging from 1 to 64 in length were generated for the experiment. For each test output stream, signatures by ones counting, transition counting, and signature analysis are generated for fault detection to estimate the probabilities of aliasing.

Fig. 3 shows that each probability of aliasing curve seems to be converging to a certain small number, which implies that when an excessive amount of test patterns is applied it makes relatively little difference which test method is used. But the performance can be significantly different when the number of test patterns is in the magnitude of tens. From this study, it is clear that signature analysis is the best of the three. Ones counting and transition counting rank second and third, respectively.

As is indicated in the analysis, the performance of signature analysis is independent of the p_1 characteristic. In contrast, p_1 has a significant effect on ones counting and transition counting. In this simulation when p_1 is set to be 0.2 instead of 0.5, i.e., with each fault-free output bit value tending to be 0, the probabilities of aliasing of ones counting and transition counting decrease sharply. In investigating the effect of the p_2 characteristic, ones counting and signature analysis perform consistently as p_2 gets larger, i.e., it is easier to detect a fault if more error bits occur in the test outputs. But this is not the case for transition counting. The performance of transition counting tends to be optimal at $p_2 = 0.5$ and deteriorates as p_2 gets greater or smaller.

IV. CONCLUSION

In this study, we found that the type of check-sum compression is more likely to cause signature aliasing than the type of polynomial division. The performance of a check-sum technique is affected by both the circuit syndrome and the fault to be detected, thus showing large variance in the effectiveness of fault detection. Among them, transition counting is found to be worse than the simpler ones counting. On the other hand, the performances of polynomial divisions realized by feedback shift registers are more desirable, since they are independent of the circuit syndrome, and are asymptotically independent of the fault condition as well. The model of circuit error output patterns discussed here is useful as a basis for examining the performance of feedback shift registers with respect to the number of random test

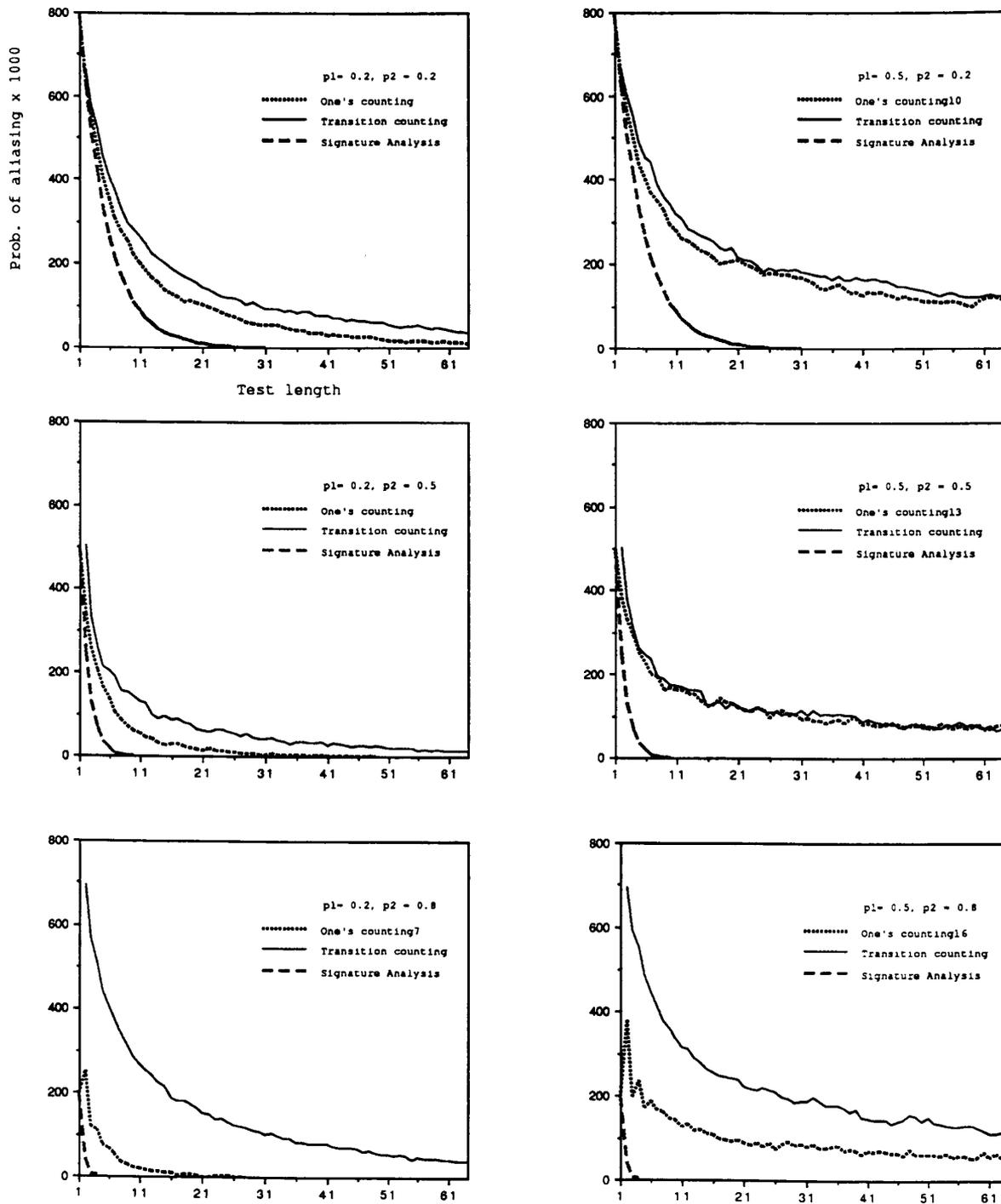


Fig. 3. Performance evaluation of three compression techniques.

inputs applied in practice, which can lead to the efficient use of random testing.

ACKNOWLEDGMENT

The authors would like to thank Prof. J. P. Hayes for his insightful comments and constructive criticism that considerably improved the content and readability of this article.

REFERENCES

[1] J. P. Hayes, "Transition count testing of combinational logic circuits," *IEEE Trans. Computers*, vol. C-25, pp. 613-620, June 1976.

- [2] H. Fujiwara and K. Kinoshita, "Testing logic circuits with compressed data," in *Proc. Int. Symp. Fault-Tolerant Computing*, June 1978, pp. 108-113.
- [3] R. A. Frohwerk, "Signature analysis: A new digital field service method," *Hewlett-Packard J.*, pp. 2-8, May 1977.
- [4] R. David, "Feedback shift register testing," in *Proc. Int. Symp. Fault-Tolerant Computing*, June 1978, pp. 103-107.
- [5] J. E. Smith, "Measures of the effectiveness of fault signature analysis," *IEEE Trans. Computers*, vol. C-29, pp. 510-514, June 1980.
- [6] J. Savir, "Syndrome-testable design of combinational circuits," *IEEE Trans. Computers*, vol. C-29, no. 6, pp. 442-451, June 1980.

A Rad-Hard, Low-Noise, High-Speed, BiFET Charge Preamplifier for Warm Liquid Calorimetry in the SSC

Kuok-Young Ling, Peter M. Van Peteghem, Sang-Yong Lee, Hain-Ching Liu, and Hector Sanchez

Abstract—A fully integrated BiFET charge preamplifier is described which meets the specifications imposed by the Superconducting Supercollider (SSC): a rise time under 100 ns, total noise less than 1000 electrons rms, and power consumption below 80 mW. It has been designed for a detector capacitance of 10 pF and tested up to a total gamma dose of 1.44 Mrd and neutron fluence of 2×10^{13} n/cm². An industrial junction-isolated BiFET process with an 80-MHz f_T for the P-JFET's, 260 MHz for the n-p-n's, and 10 MHz for the p-n-p's was utilized to implement the preamplifier circuit.

I. INTRODUCTION

THE core of particle physics experiments, conducted to observe and study the characteristics of elementary particles, involves high-energy proton-proton beam collisions inside a collider. Secondary emission from a collision is traced in a calorimeter containing a large number of capacitive detectors. The trajectory of the subatomic particles can be reconstructed by detecting the ionization charges created as these particles traverse the calorimeter. The nature and properties of these particles can thus be determined. Consequently, one of the most crucial components of the front-end electronics is the charge preamplifier, which detects and converts a charge into a (low-impedance) voltage signal. Fig. 1 shows a typical circuit configuration of such a charge-sensitive amplifier system. The detector, represented by capacitor C_D , is connected to the charge preamplifier through the high-voltage decoupling capacitor C_C since V_{BIAS} is usually several kilovolts.

Manuscript received March 8, 1990; revised July 14, 1990. This work was supported in part by DOE Grant DE-AS05-81ER40039 and by NSF Grant MIP-8809365.

The authors are with the Department of Electrical Engineering, Texas A&M University, College Station, TX 77843-3128.

IEEE Log Number 9040722.

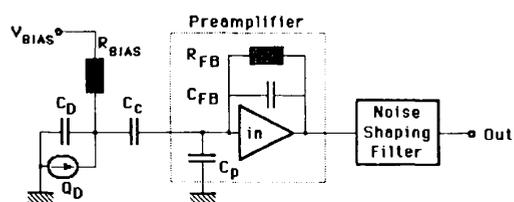


Fig. 1. Circuit schematic of charge preamplifier system.

The Superconducting Supercollider (SSC) imposes very challenging specifications on the charge preamplifier. The collision rate will be in the order of 60 MHz. A preamplifier rise time not exceeding 100 ns [1] provides a reasonable trade-off between the time resolution of successive events and the total rms noise. Such a requirement necessitates mounting the preamplifiers directly on the detectors [2], [3]. As a result, the preamplifiers will receive high levels of nuclear radiation. Annual total gamma dose of 100 krd to 1 Mrd, and neutron fluence in the order of 10^{13} n/cm² are expected, depending upon the locations of the detectors [4]. In addition, the total noise should be kept under 1000 electrons rms, since the collected charge can be as low as 4000 equivalent electrons. Power dissipation is a serious concern due to the large number of preamplifiers that are needed; a power consumption of 80 mW per channel is deemed reasonable [1].

In this paper, a new monolithic BiFET charge preamplifier [5] is described which meets the specifications imposed by the SSC: a rise time under 100 ns, total noise less than 1000 electrons rms, and power consumption below 80 mW. It has been designed for a detector cell of 10 pF for warm liquid calorimetry experiments [3] and tested up to a total gamma dose of 1.44 Mrd, at a dose rate of 40 rd/s, and neutron fluence of 2×10^{13} n/cm².