NSF EDA Workshop Evolution and Basic Science Foundation of EDA Research

Prepared & Presented by Prof. Pinaki Mazumder NSF & Univ. of Michigan

Also included at the end A Write-up by Pinaki Mazumder on EDA Evolution and NSF Funding

Topics for Discussion

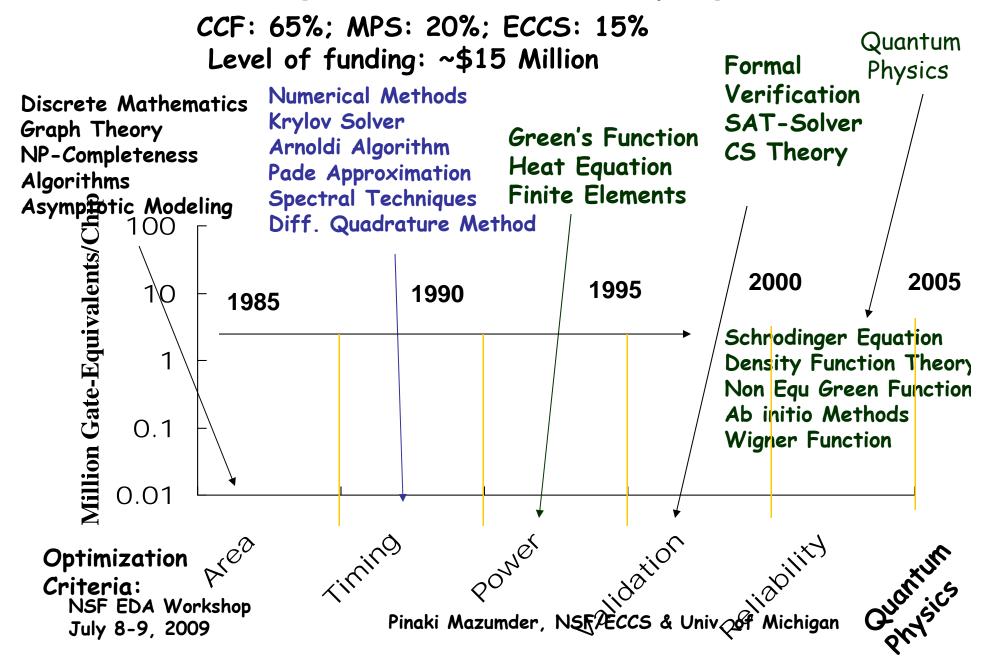
Basic Science Issues in EDA and NSF Funding

- -- evolution of EDA
- -- how has EDA been supported in the past
- -- how to support it in the future as it meets new challenges

Members of Breakout Session:

- 1. Richard Lipton, Georgia Tech University
- 2. Bill Joyner, SRC
- 3. Joydeep Roychowdhury, UCB
- 4. Chris Myers, Univ. of Utah
- 5. Ed Clarke, Carnegie Mellon University
- 6. Rob Rutenbar, CMU & Univ. of Illinois
- 7. Suresh Venkatasubramanian, Univ. of Utah

6.1 Funding in EDA: Underlying Theories



6.1 Funding in EDA: Underlying Theories

- Verification -SAT algorithms, BDD, SAT Modulo Theories, Models of computation for concurrency, Theorem Provers, Proof Checkers, Static Program Analysis, Programming Language and Algorithms Theory, Symbolic Evaluation, Probabilistic and Stochastic Analysis, ...
- Analog EDA Combinatorial and Numerical Algorithms,
 Statistical Algorithms, Monte Carlo, Stochastic Differential Equations, Swarm models,
- Simulation Fast stochastic approaches, nonlinear and dynamical systems, homotopy techniques, nonlinear model order reduction, ...
- Biology: 1. Stochasticity and Unreliability, 2. Abstraction, 3. Scalability

NSF EDA Workshop July 8-9, 2009

Taxonomy of EDA Research - Evolutionary Criteria

- First Generation EDA Tools Targeted Mainly Silicon Area Optimization
- Second Generation EDA Tools Targeted Mainly Timing Optimization in addition to Silicon Area
- Third Generation EDA Tools Targeted Mainly Power Optimization in addition to Timing and Area
- Fourth Generation EDA Tools Addressed Design Reliability Issues (2000-) in addition to Power, timing and Area
- Future Generation EDA Tools will Address Multiscale Modeling of Electronics and Biological Systems

#1 Area Optimization Era

CS Theory served as the bedrock of the First Generation EDA Tools

- Thomson AT^2 Leiserson: Optimal Area
- $o\left[\frac{N^2}{\log^2 N}\right]$ for PSN and *CCC*
- · Asymptotic analysis of VLSI complexity
- NP-completeness of Interval Graph (Gate Matrix), Horizontal Constraint Graph in Channel Routing, Optimal PLA folding, ...
- · SAT Solver for layout design
- · Optimization techniques: GA, SA, Eigenvalue,

Mincut, Quadrisectioning, Force-directed, ...

NSF EDA Workshop

July 8-9, 2009

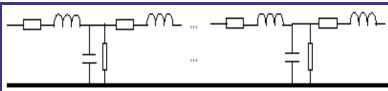
Pinaki Mazumder, NSF/ECCS & Univ. of Michigan

#2. Timing Optimization Era

Numerical Methods served as the bedrock of the Second Generation EDA Tools

Extract Per Unit Length (PUL): R, G, L, and C wiring

parameters



 $\frac{\partial}{\partial x}i(x,t) = -C(x)\frac{\partial}{\partial t}v(x,t) - G(x)v(x,t)$ $\frac{\partial}{\partial x}v(x,t) = -L(x)\frac{\partial}{\partial t}i(x,t) - R(x)i(x,t)$

Write Telegrapher's Equations

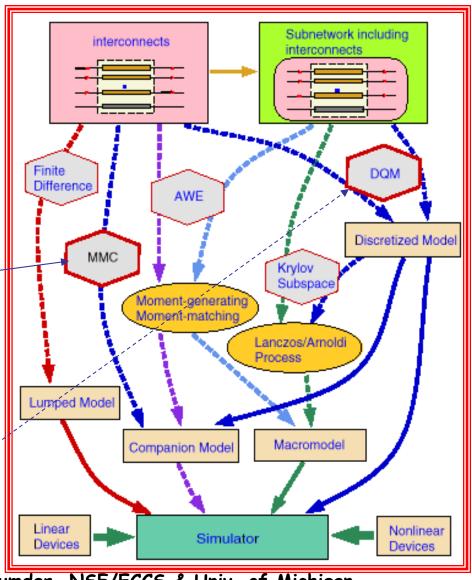
- Time-domain
 - · KCL
 - · KVL
- s-domain
- Solve Partial Differential Equations
- Develop Equivalent Circuit Model

Interconnect Delay Modeling

Q.W. Xu and P. Mazumder, "Equivalent-Circuit Interconnect Modeling Based on the Fifth-Order Differential Quadrature Methods," IEEE Transactions on VLSI Systems, Vol.11, No.6, Dec. 2003, pp.1068-1079.

- · Finite Difference
- · Method of Characteristics
- Modified Method of Characteristics (MMC)
- Asymptotic Wave Eval.
- Reduction Methods
 - Krylov Subspace
- Differential Quadrature
 Method (DQM)

NSF EDA Workshop July 8-9, 2009



FD-TD: Lumped element modeling

Diode current:

$$I_d = I_0 \left(e^{\frac{V_d}{\eta V_T}} - 1 \right)$$

Diode location: (i,j,k) in free space, with current flow in positive z.

Electric field update strategy:

$$E_{z(i, j, k)}^{n + \frac{1}{2}} = \frac{1}{2} (E_{z(i, j, k)}^{n + 1} + E_{z(i, j, k)}^{n})$$

Maxwell's curl equation (Ampere's law):

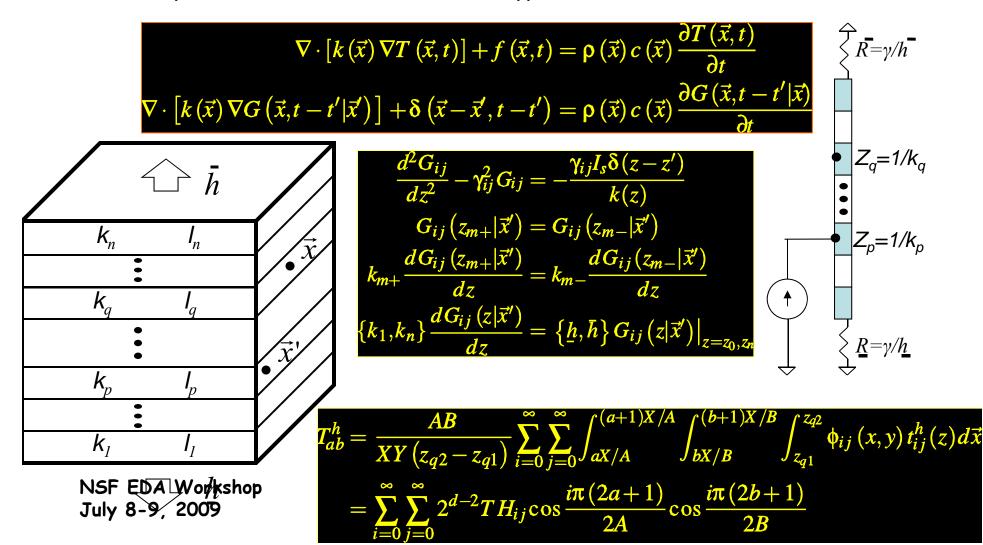
$$E_{z(i,j,k)}^{n+1} = E_{z(i,j,k)}^{n} + \frac{\delta t}{\varepsilon_{0}} \nabla \times H_{(i,j,k)}^{n+\frac{1}{2}} - \frac{\delta t}{\varepsilon_{0} \Delta x \Delta y} I_{0} \left[e^{-(E_{z(i,j,k)}^{n+1} + E_{z(i,j,k)}^{n})((\Delta z)/(2V_{T}))} - 1 \right]$$

Transcendental equation solved by Newton-Raphson.

B. Wang and <u>P. Mazumder</u>, "Integrating Lumped Networks into Full Wave TLM/FDTD Methods Using Passive Discrete Circuit Models." *Proceedings of IEEE International Symposium on Circuits and Systems*, May 2005, pp. 1948-1951.

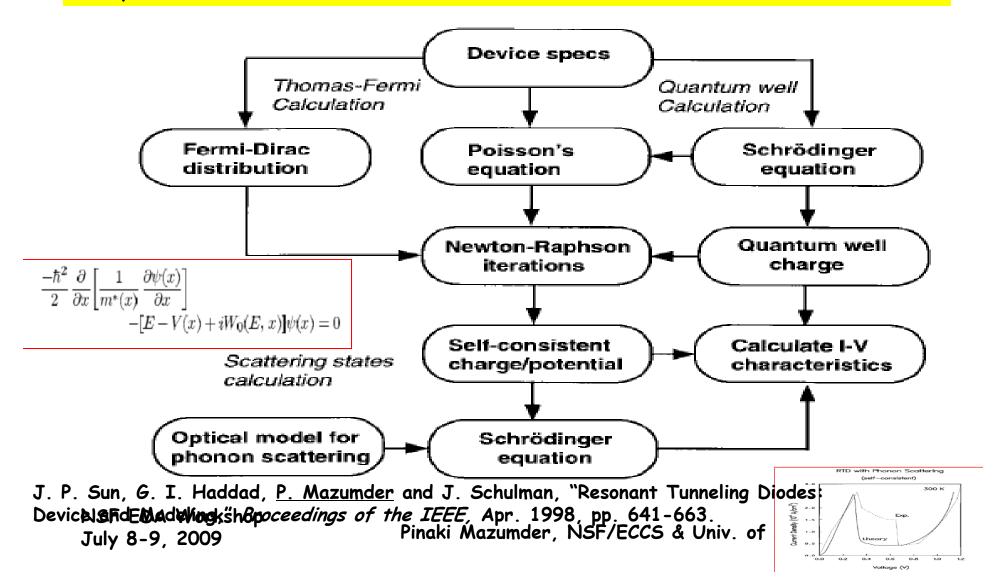
#3. Power Optimization Era: Green's Function Based Full-Chip Thermal Modeling

B. Wang and <u>P. Mazumder</u>, "Accelerated Chip-level Thermal Analysis Using Multilayer Green's Function," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 26, No. 2, Feb. 2007, pp. 325-244.



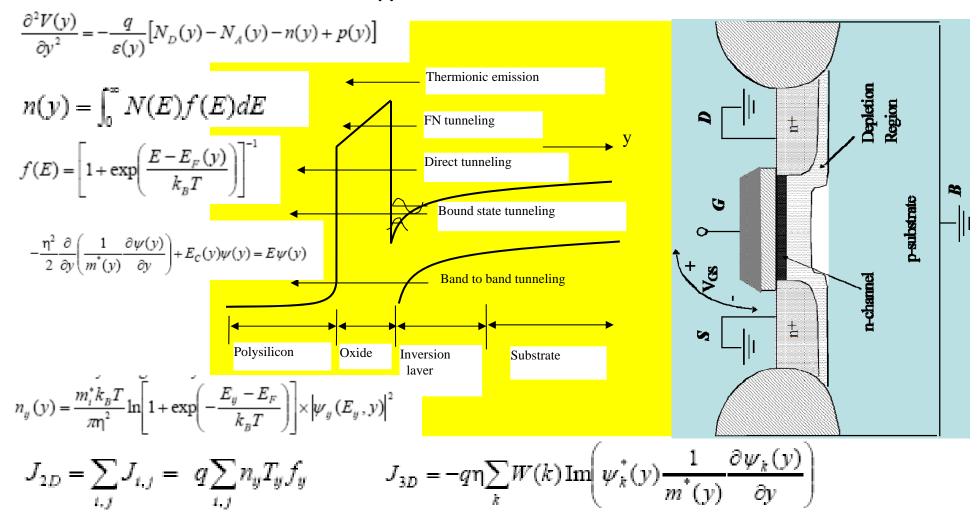
#4. Quantum Physics Era: Self-Consistent Poisson & Schrödinger Equation Solver

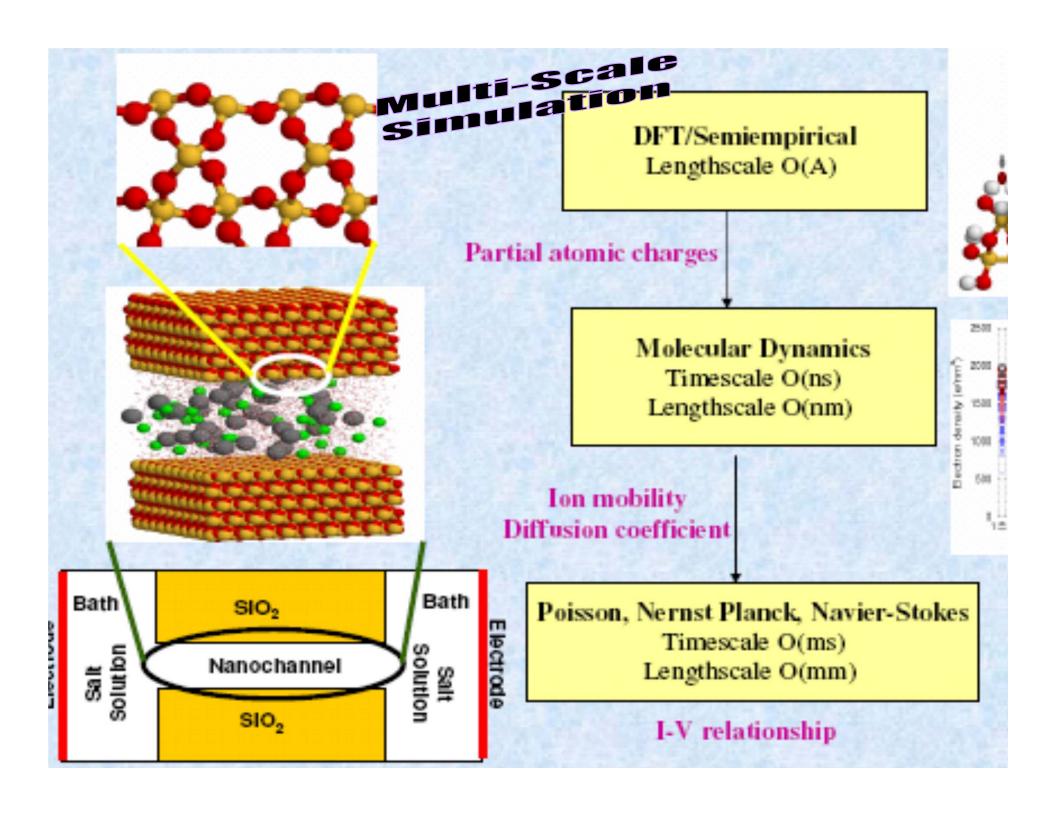
Physics serves as the bedrock of the Fourth Generation EDA Tools



Gate Leakage Currents Model

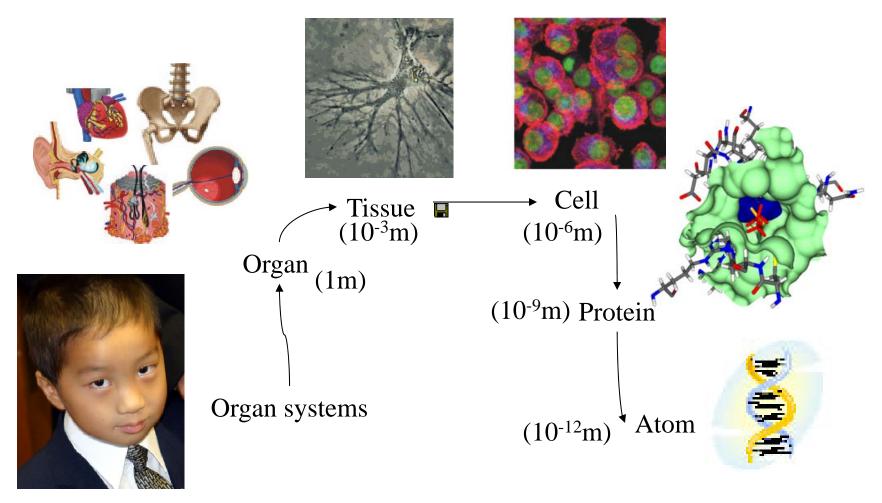
J. P. Sun, W. Wang, N. Gu and <u>P. Mazumder</u>, "Gate Current and Capacitance Models of Nanoscale MOSFETs," *IEEE Transactions on Electron Devices*. vol. ED-53, no. 12, Dec.2006, pp. 2950-57.





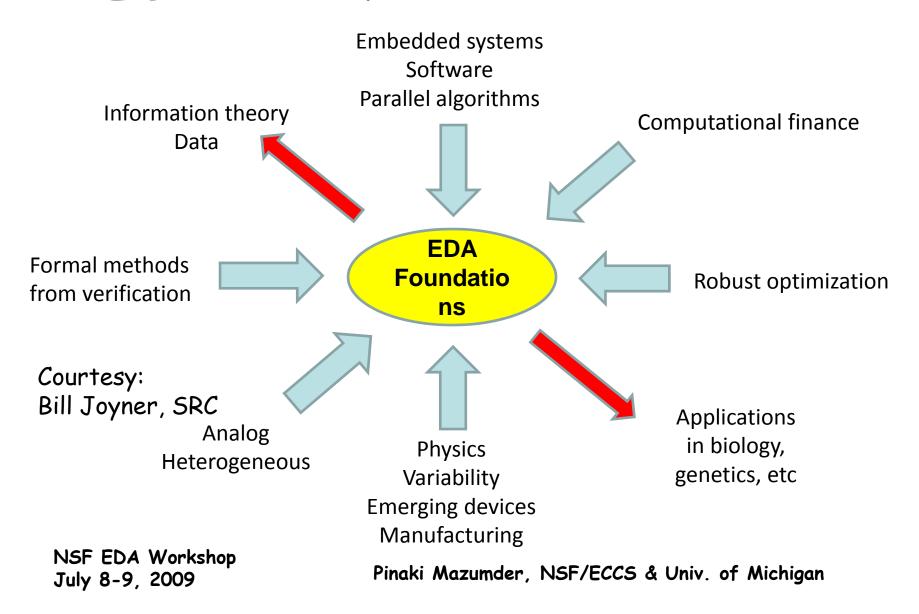
#5: Biosystem Multiscale Modeling Era

Biology/Bioengineering challenge (from top to bottom)
Courtesy: Peter Hunter, University of Auckland



NSF EDA Workshop July 8-9, 2009

EDA as a Foundational Area



Observation #1 by the Break-up Session Members: Incremental research leads to transformative research and that is quite common in the EDA field

Observation #2 by the Break-up Session Members: Beyond Toy Problems. Core scientific value for large scale problems

Challenging and Unsolved Problems:

System Design: 1. Thermal, 2. Reliability, 3. Quantum Physics

Verification: 1. Scalability, 2. Heterogeous Mixed System Design (Digital, analog, mechanical, data + control, ...),

Analog: 1. Productivity, 2. Verification and validation, 3. Wide frequency spectrum

Simulation: 1. Scalability and Abstraction, 2. Stochasticity, Noise, Variability, 3. Mixed signal and mixed domain (hardware & software)

NSF EDA Workshop Multil Core: 2009 Parallel Algorithms, 2. Thermal, 3. Verification

Evolution of EDA:

Although the history of design automation algorithms such as Kernighan and Lin's bi-partitioning heuristics and Kenneth Hall's r-dimensional quadratic placement procedures predates the VLSI era, it was not until the early Eighties when the myth of VLSI chip design and fabrication was unveiled by Mead and Conway to cultivate VLSI education in universities, research in VLSI system design and electronic design automation (EDA) has flourished expansively to help create VLSI design automation tools for logic synthesis, layout generation, circuit simulation, design verification, reliability modeling, chip testing, debugging, and yield analysis. It is beyond the scope of this workshop report to exhaustively chronicle the evolution of EDA research during the last three decades and to catalog how core disciplines of sciences such as physics, mathematics, computer science, statistics, and biology have shaped the EDA research by establishing the foundation of the underlying theories for multi-criteria design optimization and complexity management. Broadly, the VLSI layout automation tools can be demarcated in the evolutionary time scale into distinct eras depending on their chief optimization criterion, namely, area, timing, power, reliability, and nano-scale issues.

NSF EDA Workshop July 8-9, 2009

In the early Eighties, silicon area was at premium and the underlying theoretical foundation of those layout tools was rooted in graph theory (mincut, quadri-sectioning), convex optimization (geometric programming), stochastic methods (simulated annealing), evolutionary biology (genetic algorithms), physical laws (force-directed relaxation methods), circuit theory (energy minimization in resistive networks), and spectral methods (eigenvalue based partitioning). In the mid Eighties, stringent timing constraints in EDA tools motivated the development of theoretical underpinning for interconnect delay models by using linear algebra and matrix solvers (Krylov sub-space, Arnoldi, Pade, Pade via Lancoz algorithms), numerical analysis (differential quadrature method, finite difference), frequency domain solvers (method of characteristics, FDFD), and other theoretical techniques.

In the early Nineties, energy optimization requirements in EDA tools led to the development of finite element method (FEM) and gridded techniques for solving the second-order PDE associated with the Heat equation. Further, the needs for integration of full-chip thermal analysis with chip layout packages were realized by applying the fast Fourier and discrete cosine transformation techniques to accelerate the multilayer Green's function solvers over the quadruple integral spaces. Then, in the late Nineties, higher reliability and quality assurance demands led to the development of technology-centric EDA tools that tackled lithographic limitations, process variations, and anomalous operating conditions. Formal design verification and validation methods were also adopted in EDA tools to ensure correctness of the system design by using model checking, SAT solver, static analysis, and other mainstream CS theories.

By the turn of the new millennium, the VLSI industry made a quantum leap by shattering the red brick barriers of 100 nm and rapidly inching towards 32 nm nodes. Consequently, the new-generation EDA design tools for nanoscale CMOS chips started adopting computational quantum physics (density function theory, non-equilibrium Green's function, Wigner's function) to tackle the nano-scale issues such as leakage currents through high-k gate dielectrics, as well as to develop multiscale modeling for the beyond Moore's Law technologies such as carbon nanotubes, Graphene and tunneling FETs, quantum dots, single electron transistors, and molecular devices.

July 8-9, 2009

NSF Funding:

Academic EDA research has been supported mainly by NSF funding that has fluctuated between \$10 million and \$15 million for the past one and a half decades. The bulk of NSF EDA funding has been given by the CISE Directorate under its core DA program, while additional awards, accounting for almost 20% of all NSF EDA grants, have been provided by ECCS division in the Engineering Directorate and DMS division in the Mathematical and Physical Sciences Directorate. Because the main mission of NSF is to foster ground breaking discoveries grounds up, the EDA awards are rather multifarious, variegated and disparate, covering the broad spectrum of EDA research ranging from high-level synthesis of mixed-signal systems to multiscale simulation of emerging technologies. Special research initiatives like Information Technology Research (ITR) and National Nanotechnology Initiative (NNI) have funneled in additional funding to boost EDA research activities.

NSF EDA Workshop July 8-9, 2009

The CISE Emerging Models and Technologies (EMT) program, which has been recently disbanded, had also stimulated EDA research in disruptive nano, bio and quantum technologies. Typical EDA projects funded by EMT aimed at developing photonics clock distribution networks, synthesis of biomolecular computing systems, DNA computing using self-organized Wang tiles, multiscale modeling of nano and molecular systems, and synthesis of quantum logic circuits. It is not clear how the money, nearly \$3 Million, that EMT used to spend on EDA research will be distributed in the re-clustered CCF division.

The DMS division had regularly funded proposals that had mathematical underpinning for EDA research, for example, Markovian modeling to study convergence of simulated annealing algorithms, convex programming and polyhedral methods, algorithmic semi-algebraic geometry and topology, nonlinear programming under density inequalities, and so on. The ECCS division has funded several multiscale modeling and simulation projects for emerging nano technologies and quantum engineering systems.

NSF has also promoted young educators through its CAREER awards program that used to fund about 10 new EDA projects in 1996 through 2001, but recently the program has shown somewhat declining trend, namely, 6 CAREER awards in 2006.

NSF EDA Workshop July 8-9, 2009

CONTACT PROF. PINAKI MAZUMDER AT pinakimazum@gmail.com mazum@eecs.umich.edu