Memristor Technology in Ultra-Dense Neuromorphic and Non-Volatile Memory Architectures

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U of M

Twenty First Century's Gold Rush for Discovery of Memristors

These are academic research findings, industry is secretive

REF-ERENCE	Structure	OFF/ON Ratio	Retention time (s)	Endurance Cycles	Energy Consumption (J)*
Che05	$Cu/CuO_x/TiN$	$>10^3$	>1	>600	6.3E-12
Sak03	$Cu/Cu_2S/Au$	$>10^6$	$>10^3$	>1	7.0E-8
Gua07	$Si/ZrO_2/Au$	$>10^3$	$>10^3$	$>10^2$	No data
Lee07	$Cu/Mo_x/Pb$	>10	$>10^5$	$>10^6$	1.0E-8
Don08	Si/a-Si/Ag	$>10^4$	$>10^6$	$>10^4$	4E-12
Gua08	$Ti/ZrO_2/Cu$	$>10^6$	$>10^4$	$>10^4$	8.75E-10
Bec00	$SrRuO_3/SrZrO_3/Au$	>20	$>10^7$	No data	1.38E-07
Gre07	Si/Rotaxanes/Ti	~10	~ 10^4	~10	No data
JoLu08	Ag/a-Si/p-Si	$>10^4$	$>10^7$	$>10^6$	1E-15

Outline of the Talk

- What is Memristor?
  and Memristor Technology
- Memristor in Neuromorphic Systems
- Verilog Modeling of Position Detector
- Memristor Based Terabit Memories

University of Michigan Memristor Structure

- The device consists of
- Ag/a-Si/p-Si materials

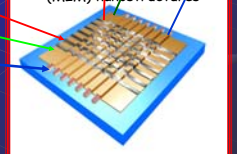
Fabrication by: Prof. Wei Lu

Low Resistance

$V_{app} > V_{th1}$

High Resistance

$V_{app} < V_{th2} < V_{th1}$



Ag/a-Si/p-Si gives highly controllable and reliable switching behavior

What is a Memristor?

Conservation of Energy Principle Applied to Electrical Components

1870 Kirchoff's Law For R, L and C

The 4th Circuit Element found in 1971 by Prof. Chua who called it Memristor

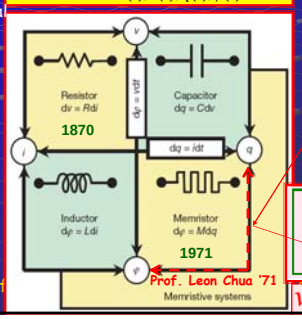
2008 Nanoscale

Kirchoff's Law for a Series RLC Circuit:

$$V_R(t) + V_L(t) + V_C(t) = v(t)$$

$$Ri(t) + \frac{d\phi(t)}{dt} + \frac{q(t)}{C} = v(t)$$

State Variables: $i(t); v(t); q(t); \phi(t)$



$$\binom{4}{2} = \frac{4 \times 3}{2 \times 1} = 6$$

$(v, i) = R$

$(q, i) = C$

$(\phi, i) = L$

$dq = idt$

$d\phi = vdt$

(Faraday's Law)

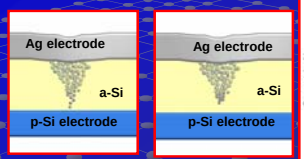
$(\phi, q) = M$

Memristance

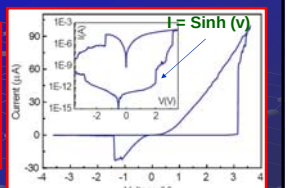
$$M(q) = \frac{d\phi}{dq} = \frac{vdt}{idt} = \frac{v}{i}$$

$$v = M(q)\, i$$

Resistance Switching Characteristics



Single filament formed by a chain of ions – digital switching (memory)

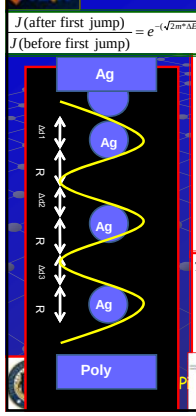


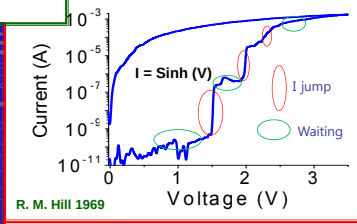
- Exponential conductance change Approximated by Sinh Function

Fabricated by Prof. Wei Lu @ UM

UNRAVELLING THE IONIC TRANSPORT AT NANOSCALE

$$\frac{J(\text{after first jump})}{J(\text{before first jump})} = e^{-(\sqrt{2m^*\Delta E}/\hbar)\cdot 2(d_2-d_1)}$$





R. M. Hill 1969

$$T(\Delta E) \cong e^{-2\gamma} = e^{-(2\sqrt{2m^*\Delta E}/\hbar)d}$$ Transmission Coefficient

$$J(V) = \frac{qm^*}{2\pi^2\hbar^3}\int_0^\infty [f(E) - f(E+qV)]dE \times T(\Delta E)$$

$$\propto (D.O.S.) \times T(\Delta E) \times \ln\left[\frac{1+\exp(E_F - E)/kT}{1+\exp(E_F - E - qV)/kT}\right]$$

$$\Rightarrow J(V,T) \cong \frac{8\pi me}{h^3\beta^2}\frac{\pi\beta kT}{\sin\pi\beta kT}\exp(-A\phi^{3/2})\begin{cases}\sinh\left(\frac{eV}{kT}\right)\exp\left(-\frac{\delta E}{kT}\right) & \text{for } \delta E > kT \\ \sinh\left(\frac{eV}{kT}\right)\left(\frac{kT}{\delta E}\right) & \text{for } \delta E < kT\end{cases}$$

$$J(V,T) \cong \frac{8\pi me}{h^3\beta^2}\frac{(\pi\beta kT)^2}{\sin\pi\beta kT}\exp(-A\phi^{3/2})$$

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- Memristor Technology
- Ionic Transport Modeling
- Memristor in Self-Healing of Crossbar
- Memristor in Cognition (Position Detector)
- Memristor Based Terabit (Gargantuan) Memories

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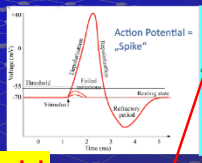
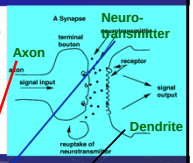
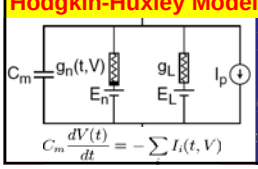
Biological Neuron Model

Ionic Transport in Biological Neuron & its Silicon Implementation

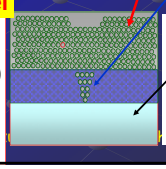


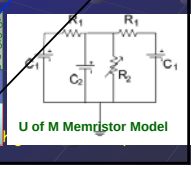


Hodgkin-Huxley Model



$$C_m\frac{dV(t)}{dt} = -\sum I_i(t,V)$$

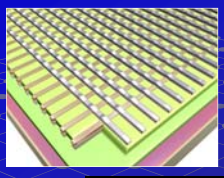


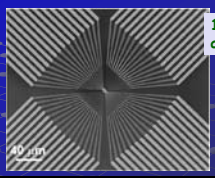


U of M Memristor Model

Fabricated by Prof. Wei Lu @ UM

High Density a-Si Based Nano-Crossbar

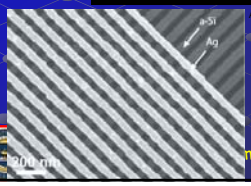


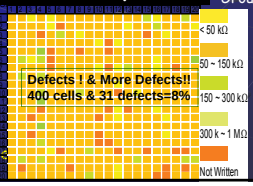


1kb crossbar array

Jo et al. *Nano Lett.*, 9, 870 (2009). From Prof. Wei Lu's Research Group

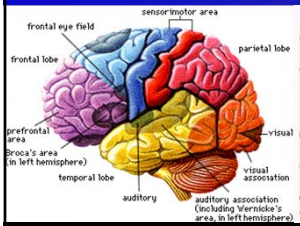
It is Scalable and CMOS Compatible.

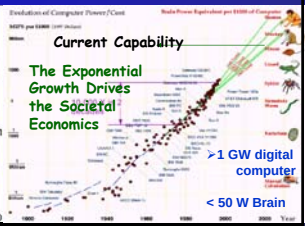




Defects ! & More Defects!!
400 cells & 31 defects=8%

The Holy Grail of Computing -- Can we spill human brain on Silicon?





Facets of Neuromorphic or Brain-like Computing:

Self-Healing (Robust) Spike Learning
Cognition (Visual, Auditory, Tactile) Huge Memory

Neuromorphic Self-Healing Memory Design using Memristor Array

Product Code (SEC), Augmented PC (DEC) → Requires Muxes (~8%)
Hamming Code (SEC) → Higher Overhead
Projective Geometry Code (DEC/TED) → Galois Field Decoding, …
BCH & Reed Solomon (DEC) → Decoding complexity is high

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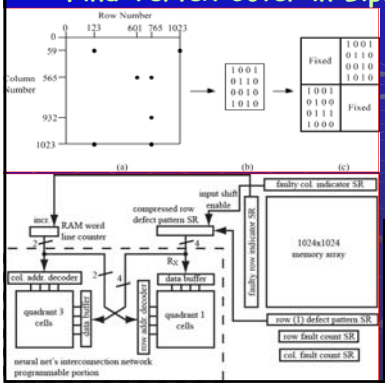
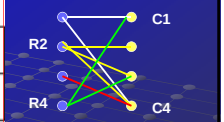
Compaction of Faulty Array & Find Vertex Cover in Bipartite Graph

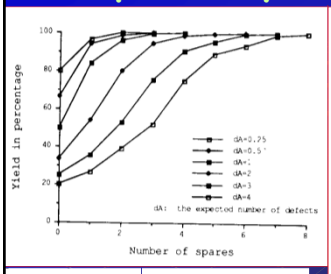


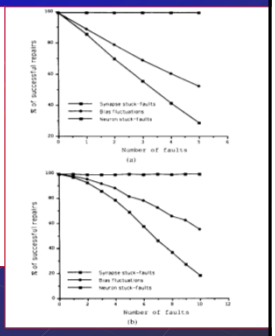


Find Vertex Cover:
[R2, R4; C1, C4]
Defective Cells are Edges in Bipartite Graph

Unrestricted Vertex Cover Problem can Be solved in Polynomial Time by Bipartite Graph Matching Algorithm. However, Restricted Vertex Cover Problem is NP-complete.

Reparability & Robustness





$$Y_0' = \left(\frac{Y_0}{1 + B\delta Y_0/\alpha}\right)^{\alpha}, \qquad Y_N = P_r + \frac{(1 - P_r)Y_0}{1 + B\delta Y_0}$$

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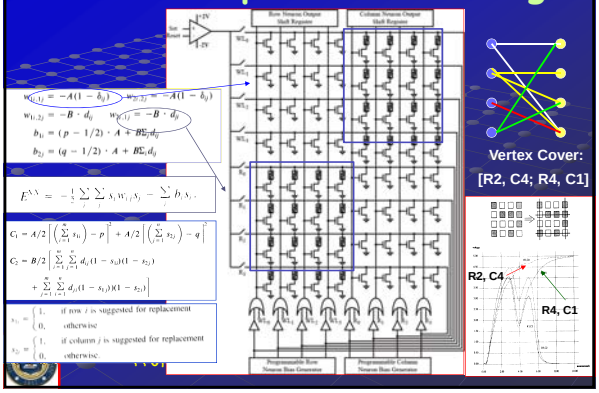
Neuromorphic Self-Healing



Vertex Cover:
[R2, C4; R4, C1]

EVOLUTION OF NEUROMORPHIC COMPUTING:

Perceptron ('60)
(10 E 1 neurons)

Neural Net ('80)
(10 E 3 Neurons)

Neuromporphic Hardware ('90)
(10 E 6 neurons)

Nanocrossbar
(10 E 10 neurons)

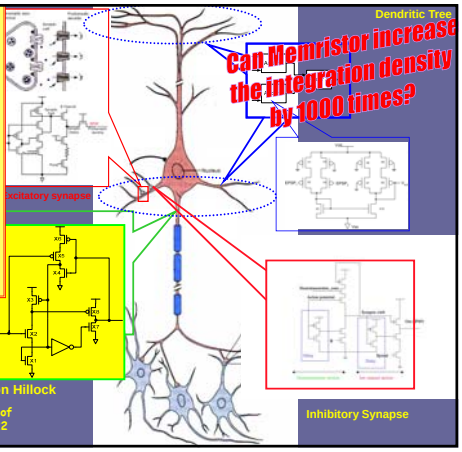
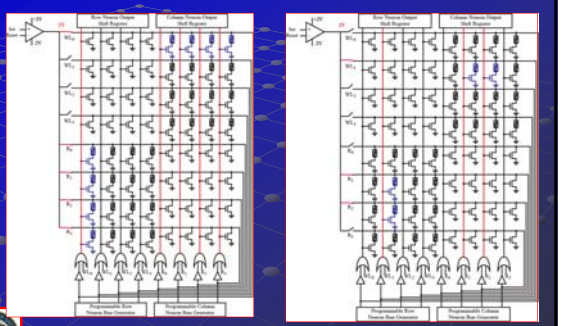


Figure from Principles of Neural Science [2] p.22

Reset & Write Phase



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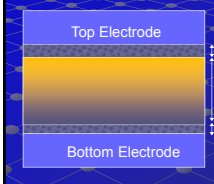
Analog a-Si Memristors

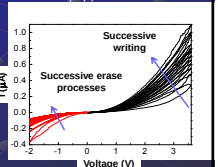
- Uniform motion of the conducting front – analog switching (memristor)
- Creation of uniform conducting front by co-sputtering of a-Si & metal



DARPA SyNAPSE PROJECT WITH HRL LABORATORIES

sputtered a-Si only
co-sputtered Si & Ag (~ 20nm)
mixture ratio (rough # of atoms), gradual change
i.e. Si : Ag = 20: 1 (bottom) → 10: 1 (top)
sputtered a-Si only

All Credits Go to Prof. Wei Lu's Outstanding Research Group



- Incremental conductance change
- Conductance ∝ total charge through the device
- Highest process temperature < 260°C

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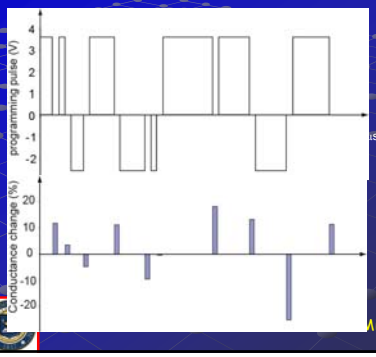
Memristor: A New Paradigm Circuit Design

Programming pulses with different pulse widths



Conductance controlled by the pulse width, and can be changed incrementally.

1. Digitally Controlled
2. Constant Amplitude
3. Temporal Correlation

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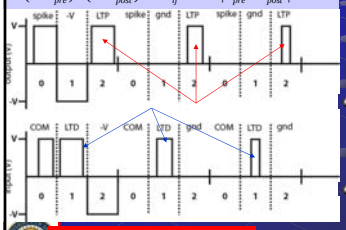
Neuron Spiking Signals and STDP Control

Hebbian-Type STDP Learning Model

Neurons that "FIRE" together, also "WIRE" together. – D. Hebb

$$\frac{d}{dt}w_{ij}^{LTP} = \gamma^{LTP}.d_a.\exp\left[-\frac{t-t_{pre}}{\tau_a}\right]\times d_b.\exp\left[-\frac{t-t_{post}}{\tau_b}\right]$$
$$\times u(t-t_{pre}).u(t-t_{post}) \Rightarrow w_{ij}^{LTP} \uparrow \text{if } |t_{pre}-t_{post}| \downarrow$$



- Time Division Multiplexing
  - Events occur at proper timeslots
  - Long Term Potentiation can only occur in the 2nd timeslot
  - Long Term Depression can only occur in the 1st timeslot
  - Inputs are considered only in the 0th timeslot
- Each pulse of amplitude V is not enough to make a significant change to memristance
- When there's a net difference with amplitude 2V, memristance changes

Neuron spikes in first frame

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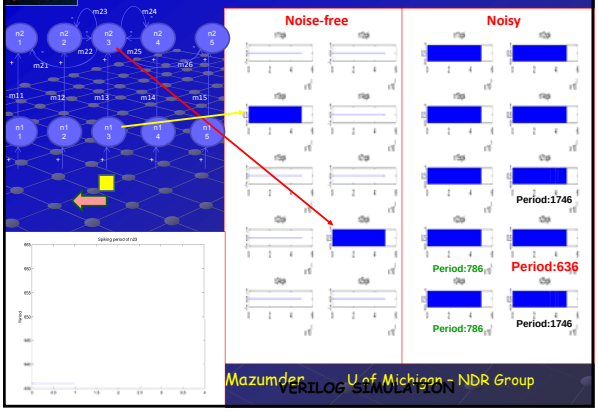
STDP-Based Position Detector



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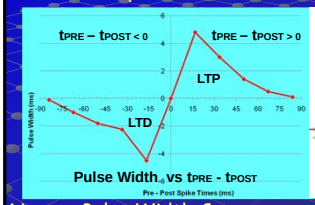
VERILOG SIMULATION

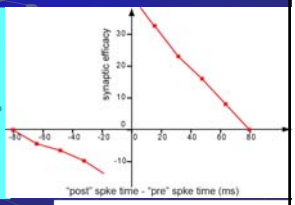
SPDT with Memristor

Pulse Width vs. Pre and Post Neuron Spike Times



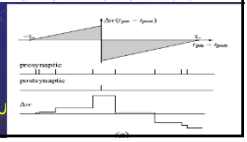
Pulse Width vs tPRE - tPOST

STDP obtained using memristor synapse



Neuron Pulse Width Curves (across a synapse)

For LTP case: The Post neuron is at –V while the Pre neuron at +V
For LTD case: The Pre neuron is at –V while the Post neuron at +V
LTP case is taken as positive while the LTD case negative



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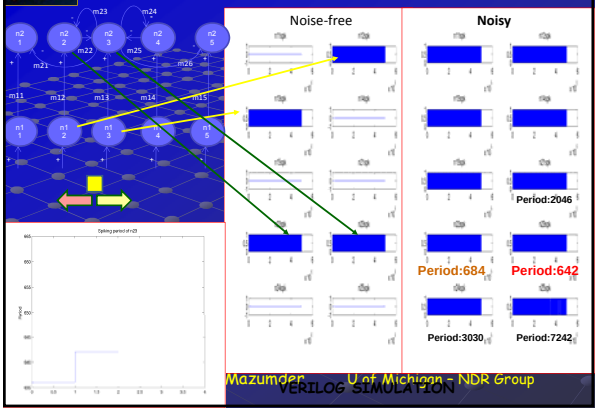
Position Detector



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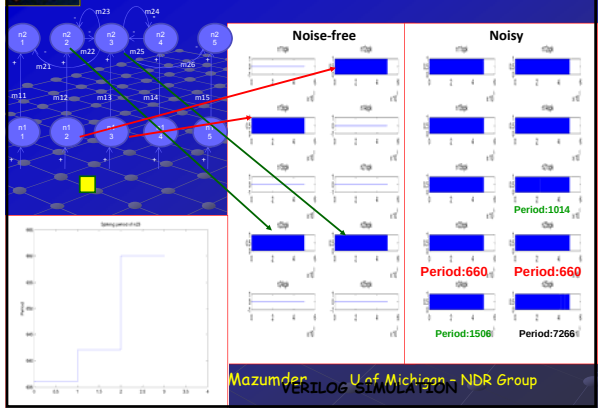
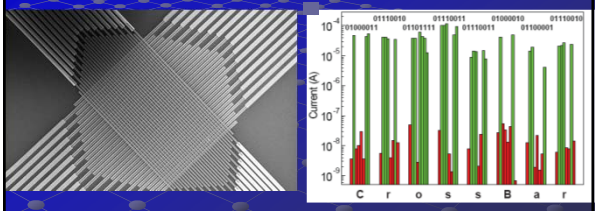
VERILOG SIMULATION

STDP Based Position Detector



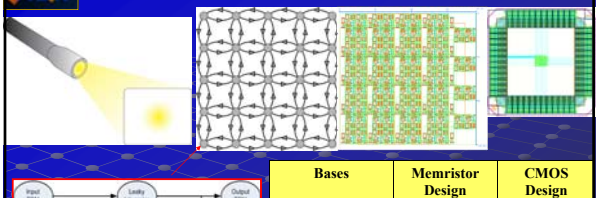
VERILOG SIMULATION

Improved Memory Array



- Improved memory to reduce series resistance associated with p-Si electrodes.
- Random programming of the array achieved.

STDP Neural Circuit for Position Detector



Bases	Memristor Design	CMOS Design
Synaptic area	< (0.5µm x 0.5µm)	17µm x 16µm
Synaptic Density	➢4 devices/µm² x1000	0.0037 devices/µm²
Neuron area	20µm x 10µm	8µm x 12µm
Neuron Density	0.005 devices/µm² x2	0.0104 devices/µm²
Volatility	Nonvolatile	Volatile

Yield Map of 1kb Crossbar Array

- Results from 100 bits tested using automated write/erase pulses
- On/Off > 10^3 for all devices that can be written
- -> 92% yield. Excellent reproducibility and reliability

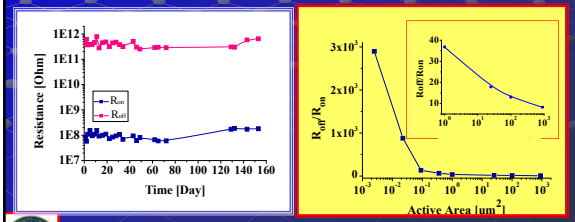
Jo et al. *Nano Lett.*, 9, 870 (2009).

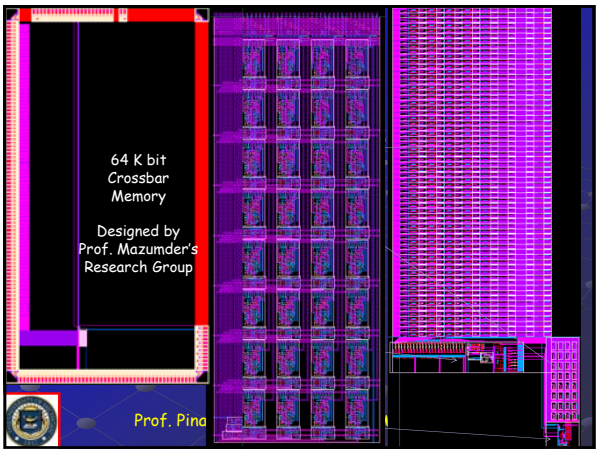
Outline of the Talk

- What is Memristor?
- Memristor Technology
- Ionic Transport Modeling
- Memristor in Neuromorphic Systems
- Simulink & Verilog Modeling
- Memristor Based Flash Memories

Data Retention Time

- More than 150 days without noticeable degradation at room temperature
- A-Si is superior to many complex oxides for data retention



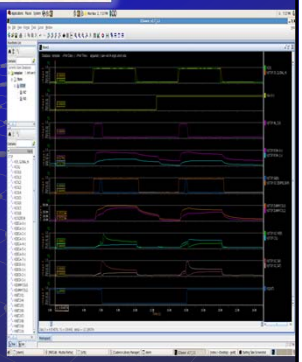


R&D Work Needed for Memristor NV Memory: Fault Modeling, Test Algorithms, Testable Design, Diagnosis, Repair, Reconfiguration, Error Correction & Detection, Soft Error Modeling, Yield Modeling, Noise Modeling, Power Dissipation, Macro Modeling, Q&A

Simulation Results

Temperature = 25C	First Row, First Col	First Row, Last Col	Last Row, First Col	Last Row, Last Col
Read Access Time	1.00422 ns	1.00753 ns	1.03404 ns	1.03515 ns
	Read 0 (QOUT Falling)		Read 1 (QOUT Rising)	
Dynamic Current	162.9 uA		175.25 uA	
Leakage Current	1.113 uA			
Peak Current	2.28 mA			

Temperature = 125C	First Row, First Col	First Row, Last Col	Last Row, First Col	Last Row, Last Col
Read Access Time	1.248 ns	1.265 ns	1.318 ns	1.322 ns
	Read 0 (QOUT Falling)		Read 1 (QOUT Rising)	
Dynamic Current	191.79 uA		201.68 uA	
Leakage Current	13.655 uA			
Peak Current	2.045 mA			



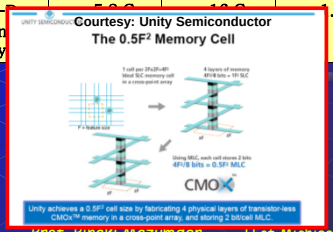
SPICE simulation waveforms

Mazumder's Research in Semiconductor Memories

BISR Memory Compiler by Mazumder Research Group

A Case for Gargantuan Memory

Cell Size	200 n x 200 n	100 n x 100 n	10 n x 10 n
2-D technology	~ 1.3 G	~ 4 G	~ 350 G
3-D technology			1.4 T



End of Talk

Mercel Proust: Remembrance of the Things Past

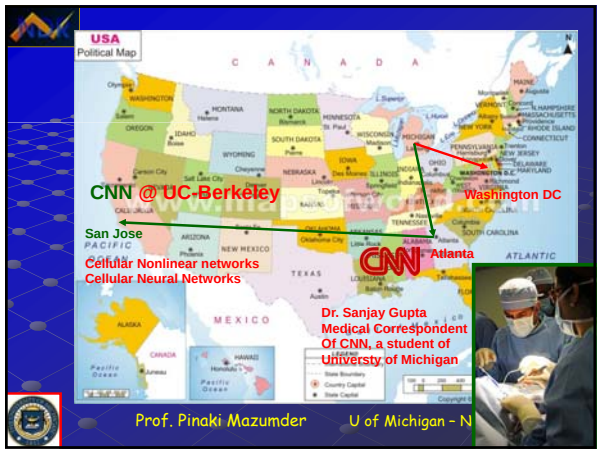
Thank You

NSF had sponsored the First Memristor Workshop in Nov 2008 soon after the wide scale media coverage and then this workshop with the following objectives:

To spur research activities – Can we fabricate memristor based circuits without the crossbar architecture?
What new applications?
How do they compare with others?
Demonstration of fabricated chips

To promote Education – How memristors, memcapacitors, and meminductors will influence teaching of circuit theory, VLSI design, …? How memristors can be adopted in CMOS chip design projects?

Resistive Memories – where things stand in industry?
what are defect densities?
what sort of scattering of delays?



End of Talk

Mercel Proust: Remembrance of the Things Past

Thank You

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CNN vs. CNN

Invented by:	Prof. Leon N. Chua Intellectual Giant	Mr. Ted Turner Business Giant
Started:	Ideas conceived in 80's	Started in 1980
Major Milestone:	IEEE TCAS 1988	Challenger Disaster, 1986
Subscriber:		90 Million
World Popularity:	Europe, Japan	Asia and Europe
US Competitor	Intel Chips	Fox News

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NRI Workshop on Nano Architectures

Prof. Pinaki Mazumder
Univ. of Michigan
Program Director
Emerging Models & Technologies
CISE Directorate
National Science Foundation

NSF@VA

CSE-UM@MI

Where Does CNN Belong: ANN, MPP, SPN?

Does it belong to Artificial Neural Network Hierarchy?

Perceptron, Feed Forward Network, Hopfield Network, Boltzmann Machine, Kohonen Self Organizing Map, Recurrent Network, etc.

Features: Learning capability, Back propagation, …

Is CNN (1988) an Artificial Neural Network?

CNN uses ANN terminologies like neurons and neural network that induce people to consider it as an ANN, but CNN does not allow ANN learning mechanisms like backpropagation.

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Does CNN Belong to Massively Parallel Processor Hierarchy?

1. Shared Memory Architecture – Sequent and Balance
2. Hypercube – Intel, N-Cube
3. Mesh Architecture like ILLIAC (UIUC), Torus (Japan) , Paragon (Intel)
4. Loosely Coupled Architectures like C.mmp and Cm* (CMU)
5. Systolic architectures like iWARP of Intel and CMU
6. Bit Serial Parallel Processor like STARAN and MPP of NASA

7. CNN does not belong here since all of them use Binary Computing.

CNN is a crossbreed between ANN and MPP that can be easily implemented in VLSI as well as Nanoscale.

CNN uses local computation paradigm of cellular network, it is regular And can be replicated and scaled easily to emulate massively parallel computation, and it's model of computation can be extended to Nanoscale

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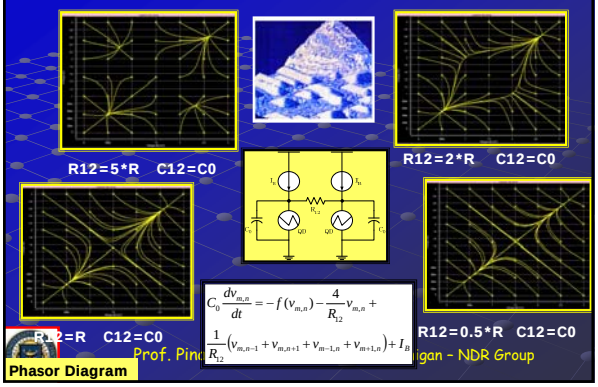
Phasor Diagram of a Q-dot Pair



Phasor Diagram

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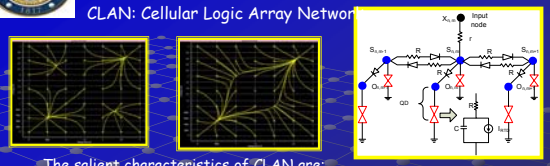
Nanoscale CNN Model of Computation

CLAN: Cellular Logic Array Networ



The salient characteristics of CLAN are:

Limited fan-out and fan-in requirements
No long interconnection for global data movement is needed
No bus structure for sharing information by multiple modules is present
No module addresses are required because of adjacency charge transfer
No global clock for data synchronization is necessary
Tessellation property of the architecture leads to scalability of design
Massively parallel input capability –
Massively parallel output capability

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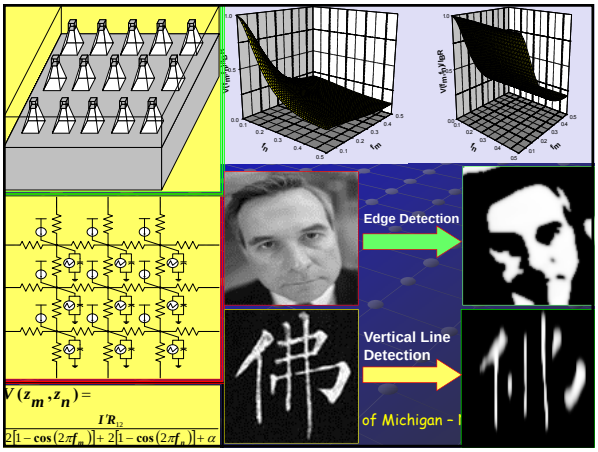

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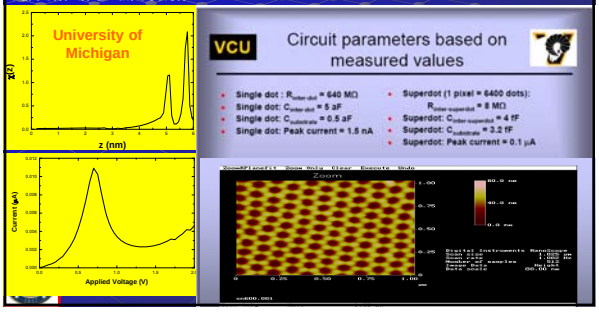
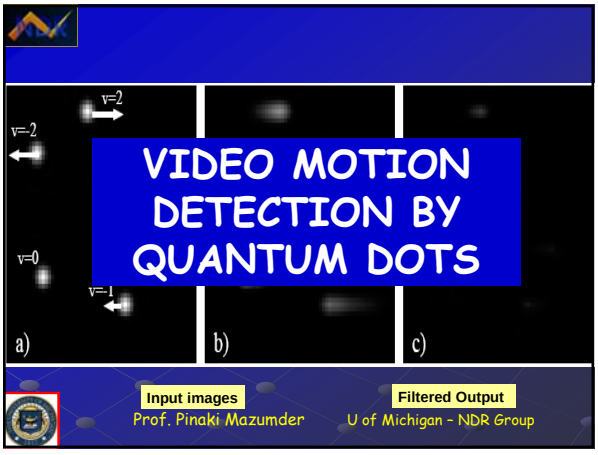
QUANTUM DOT ARRAY FOR IMAGE PROCESSING

Analytical Tunneling Current in z-direction

Measured Values of Current and Parasitic Of Fabricated Quantum Dot Array





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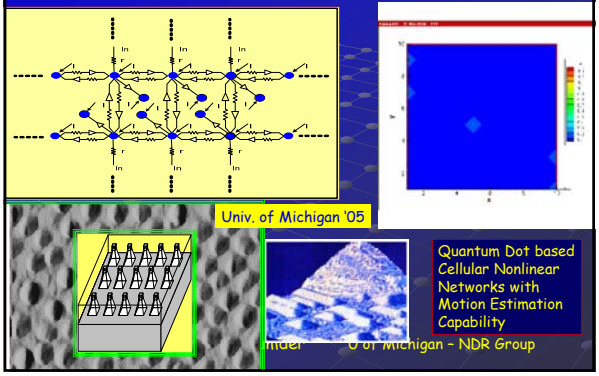
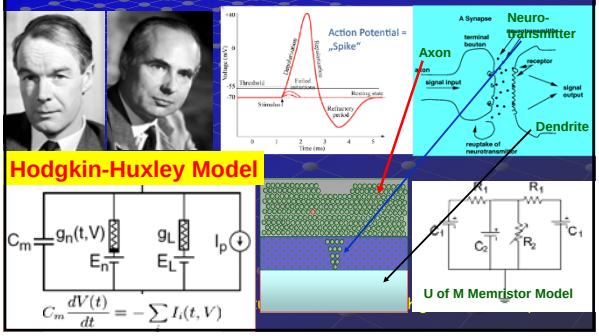
Motion Detection Using Quantum Dots



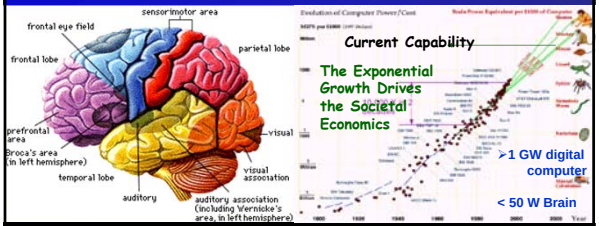
Biological Neuron Model

Ionic Transport in Biological Neuron & its Silicon Implementation



Impacts of Prof. Chua's Pioneering Inventions of CNN and Memristor

Nanoscale Architectures, Nonlinear Circuits & Brain-like Computing



Using Memristor one can implement Hebbian and Reinforcement Learning using SPIKE mode of operation

Using nanoscale CNN one can implement biological organs of sensing actuation network similar to eye, muscles, etc.