Technology and Layout-Related Testing of Semiconductor RAMs

Prof. Pinaki Mazumder

The University of Michigan

Ann Arbor, MI 48109

Phone: 313-763-2107

mazum@eecs.umich.edu

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RAM Research Overview

Circuit Techniques	Test Algorithms	Error Correction	Self Repair	Compiler
• DFT for DRAM • DFT for CAM • DFT for random test • BIST for RAM • BIST for CAM • ASIC for memory testing	• Parallel PSF • Parallel parametric tests • Parallel stress tests • Tests for embedded CAMs • Tests for device-related faults (HEMT) • Board-level testing	• Double-bit ECC • Parallel signature analyzer based ECC • Projective geometric code • Radiation study • Reliability analysis	• Pseudo-analog adaptive circuits for self-repair • Digital adaptive circuits for self-repair	• RAM compiler - Self-testing - Self-repair • ROM compiler - Self-testing - Self-repair

- Books written by P. Mazumder
  - Testing and Testable Design of High-Density RAM, 1996
  - Fault Tolerance of RAM, 1998

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Outline of the Talk

- RAM Fault models / test complexity
- DRAM Technology-related faults/tests
- DRAM soft errors
- BIST for embedded memories
- Random-pattern testing
- SRAM test techniques
  - Techniques for cell-related faults
  - Techniques for device-related faults
- Conclusion

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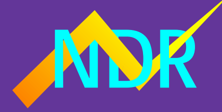

Issues Addressed

- What testing problems we encounter in giga-bit DRAMs.
- How to test technology-related faults.
- How to design BIST for embedded RAMs.
- How to test small-size memories by random patterns.
- How soft-error occurs in DRAM and what ECC.
- What type of technology-related faults occur in SRAMs due to masking and parametric defects and how to test them.
- What type of technology-related faults occur in SRAMs due to device scattering, and how to test them.

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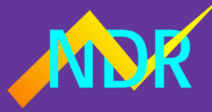
Fault Model for RAM

Stuck-at

Coupling

Pattern-sensitive



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Conventional Test Algorithms

Non-march Tests

- Checkerboard $\rightarrow O(N) \approx 4N$
- Galpat/Ping-Pong $\rightarrow O(N^2)$
- GalCol $\rightarrow O(N^{1.5})$
- GalRow $\rightarrow O(N^{1.5})$
- Walking 1/0 $\rightarrow O(N^2)$
- Butterfly $\rightarrow O(N \log N)$
- Sliding Diagonal $\rightarrow O(N^{1.5})$
- Divide and Conquer $\rightarrow O\left(\frac{4K+2}{\log K} N \log N\right)$

- ❑ Stuck-at faults
- ❑ Transition faults
- ❑ Coupling faults

March Tests

- MSCAN $\rightarrow 4N$
- ATS $\rightarrow 4N$
- Marching 1/0 $\rightarrow 14N$ $[\Uparrow(w_0), \Uparrow(r_0, w_1, r_1), \Downarrow(r_1, w_0, r_0), \Uparrow(w_1), \Uparrow(r_1, w_0, r_0), \Downarrow(r_0, w_1, r_1)]$
- MATS++ $\rightarrow 6N$ $[\Updownarrow(w_0), \Uparrow(r_0, w_1), \Downarrow(r_1, w_0, r_0)]$
- MARCH-X ($6N$), MARCH-C ($11N$), MARCH-A ($15N$), MARCH-Y ($8N$), MARCH-B ($17N$)
- 3-Coupling Faults $\rightarrow 4N \log N + 18N$
- Moving Inversion (MOVI) $\rightarrow N \log N$

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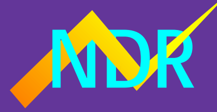
Time Required for Testing RAMs

Tests	4M (1994)	16M (1996)	64M (1998)	256M (2000)	1G (2002)	4G (2004)
3-Coupling	2m 28s	10m 45s	46m 35s	3h 21m	14h 20m	2d 13h
MARCH	2.1s	8.4s	33s	2m 14s	8m 57s	35m 47s
GALPAT	41d	22 month	29 years	457 years	7312 year	1e5 year
Sliding D.	1h 55m	15h 16m	5 d	41d	226d	7 years
PSF (K=5)	21s	83s	5m 34s	22m 15s	1h 29m	5h 56m
Row-PSF	8h 39m	2d	11d	2 month	11 month	4.5 years
	4m 2s	18m 31s	1h 24m	6h 18m	28h 8m	5 d
	43m 56s	3h 35m	17h 16m	3d 10h	16d	2.5 month

- Cycle time: $T_C = 50$ ns



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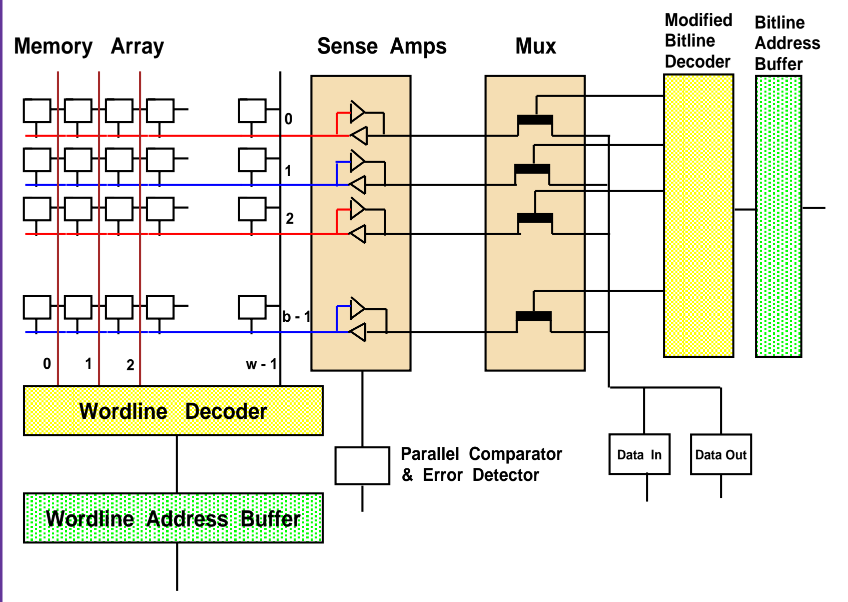
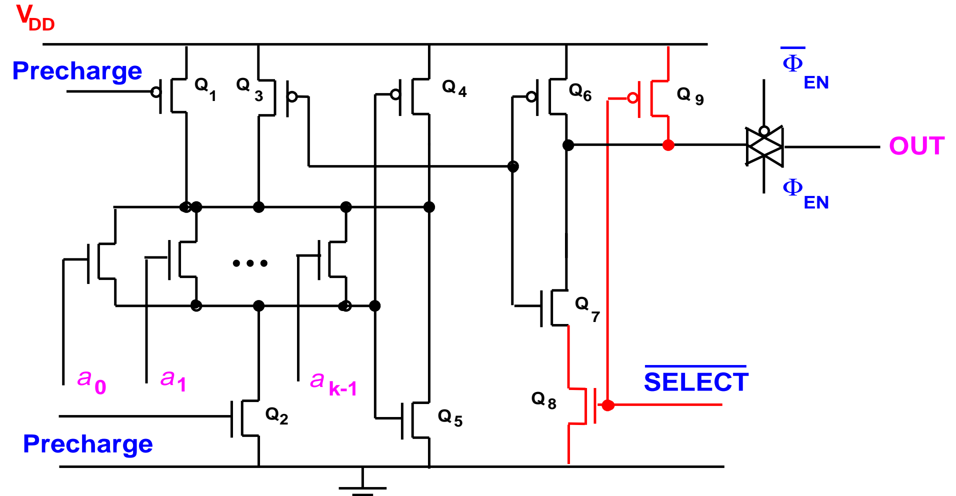
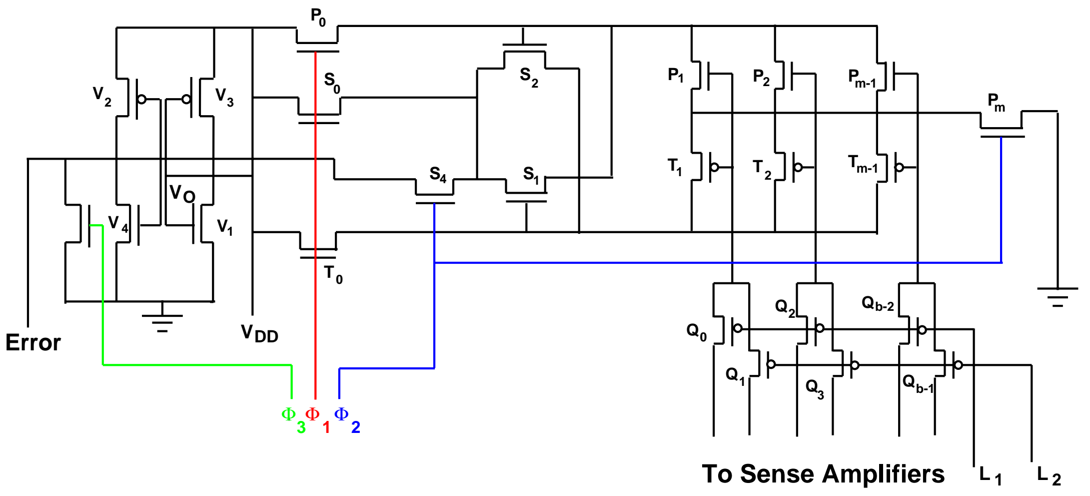
Testable Memory Design

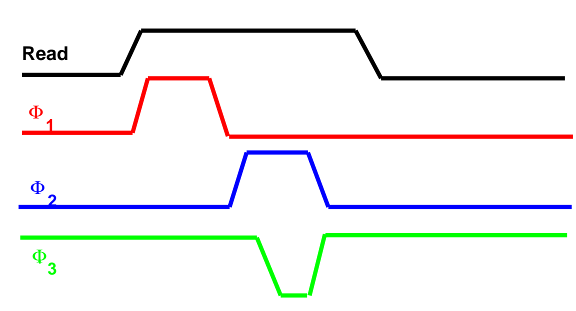


- Multiple-cell access
- Parallel read/write



- Matches pitch-width (3λ) of DRAM
- Test algorithm independent
- Low overhead





- Parallel compare

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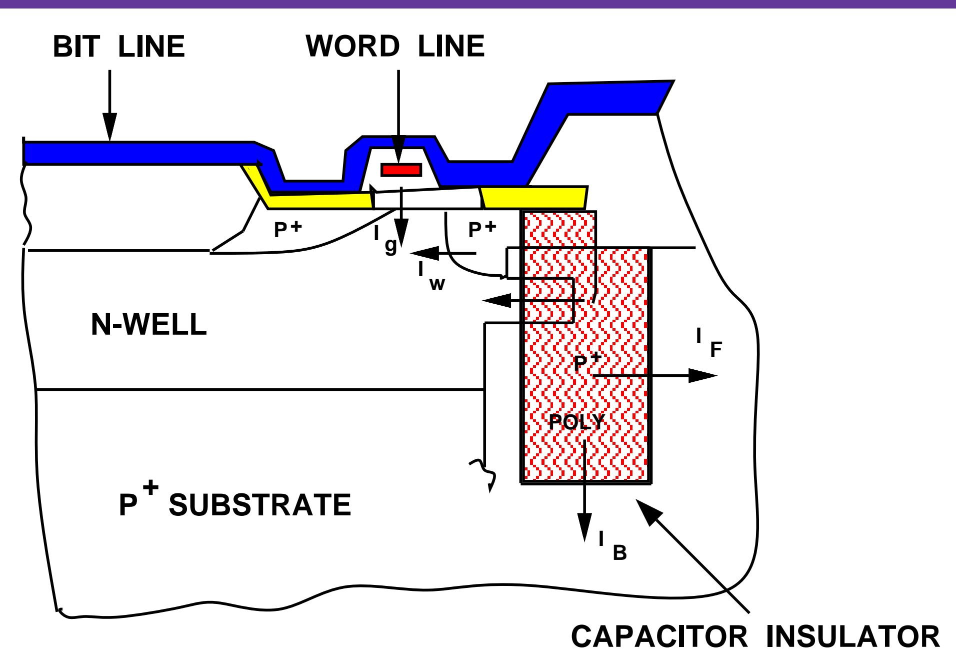
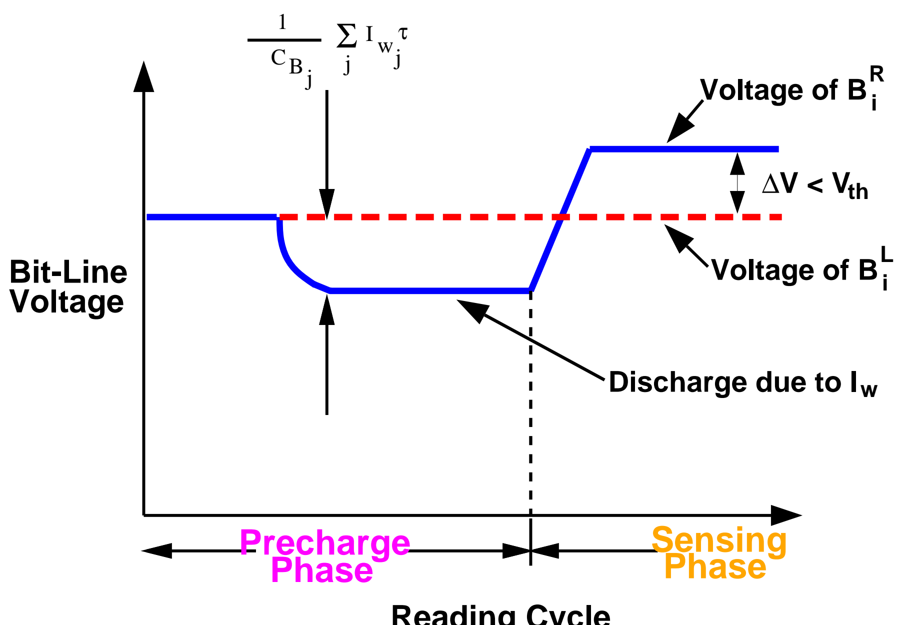
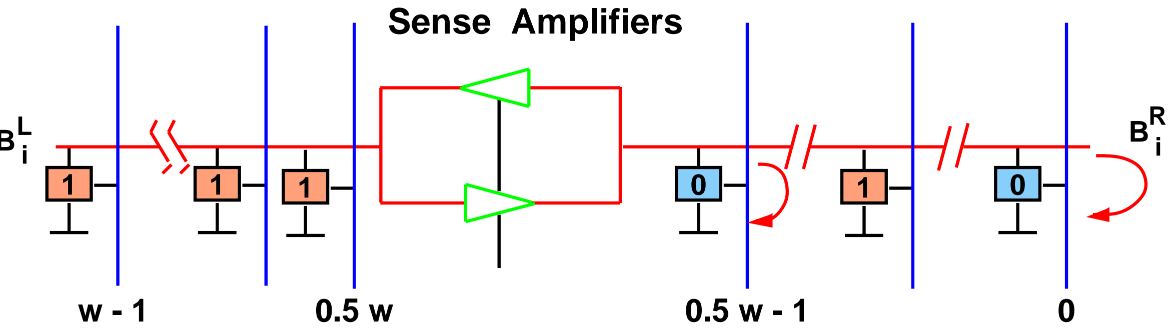
Technology-Related Faults





I_W: Weak inversion current
I_F: Field inversion current
I_B: Bulk or dark current

Column-Pattern-Sensitive Fault



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Technology-Related Faults

Bit-Line to Word-Line Crosstalk

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Testing of Technology-Related Faults

Proposed three parallel algorithms:

- **Algorithm 1**: Parallel Parametric Walking Test
  - Test Complexity: $10\sqrt{N}\tau_A + 6\tau_R$; $\tau_A \rightarrow$ Access time, $\tau_R \rightarrow$ Refresh time.
- **Algorithm 2**: Bit-line and Word-line Decoders Test
  - Test complexity: $20\sqrt{N}\tau_A + 2\tau_R$
- **Algorithm 3**: Power-supply Voltage Transition Test
  - Test complexity: $4\sqrt{N}\tau_A + 2\tau_R$

Algorithms and their Coverage of Parametric Faults

Fault Type	Algorithm 1	Algorithm 2	Algorithm 3
Weak-inversion current	No	Yes	Yes
Field-inversion current	Yes	No	No
Dark current	Yes	No	No
Gate short	Yes	Yes	Yes
Multiple selection	No	No	Yes
Single-ended write	Yes	Yes	Yes
Bit Line Voltage Imbalance	No	Yes	No
Bit Line to Word Line Crosstalk	No	Yes	No
Transmission-Line Effect	Yes	No	No

Transistor Count Overhead $= 2\sqrt{pN} + p\log N - p\log p + 12p$; $p \rightarrow$ # of Subarray

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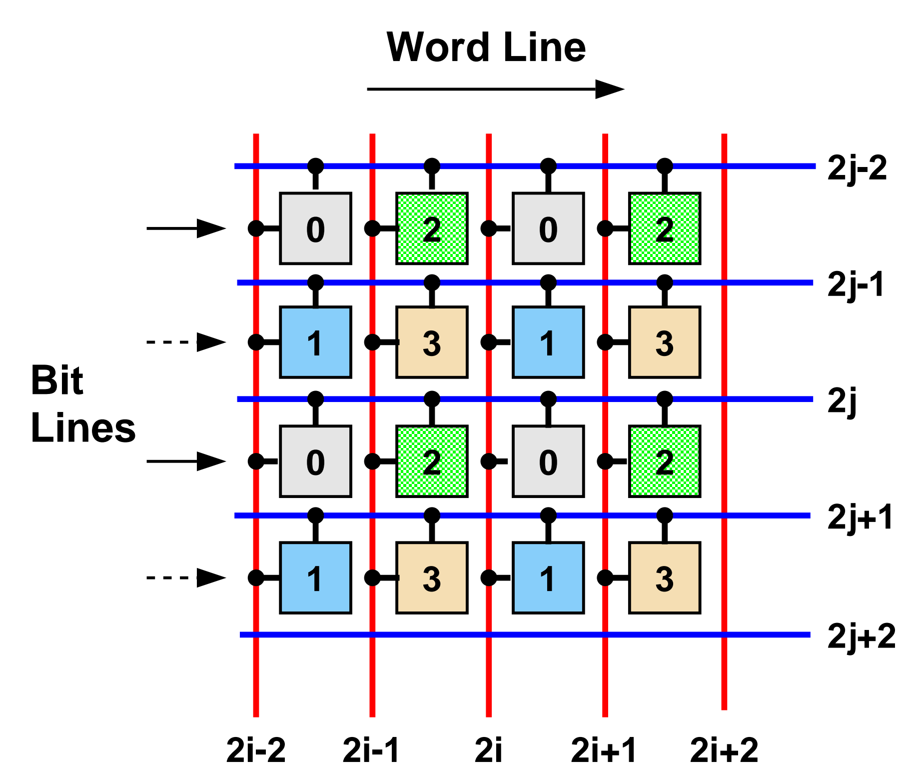
Parallel PSF Test



All possible SSPSFs and SDPSFs

Fault Type	Fault Notation			
SSPSF	↑/000,	↑/100,	↑/010,	↑/110,
	↑/001,	↑/101,	↑/011,	↑/111,
	↓/000,	↓/100,	↓/010,	↓/110,
	↓/001,	↓/101,	↓/011,	↓/111,
SDPSF	0/↑00,	0/↑10,	0/↑01,	0/↑11,
	1/↑00,	1/↑10,	1/↑01,	1/↑11,
	0/↓00,	0/↓10,	0/↓01,	0/↓11,
	1/↓00,	1/↓10,	1/↓01,	1/↓11,
	0/0↑0,	0/1↑0,	0/0↑1,	0/1↑1,
	1/0↑0,	1/1↑0,	1/0↑1,	1/1↑1,
	0/0↓0,	0/1↓0,	0/0↓1,	0/1↓1,
	1/0↓0,	1/1↓0,	1/0↓1,	1/1↓1,
	0/00↑,	0/10↑,	0/01↑,	0/11↑,
	1/00↑,	1/10↑,	1/01↑,	1/11↑,
	0/00↓,	0/10↓,	0/01↓,	0/11↓,
	1/00↓,	1/10↓,	1/01↓,	1/11↓,

Comparison of Different PSF test algorithms

RAM Size	256 Kb	1 Mb	4 Mb	16 Mb
No. of Partitions (p)	4	8	8	16
Hayes' Test $(3k+2)2^k n$	28.5 s	114.1 s	456.3 s	1825.3 s
Suk & Reddy's Test $(k+5)2^{k1}$ n	8.4 s	33.6 s	134.2 s	536.9 s
Proposed Test $195(n/pe)^{0.5}$	9.2 ms	12.8 ms	25.6 ms	36.4 ms

- Write on even/odd bit lines
- Read through parallel detector
- Tessellation reduces test complexity

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Deterministic BIST for Embedded Memories

- Covers SAF, TF, PSF, CF

Eulerian Tour

Word Line

Bit Lines

2j-2				
0	2	0	2	
2j-1				
1	3	1	3	
2j				
0	2	0	2	
2j+1				
1	3	1	3	
2j+2				

2i-2 2i-1 2i 2i+1 2i+2

(N w)

0	0	0
1	1	1
0	0	0

0	1	0
1	1	1
0	1	0

0 = <0000>
1 = <0001>
2 = <0010>
....
14 = <1110>
15 = <1111>

Hamiltonian Cycles

H2 → H1 ←

H4 → H3 ←

H5 → H6 ←

H7 → H8 ←

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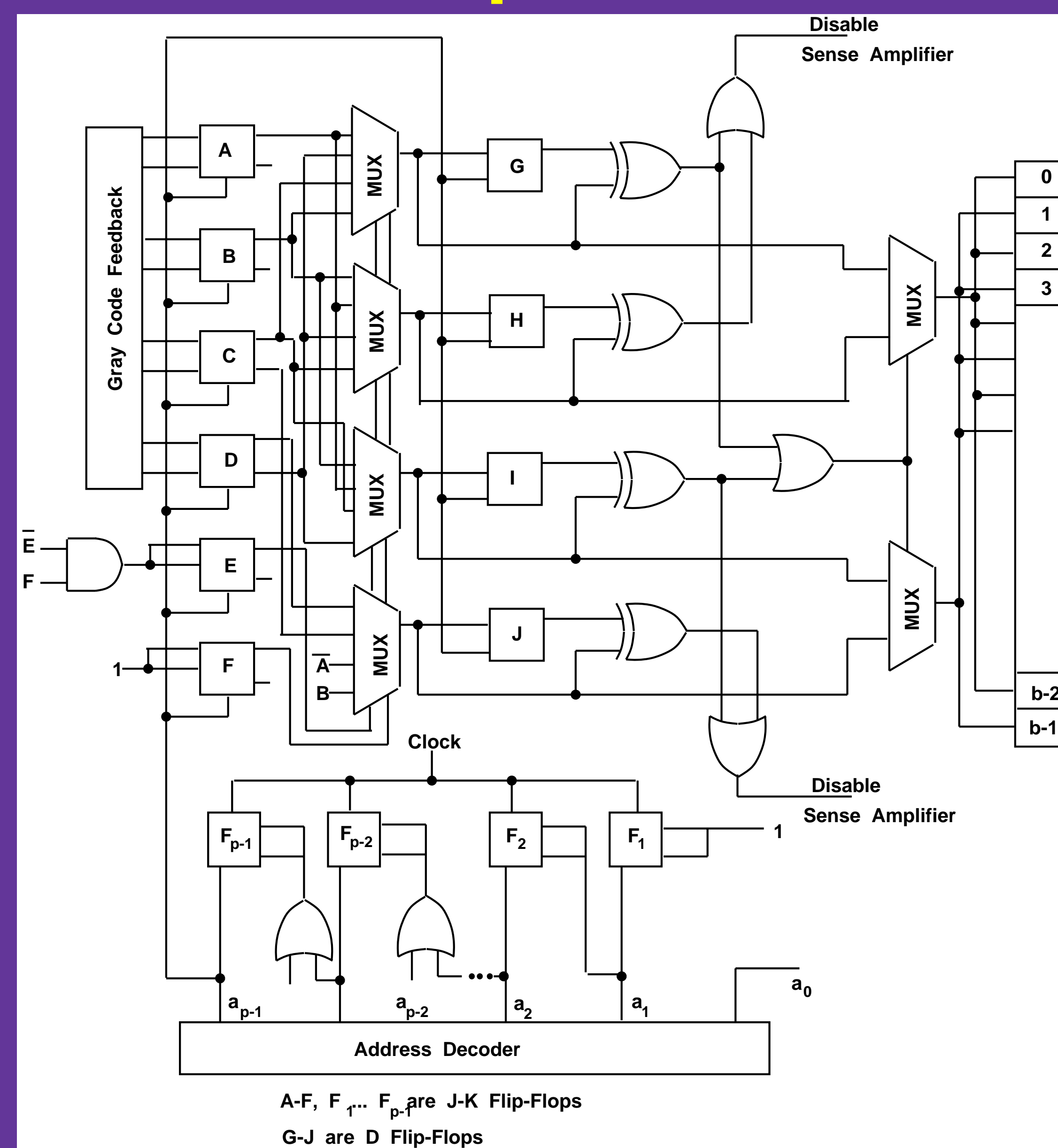
BIST Implementation of Embedded RAMs



Test Size Optimality versus BIST Hardware

Component	Hamiltonian Tour	Eulerian Tour	Extra Component
	$34w + 2b + 64$	$33w + 2b + 64$	
Flip-flop	$7 + p$	$10 + p$	3
MUX (4 to 1)	0	4	4
MUX (2 to 1)	1	2	1
XOR Gate	3	4	1
OR Gate	1	8	7
AND Gate	3	15	12
Inverter	1	1	0

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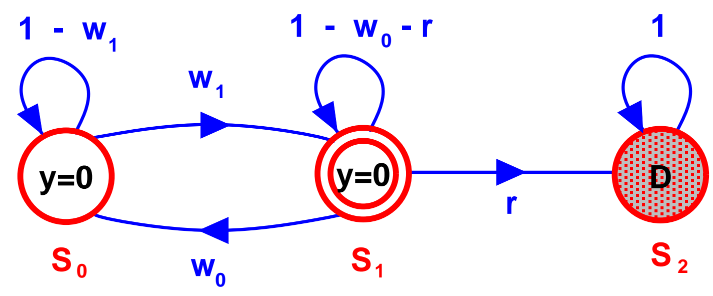
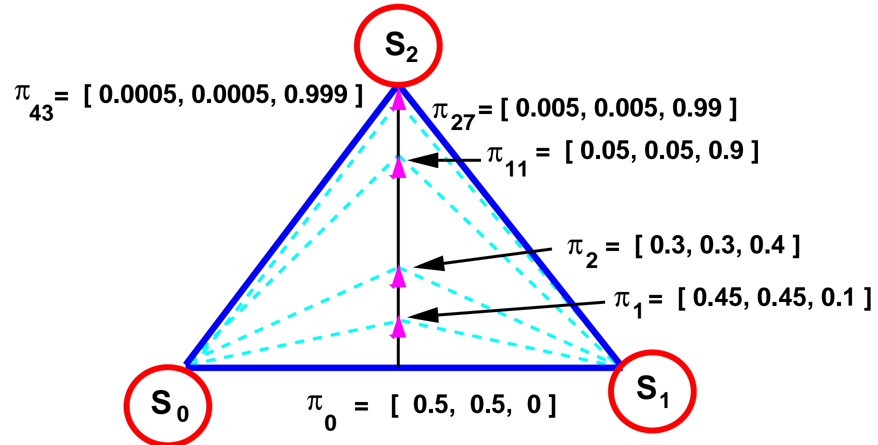
Random Testing of Embedded Memories

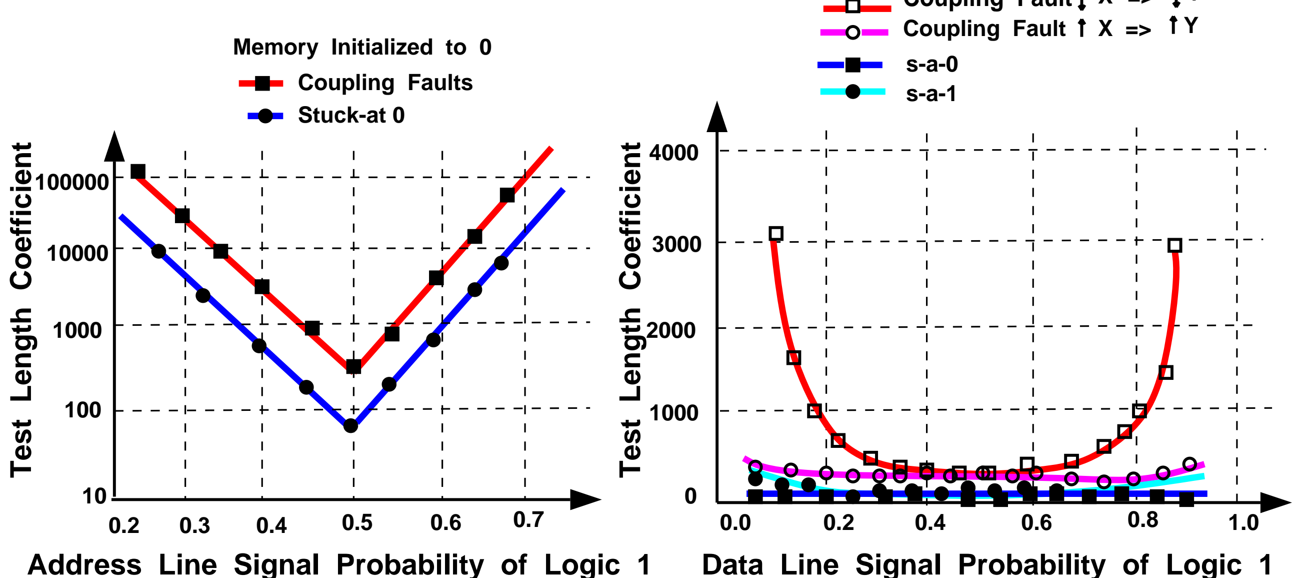
- Register file, FIFO, buffer

Stuck-at Fault





$$\begin{bmatrix} P_L(S_0) \\ P_L(S_1) \\ P_L(S_2) \end{bmatrix} = \begin{bmatrix} 1-w_1 & w_0 & 0 \\ w_1 & 1-w_0-r & 0 \\ 0 & r & 1 \end{bmatrix}^L \begin{bmatrix} I_0 \\ 1-I_0 \\ 0 \end{bmatrix}$$



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Random Testing of Embedded Memories

$CF_{id}(\uparrow,0)$

$SNPSF\,(\uparrow,S)$

100,000 sample random tests for ↑ X => ↑ Y obtained by fault simulation. Average Test Length Coeff. = 30.

Quality of Detection

Number of Samples

L=225

Number of Samples

Quality of Detection

Test Length Coefficient

Static NPSF <^, S>

Neighborhood Size

3 Cells
4 Cells
5 Cells

L=1531

Quality of Detection

Test Length Coefficient

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DFT for Random Testing

- No memory initialization problem
- No LFSR / No aliasing

LATCH ENABLE
EVEN
ODD
LATCH ENABLE
TP
P_j
R_j
L^E_j
L^O_j
E_j
O_j
O_{E_j}
O_{O_j}

0 1 WORD LINES w - 1
b - 1
1 BIT LINES
0
Error Latch Enable
O_0 E_0 O_1 E_1 O_{w-1} E_{w-1}
WRITE-SENSING LATCHES
LATCH ENABLE
ODD
EVEN

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Soft Error in DRAMs

Transfer Gate
Bit Line
Isolation
Word Line
N+
P-
P+
Storage Node
Cell Plate
α
α –Particle

Voltage
$V_P = V^*$
1 is Read
$\Delta V > V_{th}$
$\Delta V > V_{th}$
0 is Read
Precharge
Sense

Voltage
V^R
α - Particle
$\Delta V < V_{th}$
Precharge
Sense

Voltage
V^R
α- Particle
$\Delta V < V_{th}$
Precharge
Sense

Sense Amplifiers

$\overline{\text{BIT}}$
BIT
WORD LINE
WORD LINE
Q_C
Q_C
Q_R
Q_R
Q_C
Q_C
Reference Cell
Reference Cell
0

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The Soft-Error Rate Simulation System

MASK AND PROCESS INFORMATION

3D TOPOGRAPHY SIMULATION

PROCESS SIMULATION DEVICE SIMULATION

METAL-WIRING TOPOGRAPHY

PARASITIC DEVICE PARAMETER

EQUIVALENT CIRCUIT

ALPHA-PARTICLE EMISSION RATE

SPICE SIMULATION

PROBABILITY OF ALPHA-PARTICLE INCIDENCE (P)

SOFT ERROR OCCURRENCE FUNCTION (F)

SOFT-ERROR RATE
S = P x F

Alpha-Particle Incidence Probability Calculation

Alpha-particle Source

ΔV_n

Rutherford Scattering in Oxide

Diffusion Layer

ΔA_m ΔA_0

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Double-Error Correcting Codes

BIT LINES

WORD LINE

SENSE AMPLIFIERS

MUX PARITY XOR

X(i)

Y(j)

D(t)

Augmented Product Code

INPUT ADDRESS

Subarray No. 1 Subarray No. 2 Subarray No. 3 Subarray No. 4

Total Number of Information Bits = 64.

Total Number of Parity Bits = 49 (not shown).

Bits labeled identically are accessed simultaneously to compute q_1

Bits in a row are accessed simultaneously to compute p_1

Euclidean Space

Projective Geometry Space

Field Plane Hexagon

Comparison of Some Coding Techniques

Criterion	Hamming Code (SEC)	Product Code	Projective Geometry	Mazumder 's APC
Cell Redundancy	$\lg(1+n)/n$	$2(s/n)^{1/4}$	$2/n^{1/3}$	$3(s/n)^{1/4}$
Min. Code Distance	3	4	6	5
Error Correction	SEC	SEC	DEC/TED	DEC
Fault Detection	Simple	Simple	Complex	Simple
Address Computation	Simple	Simple	Galois Field	Simple
Layout Complexity	Low	Low	High	Medium
Area Overhead	Low	Low	High	Medium
Decoding Time	Small	Small	Large	Medium

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Technology-Related Tests for SRAMs

TECHNIQUES USED

SIMULATION

INDUCTIVE FAULT ANALYSIS (IFA) FOR LAYOUT DEFECTS

(Models shorts and opens as spots of missing metal or extra metal, e.g., data-retention problem due to broken load)

ANALOG CIRCUIT SIMULATION (VIA SPICE)

(for various design, layout, and wide device parameter scattering related defects)

CURRENT MEASUREMENTS

QUIESCENT POWER SUPPLY CURRENT (I_{DDQ})

(for stuck-open and bridging faults)

DYNAMIC POWER SUPPLY CURRENT (I_{DD})

(for more detailed defect mechanisms, e.g., gate-oxide short, punch-through, leakage)

OPEN-CIRCUIT TEST + CELL-ARRAY CURRENT TEST SOFT DEFECT DETECTION (SDD)

(for stuck-open faults and static data loss)

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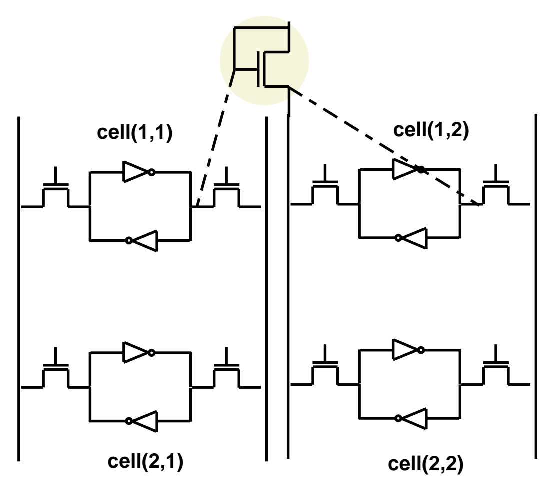
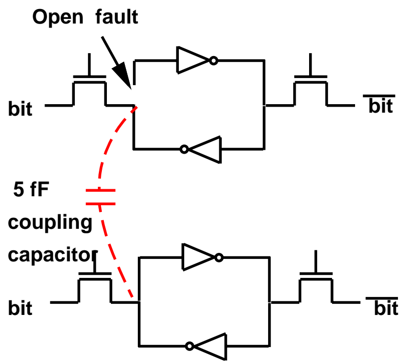
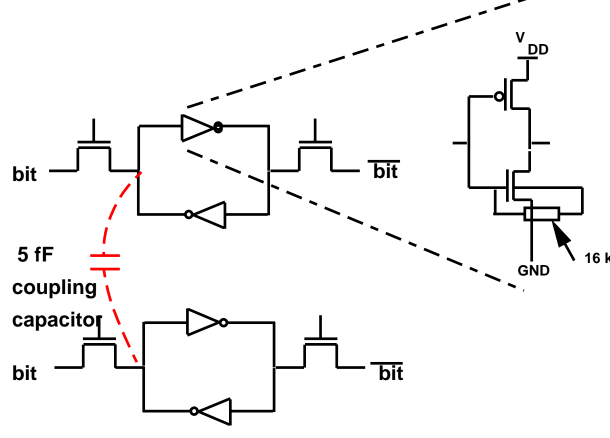
Defect Models in SRAM



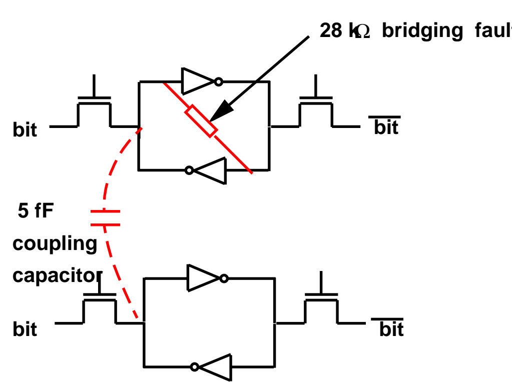
PSF induced by means of a diode-connected P-type transistor



PSF caused by open fault and a weak coupling capacitor



PSF caused by oxide short and a weak coupling capacitor



PSF caused by bridging fault and a weak coupling capacitor

Dynamic Current (I_{DD}) Testing

- Diode-connected transistor short
- Open Fault
- Gate oxide short
- Bridging faults
- Use current monitors for:
  - Voltage transient
  - Ground transient

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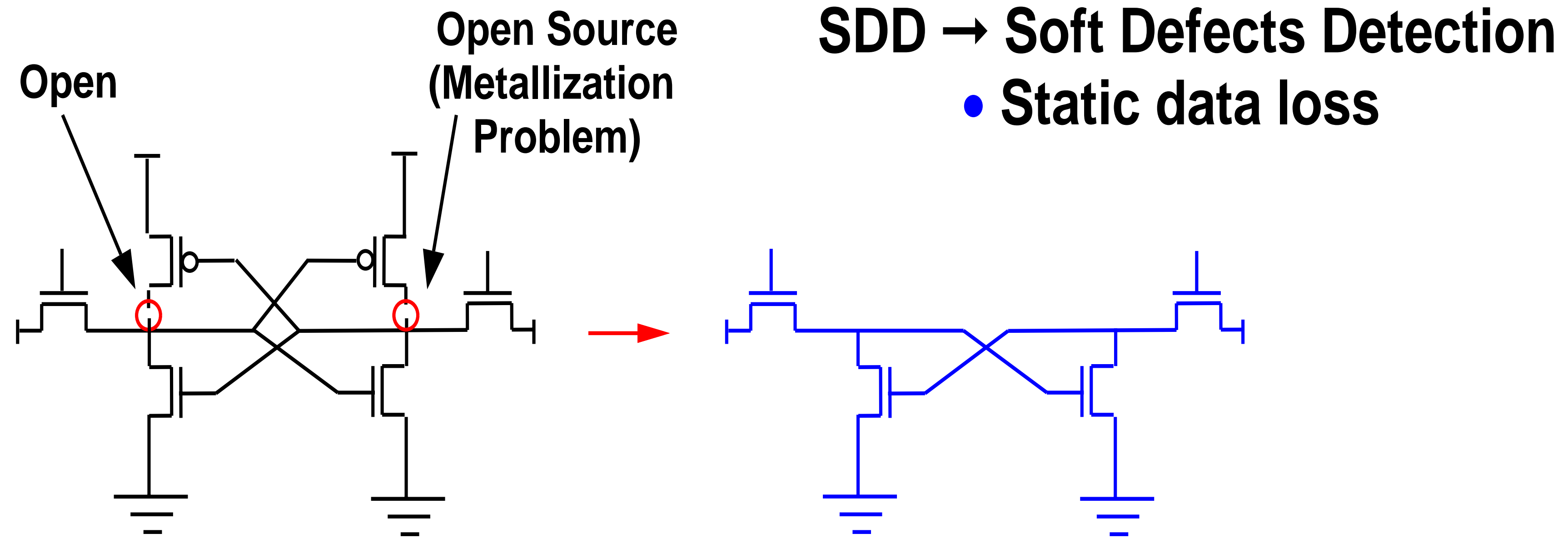
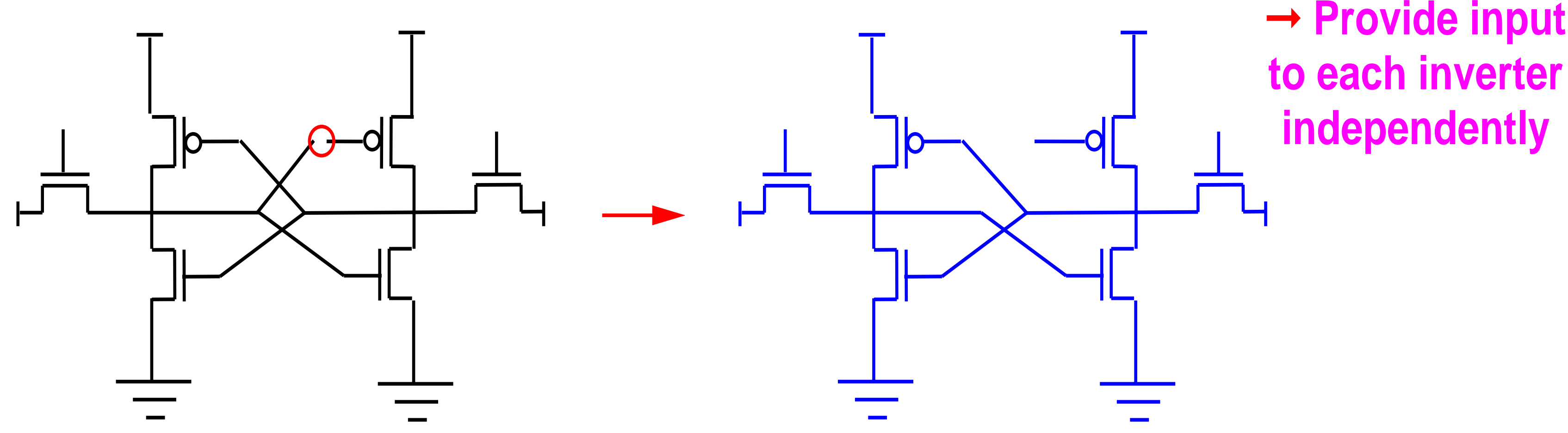
Fault Models for SRAMs

SDD → Soft Defects Detection

- Static data loss



Open source fault and its equivalent circuit.



→ Provide input to each inverter independently

Open gate fault and its equivalent circuit

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High Electron-Mobility Transistor

SOURCE GATE DRAIN

Metal

n-AlGaAs

2D Electron Gas

GaAs (undoped)

n - GaAs Substrate

GATE

SOURCE

DRAIN

$$C_{GS} \cong 5C_{DG} \cong 10C_{DS}$$

GATE

C_{GS} I_{DS} C_{DG}

SOURCE

DRAIN

C_{DS}

I_{DS}

Linear

Saturation

Kink Effect

V_T

V_{DS}

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Defect Classification in GaAs SRAMs

Primary defects

- Material-related: compositional purity, crystalline perfection, control of stoichiometry
- Examples:
  - Threshold voltage variation
  - Mobility degradation
  - Charge-trapping
  - Oval defects
  - Kink effect in I-V characteristics

  Threshold voltage spread: $V_{TE} = 0.278$ V, $\sigma(V_{TE}) = 11.3$ mV
  $V_{TD} = -0.602$ V, $\sigma(V_{TD}) = 14.2$ mV

Secondary defects

- Wafer-processing-related
- Examples:
  - Stuck-at faults
  - Bridging faults
  - Ohmic contact degradation

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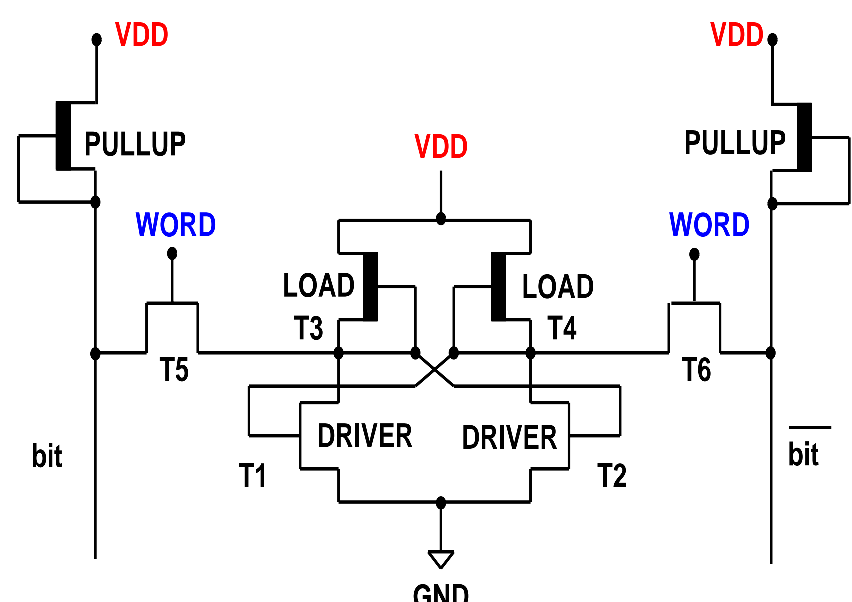
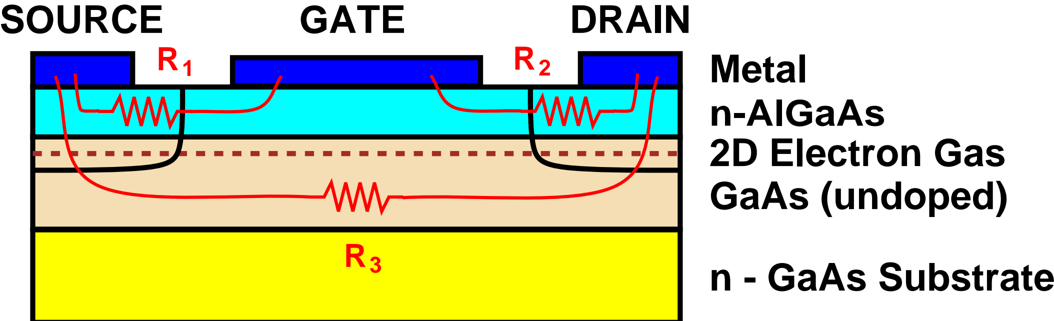
Gallium Arsenide HEMT RAMs

Basic RAM Cell



- $\alpha = I_{DS}(\mathrm{ON})/I_{DS}(\mathrm{OFF})$
  $\alpha_{Si} = 10\mathrm{K},\ \alpha_{GaAs} = 200$ → High leakage current
- $V_{DD} = 1\mathrm{V},\ V_H = 0.8\mathrm{V},\ V_L = 0.2\mathrm{V}$
- $\mu_{HEMT} = 20\mu_{Si}(300°\mathrm{K})$
  $\mu_{HEMT} = 200\mu_{Si}(77°\mathrm{K})$

Cross-sectional View



- $R_1, R_2 \approx 100\Omega$ to $2\mathrm{K}\Omega$ → Read/write failure, delay faults
- $R_1, R_2 > 5\mathrm{K}\Omega$ → Correct performance

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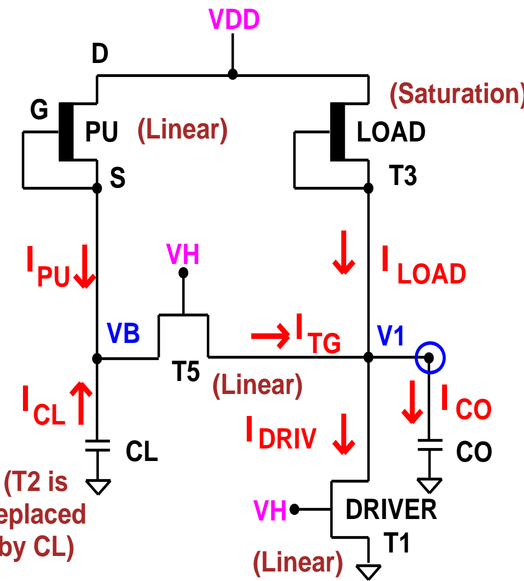
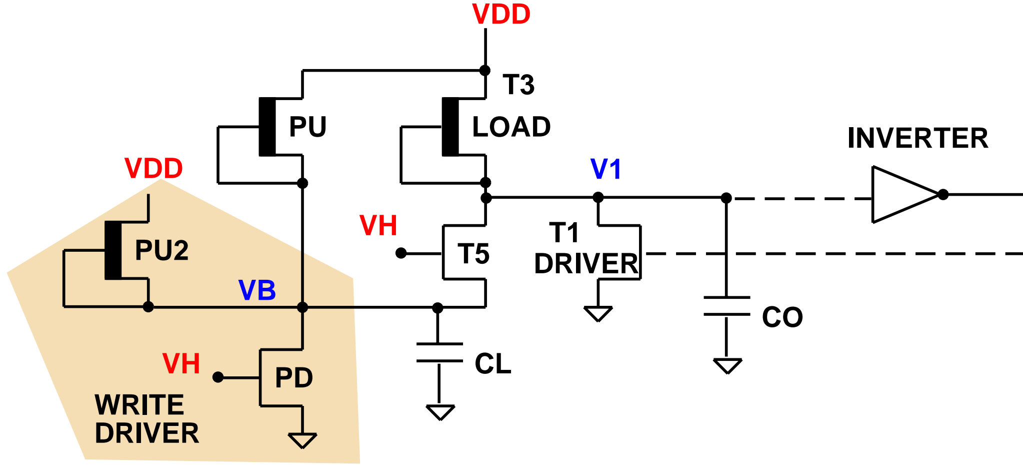
Read/Write Operation

Goal: To determine the range of the V_{TD} and V_{TE} for which V_1 at the end of read does not increase above V_T of T_2.



Write Operation



$$V_1 = \frac{(\beta'_{PU} + \beta_{LO})V_{TD}^2}{\alpha\beta_{DR}(V_H - V_{TE})^2}$$

$\beta'_{PU} = \beta_{PU}\tanh(\alpha V)$,

$V = V_{DS\ of\ PU} \approx 0.1\mathrm{V}$

- Cell stability problem when $v_1 \to v_{TE}$ before READ pulse is complete

$$V_B = K_4 e^{K_0\tau} - K_1/K_0$$

$$\tau = \text{Access time} = f(\beta_{PU}, \beta_{TG}) = \frac{\log\left(\frac{K_4}{K_0}(V_B + K_0)\right)}{K_0}$$

$$K_0 = -(\beta_{PU}V_{TD}\alpha)/C_L,\ K_4 = V_H + (K_1/K_0)$$

$$K_1 = -\beta_{TG}(V_H - V_{TE} - V_1)^2/((C_L + \beta_{PU}V_{TD}\alpha V_H)/C_L)$$

$V_H \to$ Initial value of V_B

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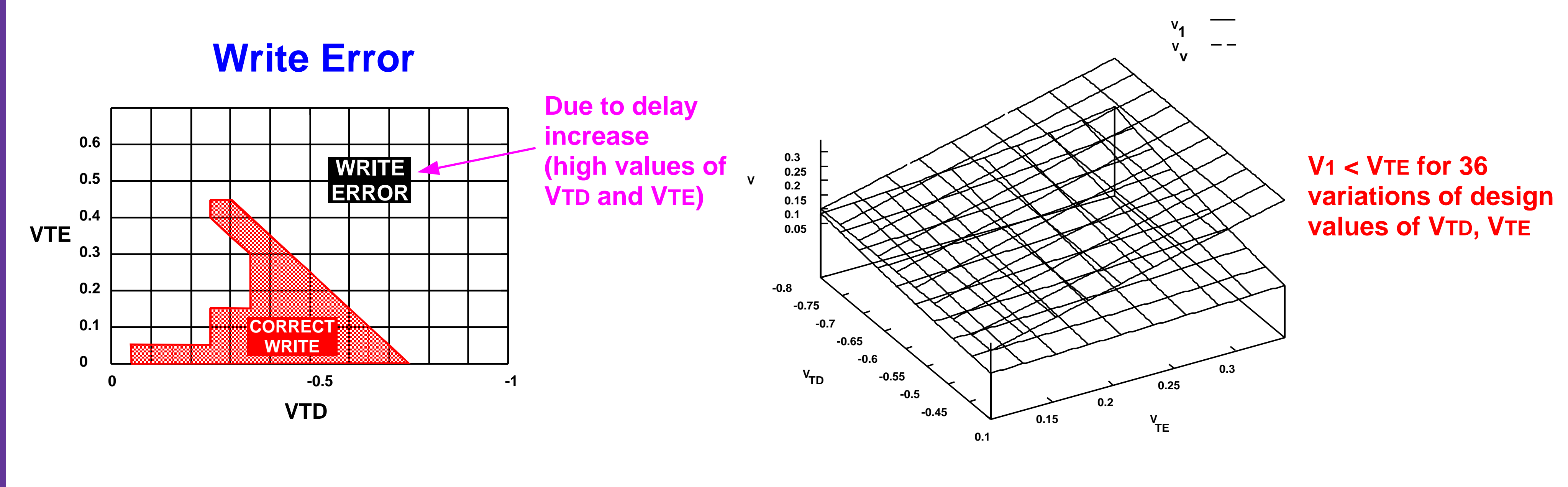
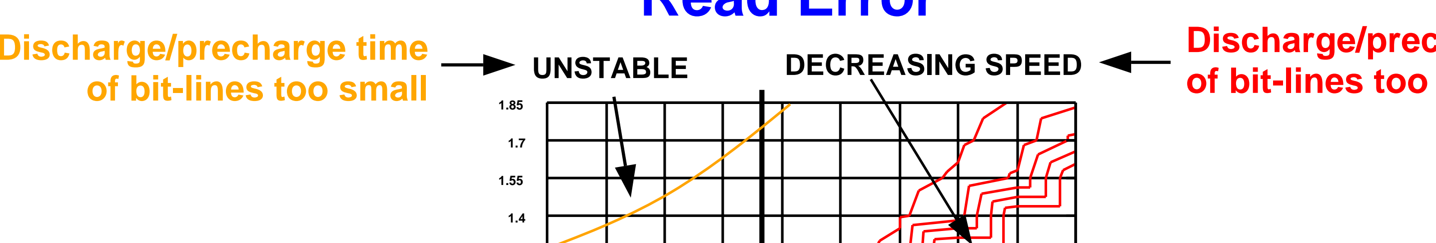
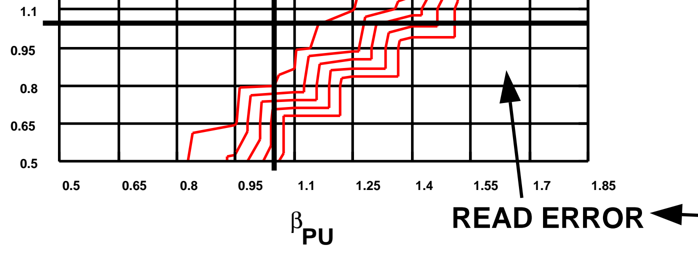
Read/Write Errors







$$0.5\,\hat{\beta} \le \bar{\beta} \le 2.0\,\hat{\beta}$$

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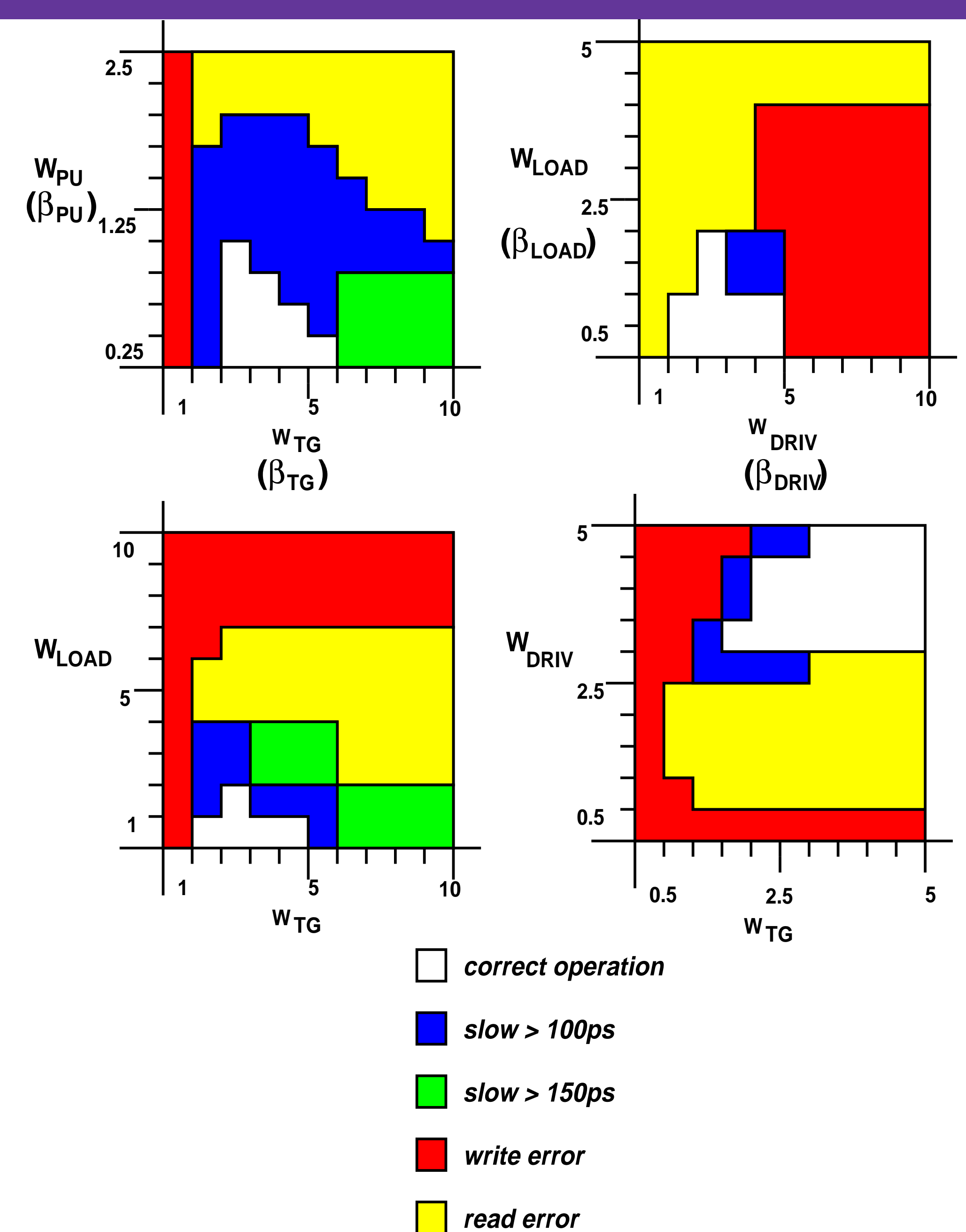
Effect of Parameter Variations

	VTE			
VTD	0.1V	0.3V	0.5V	0.6V
0.1V	Error	OK	OK	Error
0.3V	OK	OK	OK	δ > 100μs
0.5V	OK	δ > 100μs	δ > 100μs	Error
0.6V	δ > 100μs	δ > 100μs	Error	Error
0.7V	δ> 100μs	Error	Error	Error



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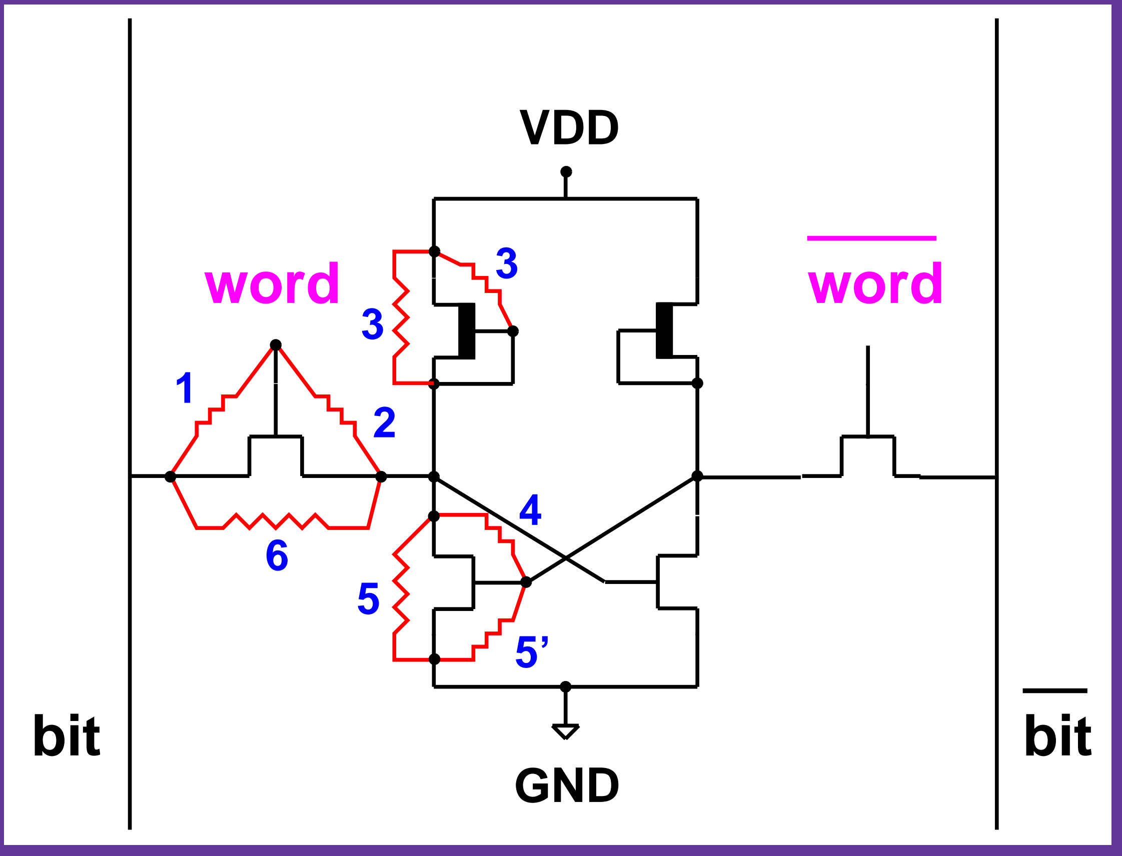
Catastrophic Failure Modes

Canonical Set of Resistive Paths

1. Bit to word-line
2. Word-line to storage node
3. Storage to power supply
4. Storage to complementary node
5. Storage to ground
6. Bit-line to storage node



- Resistance shorts between transistor electrodes (GS,GD) increases leakage currents
- Bridging of metal lines: shorts between two adjacent signals
- Stuck-open transistors

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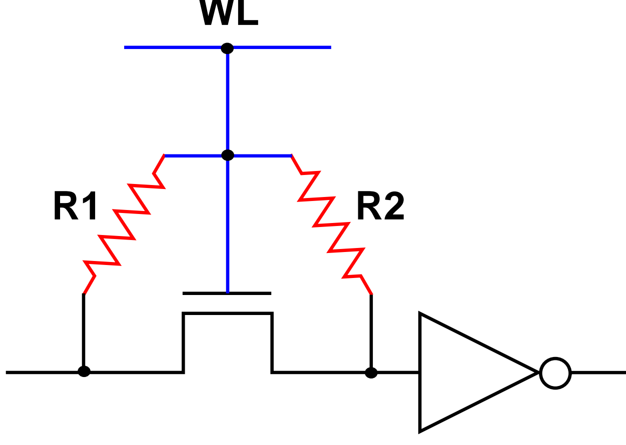
Read and Write Errors



Read and Write Errors Caused by Different Failure Modes

Gate-source short on transmission gate - *bit* line to *word* line

Resistance (ohms)	Write	Read	Comments
R1: 100	Write 0 fails Write 1 delay < 100 ps	Weak 1	Write 0 fails Write/Read 1 slow
500	Write 1 delay > 100 ps Write 0 fails	Weak 1	
1000	Delay > 100 ps	Read 0 fails	
2000	Delay > 150 ps	Same as above	

Gate-source short on transmission gate: *word* line to cell

Resistance (ohms)	Write	Read	Comments
R2: 100	Cell follows *word* line		Cell follows *word* line
500	Weak 1 - decays after 22 ps	Read 1 error	
1000	Weak 1 - decays after 60 ps	Read 1 error	
2000	Weak 1 - decays very slowly	OK	Data retention problem
5000	OK	OK	OK

Coupling between cells of the same *bit* line due to a *bit* line to *word* line short in one of the cells

Resistance (ohms)	Write	Read	Comments
100	Write 1 fails	Read error	
500	Write 1 fails	Read error	
1000	OK	Read 1 error	Cell flips to 0 when read
2000	OK	Read 1 error	
5000	OK	OK	OK

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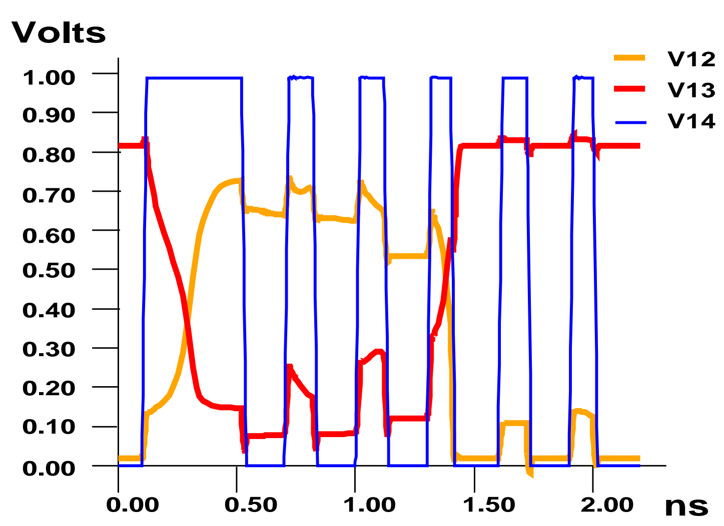
Parametric Testing for Layout Defects



- Write operation followed by three read operations, the last one causes the cell to change states

Fault Type	Causes	Tests
Stuck-at Simple coupling	Parameter variations, Resistive bridging, Leakage current (parametric)	8N March Test
Stuck-open Delay faults	Resistive Bridging / Leakage Currents	At-speed Test (8N)
Data retention Row/Column Pattern Sensitive	Missing / stuck-open transistors Resistive Bridging / Leakage Currents (parametric)	Temperature and voltage stress with stuck-at tests or exhaustive row/column patterns, Sliding diagonal

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GaAs SRAM Faults

- Design-Related Faults
  - **Causes**: Process and temperature variations causing threshold voltage shift of load and enhancement devices.
  - **Fault Types**: Delay faults + erroneous read/write operations
  - **Tests**: Perform reads and writes and compute the access delays
- Catastrophic Faults
  - **Causes**: Process and material-related gross defects
  - **Fault Types**: Shorts between transistor terminals & metal lines+ Stuck-open transistors
  - **Tests**: Sliding diagonal + tests for shorts and opens

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Concluding Remarks

- Technology and layout-related testing performs accurate fault-modeling from a circuit and layout point of view.
- Device and circuit-specific tests for SRAMs have been described. Main techniques:
  - Process and circuit simulation
  - Soft-defect detection (SDD)
  - Quiescent power supply current (I_{DDQ})
  - Dynamic power supply current (I_{DD})
- Design for testability and parallel test algorithms for DRAMs have been described.
- Deterministic and pseudorandom BIST for embedded RAMs have been described.
- Parametric failures and soft errors in DRAMs with trench capacitors have been described.

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Masking Faults

(a) Isolated Opaque Spot / Pin Dot

(b) Isolated Pinhole

(c) Edge Protrusion

(d) Edge Intrusion

(e) Break in Geometry

(f) Bridge between two Geometries

(a) Edge Protrusion + Undersized Geometry, e.g., gate structure

Nominal Size

(b) Edge Protrusion + Undersized Contact

Nominal Size

(c) Single Contact below Design Specification

Nominal Size

Minimum Size

(d) Single Contact not Cleared Out

(e) Subspecification Defect on Undersized Geometry

Nominal Size

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Fault Classification

Functional Faults
- SAF
- CF
- PSF

Device Processing Parametric Faults

Masking & Fabrication Faults

Analog Simulation
& Stress Testing

Delay Testing

Technology
& Layout
Related
Faults

IDDQ -> Static Current
IDD -> Dynamic Current
SDD -> Soft Defects

Current
& Voltage
Testing

Analytical modeling
+ Simulation
-> Behavioral modeling

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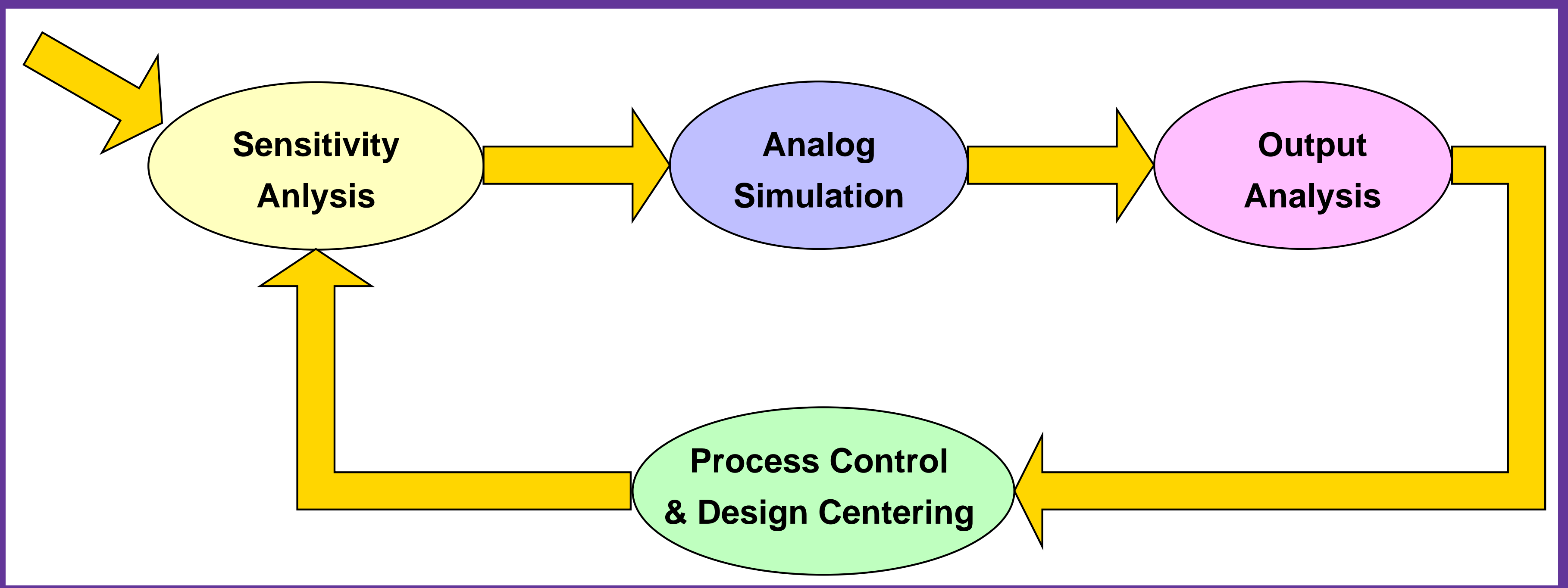
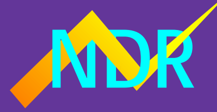
Testing of Device Spread





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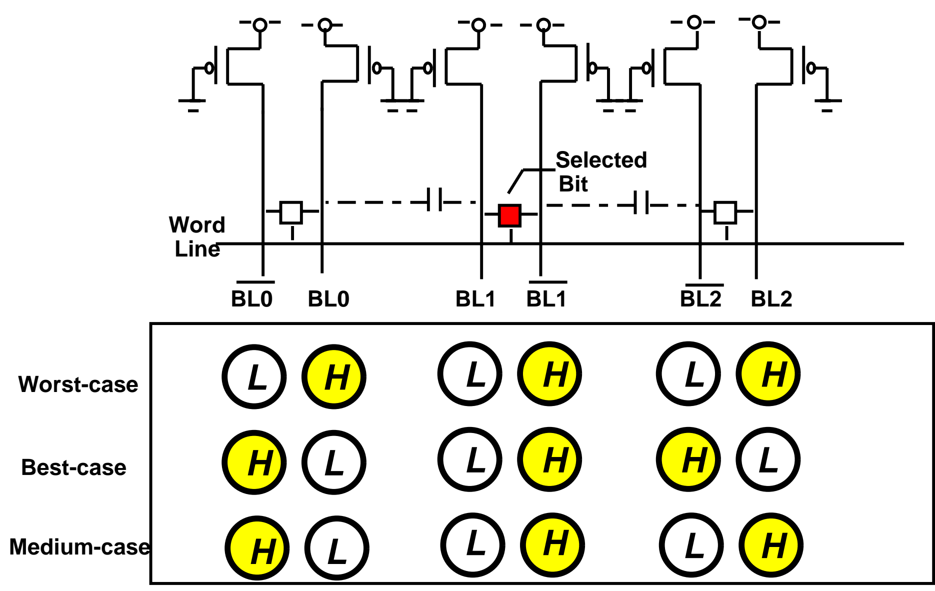
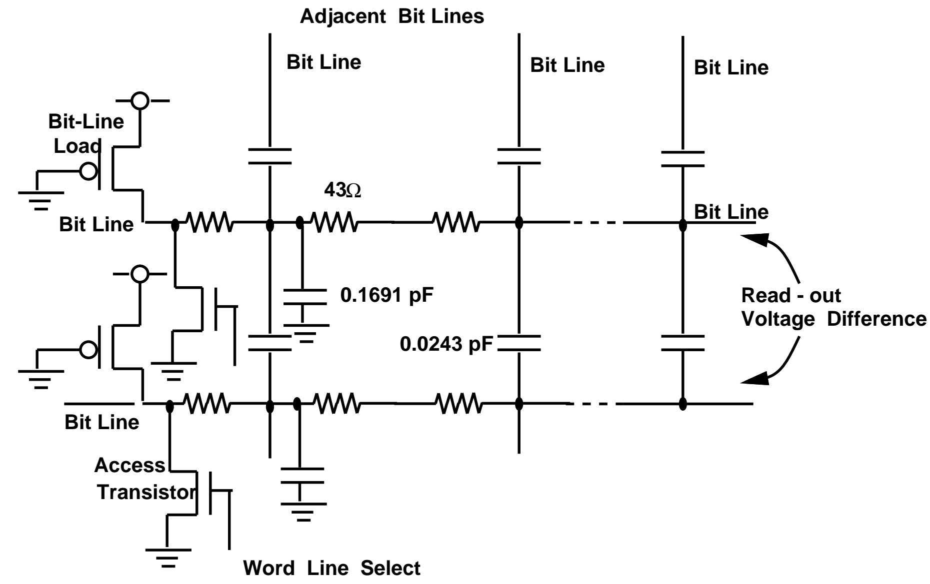
Delay Time Testing for SRAM

Simulation test pattern



Bit-line model



Simulation parameters for three generations of process technology

Proc.	# Memory Cells						Cell Size (μ^2)	PMOS Bit-line Load L/w (μ^2)		Supply V.
	1024			2048						
	CL (pf)	CB (pf)	R(Ω)	CL (pf)	CB (pf)	R(Ω)		ΔV = 200 mV	ΔV = 30 mv	
0.8-μ 1 Mb	0.194	1.353	683	0.388	2.705	1365	49.30	1.2/6.0	1.2/30	5.0
0.5-μ 4 Mb	0.187	0.853	638	0.374	1.718	1277	18.96	0.9/4.0	0.9/20	5.0
0.35-μ 4 Mb	0.238	0.412	497	0.476	0.824	995	7.29	0.6/2.6	0.6/13	3.3

CL: metal1 intermetal capacitance, CB: metal1-poly capacitance

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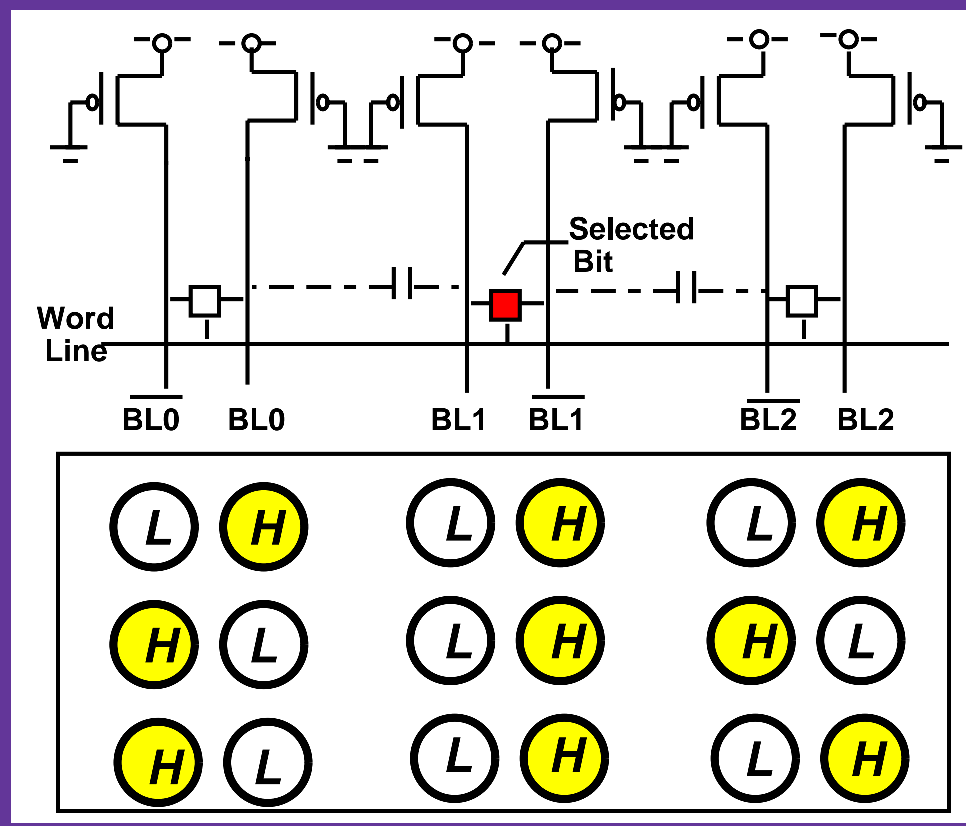
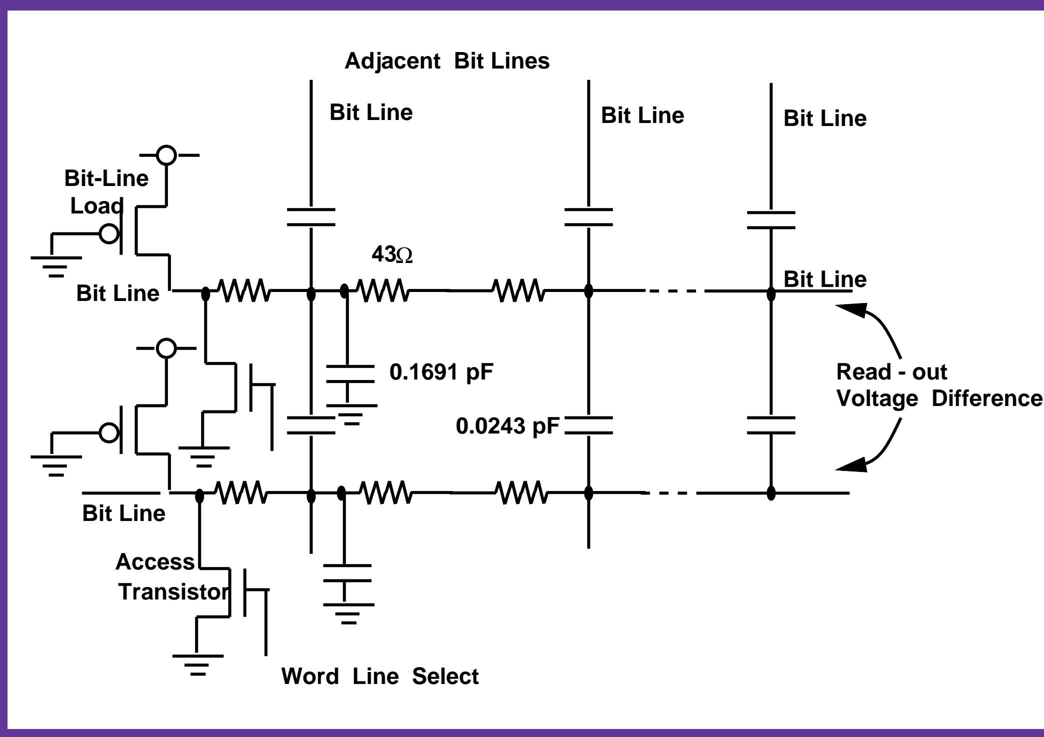
Delay Time Testing for SRAM

Simulation test pattern



Bit-line model



BISRAMGEN

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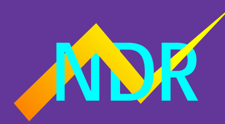

Built-in Self-Repair of VLSI Macrocells

- What?
  - Inclusion of circuitry that can **automatically** test and repair faulty components
- Why?
  - Improving the **production yield** with submicron CMOS technologies
  - Improving the **mean time to fail** and **fault-tolerance** during field use
  - Reducing the **difficulty** and **cost of external field repair** for ***embedded*** VLSI circuits, and in hazardous ***outer space*** and ***oceanic*** applications

In short, *built-in self-testing* (BIST) alone is not enough to deal with yield and reliability problems associated with modern VLSI technology

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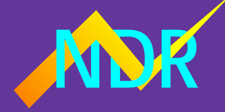

Silicon Compilation

- What?
  - Fully automatic layout generation for CMOS VLSI macrocells
- Why?
  - To reduce the design cycle time and increase the designer's efficiency
  - Layout quality can closely emulate full-custom layout quality
  - May achieve process and design-rule independence, portability and flexibility
- Why another CAD tool?
  - VLSI technology is progressing very aggressively and CAD tools for physical design are lagging behind
  - Major challenges: achieving timing targets, ensuring yield and reliability, ensuring testability and fault-tolerance, keeping cost low

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Silicon Compilation of RAMS

- Introduced in 1986 by Texas Instruments (***RAMGEN***)
- Some state-of-the-art RAM compilers:
- For simple RAM arrays without BIST and BISR:
  - ***CDARAM*** Compiler (for single and multiport RAMs) [Cascade Design Automation and Mitsubishi] (1990) [Shinohara, et al., Custom Integrated Circuits Conf.]
  - ***MEMORIST*** Compiler [Motorola and Mentor Graphics] (1992) [Tou,1992 IEEE J. Solid-State Circuits]
  - ***ARC*** GaAs MESFET RAM compiler [The University of Michigan] (1995) [Chandna, 1995, Ph.D. Thesis]
- For BIST RAMs:
  - BIST RAM Generator with **CADENCE ES2 SOLO 2030** [IMAG/TIM3 and Cadence] (1992) [Kebichi and Nicolaidis, 1992]
- For BISR RAMs:
  - *BISRAMGEN* [The University of Michigan] (1996) [Chakraborty and Mazumder]

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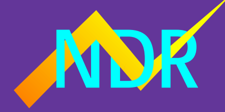

Overview of BISRAMGEN

Parameters
Technology data
Leaf Cell Library
MODULE GENERATOR
Layout of RAM-array, address generator, data pattern generator ..
Layout to Netlist converter (including parasitic extraction)
SPICE netlist
Macro-Cell Placement and Route
Verilog behavioral Model Generator
SPICE simulation and verification
BIST + BISR RAM layout
Behavioral model of BIST + BISR RAM
Functionally verified macro-cells and timing information
Back Annotation & Simulation
Functionally verified layout with timing analysis

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Self-test Technique Used by BISRAMGEN

- ***Test chosen***: Inductive Fault Analysis Based IFA-9 (or 9N test)

- Fault coverage:
  - **Stuck-at** faults
  - **Address decoder** faults
  - **Transition** faults
  - **Coupling** faults: unlinked idempotent and inversion coupling, pairwise state coupling
  - **Data retention** faults: RAM disabled for two 100ms delays

- March notation:
  - {⇑(w0),⇑(r0,w1),⇑(r1,w0),⇓(r0,w1),⇓(r1,w0),delay,⇑(r0,w1),delay,⇑(r1)}

- Two-pass testing:
  - **Pass 1:** Faults are detected and faulty addresses stored in a table
  - Pass 2: The RAM is re-tested with faulty address references being substituted by the mapped redundant addresses

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BIST/BISR Circuit Design

- Finite State Machine for Control Unit
  - **PLA**-based
  - Stores an ***espresso***-minimized version of the state table
- State Register
  - Uses 6 D Flip-Flops to encode 59 states
  - 6 state bits together with 7 status bits are used to address the PLA rows
- Test Address and Data Generators
  - Binary **up-down** counter, and **Johnson** counter, respectively, with 0 and max. count detection logic
- Reconfiguration Circuitry
  - Translation lookaside buffer (TLB) using a novel scheme for effective zero-delay penalty address diversion

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BIST/BISR Circuit Design (contd.)

- Static and Dynamic RAM Array Design
  - Uses wide-word organization and column mux'ed addressing, for better bandwidth
  - Single-port architecture
  - Simplified read/write circuitry: write select muxes, bitline pullup transistors, sense amplifier latch
  - Specified by geometry parameters: **bpc** (=bits per column), **bpw** (=bits per word), **N** (=number of non-spare rows), **S** (=number of spare rows)
  - Word-line drive circuitry includes multi-input NAND decoders and drivers
  - For DRAMs: 4T cells are used and the same sense amplifiers are used for both read and refresh, in time-multiplexed mode

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Characteristics of BISRAMGEN

- ***Process independence***
- ***Buffer sizes*** of various components can be user input
- ***Does not use*** any commercial standard cell library
- ***Fully automatic***: no netlist info needed
- ***Hierarchical place and route***
- ***Low area-overhead*** BIST and BISR design
  - **Three** layers of metal for routing

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Sample Layout Plot

(32 kilobyte SRAM)

- **Process:** CDA0.7μ3m1p CMOS
- RAM geometry parameters:
  - Number of words = 4096
  - Bits per word = 64
  - Bits per column (i.e., degree of column-multiplexing) = 8
  - Number of spare rows = 1
  - Buffer size in RAM array = 1 (i.e. minimum buffer size)
  - Strap space = 1 every 32 cells
- Layout area is about 15.5 mm^2
- Number of transistors is about 1.7 million
- **Note:** Due to column-multiplexing, 1 spare row can replace at most 8 faulty words

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Sample Layout Plot (contd.)

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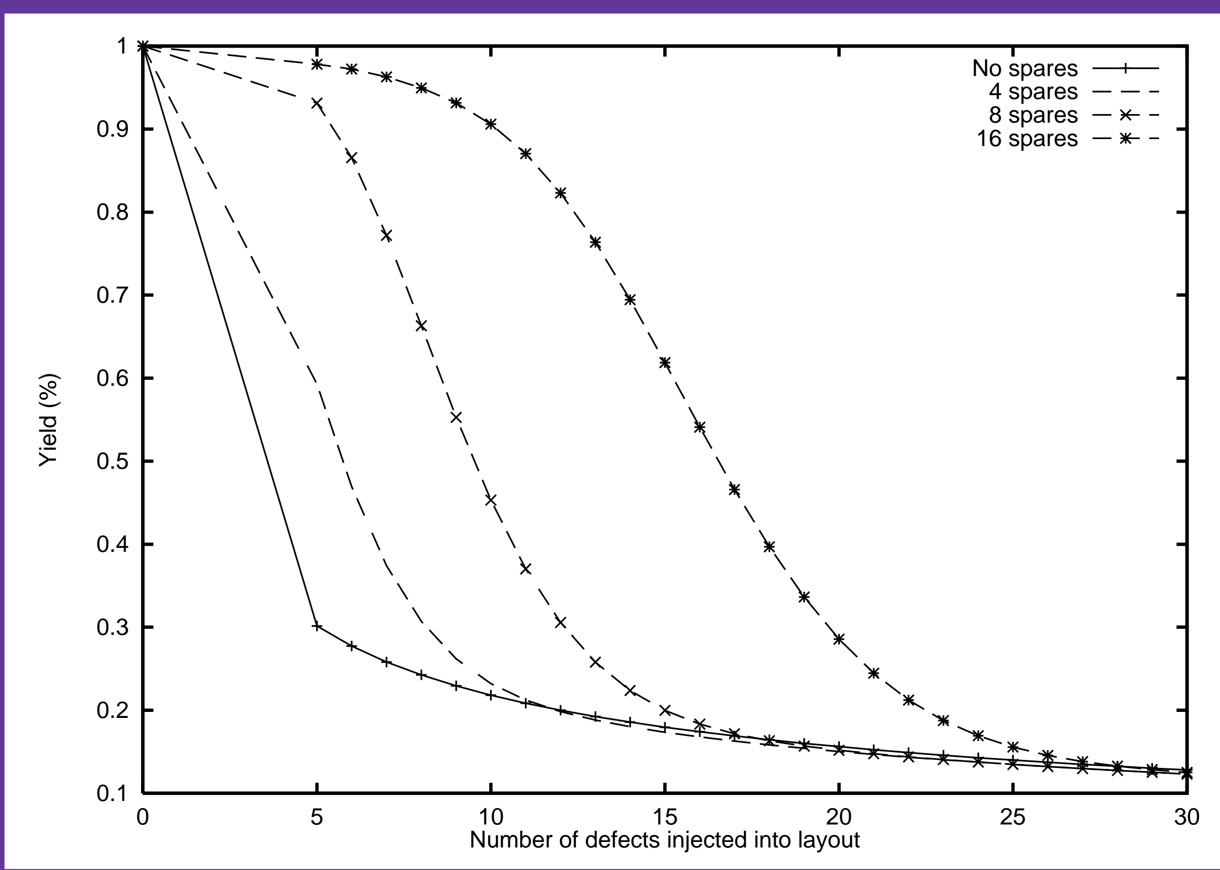
Yield Increase with BISR



- Number of rows = 1024, bits per column = 4, bits per word = 4

Chip yield is proportional to embedded RAM yield, since chip yield is proportional to the product of the yield of component macros and wiring

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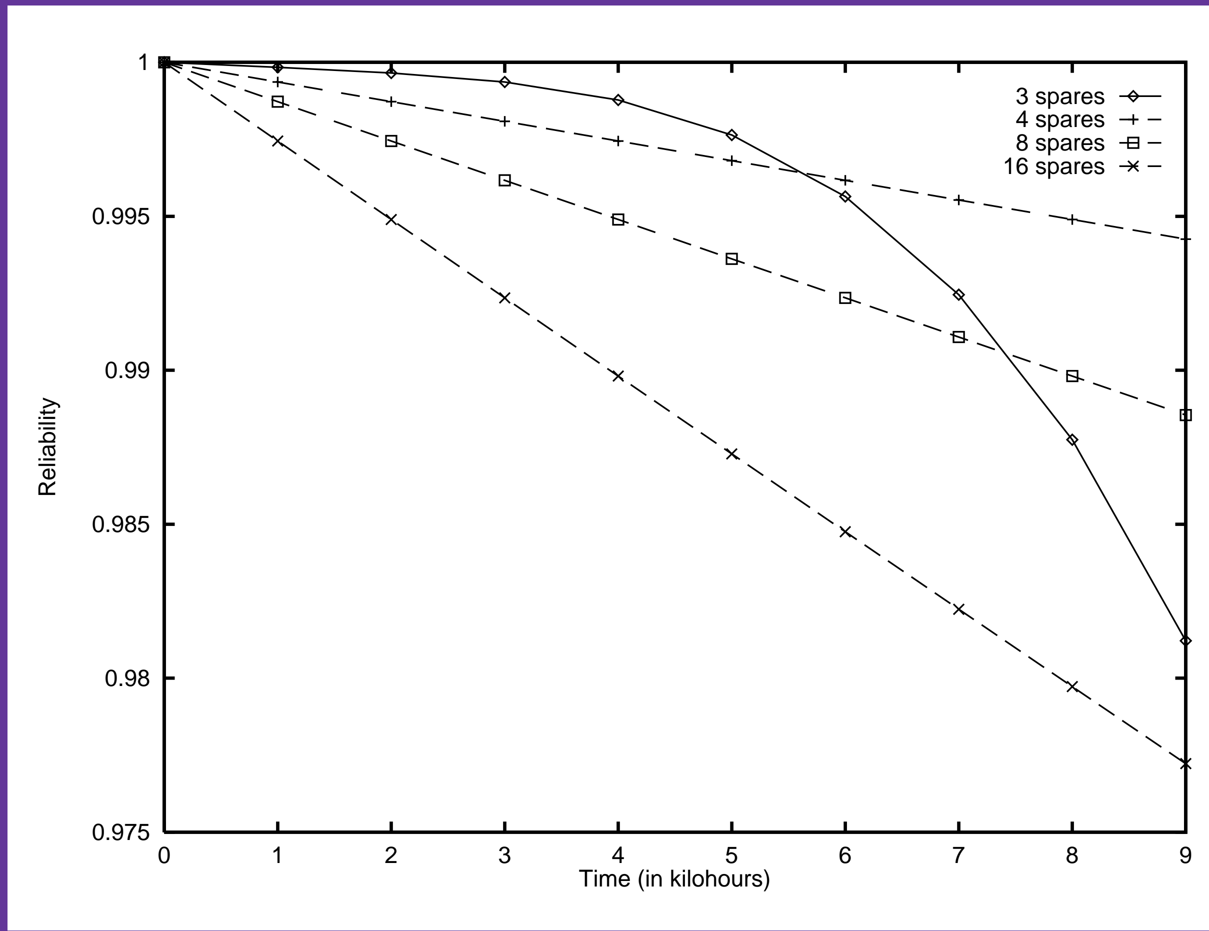
Reliability Improvement with BISR



Reliability for a RAM with BISR with a defect rate of 0.001%/kh per memory cell; the RAM has 1024 regular rows, with *bpc* = 4 and *bpw* = 4

BISRAMGEN

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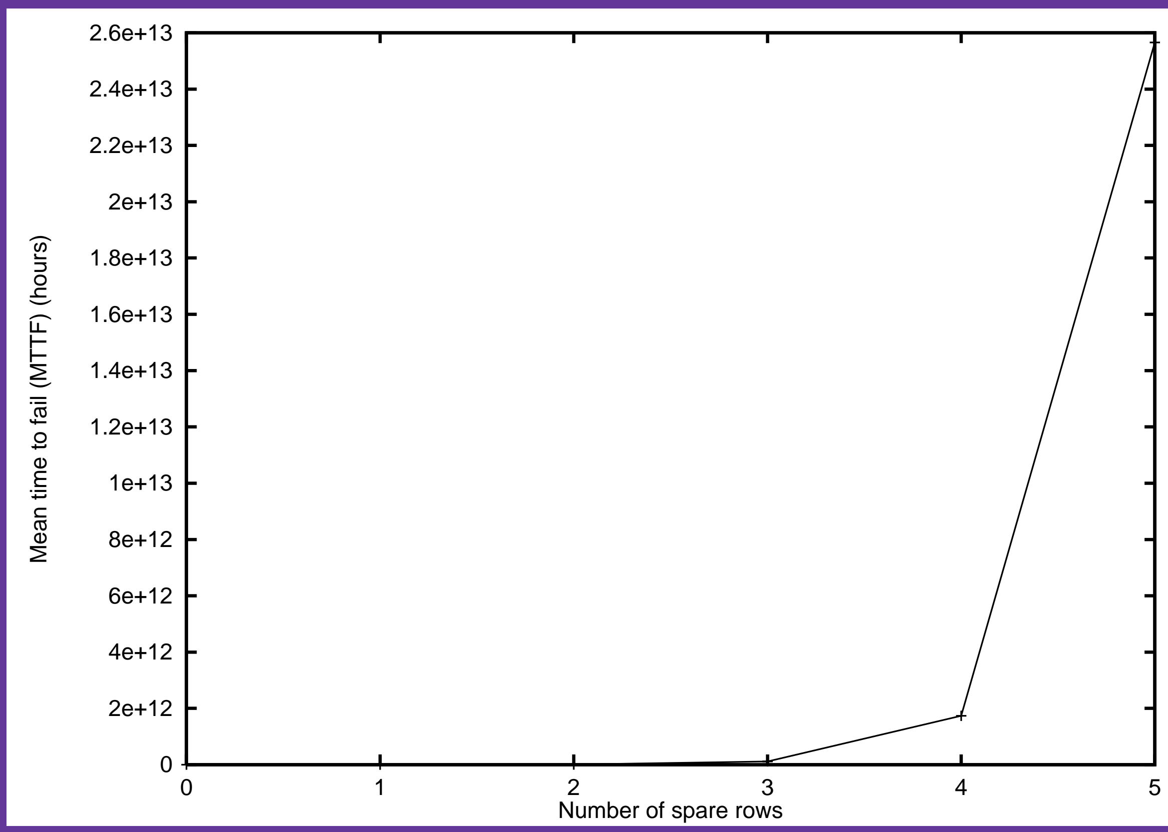
Improvement of MTTF with BISR



MTTF for a RAM with BISR with a defect rate of 0.001%/kh per memory cell; the RAM has 1024 regular rows, with *bpc* = 4 and *bpw* = 4

In contrast, MTTF without BISR would only be $1/(10^{-8}*16*1024) = 6103$ hours

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Improvement in Total Manufacturing Cost

- Total manufacturing cost per packaged and tested chip for various microprocessors; on-chip caches implemented with 2 spare rows

Name	Package Pin	Die Cost without BISR ($)	Die Cost with BISR ($)	Package Cost ($)	Test & Assembly Cost ($)	Total cost without BISR ($)	Total cost with BISR ($)
Pentium	PGA/ 273	68.00	27.55	25.00	25.00	118.00	77.55
Power PC 601+	CQFP/ 304	24.00	14.33	25.00	20.00	69.00	59.33
Alpha 21064	PGA/ 431	149.00	36.07	30.00	23.00	202.00	89.07
Super Sparc+	PGA/ 293	282.00	47.82	20.00	34.00	336.00	101.82
MIPS R 4400SC	PGA/ 447	38.00	28.98	50.00	28.00	116.00	106.98
HP PA 7100	PGA/ 504	74.00	25.75	35.00	16.00	125.00	76.75

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Die Floorplans of Microprocessors

BISRAMGEN

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Die Floorplans of Microprocessors

SRAM chip
CPU
SRAM chip
SRAM chip
Cache Management Chip
SRAM chip

6-chip MCM with 131-pin ceramic PGA package

HyperSPARC

L2 Cache
L1 Instruction Cache
Instruction Decode and Issue Logic
Floating Point Data Path
Integer Data Path
L2 Cache
Address Translation
L2 Tags
Cache / Memory Control
L1 Data Cache

Alpha 21164

BISRAMGEN

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Area Overhead with BIST and BISR as Percentage of Chip Area

- Percentage of overall chip area occupied by our proposed BIST/BISR circuitry

Name	On-chip cache (kilobytes)	On-chip cache (% floor-plan)	% Overhead w.r.t. cache	% Over-head w.r.t. chip
TI 320C80	50	22	4.0	0.88
Pentium P54C	256	26	1.2	0.31
Motorola68060	24	20.4	4.3	0.88
Power- PC 604	16-32	22.3	4.7	1.05
HyperSPARC	128/256	37.3	1.2	0.44
Alpha 21164	104	37.8	1.3	0.49

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How Many Spares to Use?

- Depends on targeted reliability (at a specific time, T), targeted yield and targeted area overhead
- Estimated by a table-driven, linear search-based, quadratic optimization approach
- Algorithm:
  - **Input:** Targets R_0, Y_0, A_0, and C (the number of bits of RAM storage required)
  - **Output:** Numbers S and N that denote the number of spares and the number of rows, respectively
  - **Objective:** To minimize ***F***, the sum of squared deviations from targets
  - **Approach:** Construct N x S tables of discrete values for yield, reliability and area overhead, with *bpc* ranging over powers of 2 from 8 to 128. For each value of *bpc*, choose (N,S) to maximize reliability and then perturb S by +/-1 to minimize ***F***
- Observation: for small values of T (<20,000 hours), use of 8-16 spare rows is advisable; for higher values of T (> 20,000 hours), optimal spare requirement drops down steadily to about 3-5 for most applications

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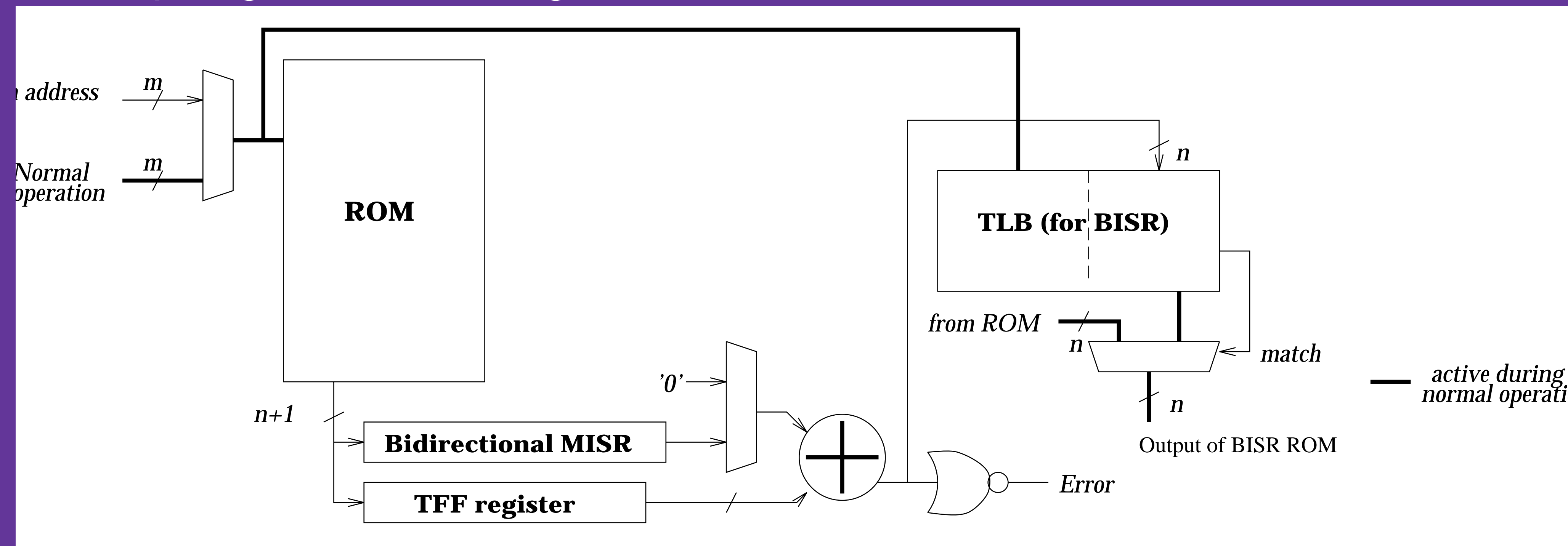
Built-in Self-repair Scheme

[Karpovsky 91]

- Detects and corrects single address errors only
- Components Reqd - Address generator, Bidirectional MISR, T-flip flop reg, set of XOR gates ...



$$t_{fault-tolerant-ROM} = max(max(t_{match}, t_{ROM}), max(t_{match}, t_{precharge}) + t_{sense}) + t_{mux}$$

FTROMgen

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Sample Layout Plot

TFF-register
MISR
ROM array
Address generator
TLB (for BISR)
Controller

(a)

(b)

(a) Floorplan of 8K x 38 ROM produced by FTROMgen [bpc = 8, # of spares = 4]
(b) Corresponding Layout

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Approximate Floorplan of Fault-tolerant ROM

multi-bit columns

Pull-up transistors

Row decoders and Word-line buffers

Memory array

ODM column

TFF reg + psedo-NMOS NOR

Bidirectional MISR

Address Generator

Column decoder

IO buffers

TLB (for BISR)

Controller

State-register

Extra circuitry

FTROMgen

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Timing Analysis, Defect Coverage and Layout Quality Estimation of SRAMs

Pinaki Mazumder

Department of Electrical Engineering and Computer Science
The University of Michigan
Ann Arbor, MI 48019

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Overview of SRAM Compiler

- Process and design-rule portable
- Flex grid cell representation
- User specified array size and aspect ratio
- Power minimization via ATD
- User programmable self-test
- Synchronous or asynchronous design
- Accurate timing analysis by SPICE path-based design cornering
- HDL model generation and back annotation
- Layout quality analysis
- Defect coverage metric

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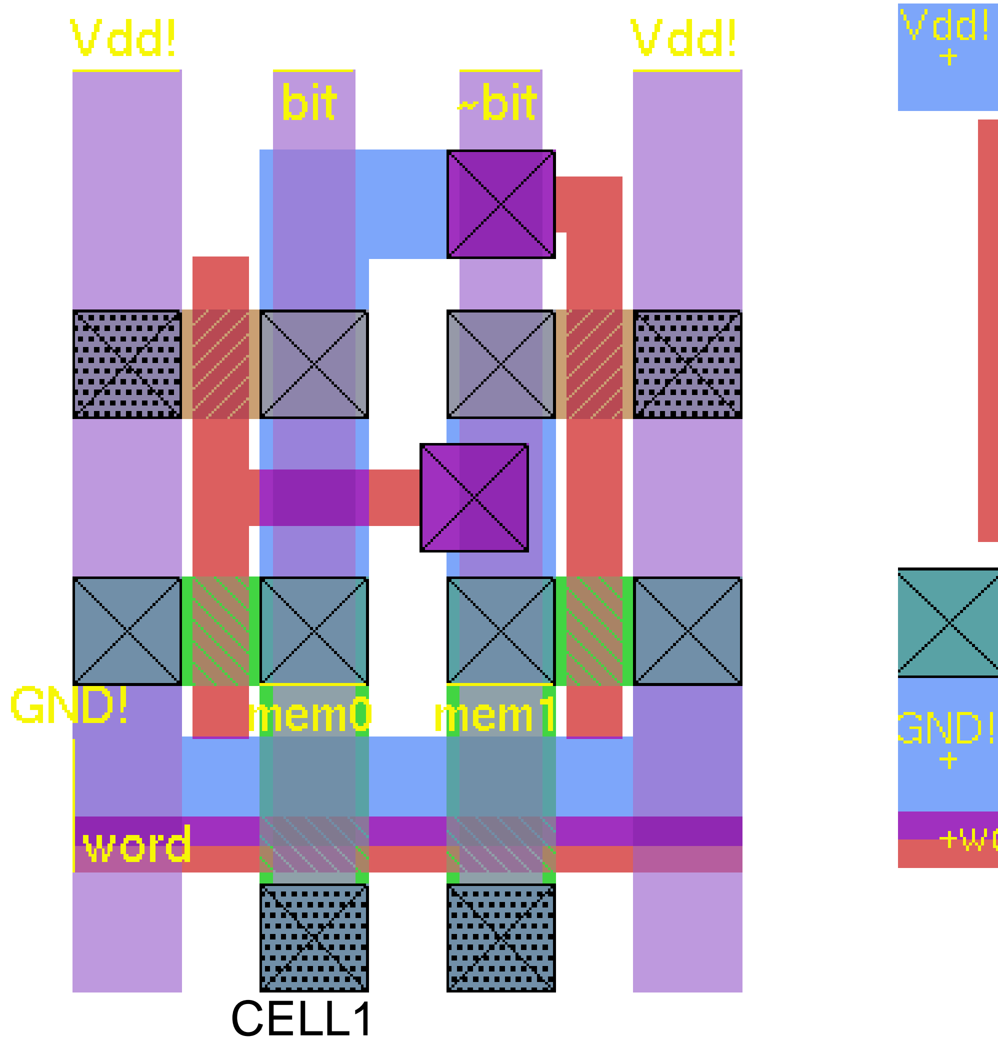
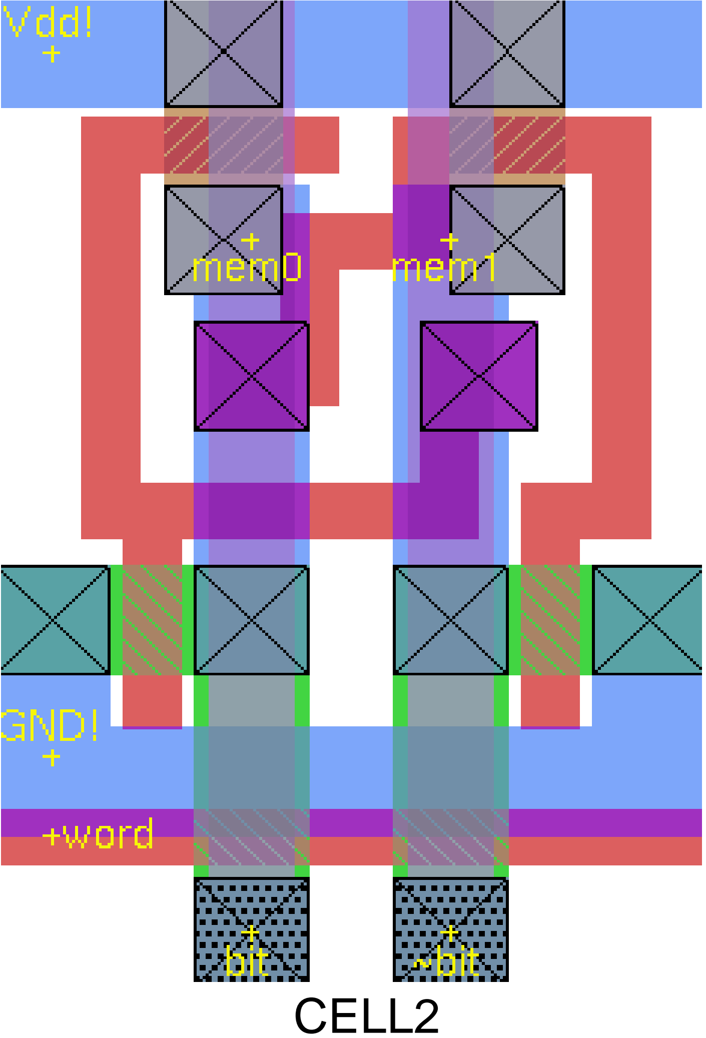
Compaq Cell Representation

- Two Compaq SRAM cells represented in SRAM compiler



CELL1



CELL2

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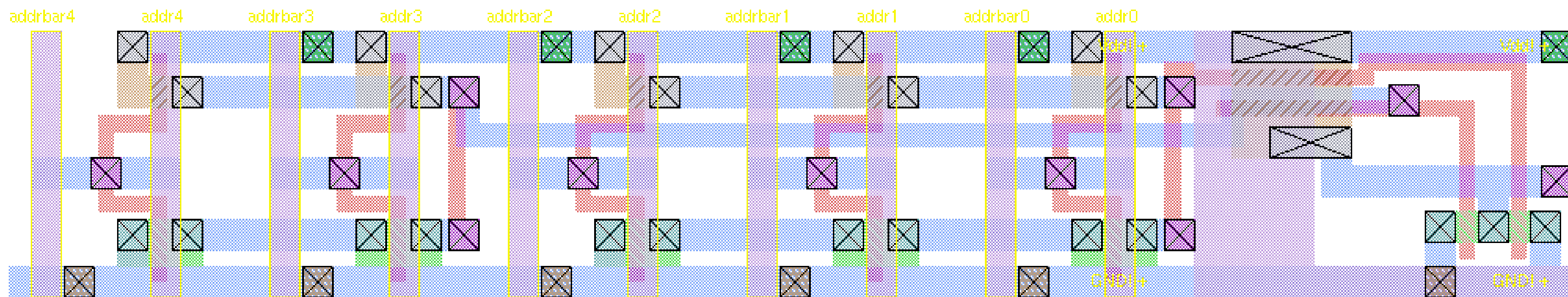
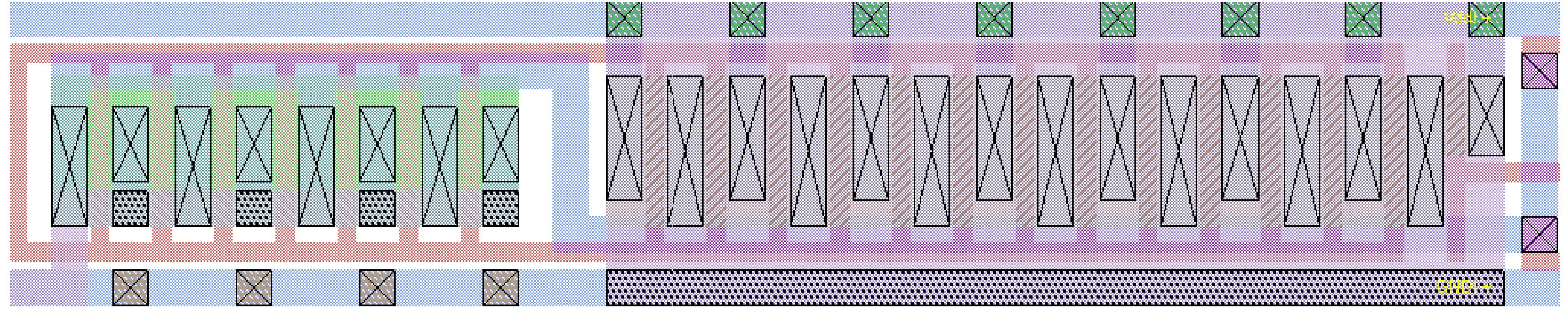
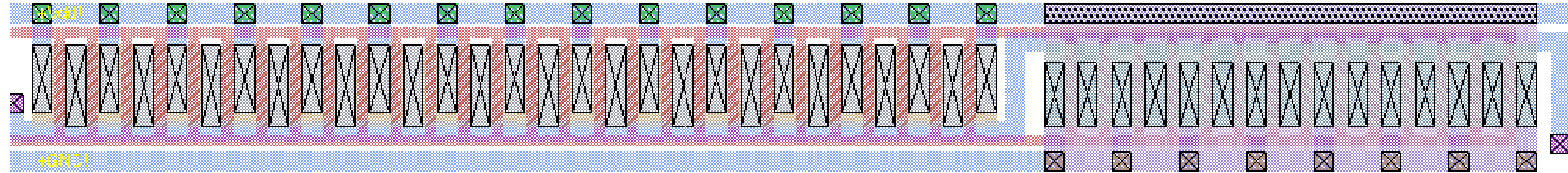
Row Decoder and Drivers



- NAND-NOR structure with maximum 12 address inputs



- NFET source of intermediate word buffer is controlled by ATD circuit.



- Word buffer is automatically sized based on user geometry specification

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Column Multiplexer

- Used to access a multi-bit column
- Precharge logic included in multiplexer circuit
- Allows use of single sense I/O unit per multi-bit column, thus reducing power consumption

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Column Decoder

- Column decoders use a NAND-NOR structure for bpc > 8
- Maximum bpc = 64

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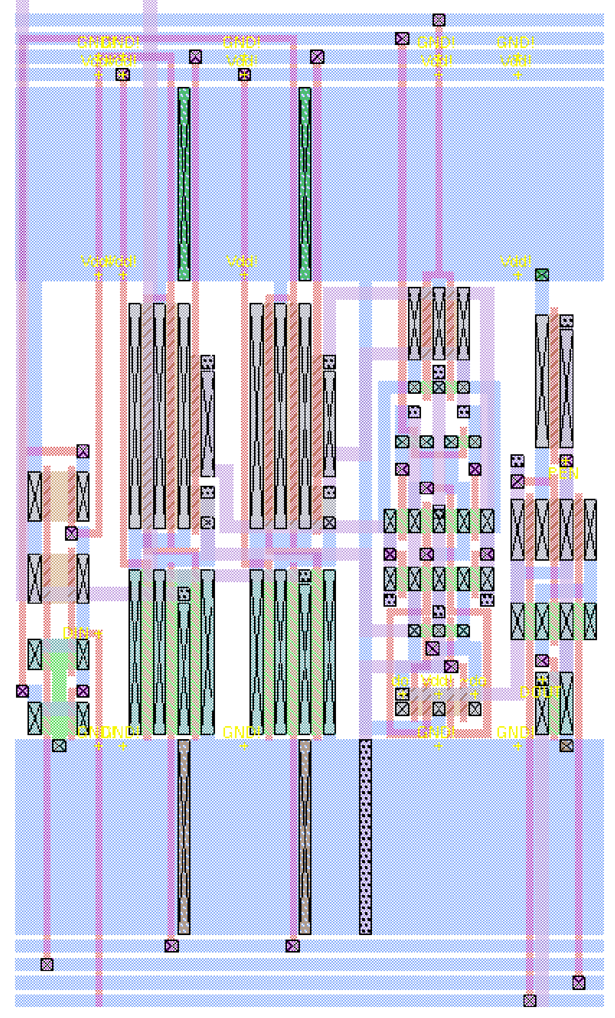
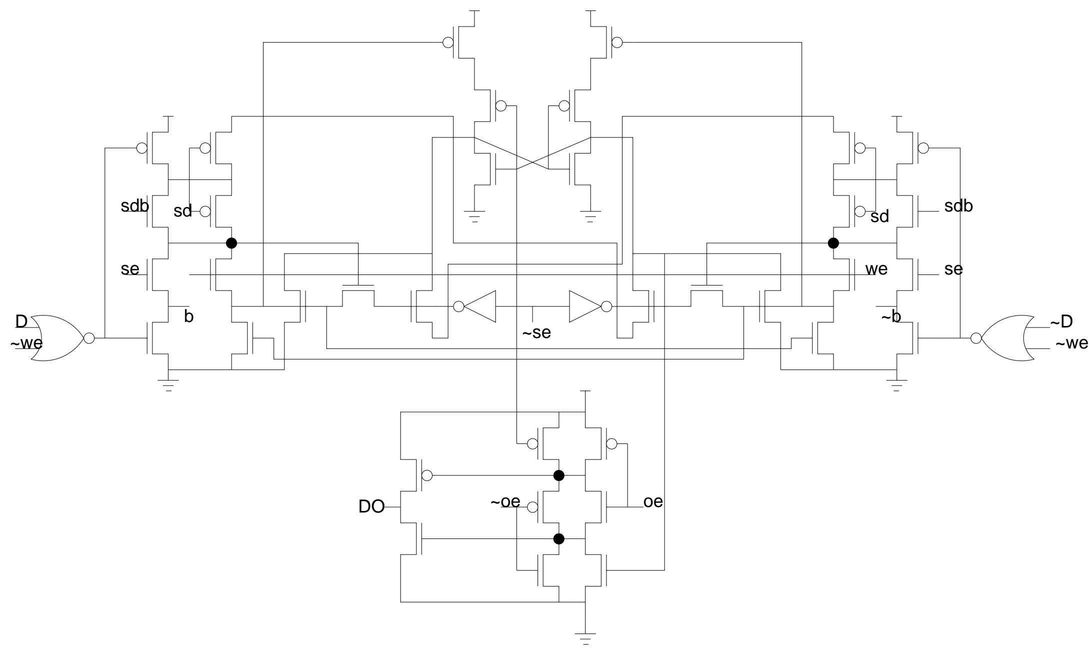
Sense I/O Circuit





- Width matched to a multi-bit column
- Allows efficient placement of synchronous registers and/or test data generation circuitry in the I/O block reducing area overhead
- Power reduction through used of address transition detection

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ATD Circuit

dbit

~we

re

~re

se

~se

- Detects address transition using a dummy RAM column
- Controls operation of address buffer, word buffer and sense I/O units

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Address Buffer

- Address buffer is activated only by address transitions
- ATD circuit controls access to latch in buffer circuit

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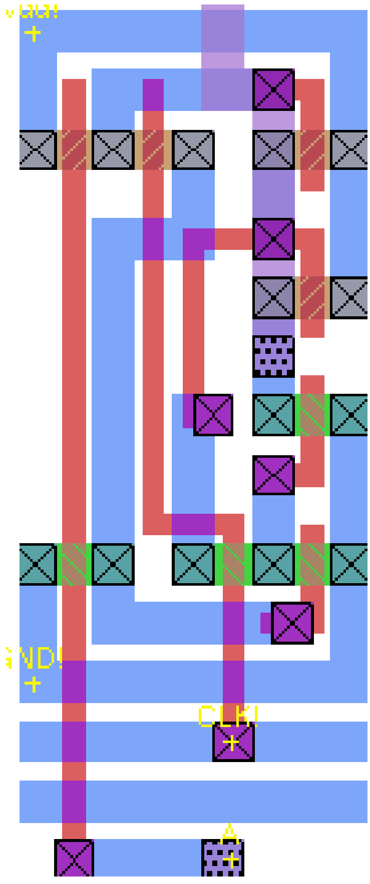
Synchronous Register Cell



- True single phase clocked logic
- Edge triggered flip-flop using 8 transistors
- Asynchronous preset/reset provided on data/address generator cells

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Write Enable Buffer

- Calibrated delay inverter chain used for asynchronous RAM operation
- TSPC register cell with asynchronous reset used to latch enable line in synchronous mode

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Test Generator Cells

Address Generator

Data Generator

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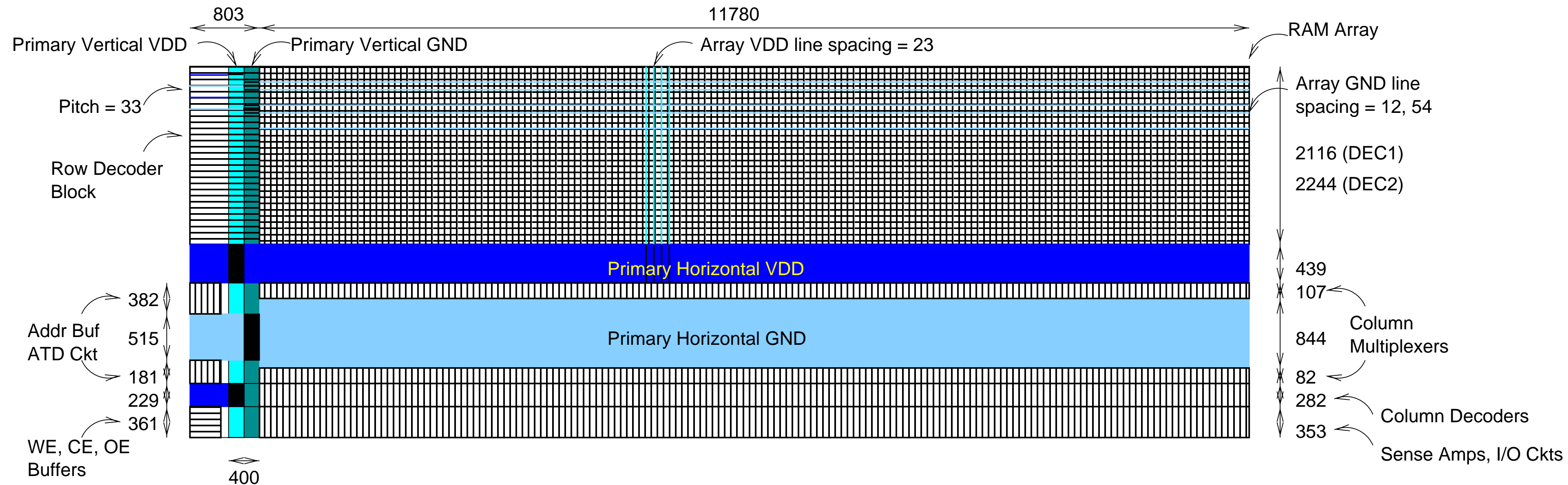
Timing of 64bx512b RAM Array



- In the CELL 1 RAM, the VDD lines of the RAM array run in vertical metal2 whereas the GND lines run in horizontal metal1
- In the CELL 2 RAM, the VDD *and* GND lines of the RAM array run in horizontal metal1
- The wide primary horizontal VDD/GND lines are sized based on clock frequency (500 MHz)

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Timing Analysis of Large Arrays

- High-level timing analysis has limitations
- SPICE simulation of very large netlists for large number of parameter and input signal combinations is highly compute-intensive
- RAM array netlists contain a large number (> 90%) of devices that are inactive during a particular memory operation
- Solution for efficient and accurate timing information
  - Generate reduced SPICE netlist of sensitized address and data path from input to output
  - Model remaining devices and wires by their effective parasitic contribution
- Results
  - Greater than 98% reduction in netlist size for moderate array sizes
  - Accurate and efficient timing analysis
  - Comprehensive design cornering
  - Quick feedback to design and optimization tools

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Design Cornering of Arrays using Compaq Cells

- Automatic SPICE path extraction for various array sizes
  - 128b - 256Kb
- Address and data input generation
- *Vdd* variation
  - 3.15V to 3.85V
- Temperature variation
  - -40C to +85C
- Optional device parameter variation
  - VTH0, U0, TOX, XJ, NCH
- Automated simulation
- Delay measurement
- Back annotation to HDL model

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Timing of 1Kb and 32Kb RAM Arrays Using Cell 1

32Kb
1Kb
Cycle time (ns)
5
4.5
4
3.5
3
2.5
2
Vdd (V)
4
3.8
3.6
3.4
3.2
3
Temp (C)
−40
−20
0
20
40
60
80
100

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Timing of 1Kb and 32Kb RAM Arrays Using Cell 2

Cycle time (ns)

8
7
6
5
4
3
2
1

32Kb

1Kb

Vdd (V)

4
3.8
3.6
3.4
3.2
3

Temp (C)

−40
−20
0
20
40
60
80
100

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64bx512b RAM Array Simulation Comparison

Comparison of Cycle Time for 64x512 RAM array using DEC1 and DEC2 cells

CELL2

CELL1

Cycle Time (ns)

6.5 6 5.5 5 4.5 4 3.5 3 2.5 2

Vdd (V)

4 3.8 3.6 3.4 3.2 3

Temp (C)

−40 −20 0 20 40 60 80 100

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Layout Quality Estimation and Defect Coverage

- Generate small RAM arrays
  - 2x2, 3x3, 4x4
- Defect distribution probability
- Defect insertion
  - 2-D inductive fault analysis
  - 3-D process induced defects
- Fault probability estimation
  - Quality metric
- Fault classification
- Netlist generation
- March test generation
- SPICE simulation and defect coverage estimation

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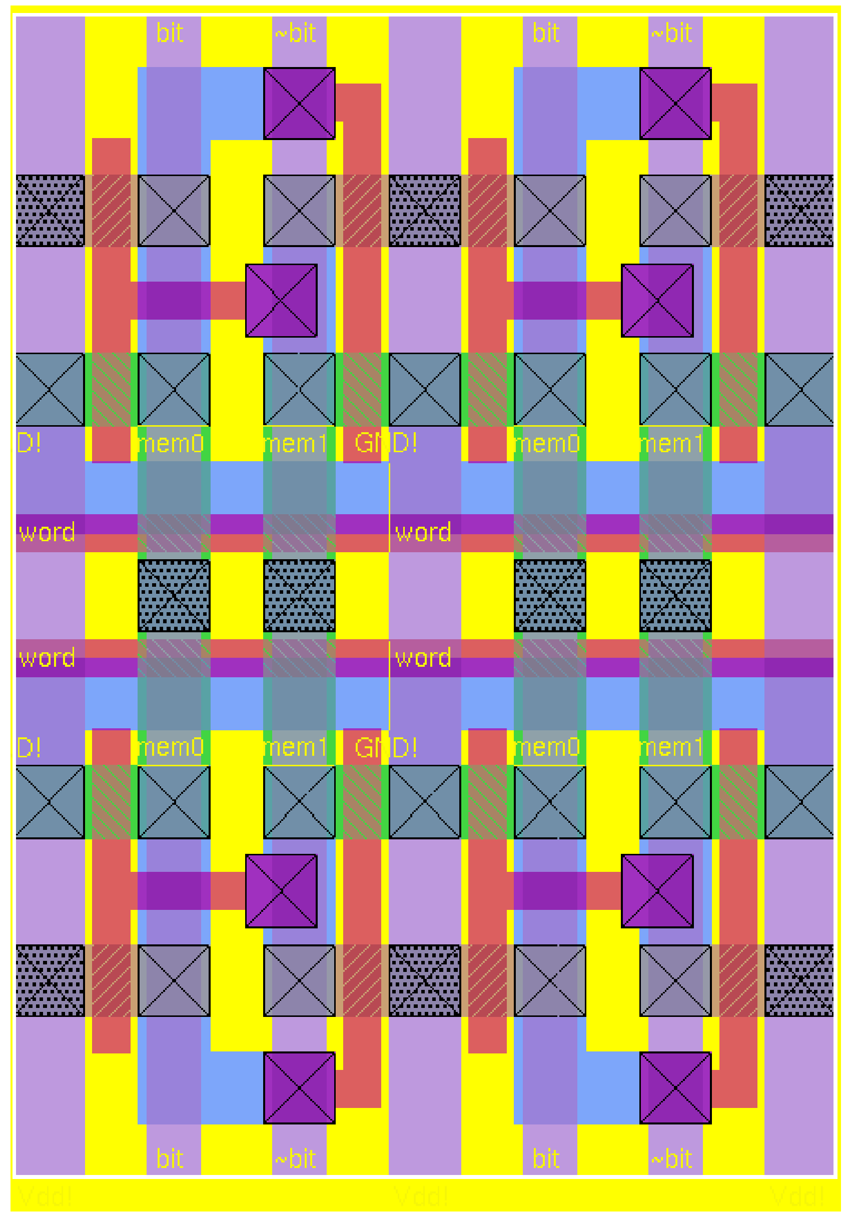
Example RAM Array Used for Defect Extraction



- 2x2 array with cell 1 shown
- Defect coverage experiments were conducted on:
  - 2x2 cell 1 array
  - 3x3 cell 1 array
  - 2x2 cell 2 array
  - 3x3 cell 2 array
- Issues
  - Obtain defect coverages
  - Compare cell quality
  - Compare extraction approaches
  - Compare results of 2x2 approach with 3x3 approach
    - 3x3 captures all mirroring effects but is much more compute-intensive

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Defect Distribution Probability

d

1/0.35

$1/x^3$

x

0.35µm

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Defect Insertion

- Inductive fault analysis
  - 2-D defect representation
    - Equal bridge and break probability densities
  - Masking level
  - Inter- and intra-layer defects
- Process induced defects (UMICH.)
  - 3-D defect representation
    - Equal conducting and non-conducting defect fractions
  - Layer and oxide thickness specification
  - Choice of defect density functions
  - Defect collapsing

Extracted defects show majority of *faults* caused are bridging in nature

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Non-conducting Defect Classification

Nodes	Description	Class
Vdd	If cell Vdd is broken data is lost after some time.	DRF
Vss	W, R1 normal. R0 fails. Cell reads 1.	SAF
Bit	R1 fails, R0 may be successful.	TF
Word	Access transistors off.	SOF
D / ND	Stored data can not be held.	DRF

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Conducting Defect Classification

Nodes	Description	Class
Vdd - Vss	Large steady-state current.	CAT
Vdd - other	Node is always stuck high.	SAF
Vss - Word	Access transistors off.	SOF
Vss - other	Node always stuck low.	SAF
Bit_x - Bit_y	Write to a cell changes data in neighbor.	CF
Word - other	Word line charged during read/write.	SAF
D - ND	Equalizes Bit and ~Bit voltage.	SAF
D_x - D_y	Write operation affects neighbors.	CF
Bit_x - D_y	Write operation affects neighbors.	CF

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Fault Probabilities and Layout Quality: 2x2 Array

Fault	CELL 1		CELL 2	
	IFA	3-D	IFA	3-D
Bridge	139	141	109	111
Break	171	42	122	47
CAT	0.128	0.198	0.0	0.001
CF	0.363	0.336	0.463	0.502
DRF	0.107	0.043	0.149	0.038
SAF	0.225	0.356	0.272	0.360
SOF	0.118	0.057	0.113	0.097
TF	0.058	0.007	0.004	0.004
Sensitivity	**24.3**	**22.4**	**23.6**	**20.9**

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Fault Probabilities and Layout Quality: 3x3 Array

Fault	CELL 1		CELL 2	
	IFA	3-D	IFA	3-D
Bridge	319	158 *	249	122 *
Break	295	58 *	314	47 *
CAT	0.120	0.165	0.0	0.001
CF	0.383	0.371	0.466	0.520
DRF	0.103	0.053	0.145	0.062
SAF	0.241	0.357	0.239	0.331
SOF	0.114	0.047	0.110	0.082
TF	0.039	0.005	0.040	0.004
Sensitivity	**23.1**	**22.7**	**23.9**	**21.8**

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Generalized March Test Generation Framework

- User input:
  - Defect statistics file
  - RAM array description
  - Arbitrary march sequence
  - Optional: peripheral circuit netlist
- Programmed test generation
  - Generate or add peripheral circuits
  - Generate SPICE simulation waveforms
  - Create SPICE command file
  - Parse defect statistics file
  - Generate netlist for each defect
  - Simulate and compare with correct expected output
  - Log results with defect coverage of march test
- March 7N and up show complete defect coverage except Vdd-Vss shorts which can be detected by I_{ddq} testing

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Conclusions

- Cell 1 demonstrated faster access times as compared to Cell 1
  - Verified by SPICE path extraction of large RAM arrays
    - Cell 2 has longer poly lengths on the back-to-back inverters and these are exposed to cross coupling with adjacent cell storage nodes
- Cell 2 is more robust as compared to Cell 1
  - Verified conclusively by our 3-D defect extraction process
    - Cell 2 has no Vdd - GND overlap leading to reduction of catastrophic shorts
    - Cell 1 has greater bit/~bit line to internal storage node overlap
  - Results of the two approaches track well for the various examples studied
- 3-D defect extraction is more realistic and captures the artifacts of process induced defects more accurately than 2-D IFA defect extraction
- March 7N tests achieved 100% defect coverage excluding Vdd-Vss shorts for the examples studied
  - The experiments show that physical defects do not manifest themselves into complex functional faults which limit memory test effectiveness
  - Thus, simple March tests achieve similar defect coverage as more complex testing schemes even though *functional fault* coverages of the tests vary

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NDR

Future Work

- Since simple March test are proven effective for defect coverage, the future work in testing will be:
  - Stress testing: Repeated read/write of a single cell introduces stresses that might lead to eventual failure. This must be detected by introducing multiple consecutive read/write operations in the march sequence. Our generalized march test framework will be modified to include address stress, data background stress and timing stress.
  - Extension to deep-submicron effects: Currently we address parameter variations of devices in order to address delay faults. This will be extended to account for electromigration, leakage currents and volatility.
  - Programmable IDDQ Test: Include onchip Iddq testing circuitry along with existing March test circuitry to account for resistive Vdd-Vss faults that are not detected by functional fault tests.
- Application of defect characterization to memory cell peripheral circuits and logic circuits used in test data and address generation.
  - To quantify robustness of different decoding and sensing approaches
  - To improve reliability of testing circuitry

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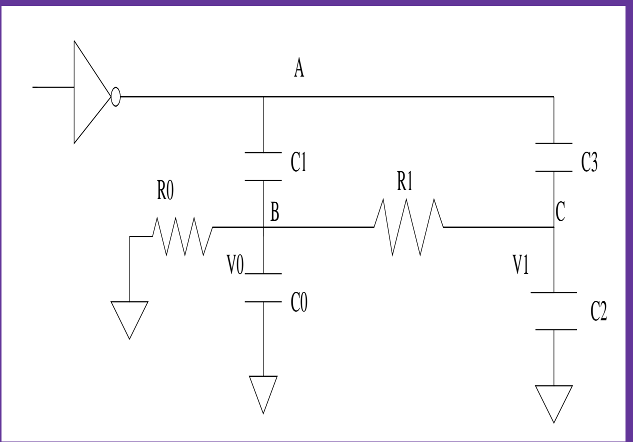
Metal-to-Polysilicon Induced Noise

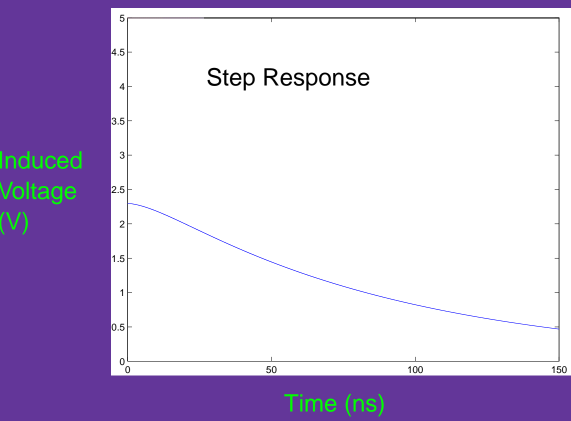


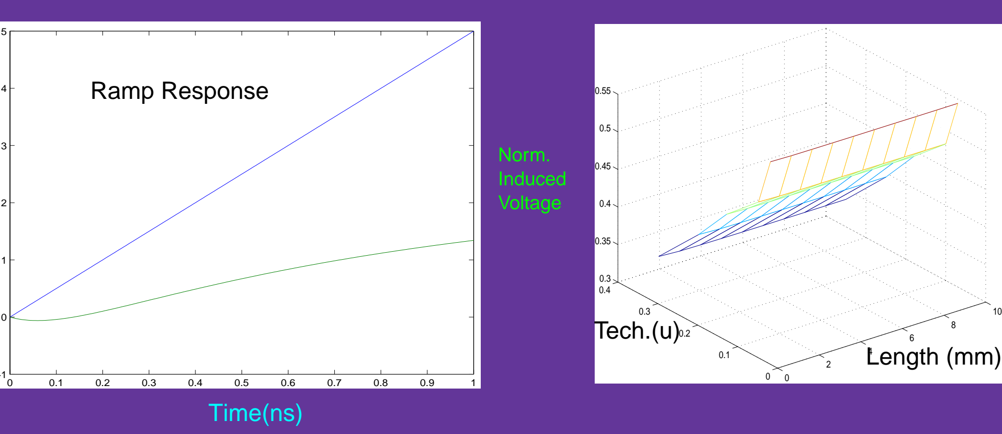
C1+C3: Coupling Capacitance of Metal and Poly

R1: Resistance of Poly.

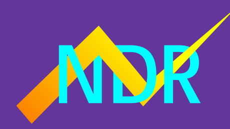
Step and Ramp Input Response

$$V_{step}(t) = A\exp(-\alpha t) + B\exp(-\beta t) \qquad V_{ramp}(t) = A\exp(-\alpha t) + B\exp(-\beta t) + \gamma$$





Peak induced voltage is proportional to coupling capacitance and time constant is proportional to coupling capacitance and polysilicon resistance.



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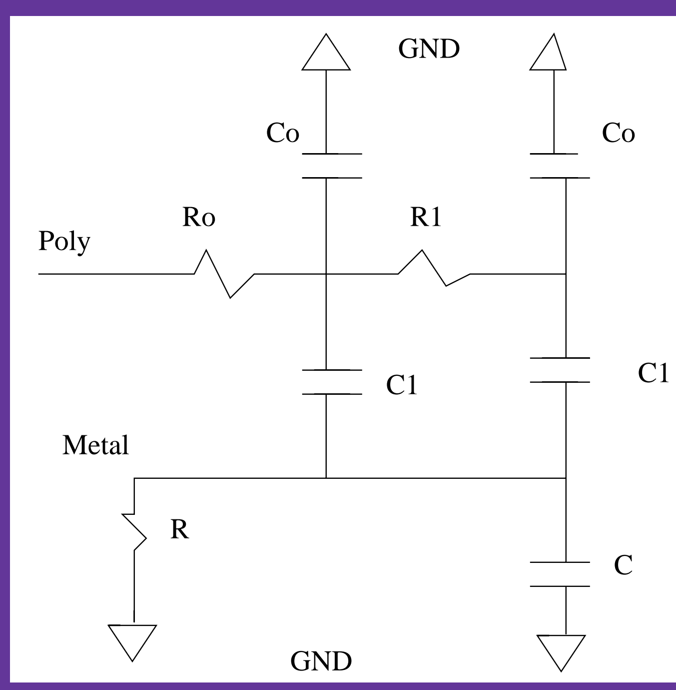
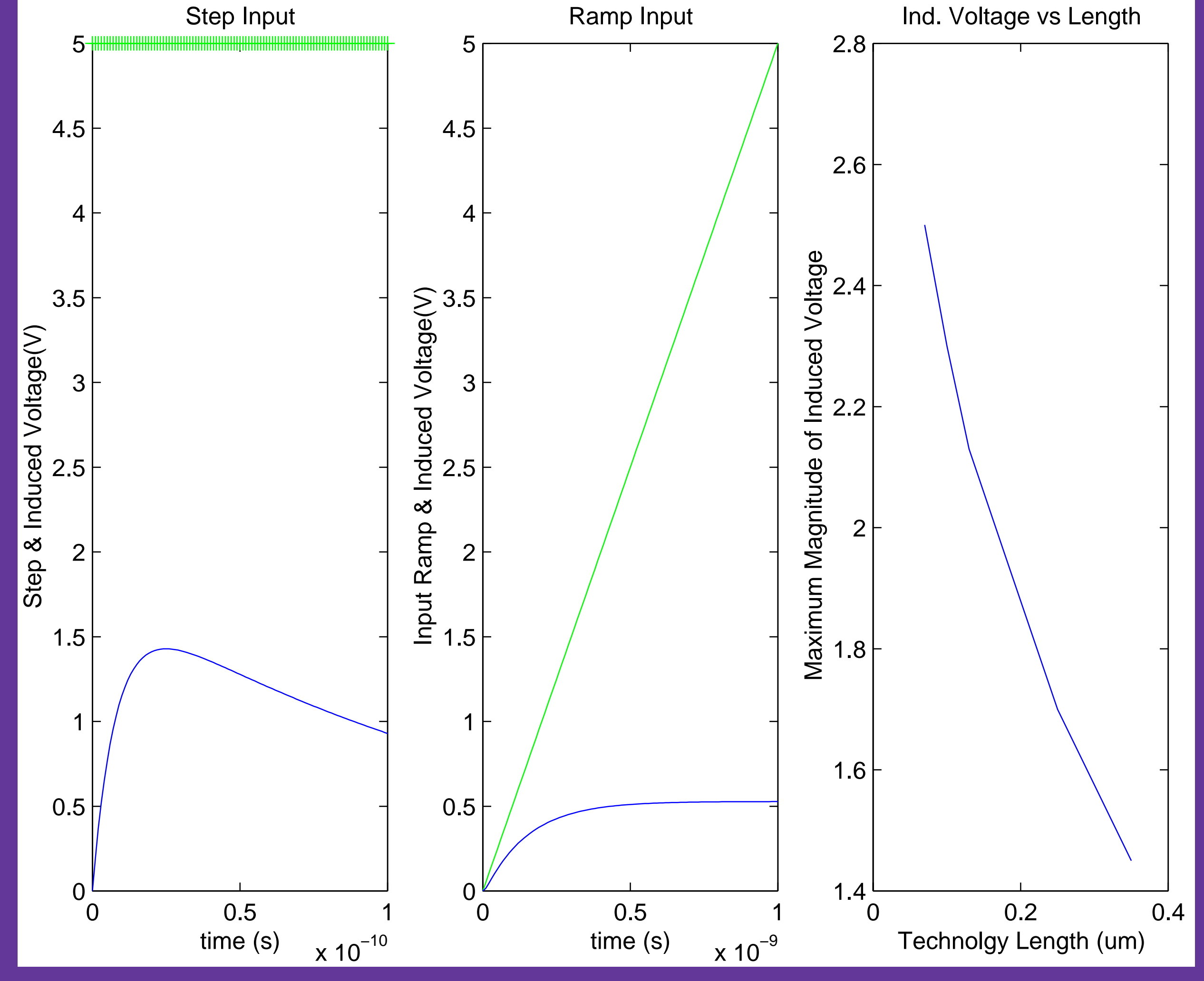
Polysilicon-to-Metal Induced Noise

$$V(t) = A\left(\exp\left(-\frac{1}{RC}t\right) - \exp(-\alpha t)\right) + B\left(\exp\left(-\frac{1}{RC}t\right) - \exp(-\beta t)\right) + C\left(1 - \exp\left(-\frac{1}{RC}t\right)\right)$$





- **C_o = poly-to-ground** capacitance
- C_1 = poly-to-metal coupling capacitance
- R_1 = poly resistance
- R_o = driver resistance
- R = driver resistance
- C = load capacitance

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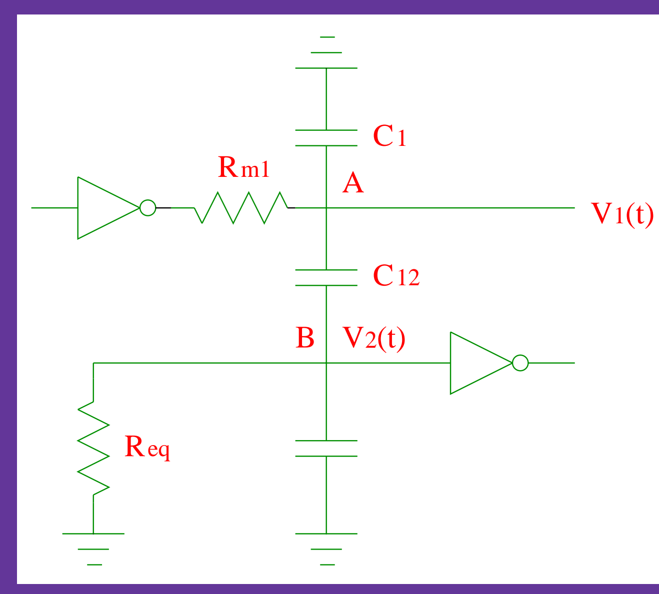
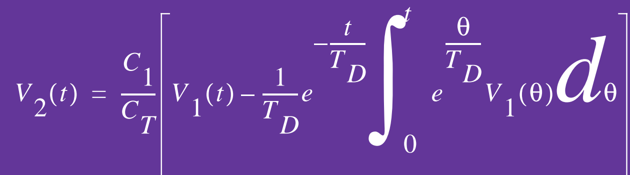
Metal-to-Metal Noise

Interconnect Capacitance and Resistance

Technology	1.0 µm	0.5 µm	0.35 µm	0.25 µm	0.18 µm	0.10 µm
Thickness/Width	0.667	0.89	1.5	2	2.5	3.5
Thickness (µm)	1.0	1.0	0.7875	0.75	0.675	0.525
Width (µm)	1.5	0.75	0.525	0.375	0.27	0.15
Metal1 to Substrate (aF/µm)	156	126	123	116.5	112	107
Metal1 to Metal1(aF/µm)	16	39.7	46	67.72	91	142
Sheet Resistance (Ω/square)	0.07	0.07	0.089	0.093	0.104	0.13





$$C_T = C_{12} + C_1$$

$$T_D = C_T \cdot R_{eq}$$

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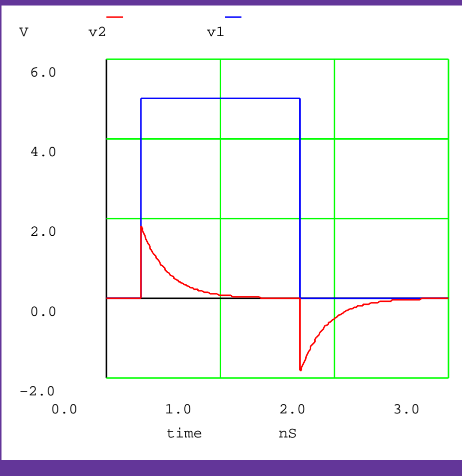
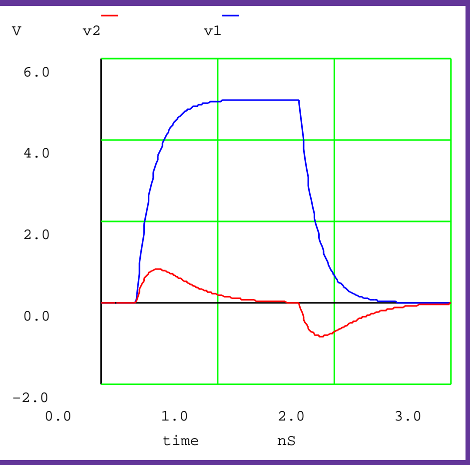
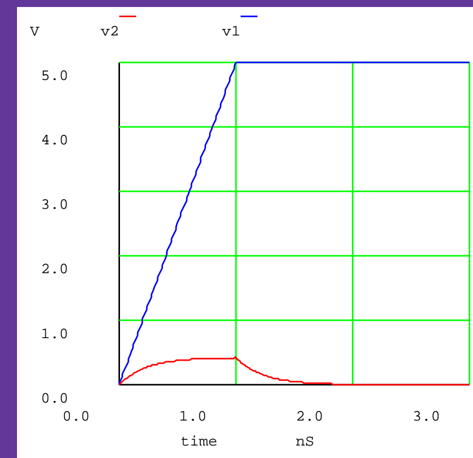
Metal-to-Metal Noise (cont'd.)

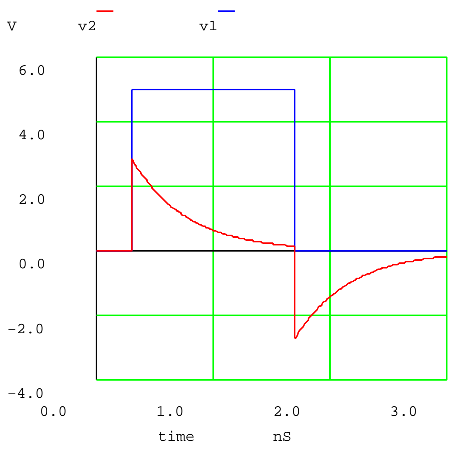
0.25 μm technology

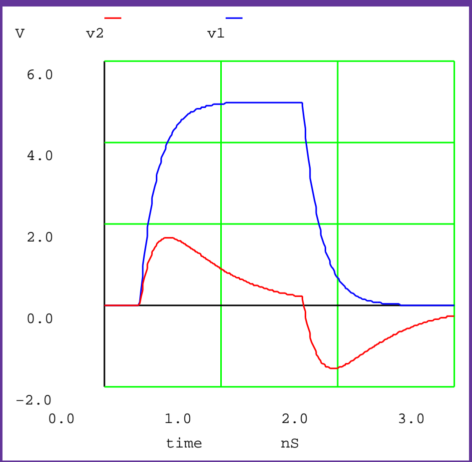


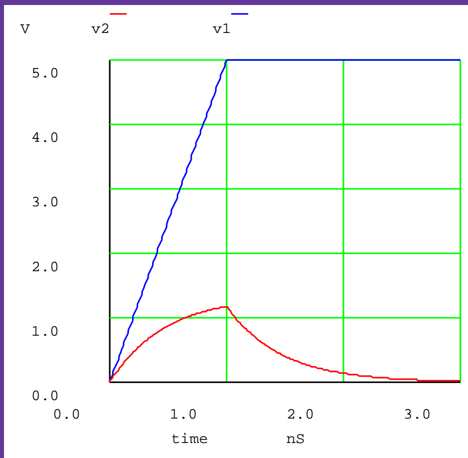




0.10 μm technology







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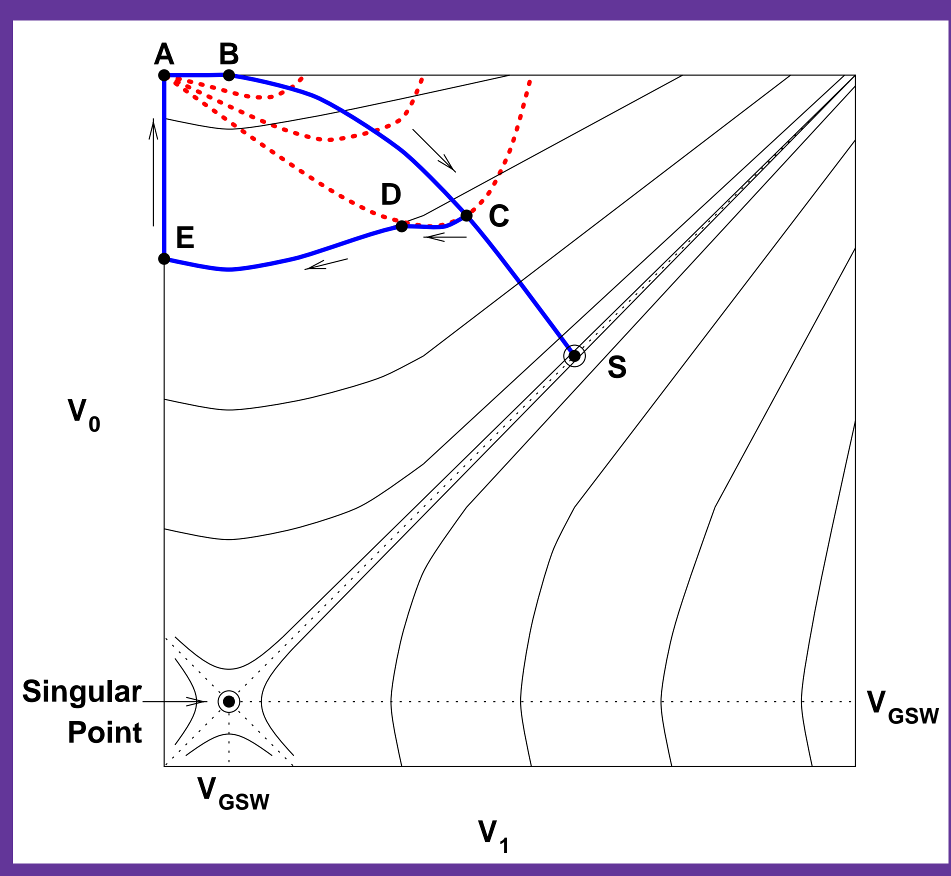
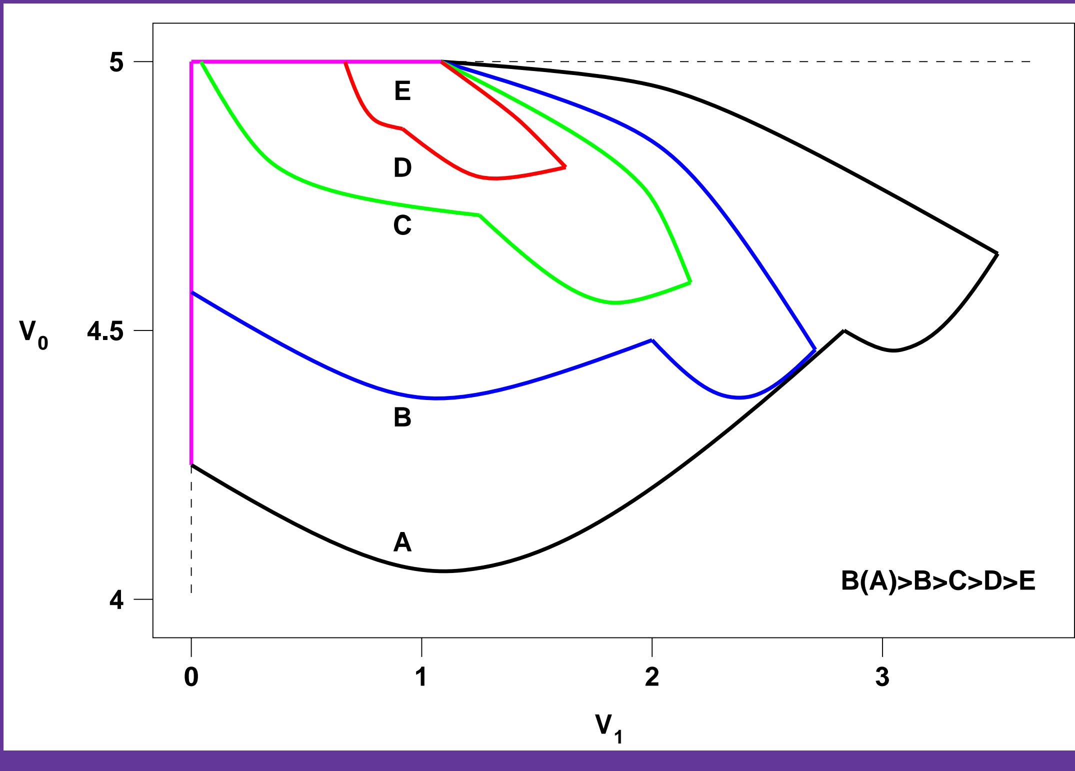
Phase Trajectories of Memory Read Process





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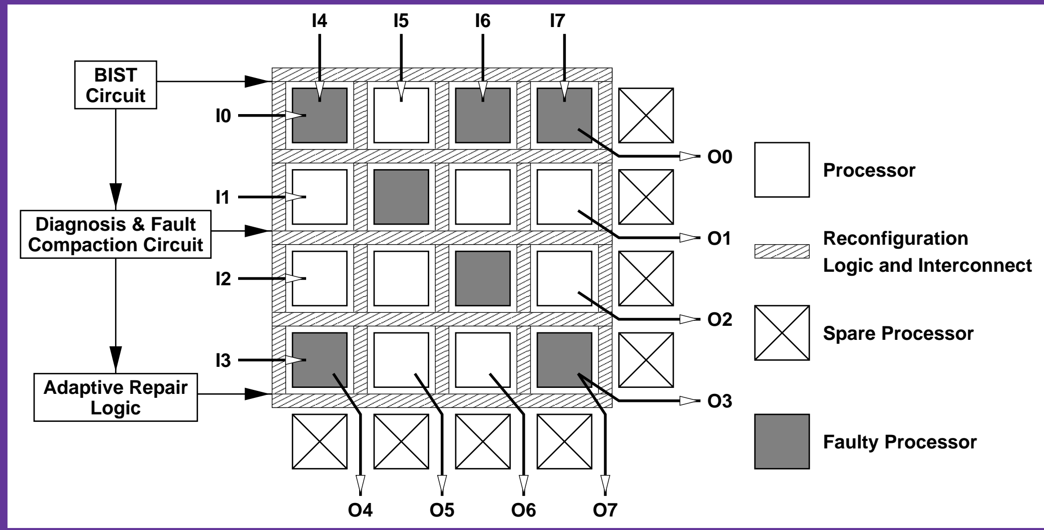
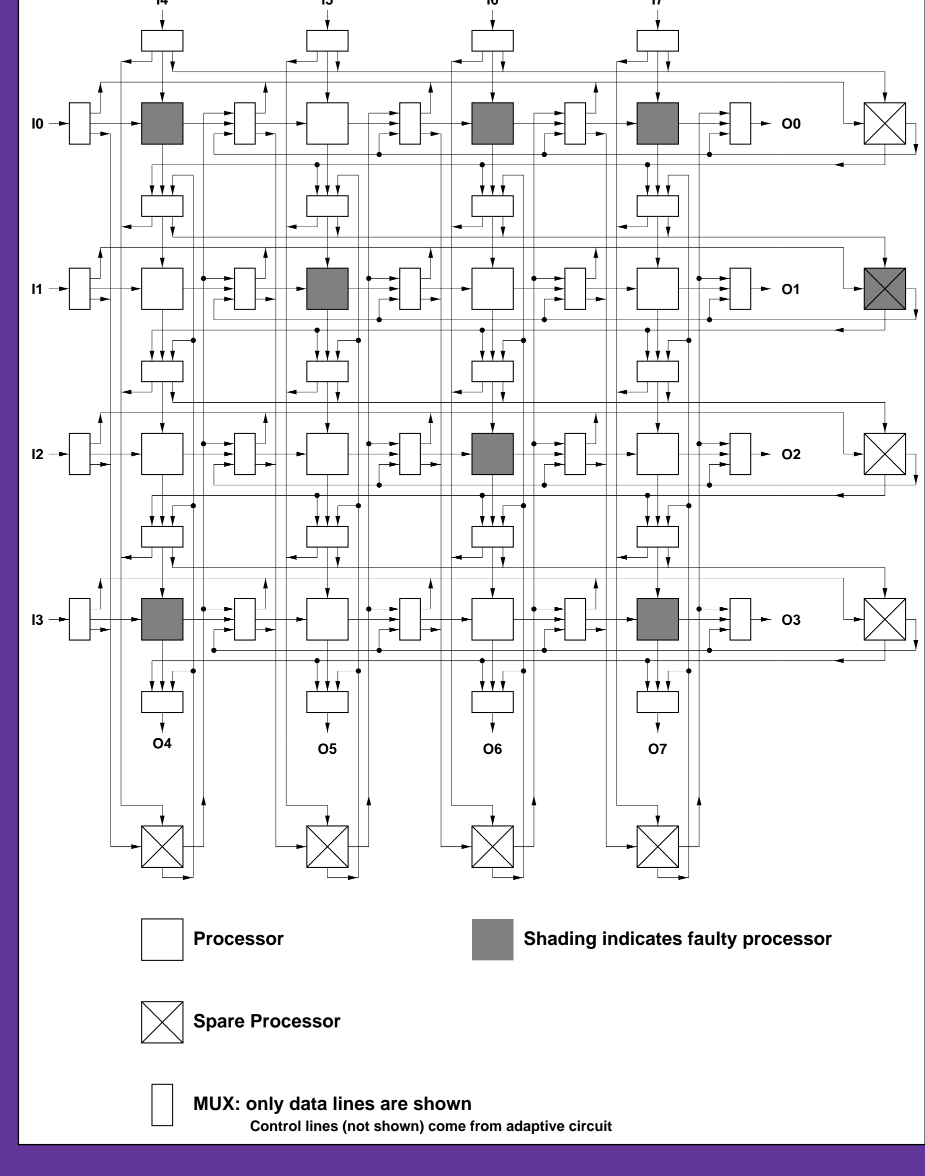
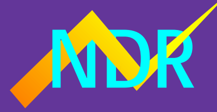
4×4 Self-Repairable Square Array Architecture

Reconfigurable Array with BISR Circuit



Reconfigurable Array with MUX Switches





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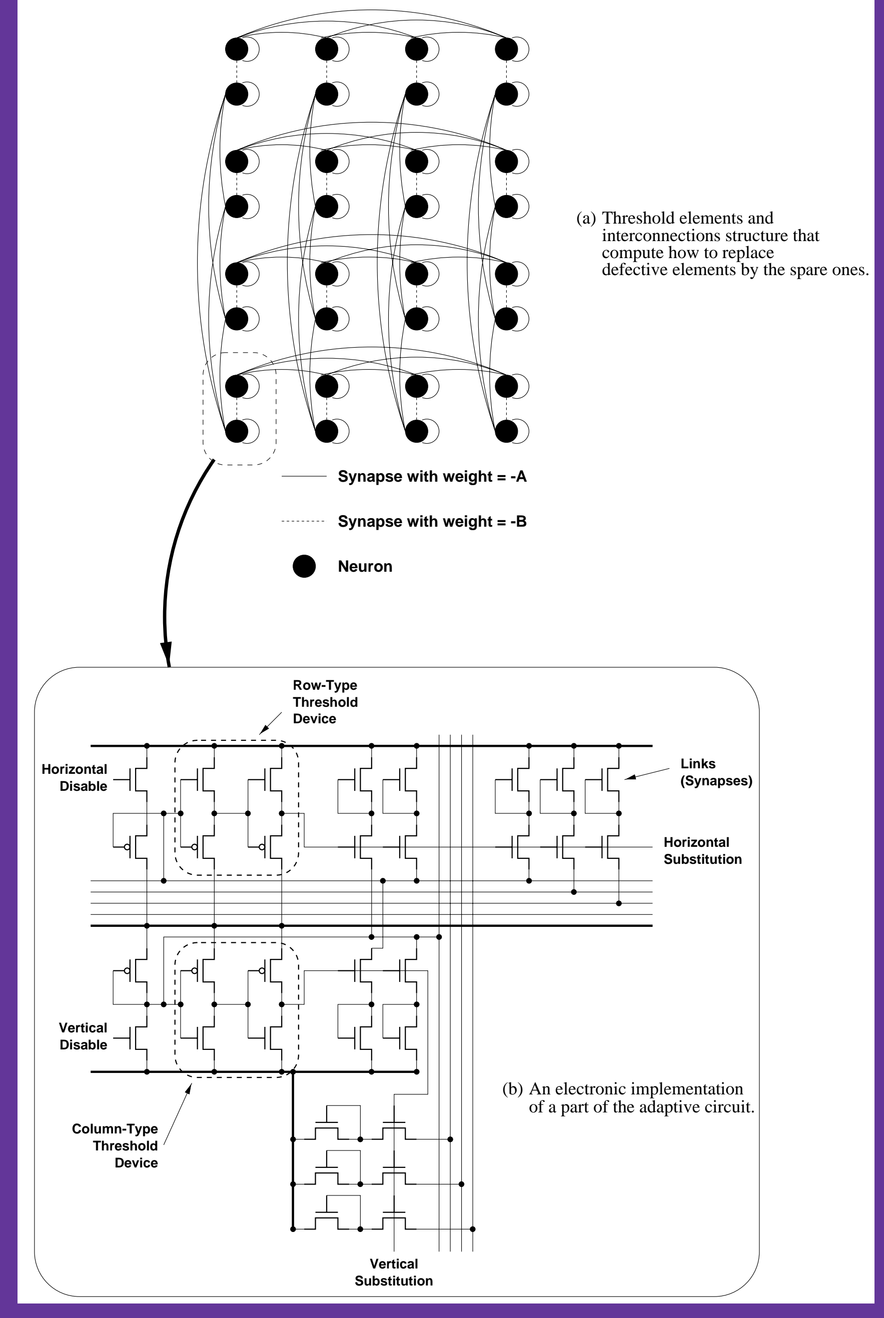
Adaptive Repair Circuit for Square Array



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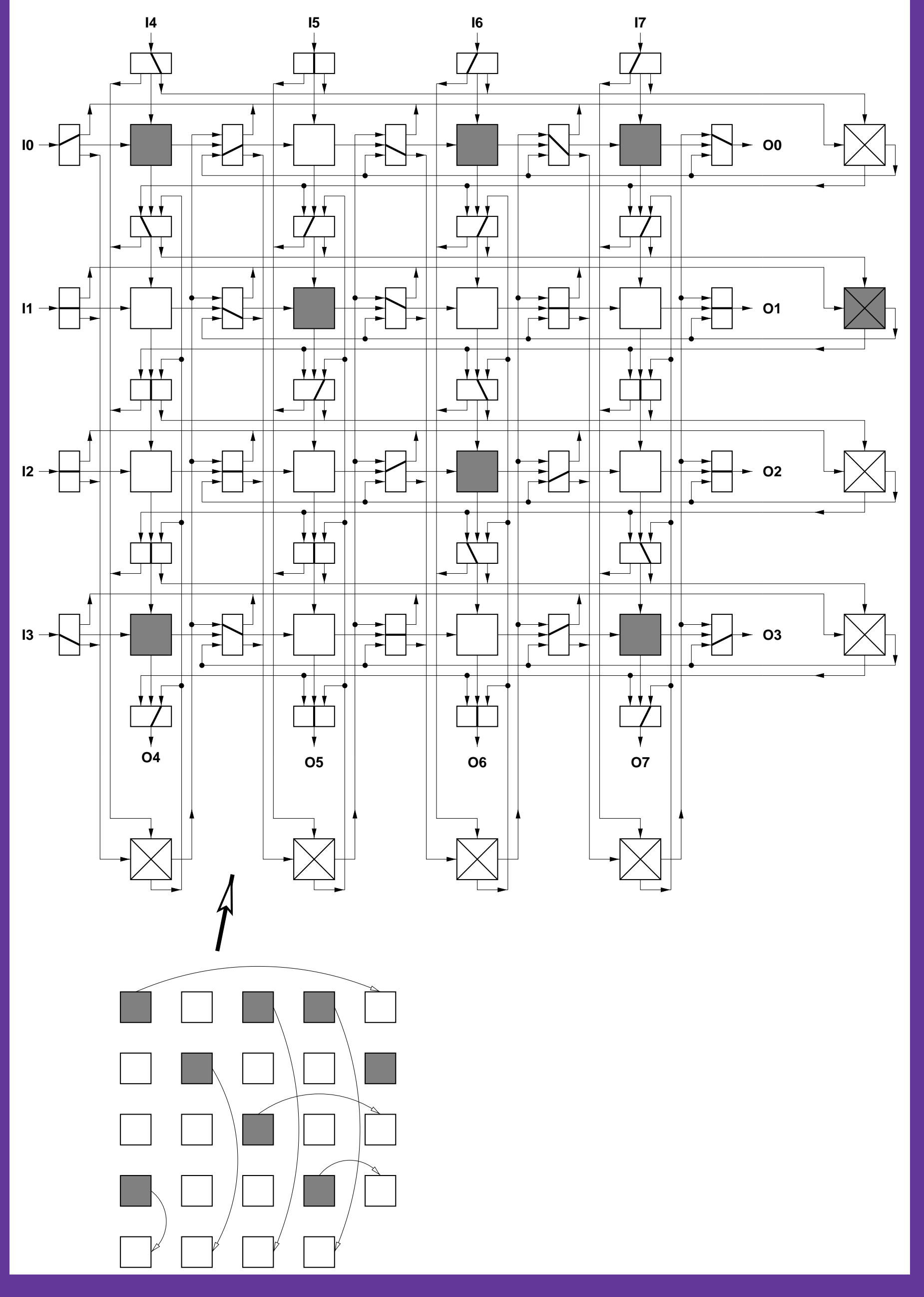
Sample Solution of Defective Array



Solution with appropriate MUX settings.
MUXs are automatically set by the outputs of adaptive circuit.

Symbolic solution showing how defective elements are replaced by spares.

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Overall Goal of the Proposed Research

Adaptive Self-Repairable Design (ASRD)

- Adaptive Self-Testing
- Built-in Self-Repair
  - Design of Programmable Switching Circuits
  - Design of Hardware Repair Algorithms
    - Development of Adaptive Circuits
    - Circuit and Logic Simulation
    - Fabrication and Testing
  - Design of Reconfiguration Circuits
  - Development of Theory
- Adaptive Self-Diagnosis

Development of Adaptive Circuits, Circuit and Logic Simulation, Fabrication and Testing → Circuits and Systems to Be Built

Subcircuits: SRAMs, PLAs, ROMs, Arithmetic and Logic Arrays
Subsystems: Square Processor Arrays, Hex Mesh, Systolic Arrays
Systems: MCMs, PCBs

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Adaptive Circuit for Memory Array

Row Neuron Output Shift Register

Column Neuron Output Shift Register

Quadrant 1

Quadrant 3

RAM Cell

Neuron Amplifier

Programmable Row Neuron Bias Generator

Programmable Column Neuron Bias Generator

R2,C4

R4,C1

R1,C3

R3,C2

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Adaptive Repair Logic and Fault Pattern Compaction

Faulty Col. Indicator SR

Incr.

Input Shift Enable

RAM Word Line Counter

Compressed Row Defect Pattern SR

Faulty Row Indicator SR

1024 X 1024 Memory Array

2

4

Col. Addr. Dec

Data Buffer

Quadrant 3 RAM Cells

Data Buffer

Row Addr. Dec.

Quadrant 1 RAM Cells

Row(i) Defect Pattern SR

Row Fault Count SR

Col. Fault Count SR

Programmable portion of the neural net's interconnection network

Row Number: 0, 64, 128

Column Number: 0, 64, 128

(a) Memory array defect pattern

1	1	0	0
0	1	1	0
0	0	1	0
0	0	1	1

(b) Compressed defect pattern

				1	1	0	0
				0	1	1	0
				0	0	1	0
				0	0	1	1
1	0	0	0				
1	1	0	0				
0	1	1	1				
0	0	0	1				

(c) Neural network RAM cell bit map

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Self-Repairable Systems

16K X 8 SRAM

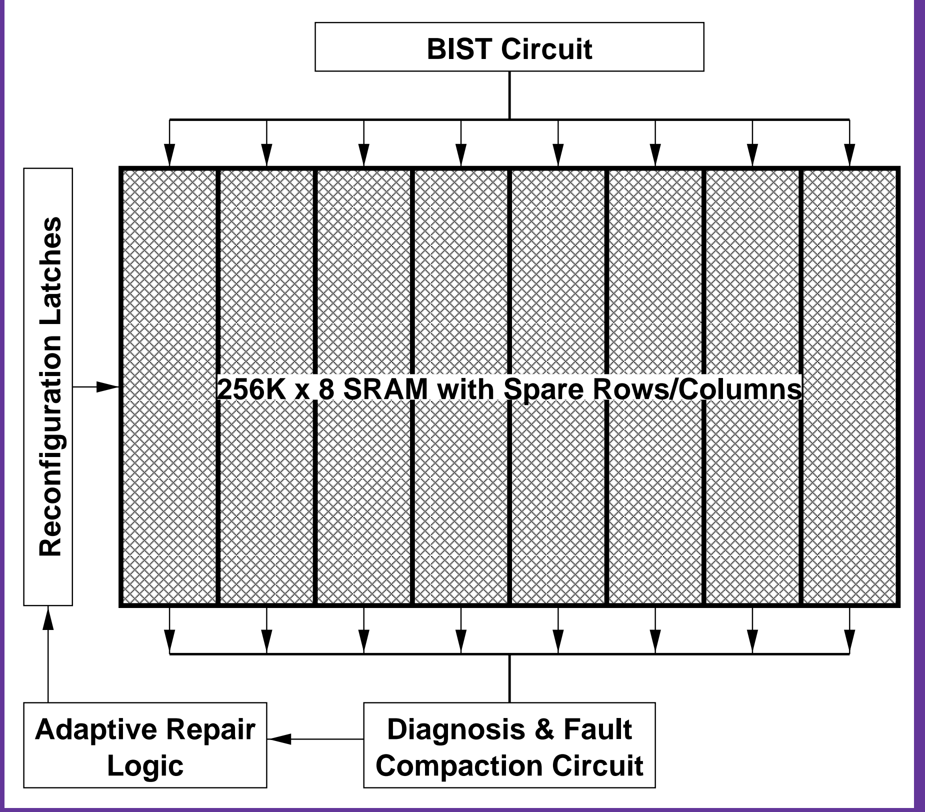
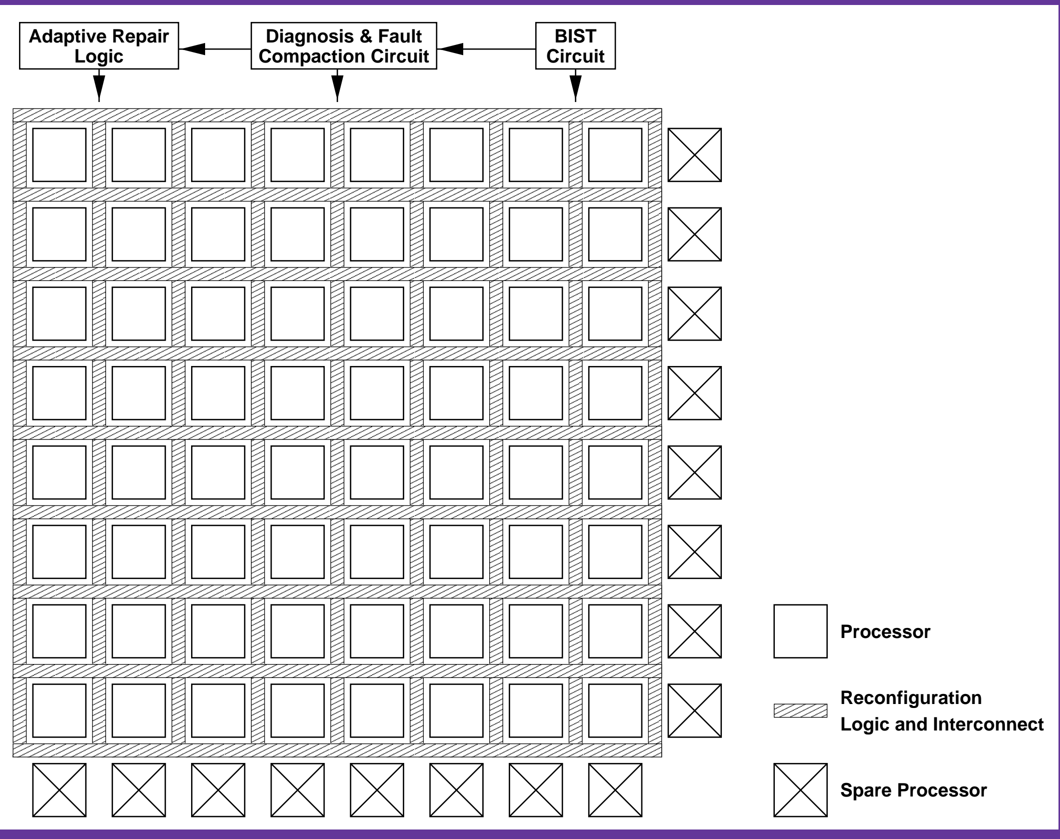


Image Processing Array



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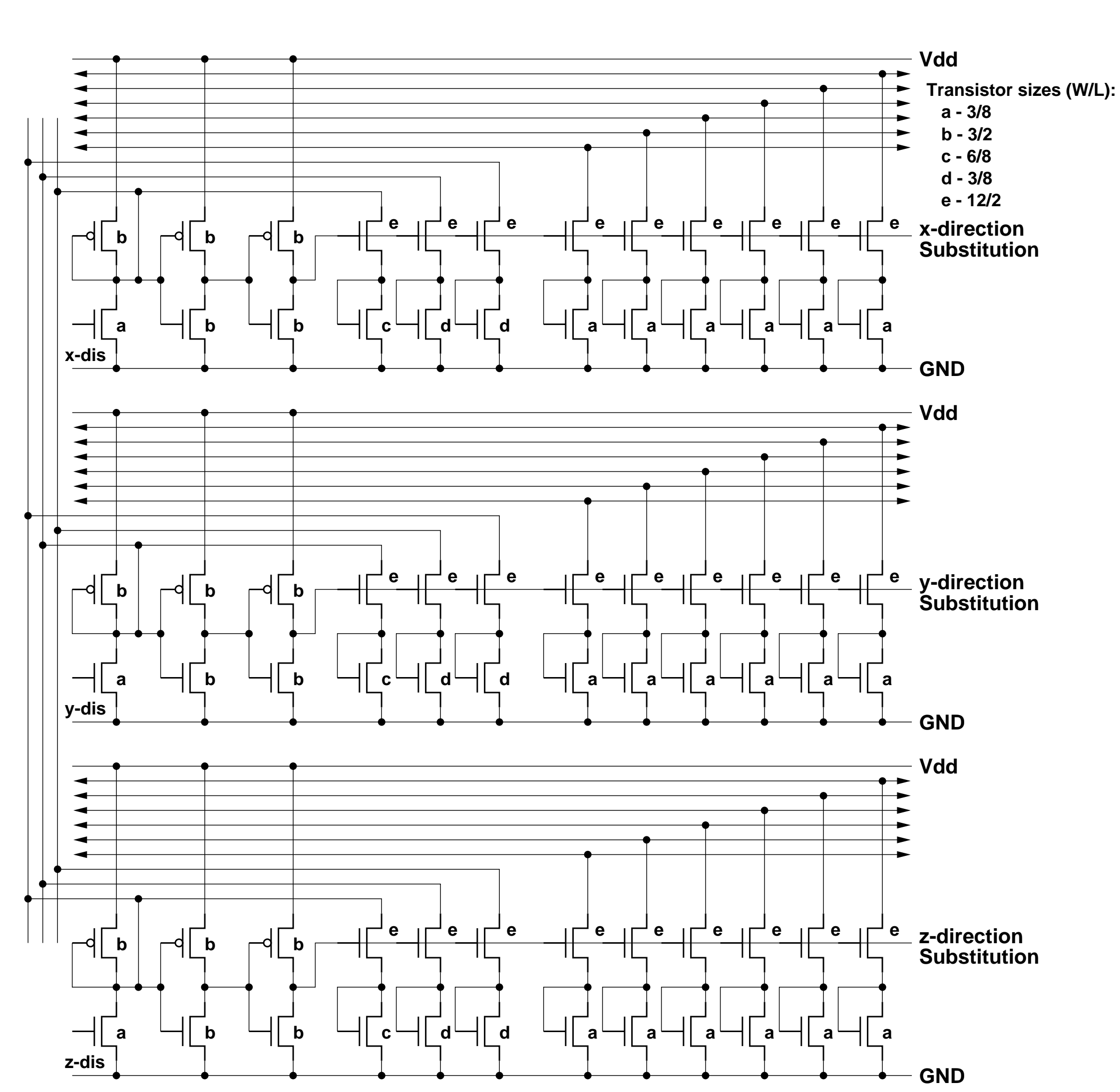
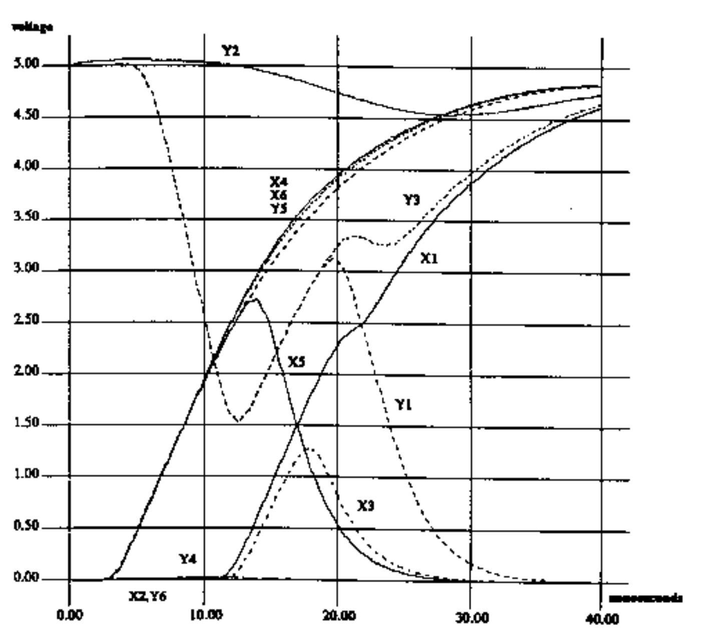
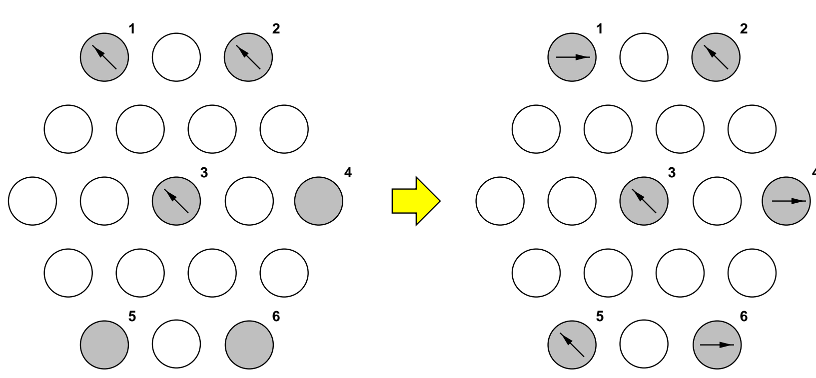
Adaptive Repair with Hexagonal Mesh







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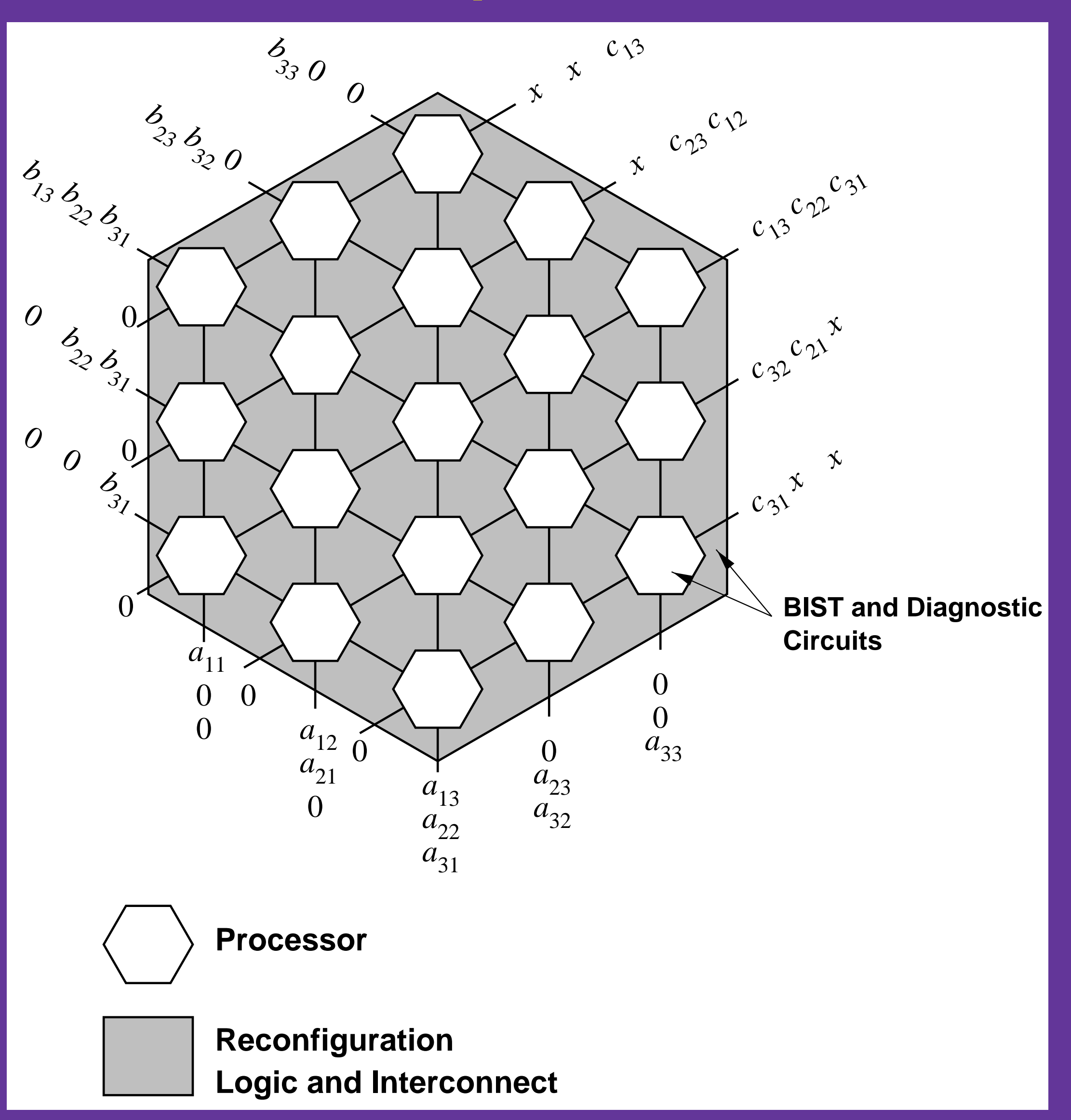
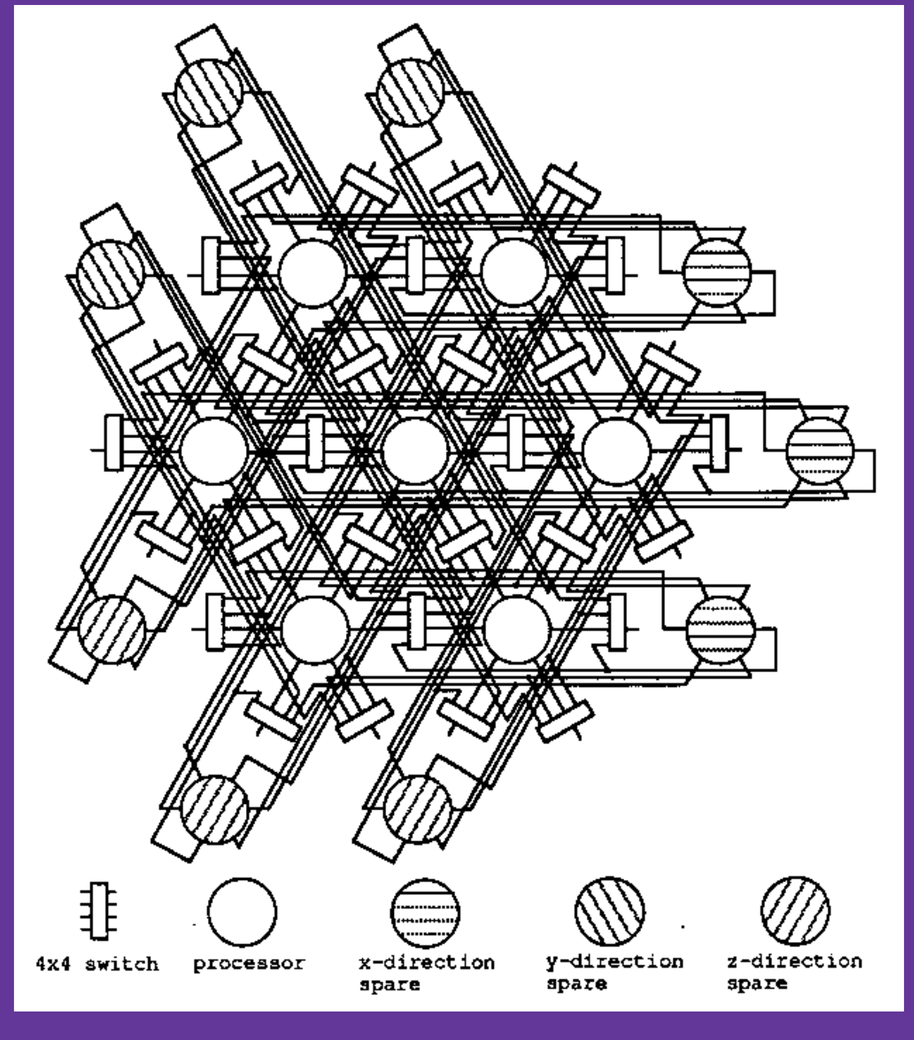
Repairable Hex Arrays

Architecture for Matrix Multiplication



Reconfigurable Hex Mesh



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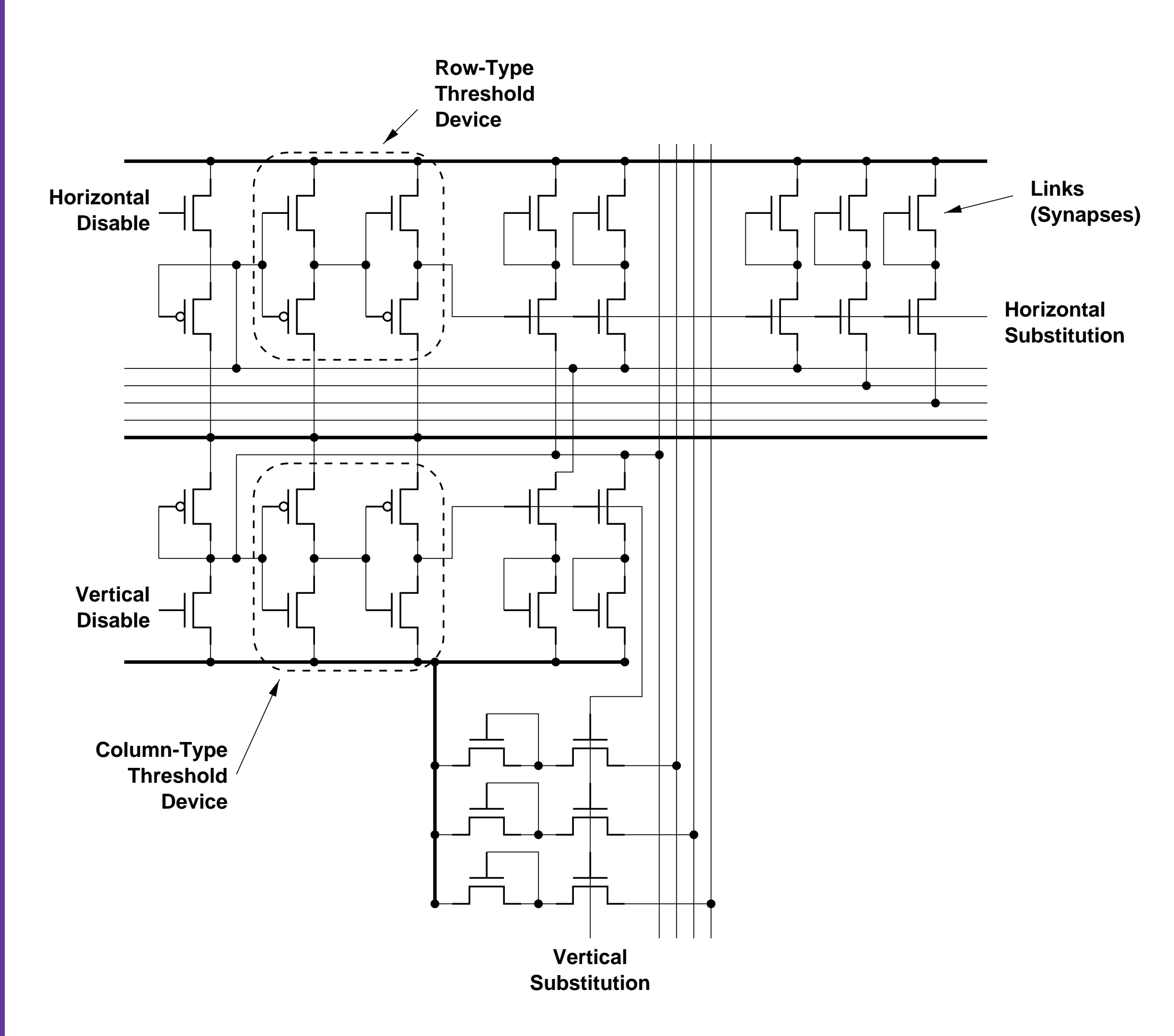
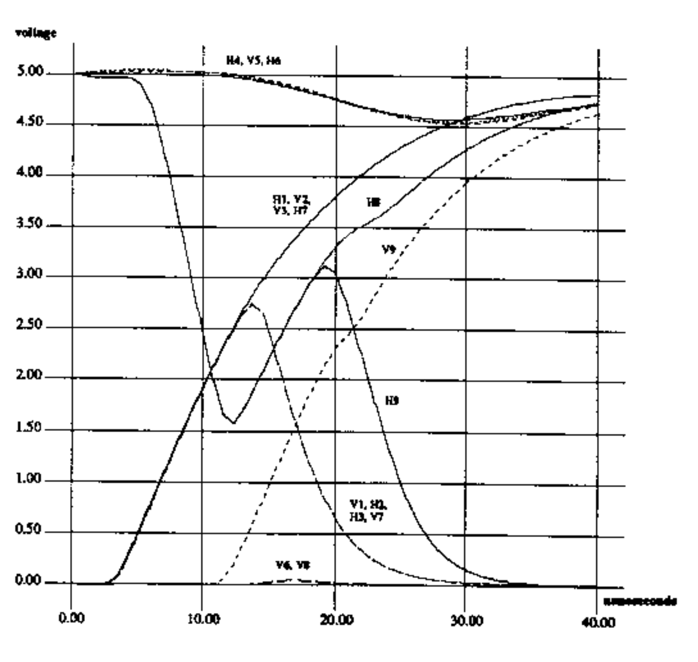
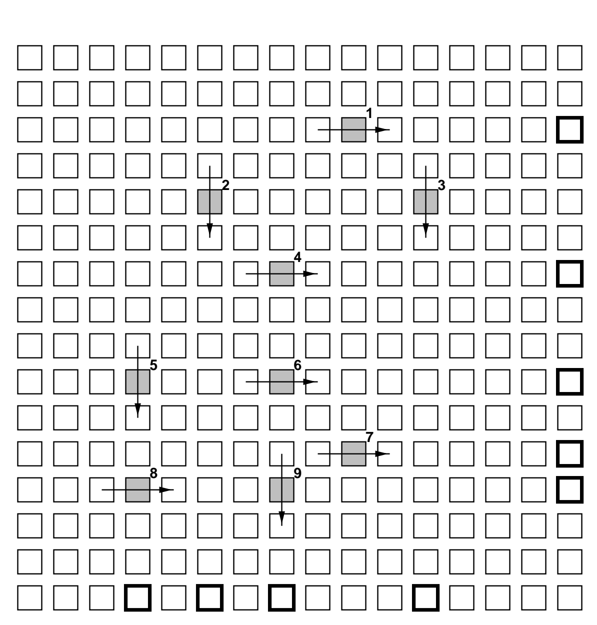
Adaptive Repair for Square Array







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Layout Research Overview

LAYOUT ALGORITHMS	PARALLEL MULTILAYER ROUTING	NEW DATA STRUCTURES FOR LAYOUT	LAYOUT ALGORITHMS FOR ON-CHIP PARALLEL PROCESSING
• GENETIC ALGORITHM BASED - multiway partitioning -standard cell placement -macrocell placement -gate matrix • DISTRIBUTED GENETIC ALGORITHM	• HEXAGONAL ARRAY FOR CONCURRENT 3-D MAZE ROUTING • MULTILAYER ROUTING MODELS ON POLYMORPHIC ARRAYS • SWITCHBOX ROUTING • CHANNEL ROUTING • MAZE ROUTING • AREA ROUTING • CHORD ROUTING	• QUAD TREE DATA STRUCTURE AND PLANAR TESSELLATIONS • OCTTREE DATA STRUCTURES AND 3-D TESSELLATIONS	• ASYMPTOTIC MODELING OF VLSI • INTERCONNECT NETWORKS EVALUATION - Topological mapping - Evaluation criteria -Evaluation technique • CELLULAR EMBEDDING TECHNIQUES -Yield-related layout techniques

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