PROF. PINAKI MAZUMDER

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•Resume: [Pdf version]
•Publications: Books [Coauthored] ; [Archival Papers; Edited Books; Book Chapters; Technical Reports]
PDF version of archival papers are available at IEEE Xplore.
•Research Accomplishments and Current Projects:
Summary of Accomplishments: 1) Nanocircuits, Nanoarchitectures and CAD Tools for Nanosystems [Overview PPT1], 2) Nanoscale and Very Deep Submicron CMOS VLSI Systems [Overview PPT2], 3) Semiconductor Memory Systems [Overview PPT3], and 4) VLSI Layout Automation [Overview PPT4].
Overview of Sponsored Research Projects: [Overview Chart]

Teaching

- EECS 270: Digital Logic Design
- EECS 312: Digital Integrated Circuit Design
- EECS 427: VLSI Design
- EECS 527: VLSI Layout Automation
- EECS 570: Parallel Architecture
- EECS 579: Digital System Testing
- EECS 598: Nanocircuits and Nanoarchitectures (F 06)

K-12 Education Software Development: [MathGuru]

Invited Talks: [Prof. Mazumder's Presentations]

NDR Group: Contact Prof. Mazumder at mazum@eecs.umich.edu

Description of Research Projects:

- **•Nanocircuits and Nanoarchitectures using RTD's and Quantum Dots (ONR, NSF, KG)**
- **•Plasmonics Interconnect Modeling: Nanoarrays, Nanowires and Nanoholes (AFOSR)**
- **•Quantum MOS Circuits on CMOS Substrates (DARPA, NSF, TI)**
- **•Modeling and Simulation Tools for Nano and Quantum Electronic Circuits (DARPA, ONR, NSF, KG)**
- **•Ultrafast Circuit Design with Compound Semiconductor Devices (DARPA, NSF, NEC, HRL, NL)**
- **•Very Deep Submicron CMOS VLSI Systems Design (ARO, NSF, SM)**
- **•CMOS Semiconductor Memory Testing, Fault Tolerance, and Reliability (ARO, NSF, DEC)**
- **•Full-chip Three-Dimensional Simulation using Finite Difference - Transmission Line Matrix (ONR)**
- **•CMOS VLSI Layout Automation: Self-repairable Memory Compilers, Placement and Routing Tools (DEC, BNR, IBM and GM)**

- **•Very Deep Submicron CMOS VLSI Reliability Issues:**

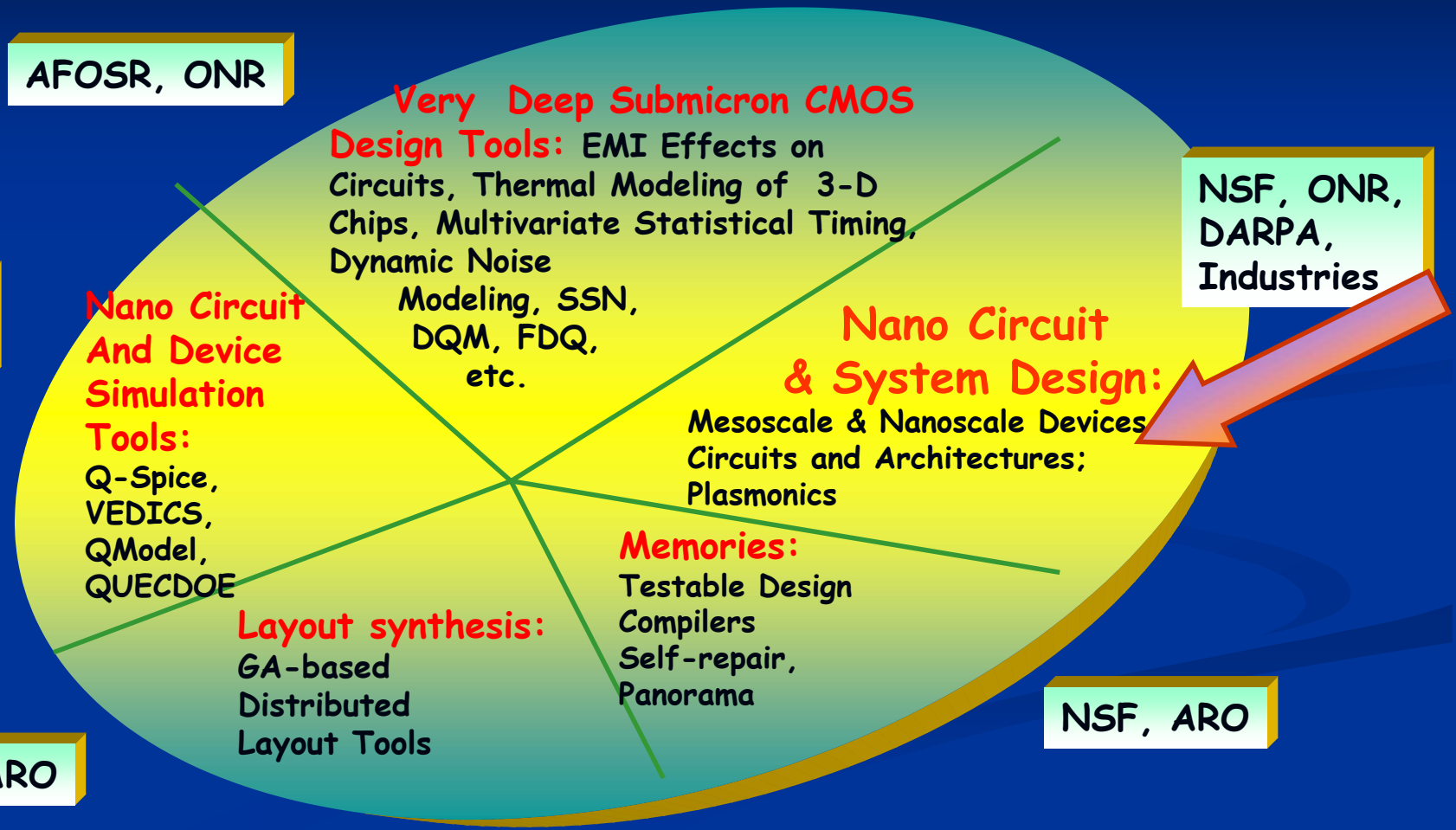
+ Electromagnetic Radiation Effects on Digital Circuits (AFOSR)
+ Simultaneous Switching Noise Effects on Caches and SRAM's (NSF)
+ Full-Chip Dynamic Noise Modeling (NSF)
+ Differential Quadrature Method for Interconnnect Delay and Timing Modeling (ONR)
+ Full-Chip Thermal Modeling by Green's Function (NSF, AFOSR)

Home Page of PINAKI MAZUMDER
http://www.eecs.umich.edu/~mazum

Names of Sponsors of Above Research Projects
(1) National Science Foundation (NSF), (2) Defense Advanced Research Projects Agency (DARPA), (3) Office of Naval Research (ONR),
(4) Army Research Office (ARO), (5) Air Force Office of Scientific Research (AFOSR), (6) State of Michigan (SM),
(7) Nippon Electric Company (NEC), (8) Bell Northern Reserach Laboratory (BNR), (9) General Motors (GM),
(9) Digital Equipment Corporation (DEC), (10) International Business Machines (IBM), (11) NanoLogic (NL),
(12) Korean Government Tera and Nanoelectronics Research (KG), (13) Texas Instruments (TI), (14) Hughes Research Lab (HRL)

Research Projects & Sponsors

PI: Prof. Pinaki Mazumder, University of Michigan



Quantum/Nano Systems Research Overview
Prof. P. Mazumder, NDR Group

Challenges: From Quantum Physics to Circuit Theory and Software Tools

CAD Tools

Q-Spice
* QMOS
* HEMT/HBT

QModel
* RTD
* Quantum Dots & Wires

QUECDOE
* 3-D Opt

VEDICS
* FD-TLM
* Full Chip

Circuits

- New Logic Families
- MVL Circuits
- Memories
- Nanopipelining
- Correlator, DDFS
- Turbocode Decoder
- Cellular Nonlinear Networks (CNN)
- Quantum Dot Image and Video Processors
- Plasmon Nanowire

Theory

- PDE and ODE based Nonlinear Circuit Analysis
- Quantum Physics based RTD & QD Modeling
- FD-TLM Ckt. Simulation

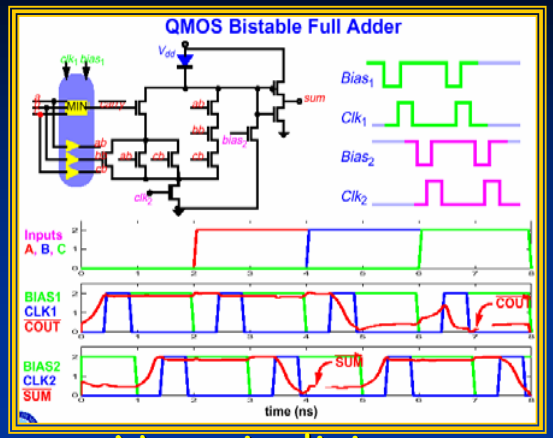
Fabrication

- SiO_2/Si-Ge based QMOS
  NRL, OSU
- InP based RTD+HEMT
  Raytheon
- InP based RTD+HBT
  KAIST, HRL
- GaSb Based RTD+HEMT
  HRL. ND

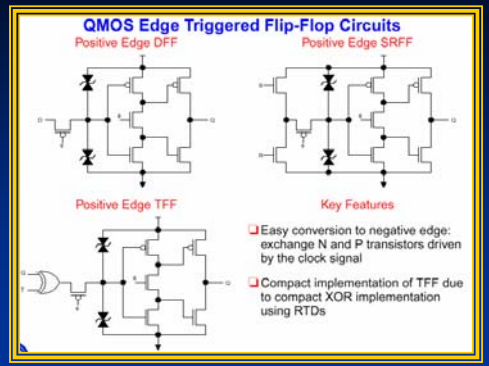
Nano-scale CMOS Design Issues
Prof. P. Mazumder, NDR Group

EM Effects on VLSI Circuits	Thermal Modeling of a 3-D Chips	Device and Interconnect Modeling	Statistical Timing Analysis	Dynamic Noise Analysis
Chebyshev's Approx & Pade Approx. for Distributed Noise Sources Finite Difference Quadrature Method	Green's Function based full-chip thermal analysis Direct Cosine Transform and IDCT for Fast Computation Hankel Transformation for Fast Computation	Envelope Function based quantum tunnel modeling of Nanoscale CMOS FET Differential Quadrature Method (DQM) for Interconnect Delay Modeling	Multivariate Normal Distributions for multi-input Domino gates Min/Max Correlation Analysis through Recursive Moment computation	Dynamic Noise Margins and Algorithms for Noise Analysis Simultaneous Switching Noise Estimation Coupling Noise Modeling for Automatic Routers

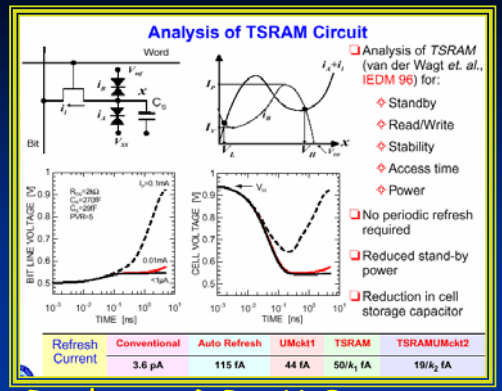
Quantum Tunneling Systems: Prof. Pinaki Mazumder, NDR Group



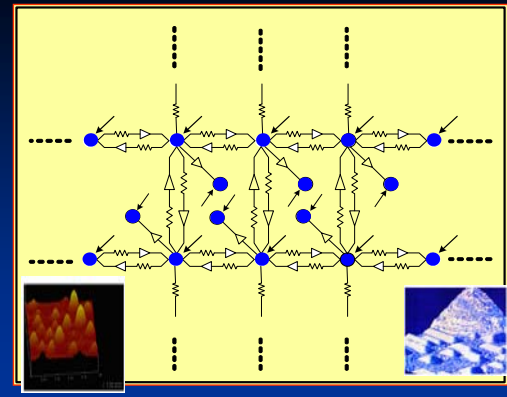
Nanopipelining Increases Speed



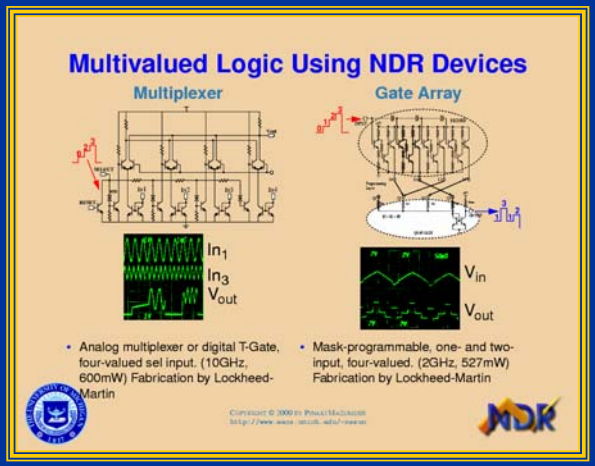
Bistability Improves Speed & Noise Margin In Dynamic Circuits



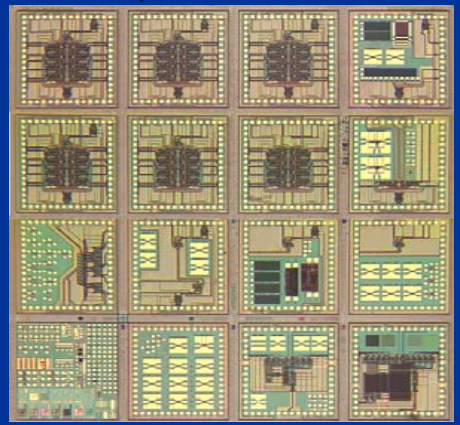
Reduces DRAM Power Consumption by X1000



Quantum Dot Array for Video Image Processing



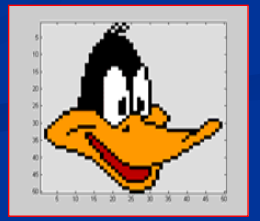
Multivalued Logic Provides Dense Integration & High Speed



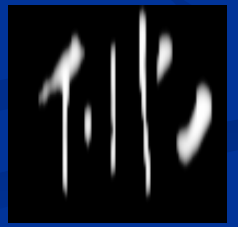
Quantum Integrated Circuits: Designed at UM And fabricated by Texas Instruments

Edge Detection

Line Detection



Color Extraction



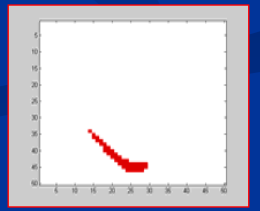


Image Processing by Quantum Dot Array

RAM Research Overview

Circuit Techniques	Test Algorithms	Error Correction	Self Repair	Compiler
• DFT for DRAM *TC-89* • DFT for CAM *TCAD-88* • DFT for random test *JETTA-92* • BIST for RAM *TIE-89* • ASIC for memory testing *JSSC-91*	• Parallel PSF *DAC-87, ITC-87* • Parallel parametric tests *JSSC-89* • Parallel stress tests *JETTA-94* • Tests for device-related faults *TCAD-93* • Board-level test *JETTA-2000*	• Double-bit ECC *JSSC-92* • Parallel signature analyzer based ECC *JSSC-93* • Projective geometric code *TC-93* • Radiation study • Reliability analysis	• Pseudo-analog adaptive circuits for self-repair *TCAD-96* • Digital adaptive circuits for self-repair *TCAD-93* • Generalized adaptive self-repair circuit techniques *TCAD-92,93*	• RAM compiler - Self-testing - Self-repair *EDAC-99* • ROM compiler - Self-testing - Self-repair *ICCD-99* *VLSIJ-99*

- Books written by P. Mazumder
  - Testing and Testable Design of High-Density RAM, 1996
  - Fault Tolerance of RAM, 2000
  - Circuit Techniques for DRAMs (under preparation)

Layout Research Overview

Layout Algorithms	Parallel Multilayer Routing	New Data Structures For Layout	Layout Algorithms for On-Chip Parallel Processing
• Distributed genetic Algorithm *TCAD-93* • Genetic-Algorithm-Based: - multiway partitioning *PH-99* - standard-cell placement *VLSIJ-91* - gate matrix *IEE Proc.-94*	• Hexagonal Array for Concurrent 3-D Maze Routing • Multilayer Routing Models on Polymorphic Arrays *TCAD-90, TVLSI-93* • Switchbox Routing *IEE Proc.-95* • Channel Routing • Maze Routing • Area Routing • Chord Routing	• Quad Tree Data Structure and Planar Tessellations *CVGIP-87* • Oct Tree Data Structures and 3-D Tessellations	• Asymptotic Modeling of VLSI *ICPP-87* • Interconnect Network Evaluation *TC-87* -topological mapping -evaluation criteria -evaluation technique • Cellular Embedding Techniques *IEE Proc.-92* -Yield-related layout techniques