COURSE ANNOUNCEMENT: WINTER 2002
EECS 527: CAD Techniques for VLSI Layouts
3 Credits, Mon, Wed 12:00-1:30 p.m.

Instructor: P. Mazumder, EECS Department

Contents: General theory and concepts of VLSI, FPGA, MCM and PCB layouts; Floor-planning, partitioning and placement techniques; High-performance wire routing; Layout compaction techniques; Custom layout techniques: Field-programmable gate arrays (FPGA's), sea-of-gates and gate arrays, gate matrix and PLA's.

Prerequisite: Instructor's Consent

Goal: This course examines the fundamental optimization algorithms that are employed in the design of high-performance CAD layout tools for VLSI and PCB systems. Commercial VLSI chips such as Intel's Pentium and Digital's Alpha chips now contain several million transistors, and, by another decade or so as per SIA Roadmap, the scale of device integration is likely to exceed 1 billion transistors per chip. This spectacular growth of VLSI integration technology cannot be economically viable unless suites of high-quality CAD tools are available for developing chip layouts in reasonable time.

In modern high-performance VLSI system design, physical layout design and the system architectural design are often interlinked in a complex way, and, consequently, the VLSI system designers must be fully conversant with the capabilities of CAD tools that perform layout tasks such as partitioning, floorplanning, placement, wire routing and chip compaction. Signal delays in numerous paths, which critically affect computing speed and system performance, depend as much on the placement and floorplanning styles as they are decided by the appropriate choice of system architecture and circuit design styles. For such applications, the commercial tools do not provide high-quality layouts; frequently, the designers are required to develop new tools or to refine the existing layout tools by adding appropriate add-on features so that the best performance of the VLSI chip can be achieved. In order to be a good VLSI engineer, you ought to learn the core design principles of VLSI layout tools and how they can be augmented to enhance and expedite your chip design projects.

Computer Usage: Some programming knowledge in C and/or C++ is required.

Evaluation: Homework (30%), Examinations (20%) and Project (50%)

Schedule - Part 1: pre-Spring Break

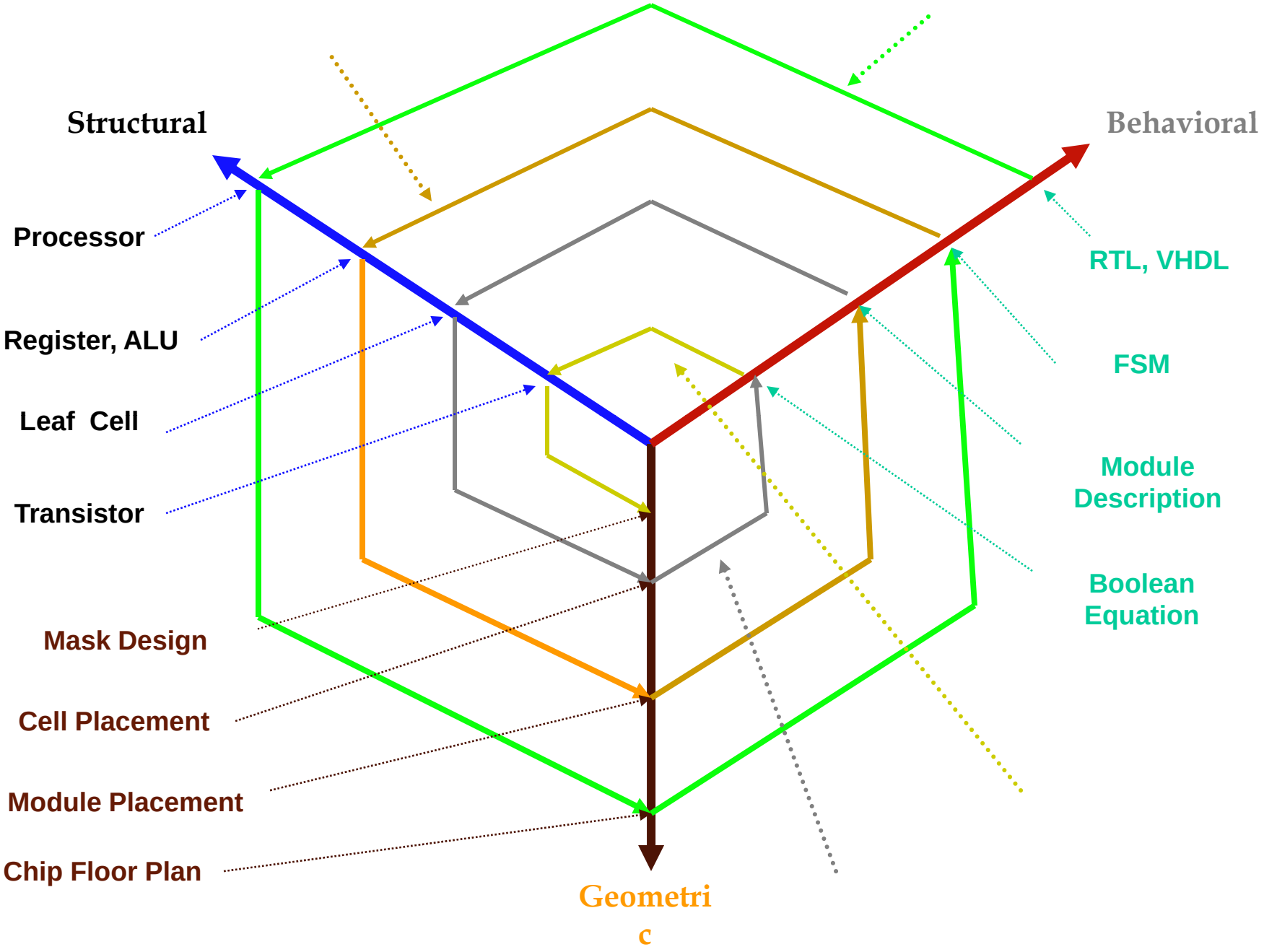
Date	Topic	Book Sec	HomeWork	Exam/Quizz
7-Jan	Introduction; Basics of Semicustom Design	Sec. 1.1, 1.2, 1.3		
9-Jan	Full Custom Design v. Semicustom Design	Sec. 1.3, 1.4, 1.5		
14-Jan	Introduction to Partitioning	Sec 2.1, 2.2, 2.3		
16-Jan	Kernighan and Lin Partitioning Algorithm	Sec 2.3, 2.4.1		
21-Jan	**MLK Day**			
23-Jan	Fidducia-Matheyese Algorithm	Sec 2.4.2		
28-Jan	Gain Look Ahead Technique	Paper 1 (suppl)		
30-Jan	Ratio Cut and Other Methods	Paper 2 (suppl)		
4-Feb	**Exam (20 mts)**; Introduction to Floorplanning	Sec 3.1, 3.2		**Quizz #1 (20 mts)**
6-Feb	Dual Graph Method of Floorplanning	Sec 3.3.4		
11-Feb	Simulated Annealing for Floorplanning	Sec 3.3.1	**HW 1 (Due)**	
13-Feb	Introduction to Placement	Sec 4.1, 4.2, 4.3		
18-Feb	Simulated Annealing for Std. Cell Placement	Sec 4.4.3		
20-Feb	Force-Directed Placement	Sec 4.4.4		
4-Mar	Passive Resistive Network Optimization	Paper 3 (suppl)		
6-Mar	Other Placement Techniques	Sec 4.5	**HW 2 (Due)**	

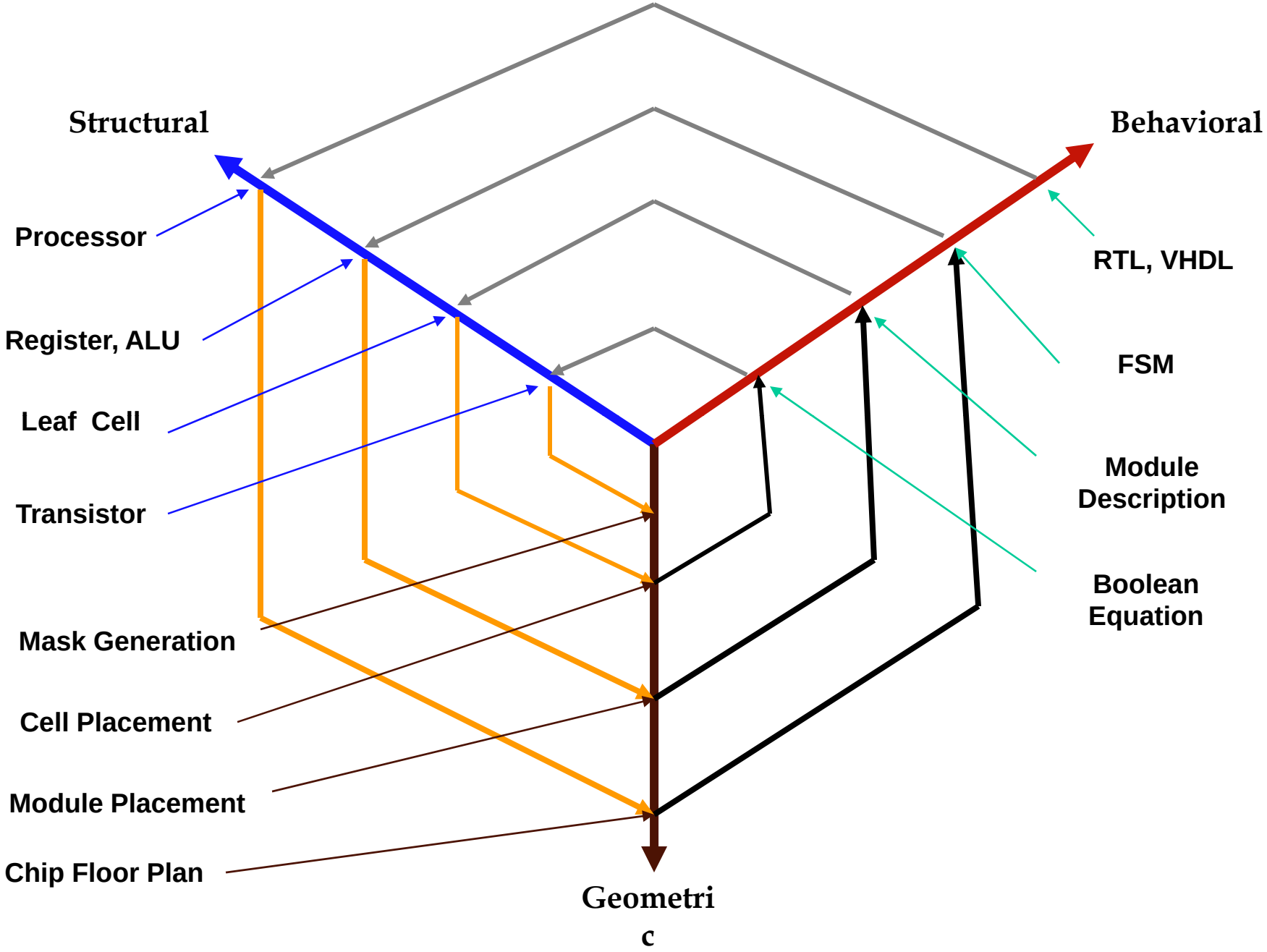
Homework is individual ; Quiz is of 20 minutes ; Final Project is individual

Semi-Custom Design Methodologies

VLSI Design Methodology

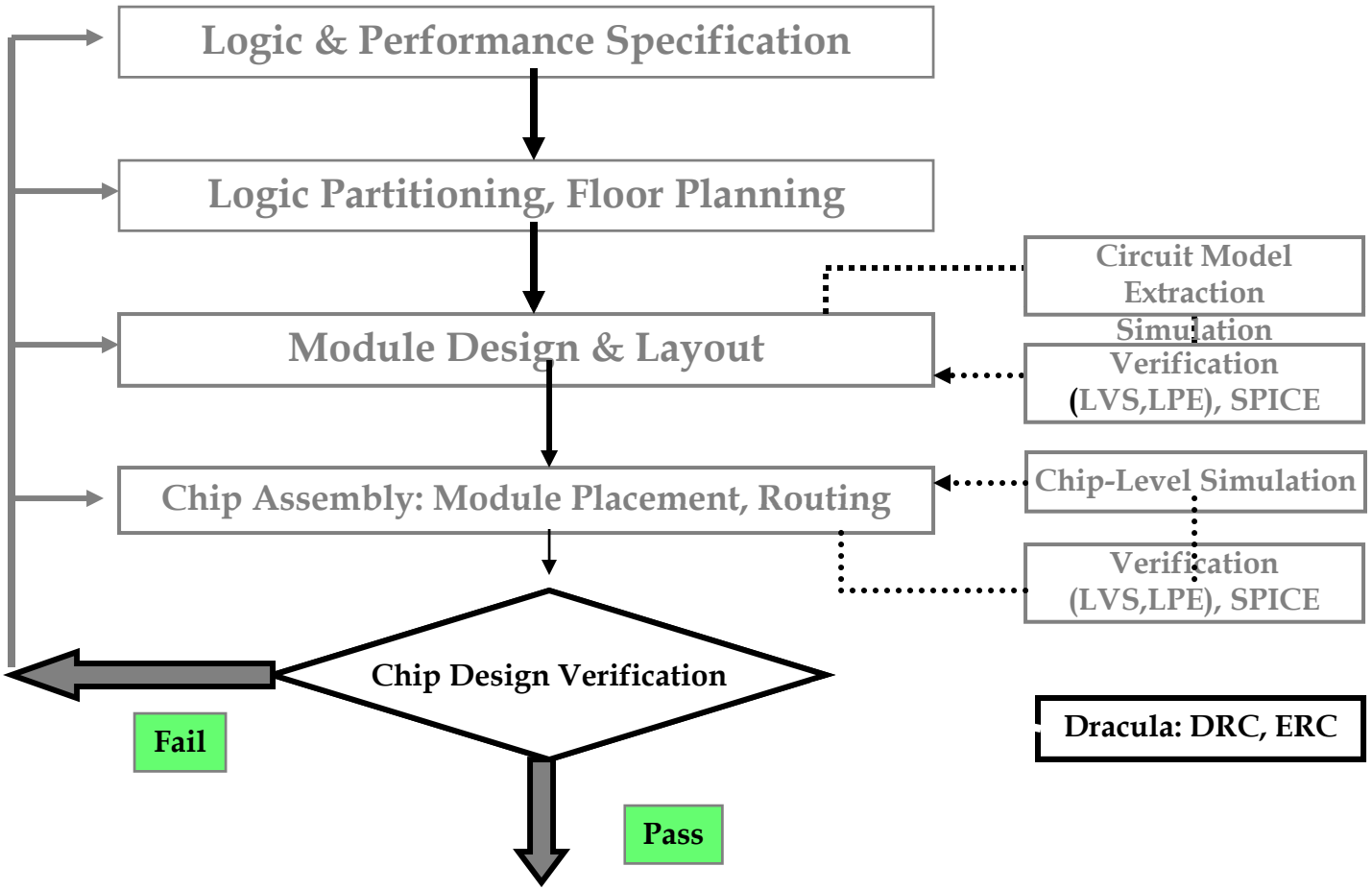
- Structural Description
  - Specifies the system's architectural components and their interconnections.
- Functional or Behavioral Description
  - Specifies the system behavior, instruction set, logic functions, I/O behavior at pins etc.
- Geometric Description
  - Specifies the physical implementation of the system such as floorplan, placement of cells, routing of blocks and layout of the cells.

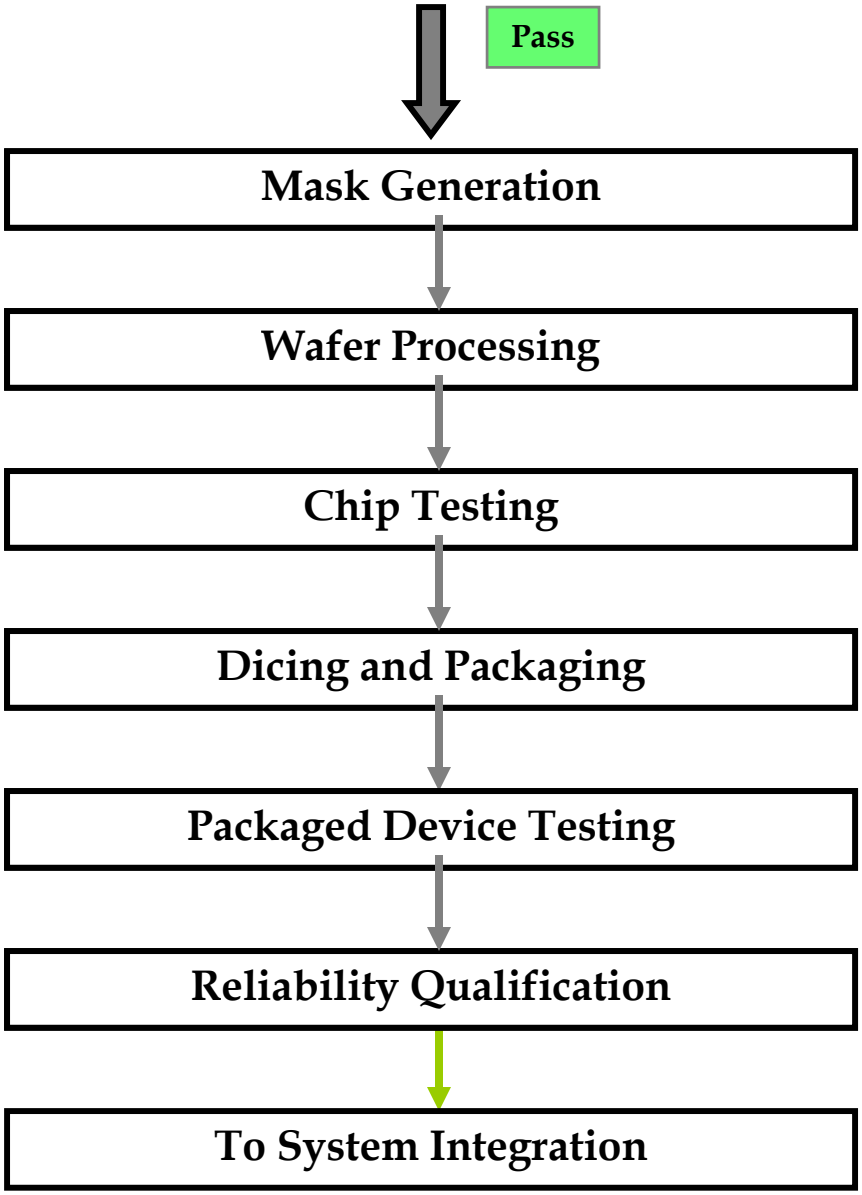

Structural
Behavioral
Processor
Register, ALU
Leaf Cell
Transistor
RTL, VHDL
FSM
Module Description
Boolean Equation
Mask Design
Cell Placement
Module Placement
Chip Floor Plan
Geometri
c



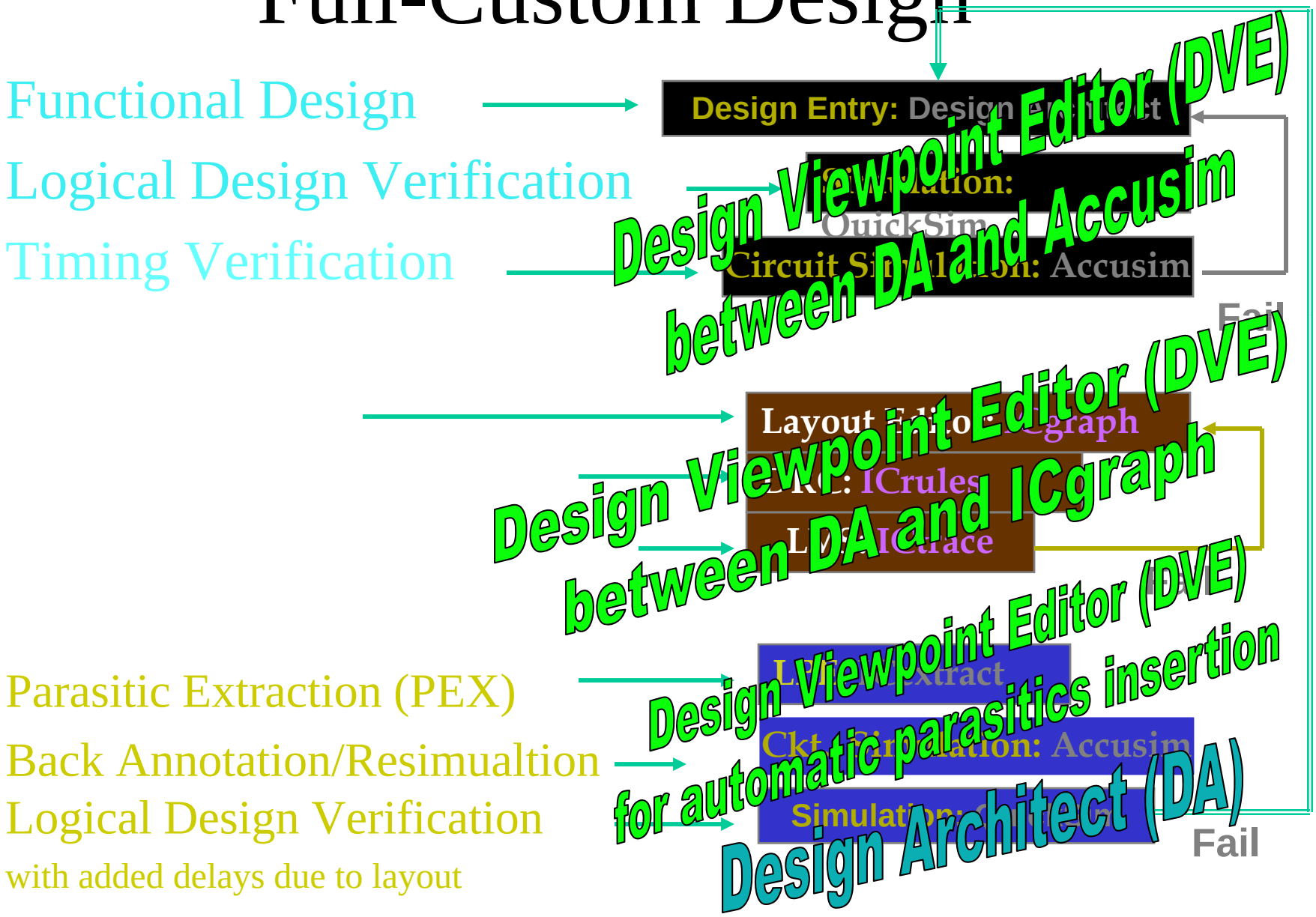
Weste & Eshraghian, pp. 21-29

Elements of VLSI Physical Design in a Full Custom Approach

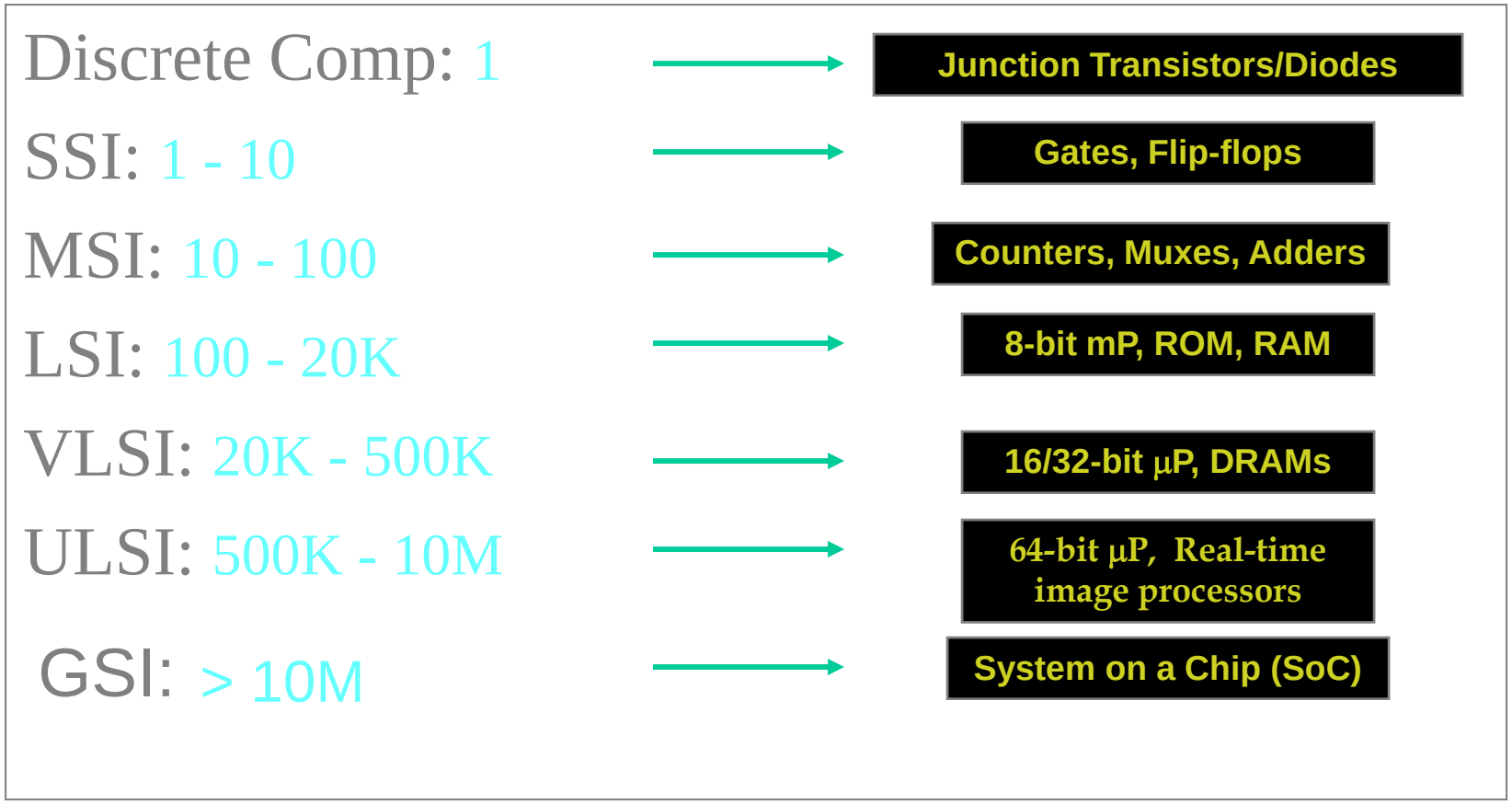



Pass
Mask Generation
Wafer Processing
Chip Testing
Dicing and Packaging
Packaged Device Testing
Reliability Qualification
To System Integration

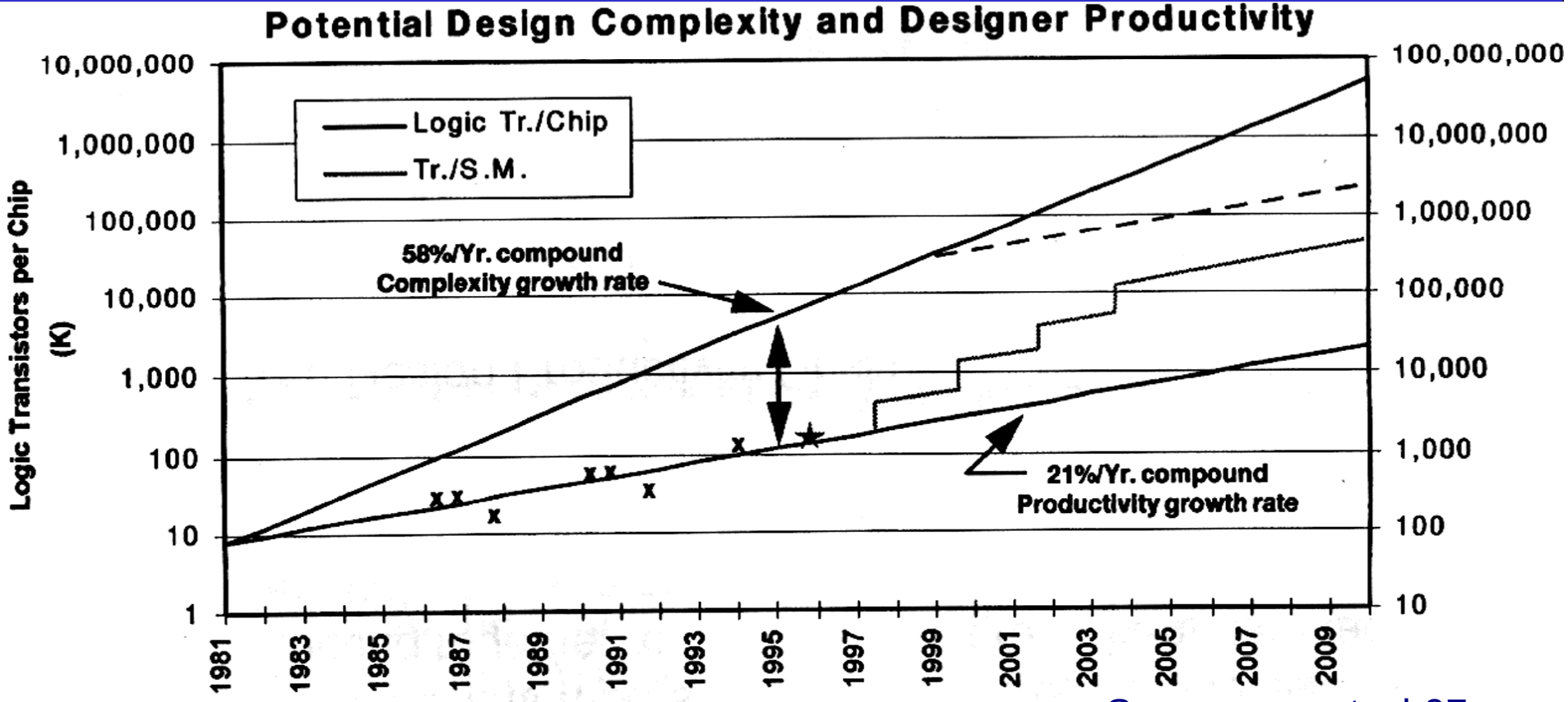
Full-Custom Design



Integration Terminologies

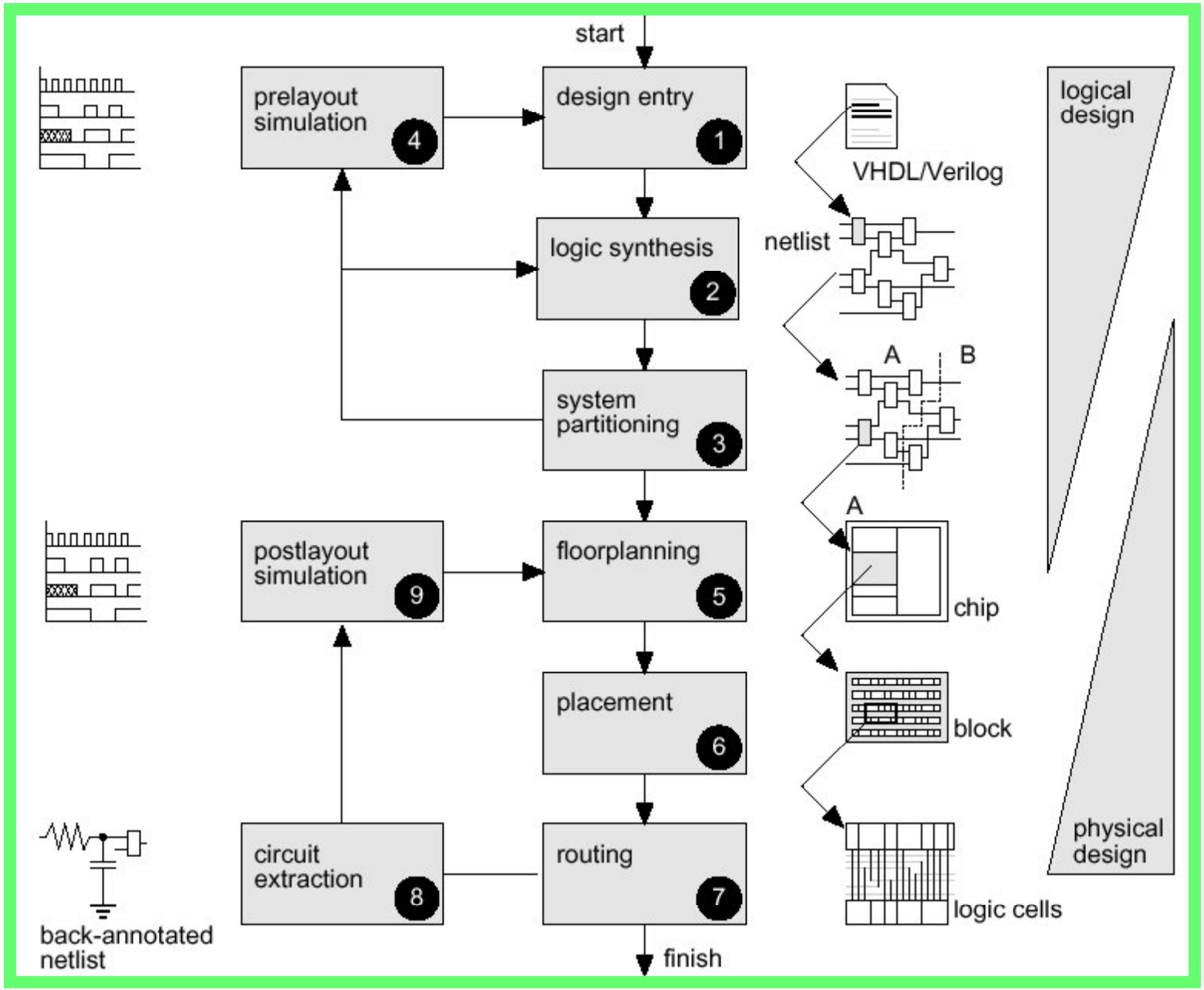


The Design Problem

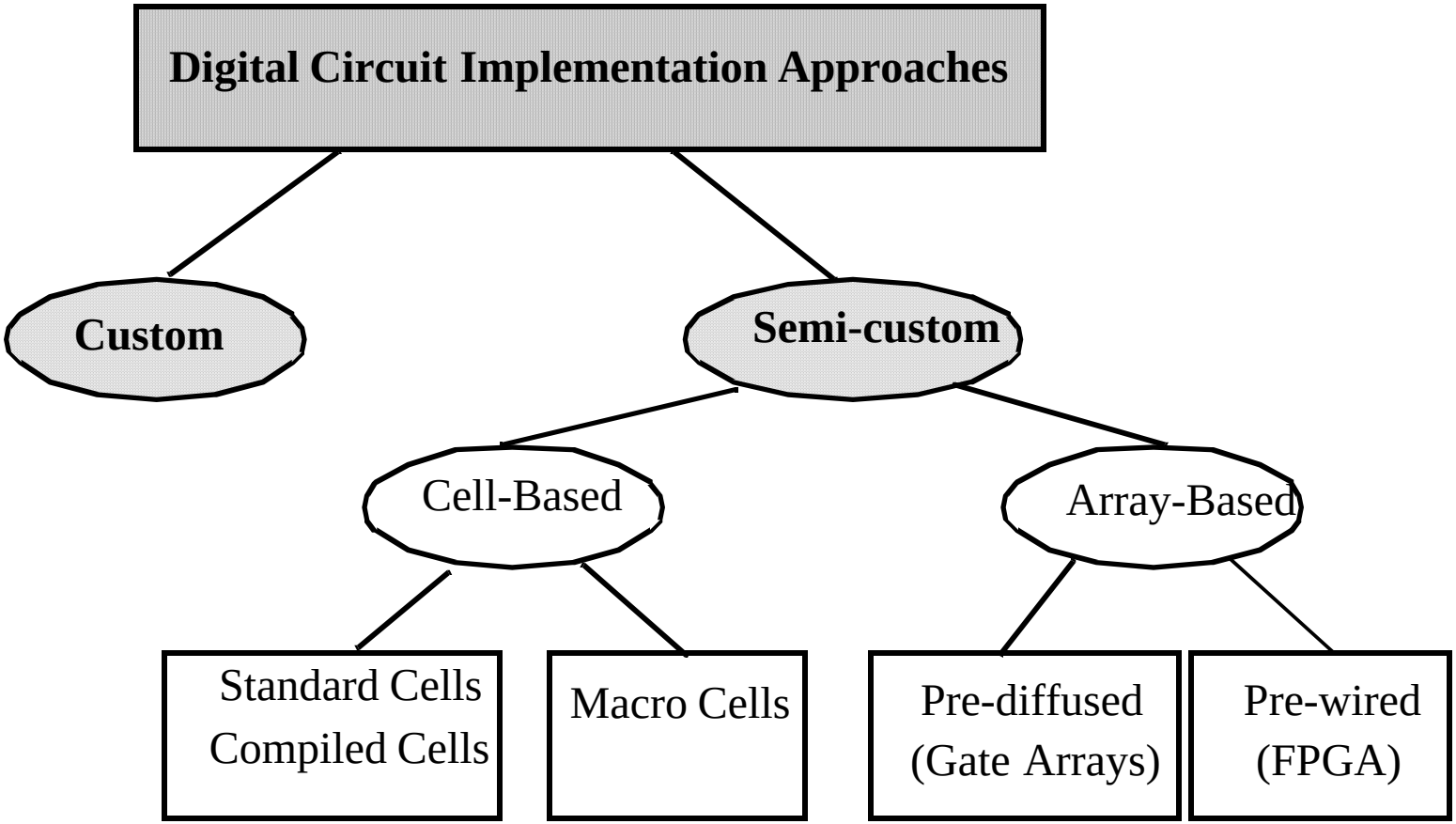


Source: sematech97

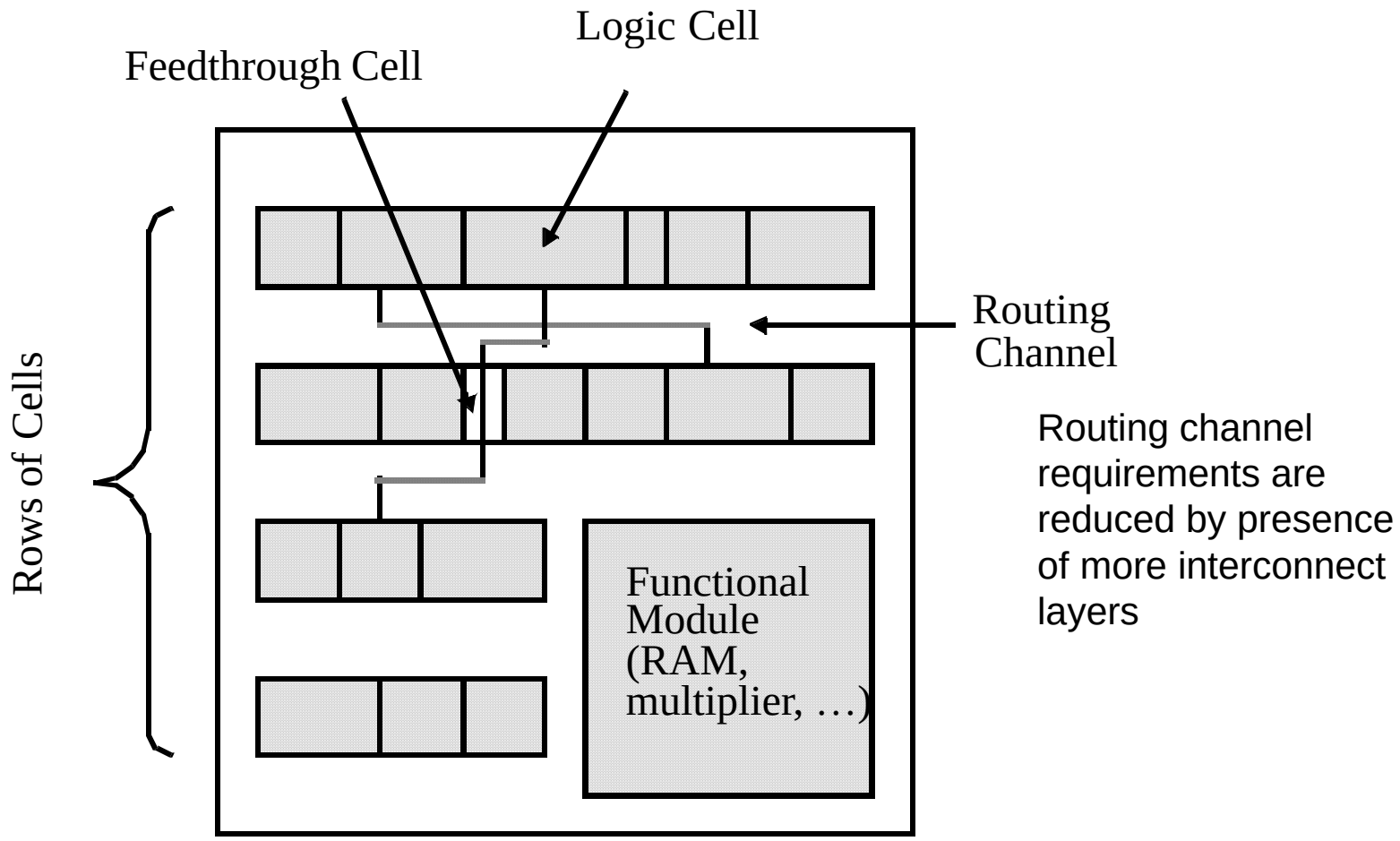
A growing gap between design complexity and design productivity


start
prelayout simulation
4
design entry
1
logic synthesis
2
system partitioning
3
floorplanning
5
placement
6
routing
7
circuit extraction
8
postlayout simulation
9
finish
back-annotated netlist
VHDL/Verilog
netlist
A
B
A
chip
block
logic cells
logical design
physical design

Implementation Methodologies

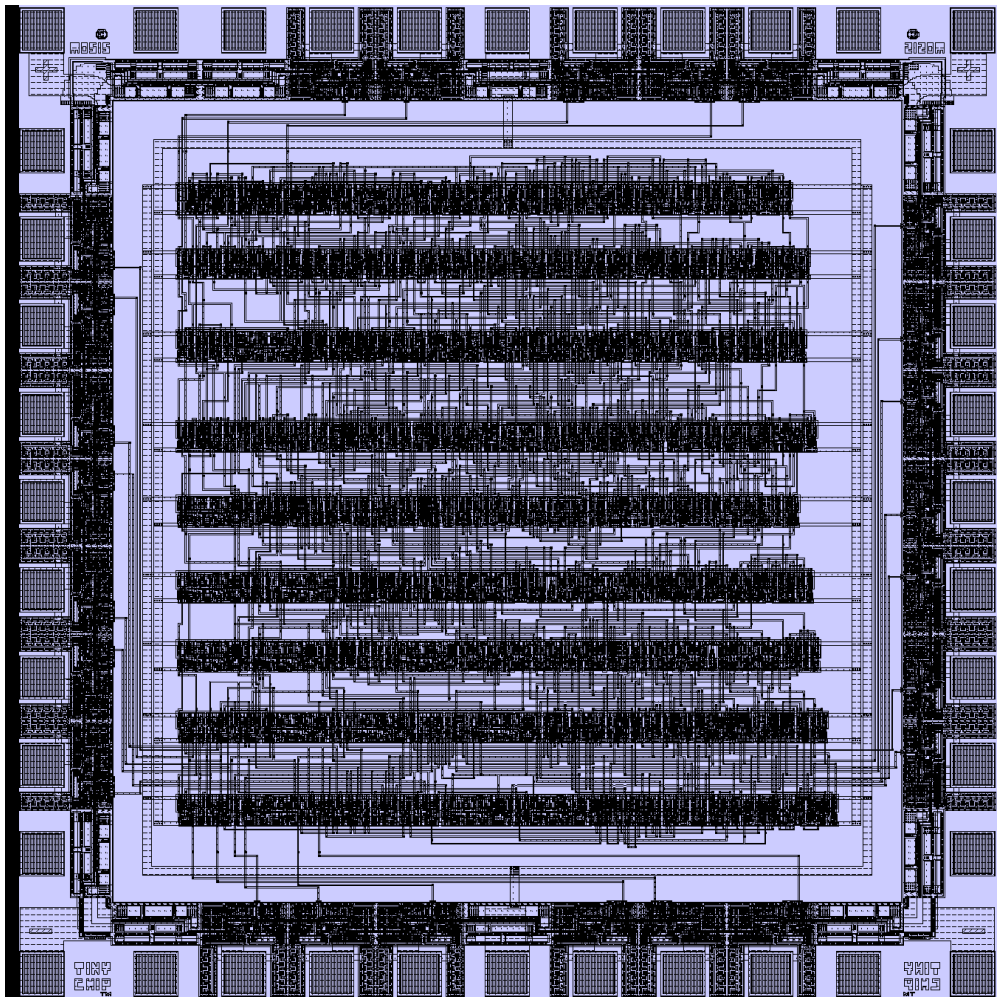


Cell-based Design (or standard cells)



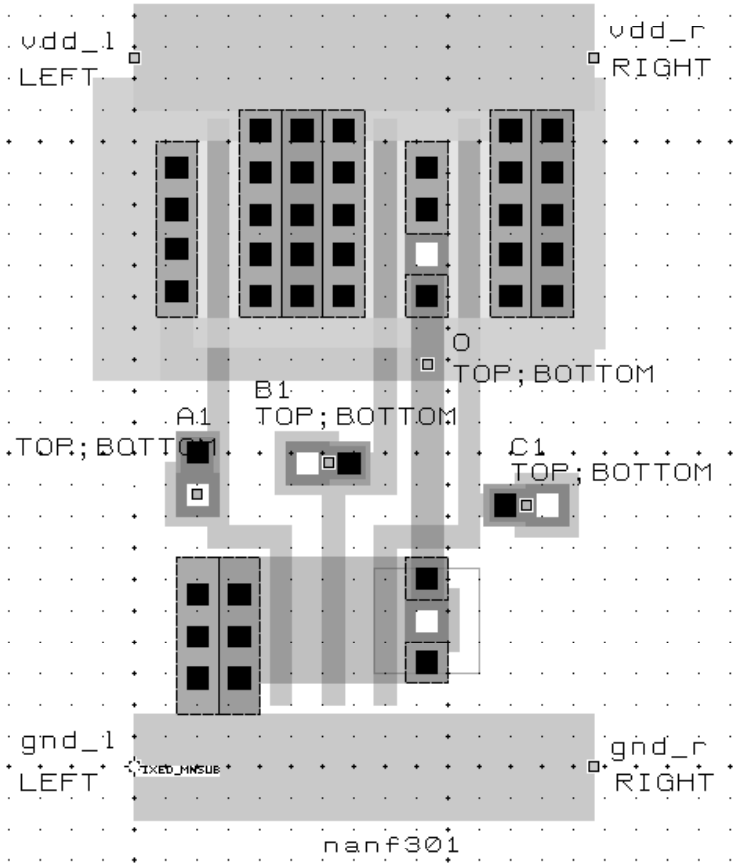
Routing channel requirements are reduced by presence of more interconnect layers

Standard Cell — Example



[Brodersen92]

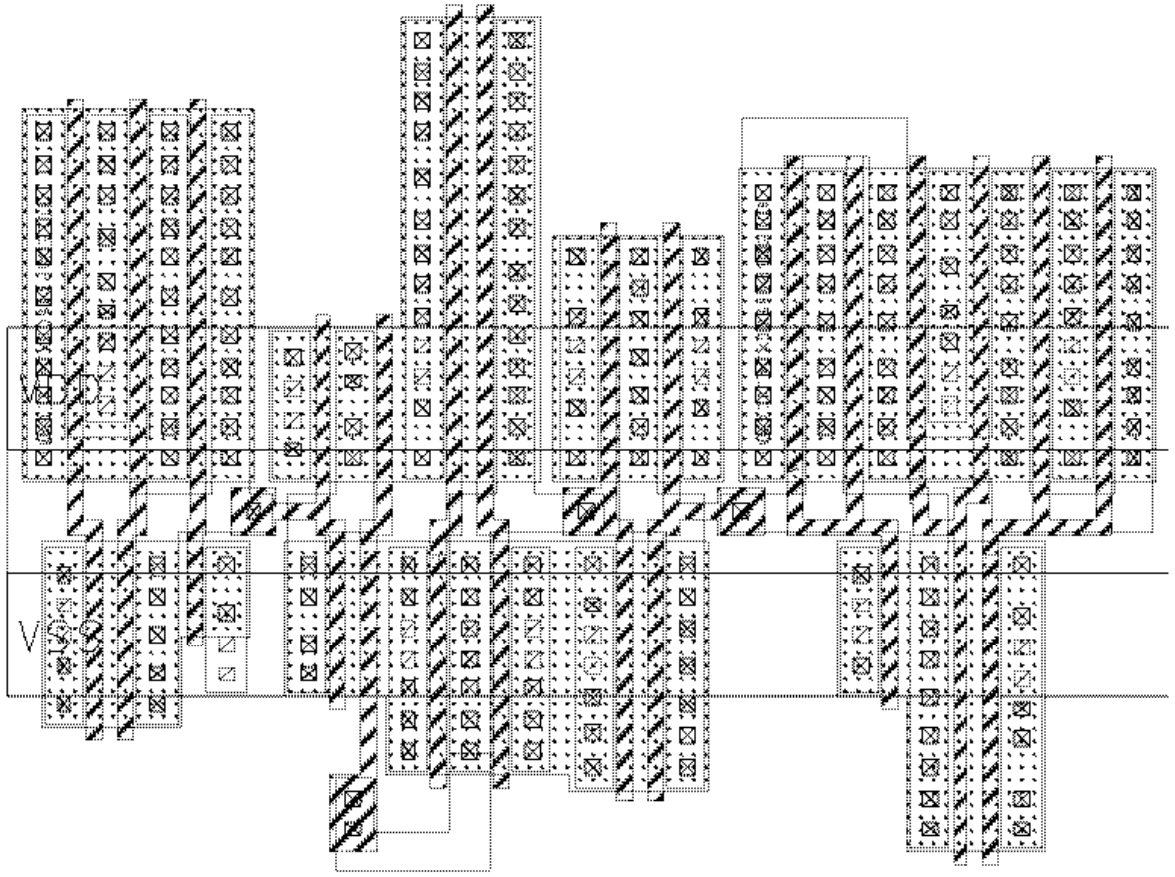
Standard Cell - Example



Fanout 4x	0.5 μm	1.0 μm	2.0 μm
A1_tphl	0.595	0.711	0.919
A1_tplh	0.692	0.933	1.360
B1_tphl	0.591	0.739	1.006
B1_tplh	0.620	0.825	1.1.81
C1_tphl	0.574	0.740	1.029
C1_tplh	0.554	0.728	1.026

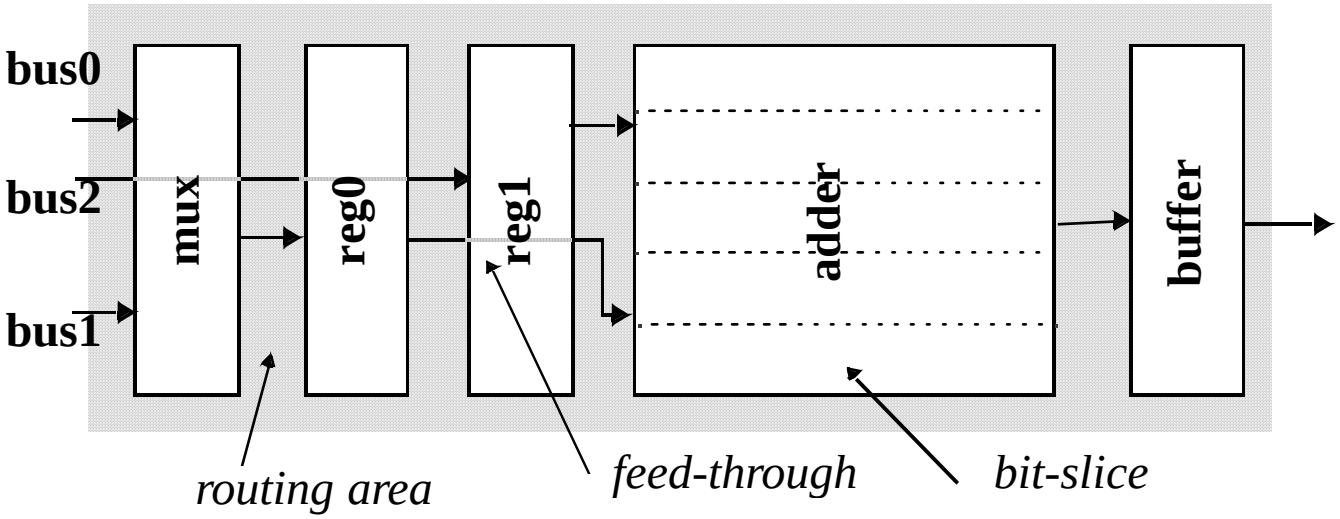
3-input NAND cell
(from Mississippi State Library)
characterized for fanout of 4 and
for three different technologies

Automatic Cell Generation



Random-logic layout generated by CLEO cell compiler (Digital)

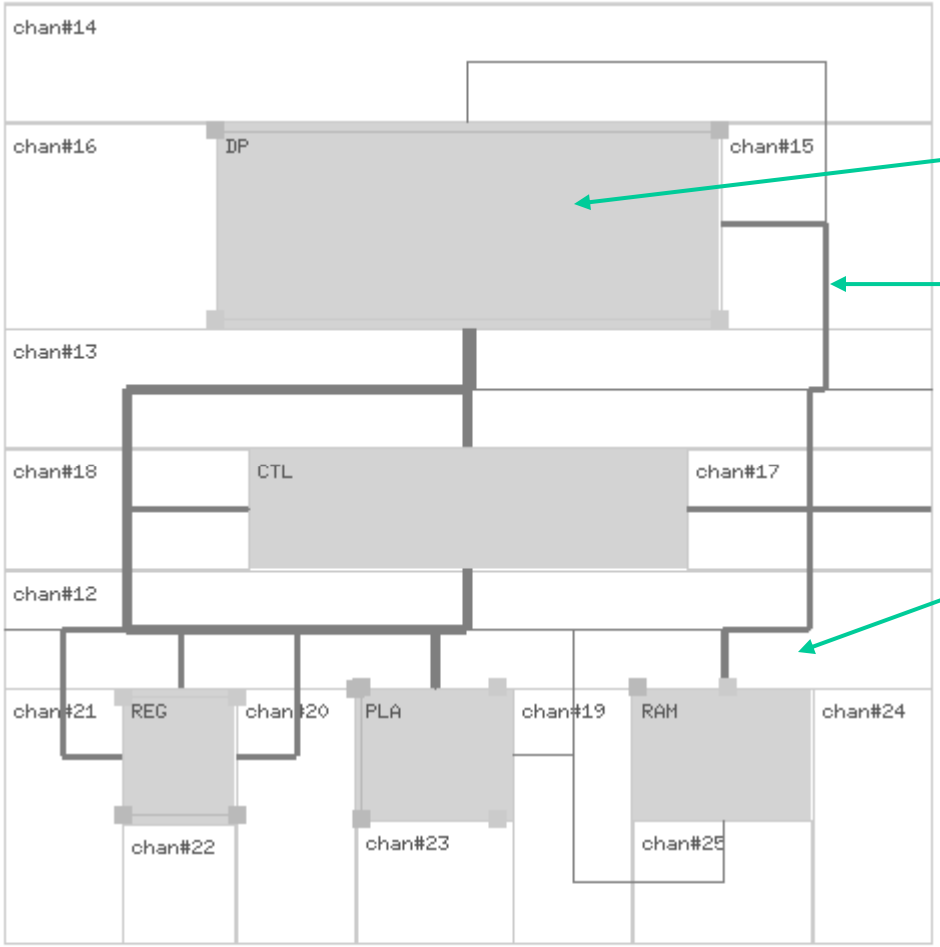
Module Generators — Compiled Datapath



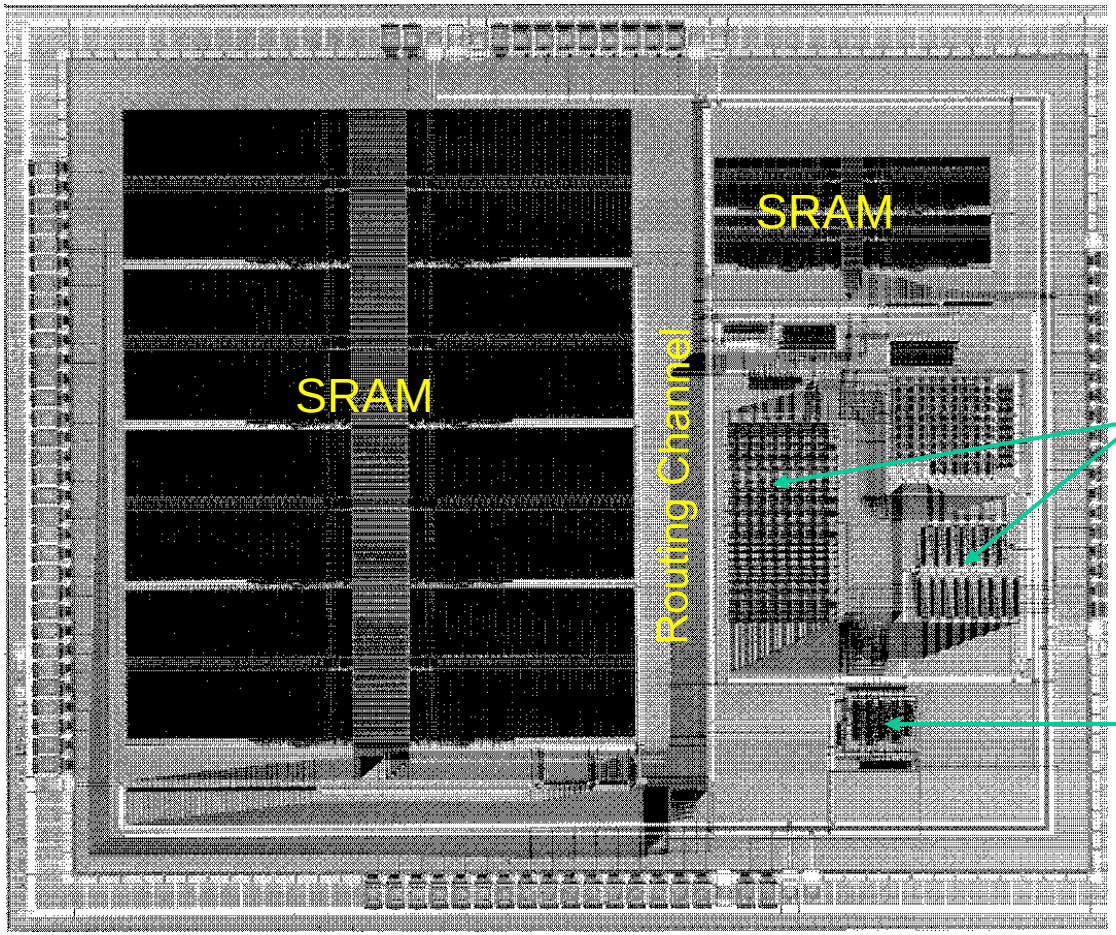
Advantages: One-dimensional placement/routing problem

Macrocell Design Methodology

Floorplan:
Defines overall topology of design, relative placement of modules, and global routes of busses, supplies, and clocks

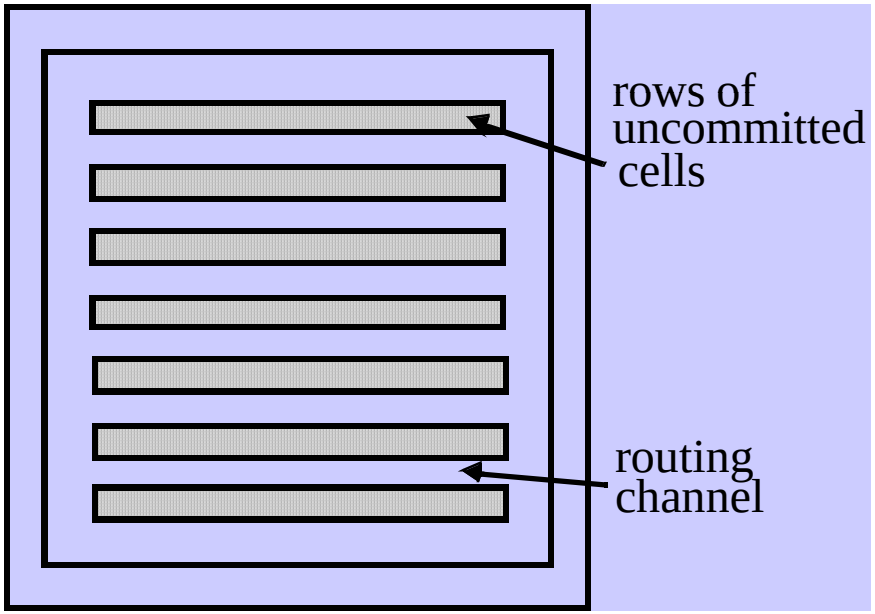


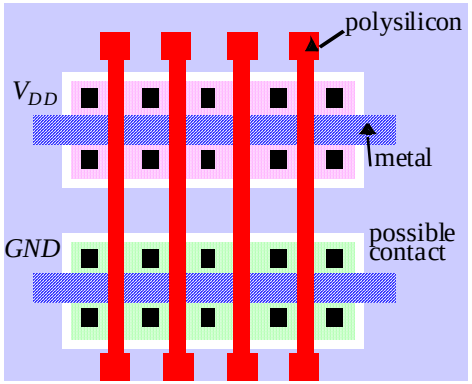
Macrocell-Based Design Example



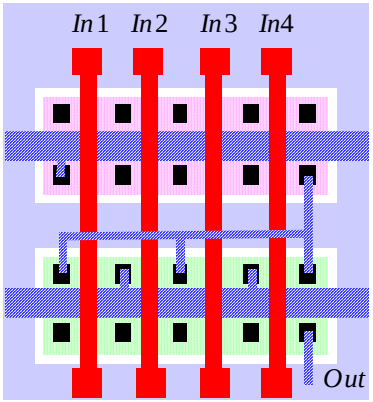
Video-encoder chip
[Brodersen92]

Gate Array — Sea-of-gates



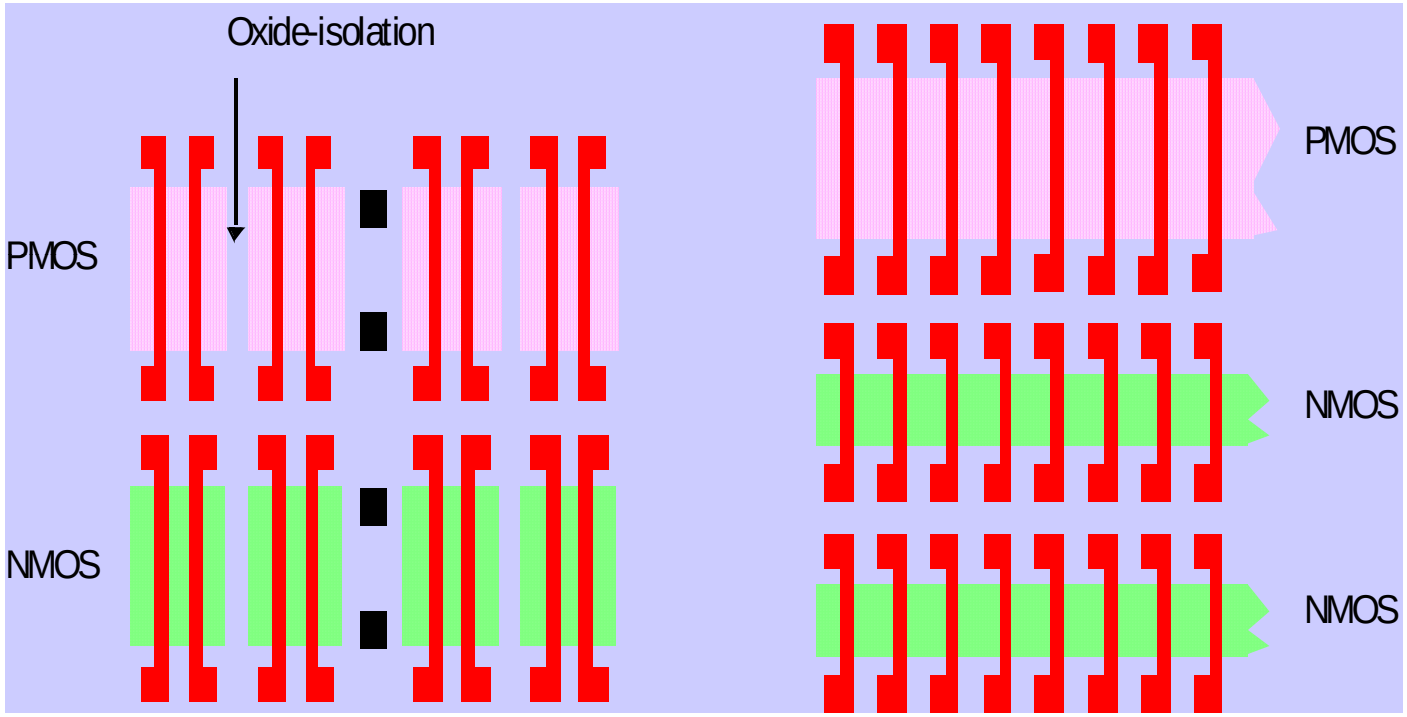


Uncommited Cell



Committed Cell (4-input NOR)

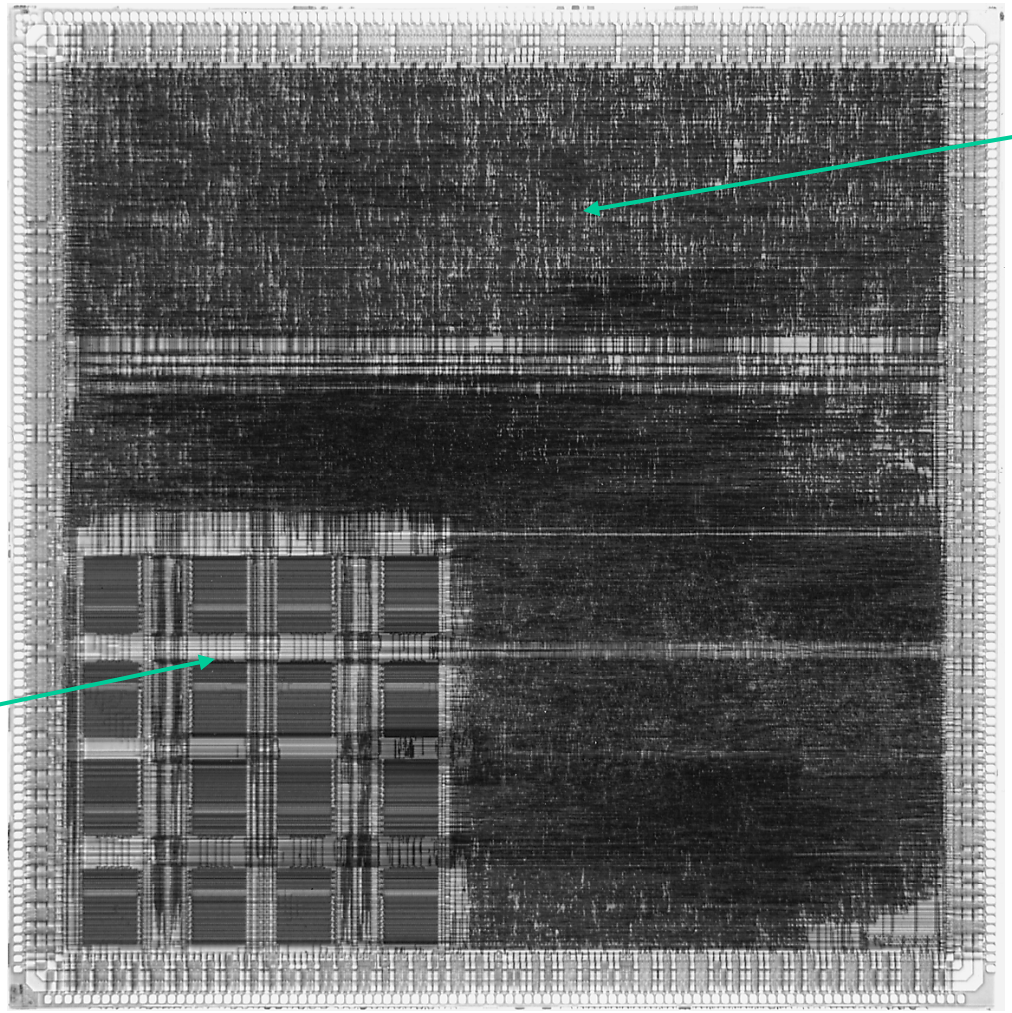
Sea-of-gate Primitive Cells



Using oxide-isolation

Using gate-isolation

Sea-of-gates



Random Logic

Memory
Subsystem

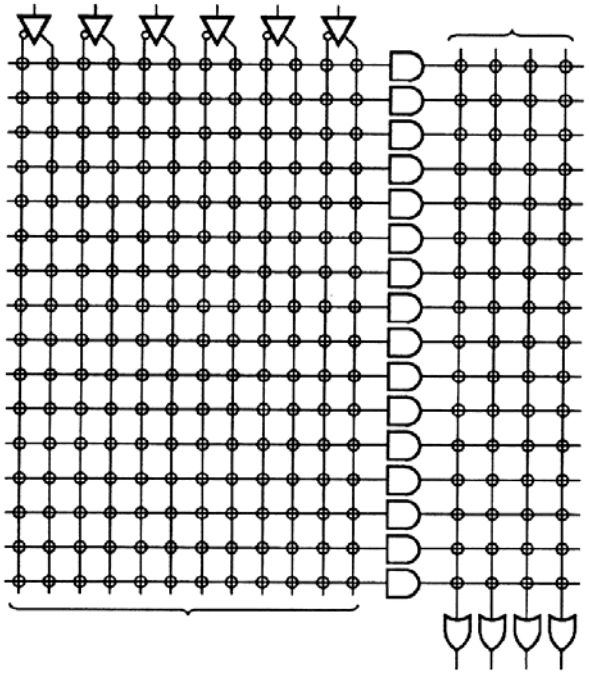
LSI Logic LEA300K
(0.6 μm CMOS)

Prewired Arrays

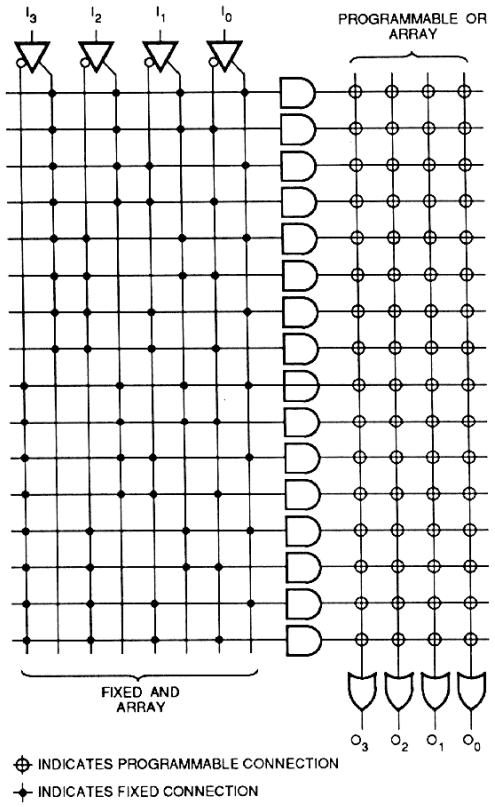
Categories of prewired arrays (or field-programmable devices):

- Fuse-based (program-once)
- Non-volatile EPROM based
- RAM based

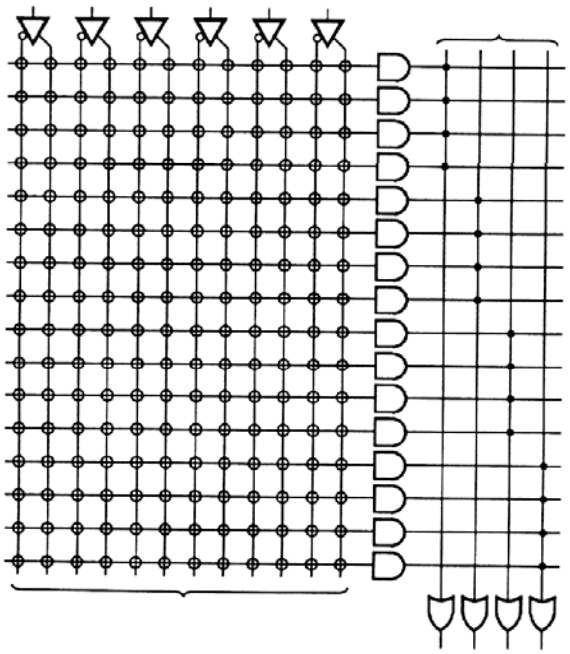
Programmable Logic Devices



PLA



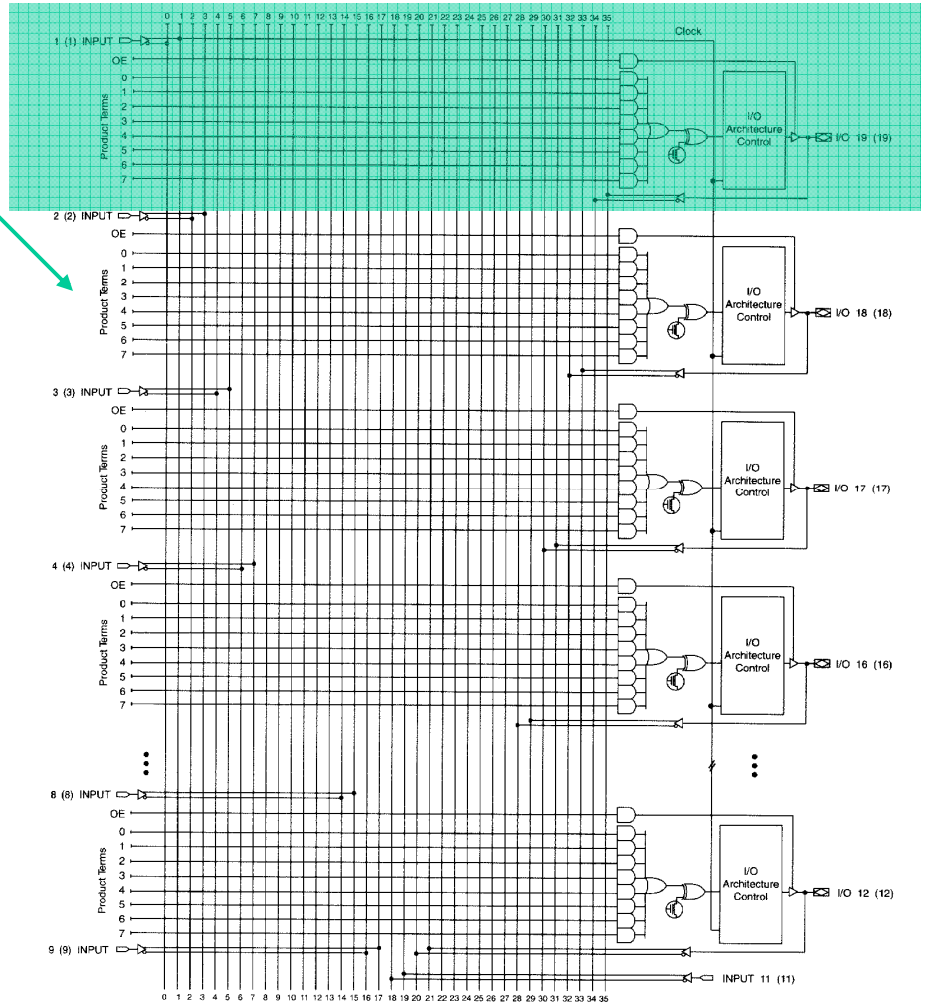
PROM



PAL

EPLD Block Diagram

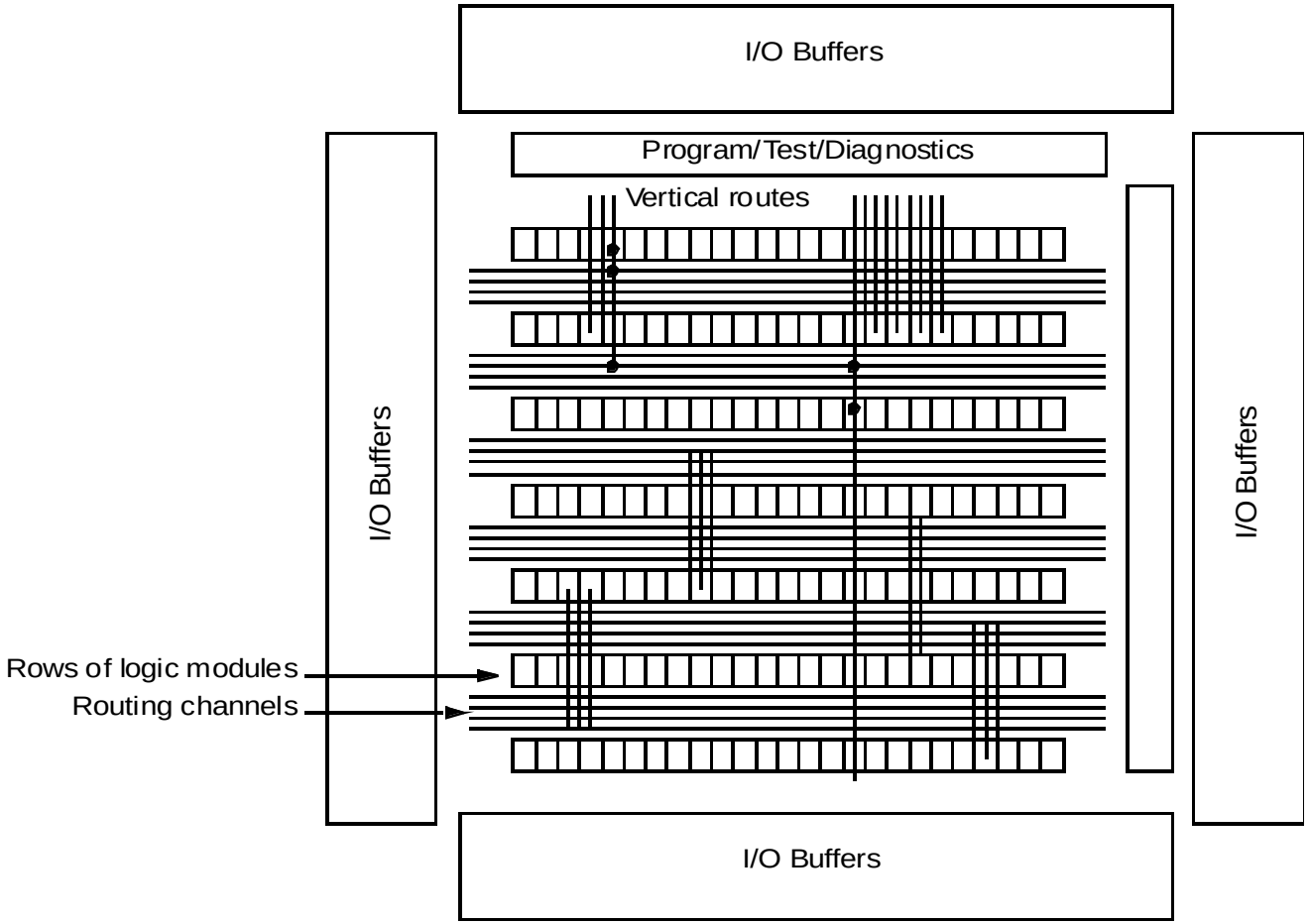
Primary inputs



Macrocell

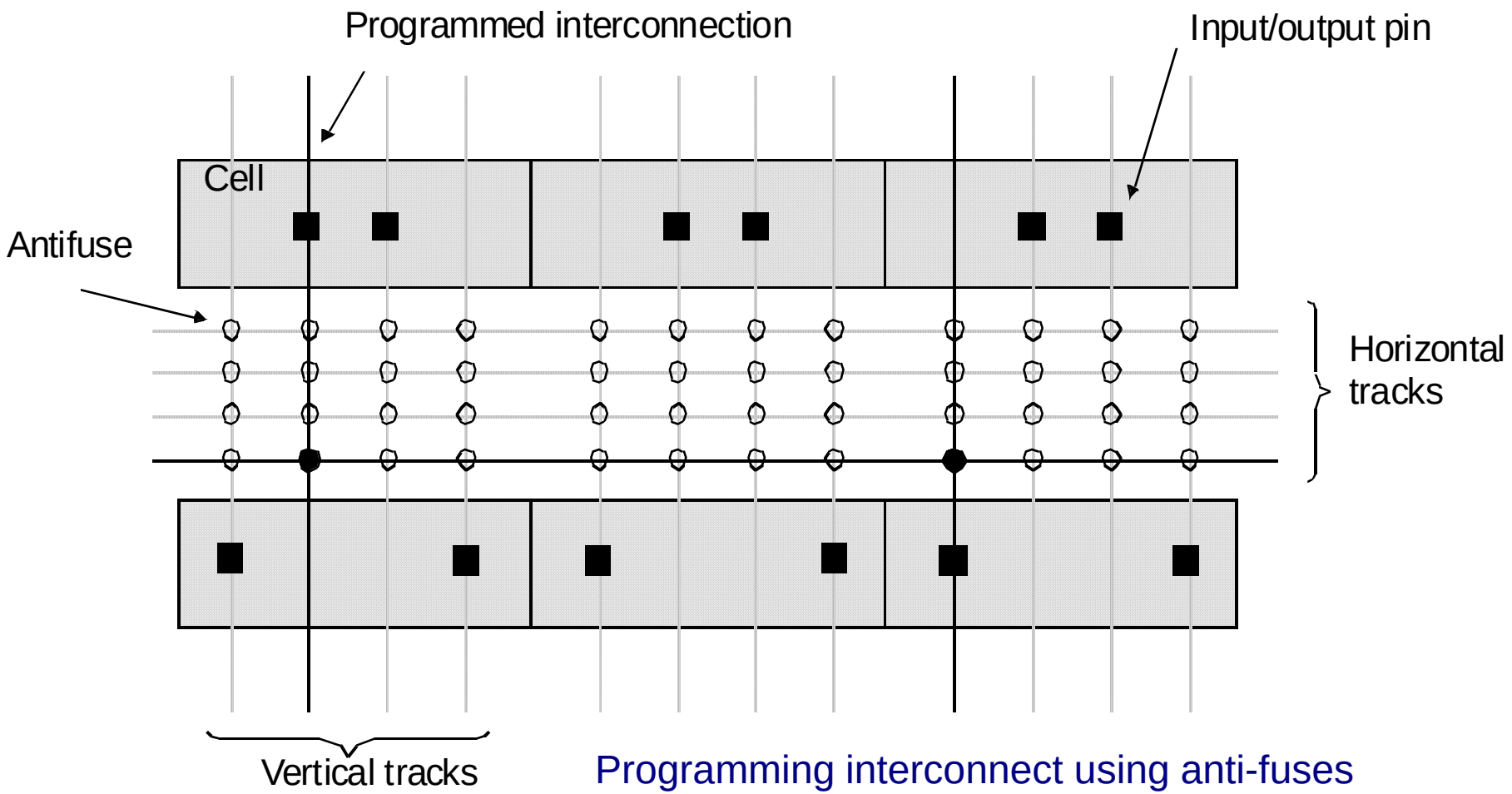
Courtesy Altera Corp.

Field-Programmable Gate Arrays
Fuse-based



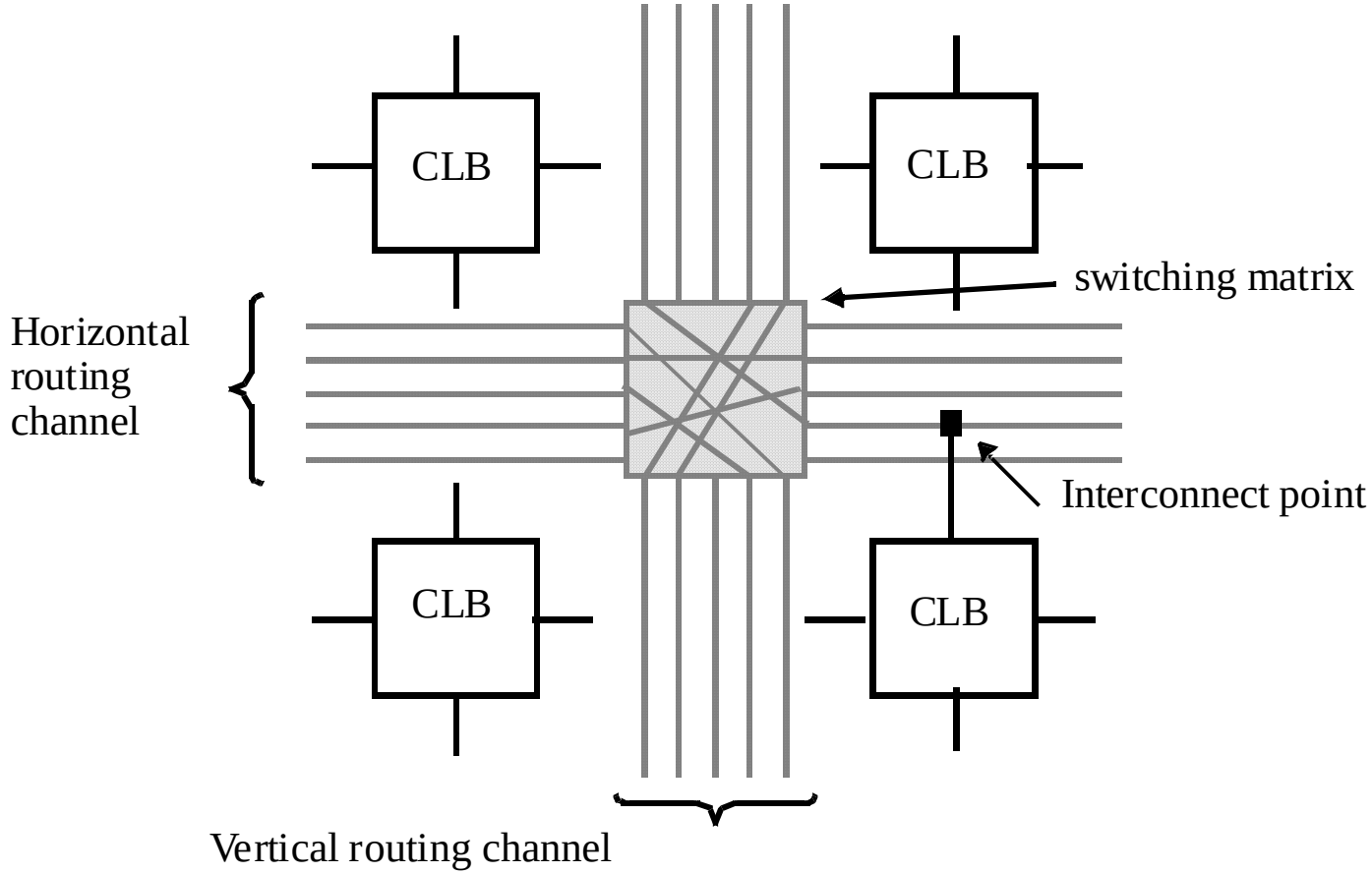
Standard-cell like floorplan

Interconnect

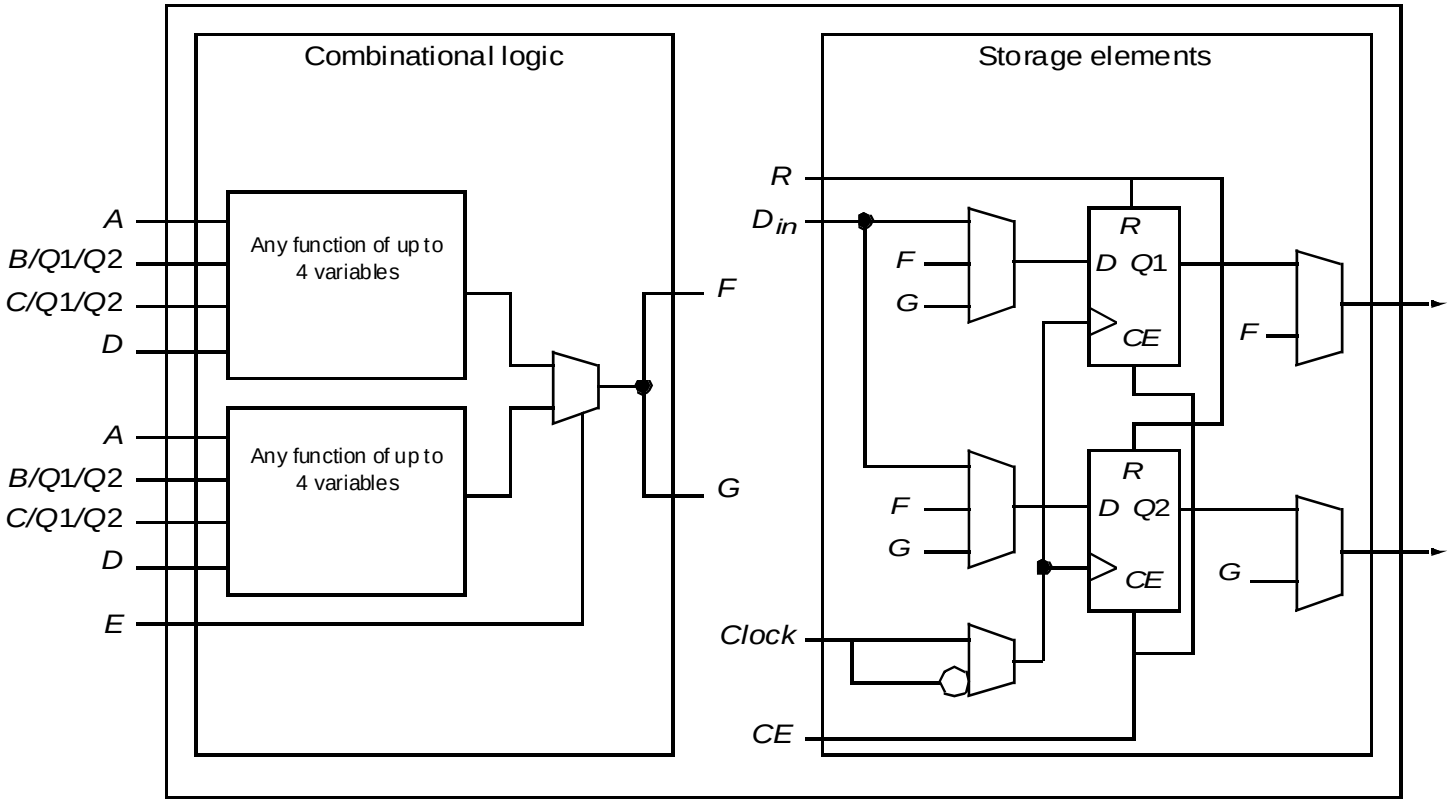


Programming interconnect using anti-fuses

Field-Programmable Gate Arrays
RAM-based

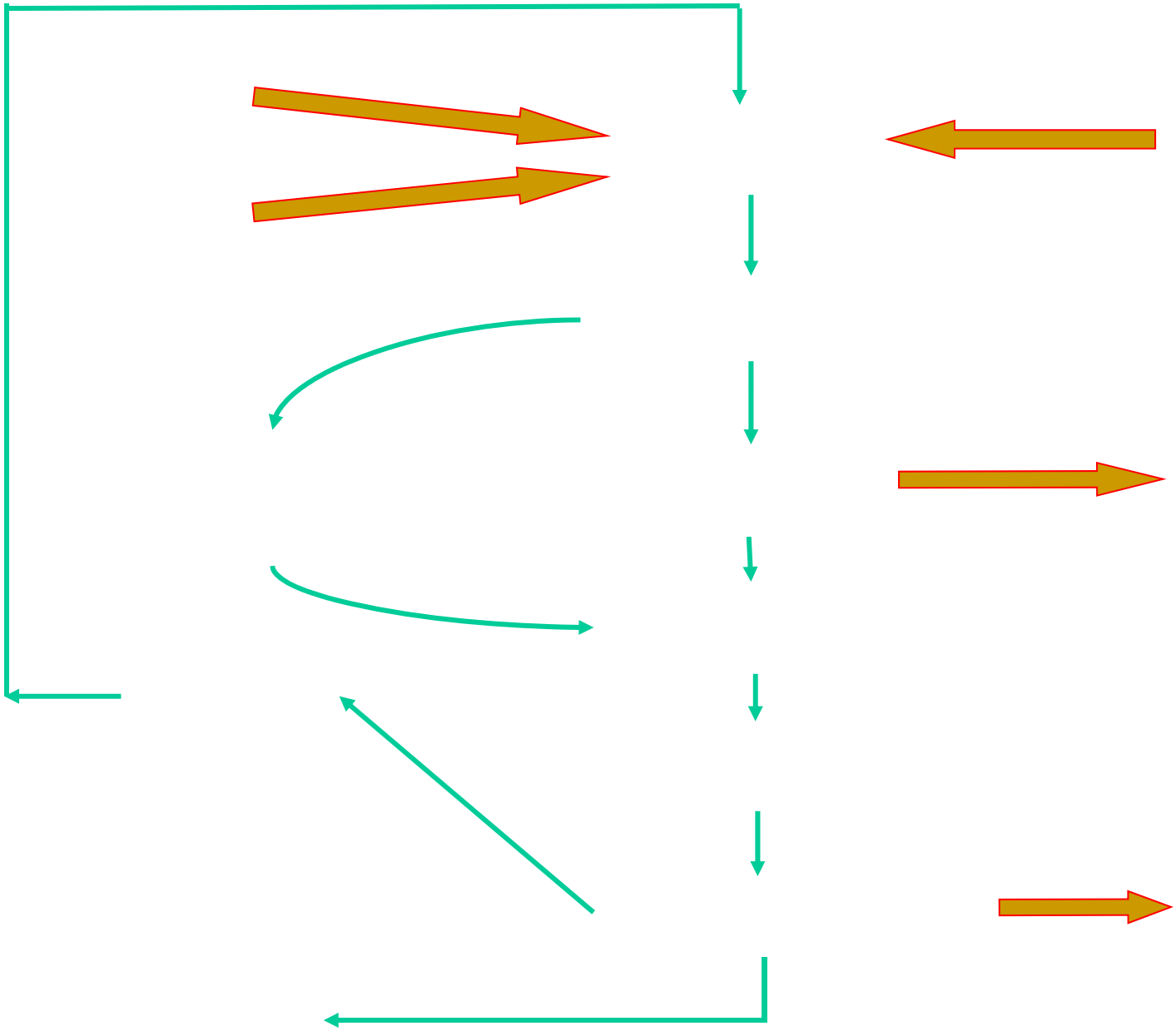


RAM-based FPGA
Basic Cell (CLB)

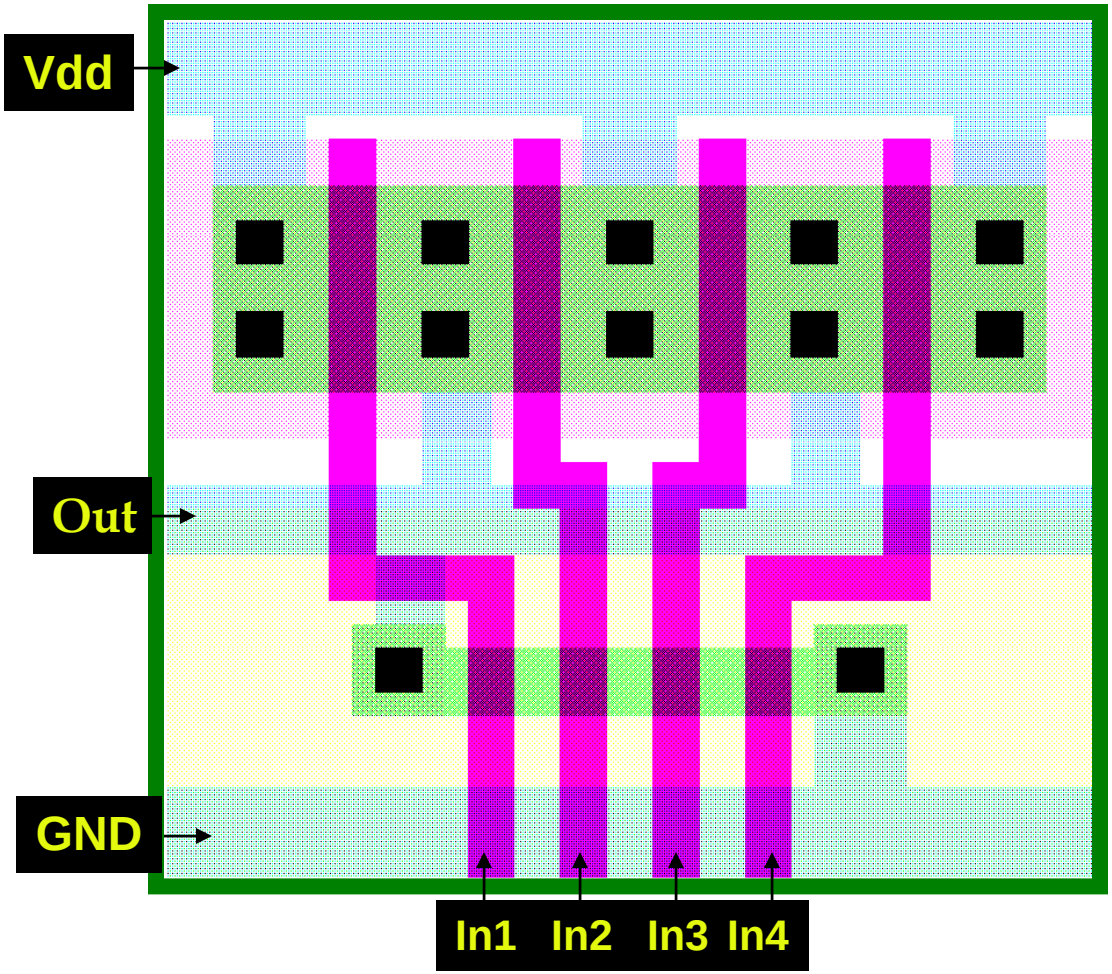


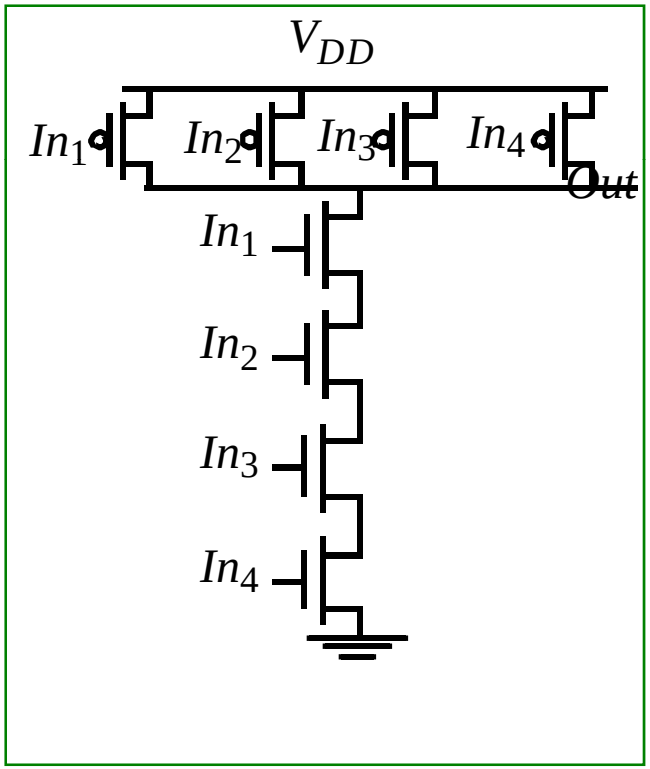
Courtesy of Xilinx

Semi-Custom Design Flow

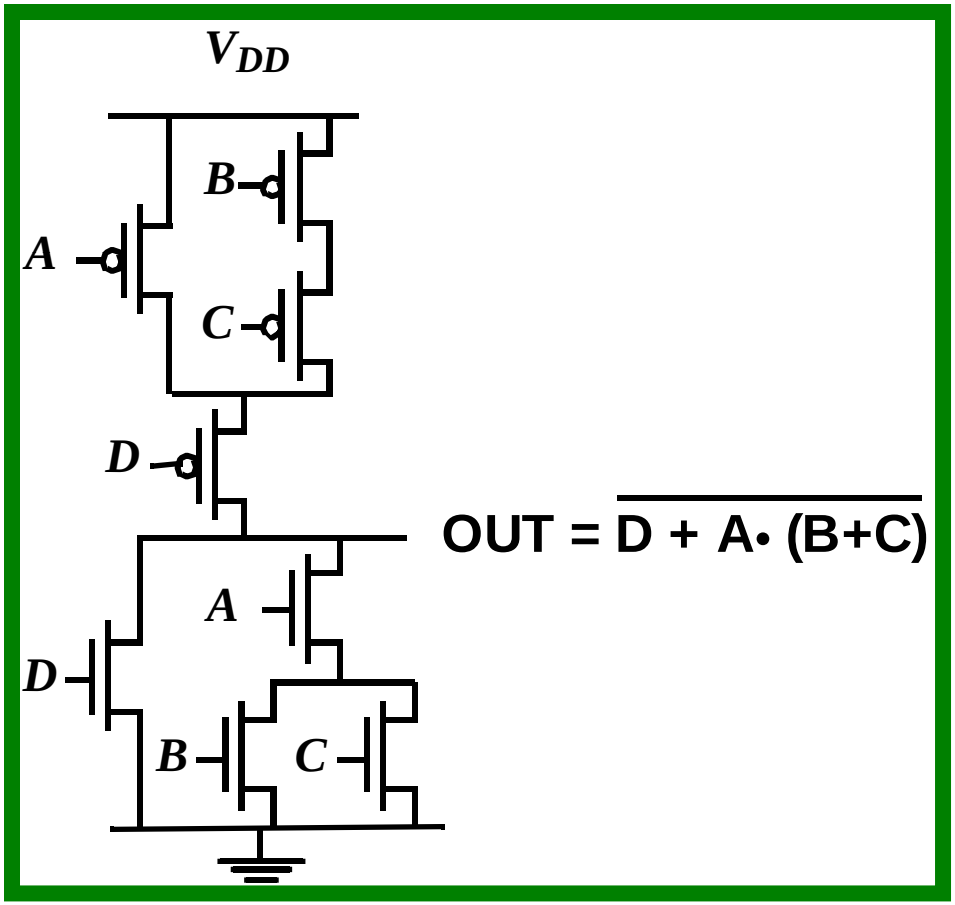


4-input NAND Gate

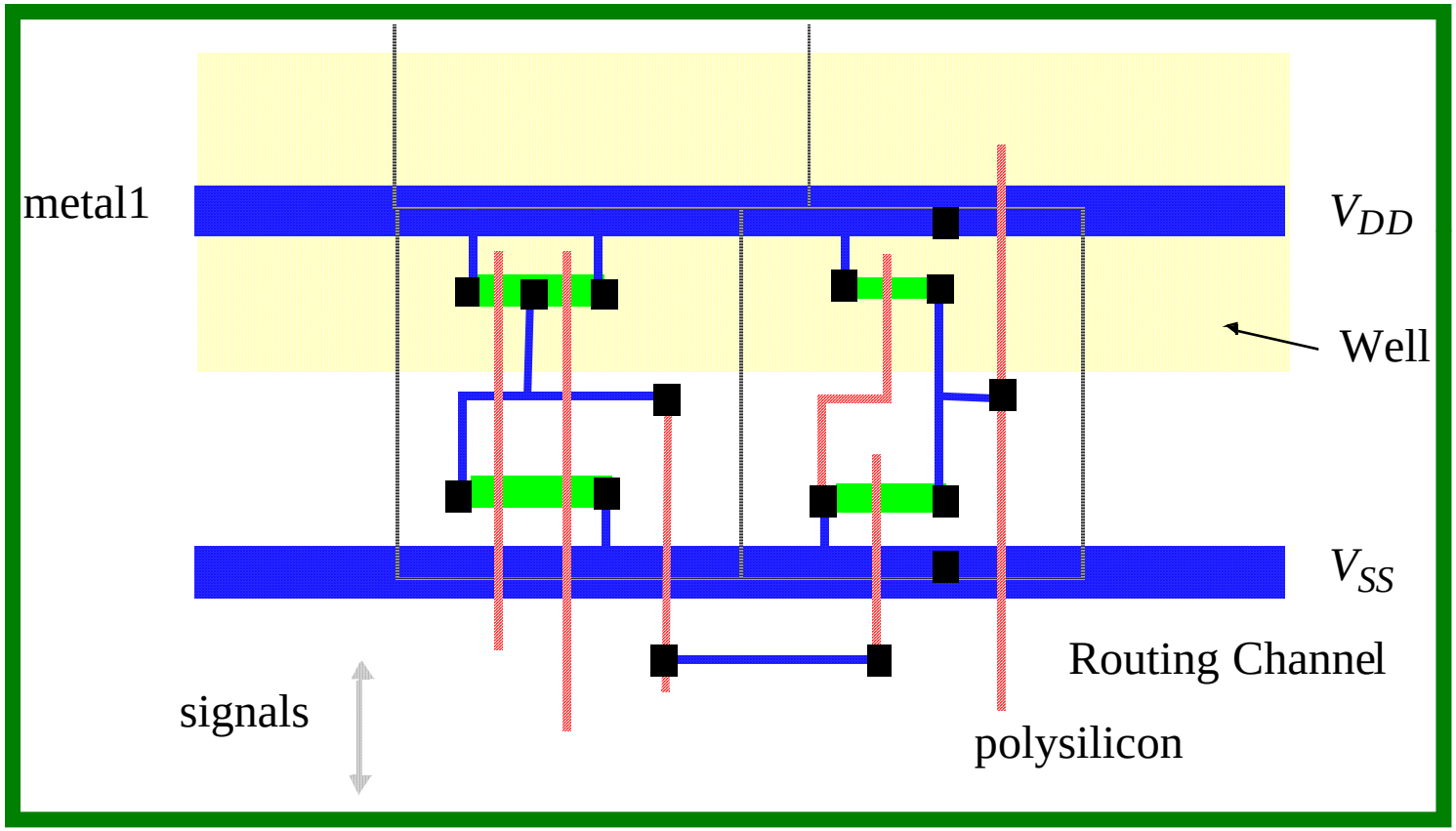




Example Gate:
COMPLEX CMOS GATE

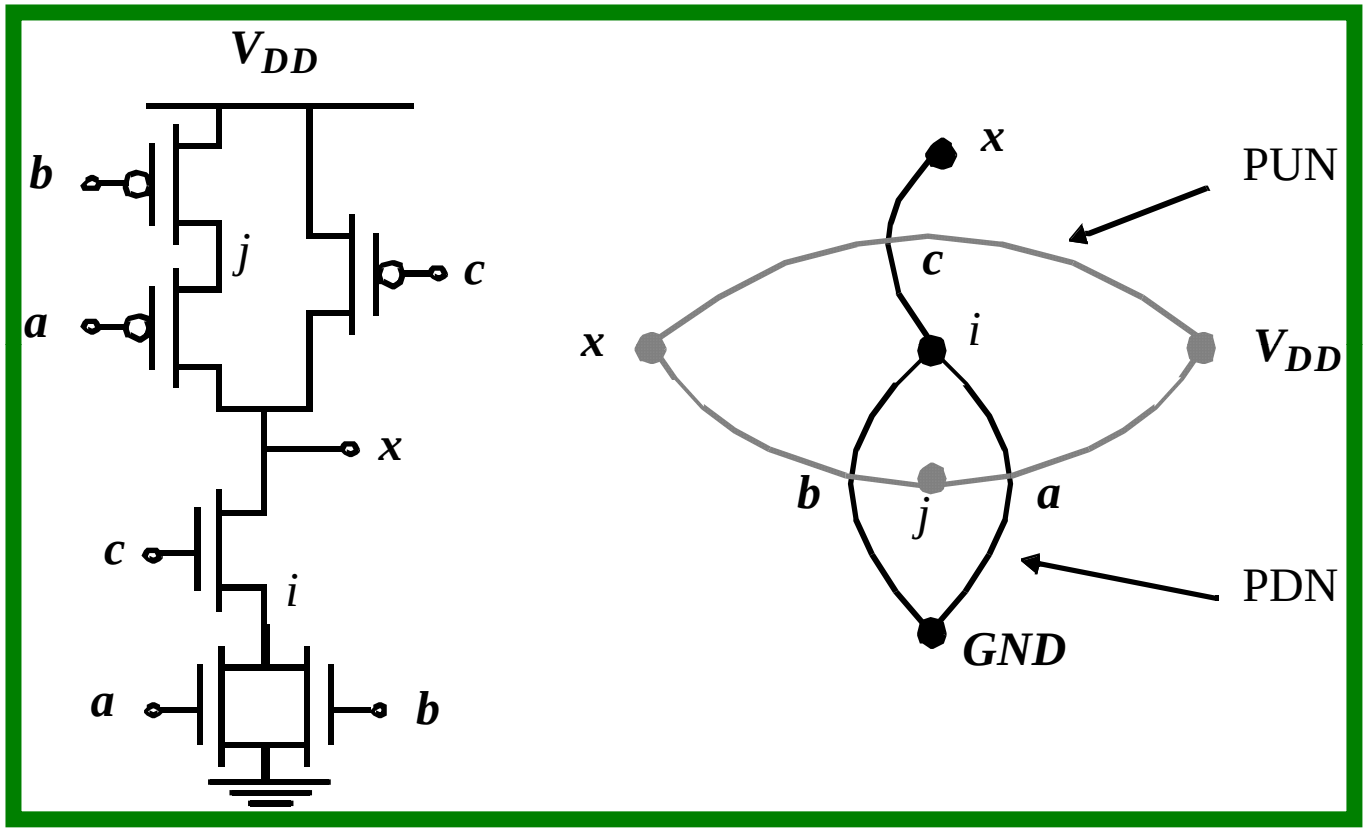


Standard Cell Layout Methodology



SERIES-PARALLEL GRAPH

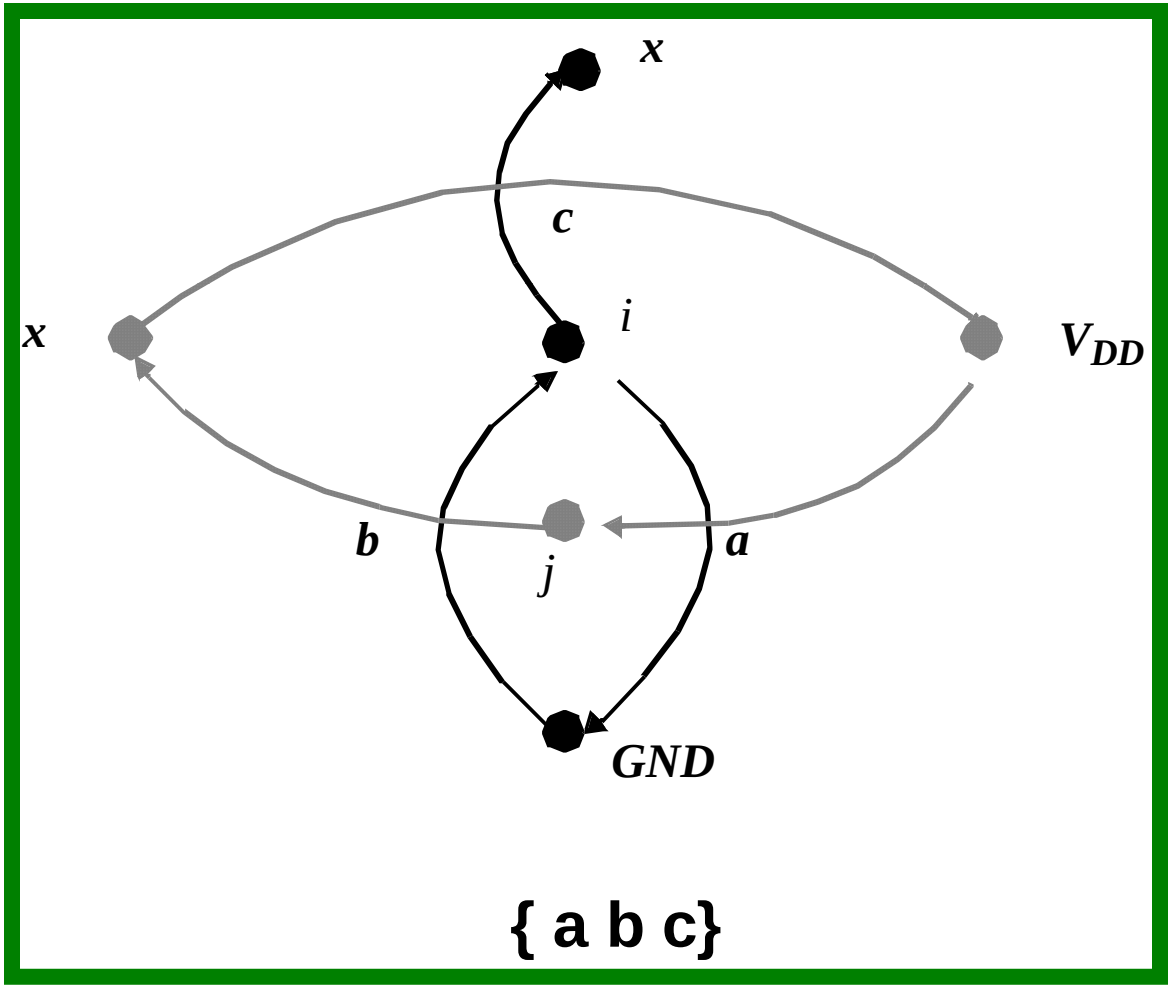
Logic Graph



X = [(A+B).C]’ = A’.B’ + C’

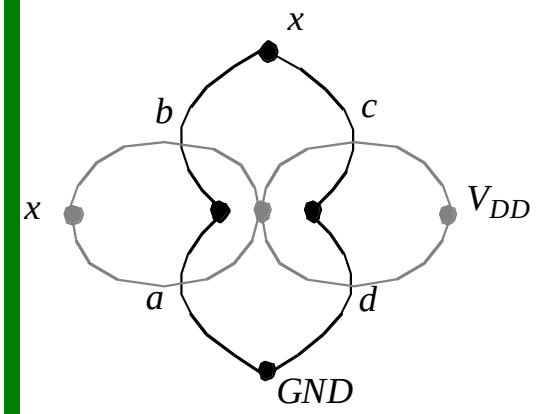
Consistent Euler Path

EULERIAN PATH THAT CREATES LINE OF DIFFUSION LAYOUT

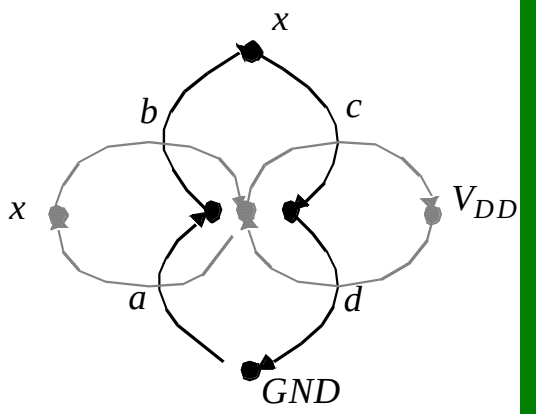


Example: x = ab+cd

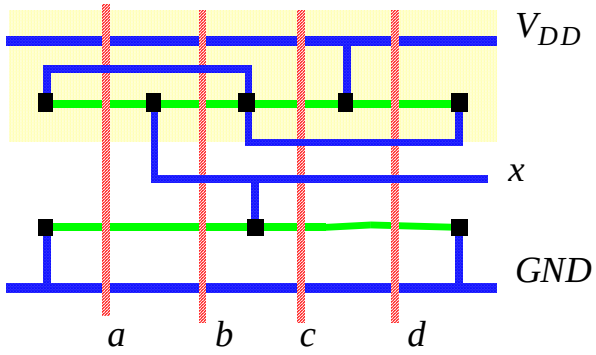
EULERIAN PATH THAT CREATES LINE OF DIFFUSION LAYOUT



(a) Logic graphs for $\overline{(ab+cd)}$



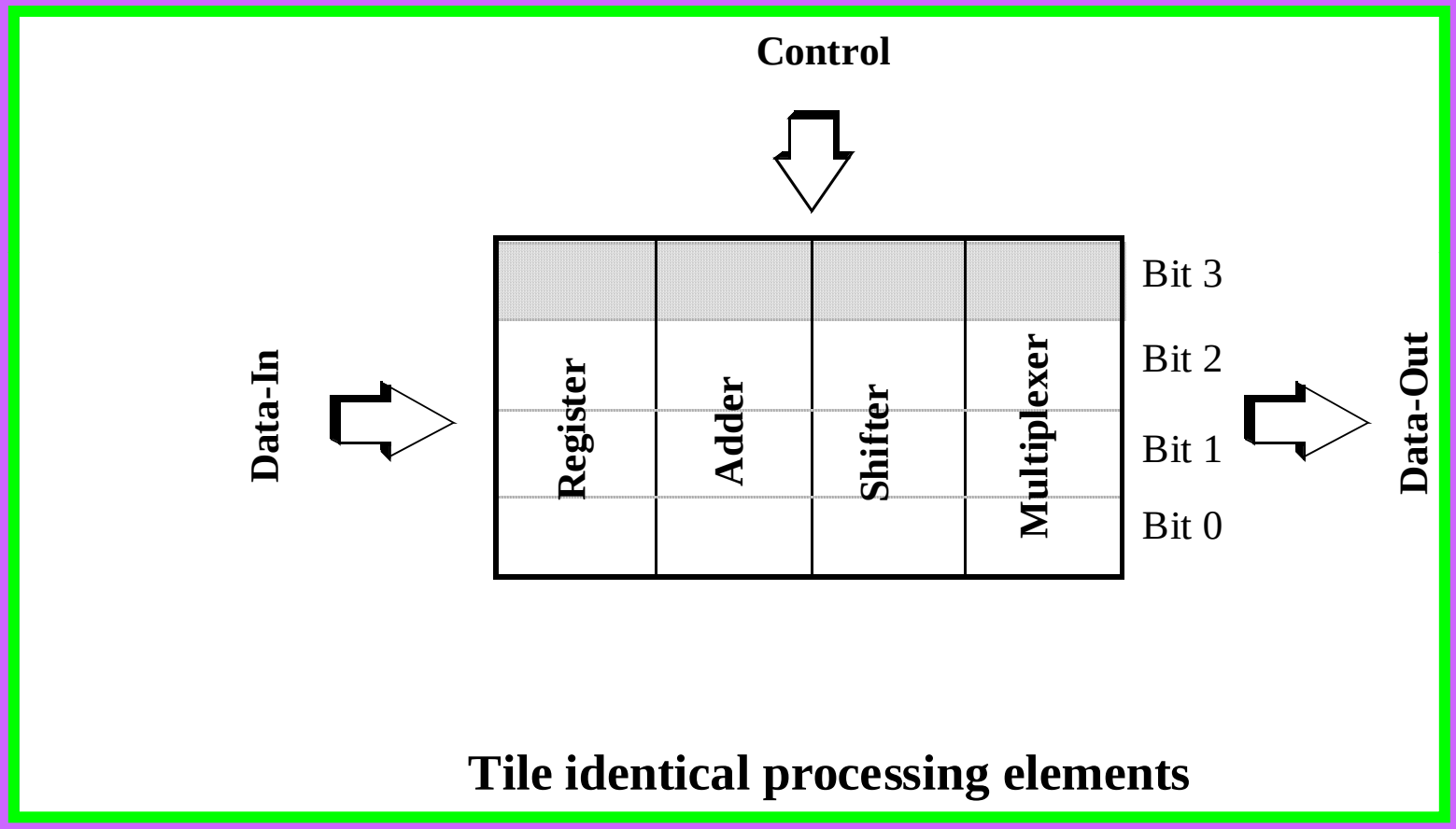
(b) Euler Paths {*a b c d*}



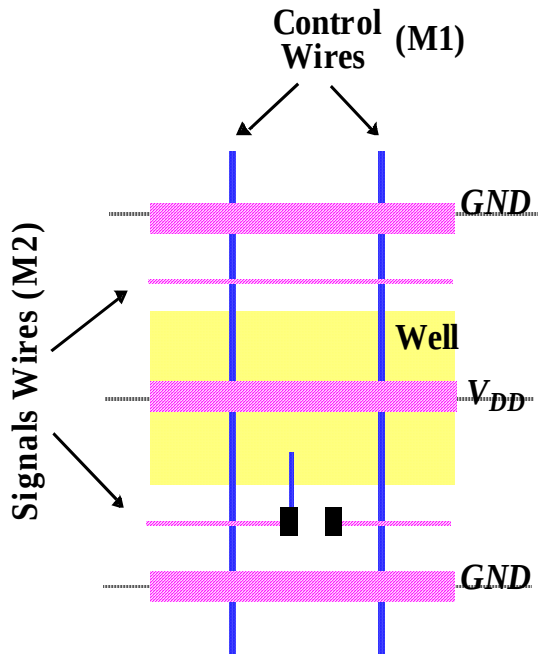
(c) stick diagram for ordering {a *b c d*}

Z = [A.B + C.D]'

Bit-Sliced Design

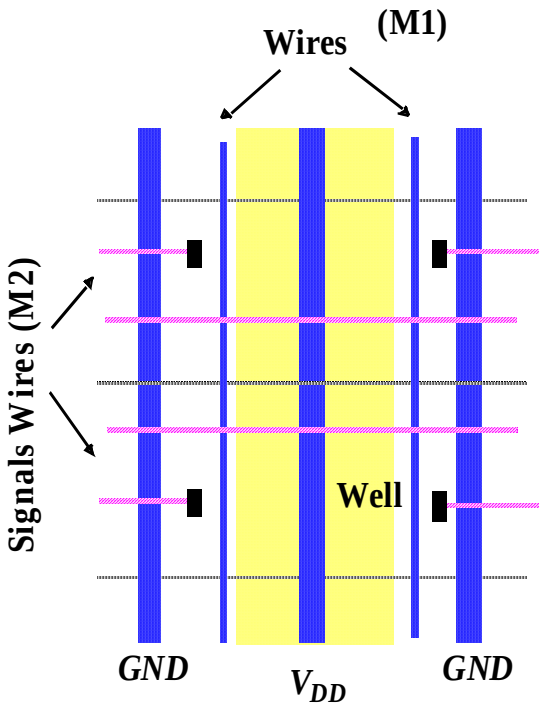


Layout Strategies for Bit-Sliced Datapaths



Approach I —

Signal and power lines parallel



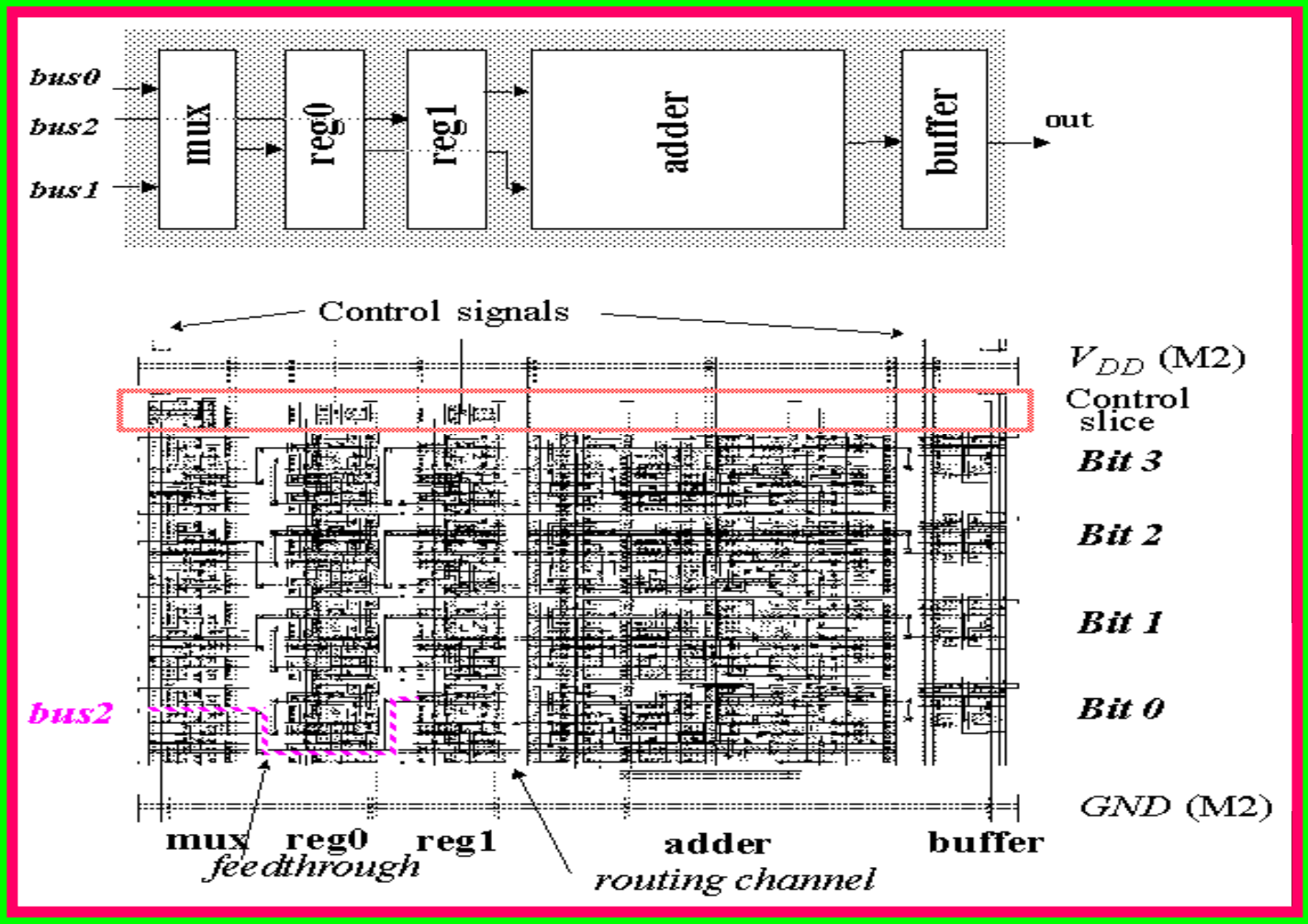
Approach II —

Signal and power lines perpendicular

In Approach 1, the wells are oriented horizontally and are shared between neighboring slices. This requires the mirroring of even and odd slices around the horizontal axis.
Vdd is also shared by slices.

Local Power and Gnd are M1 in Approach 2, while the global Power and Gnd lines may be Horizontal in M2. These lines should be dimensioned so that they can carry the peak current

Layout of Bit-sliced Datapaths

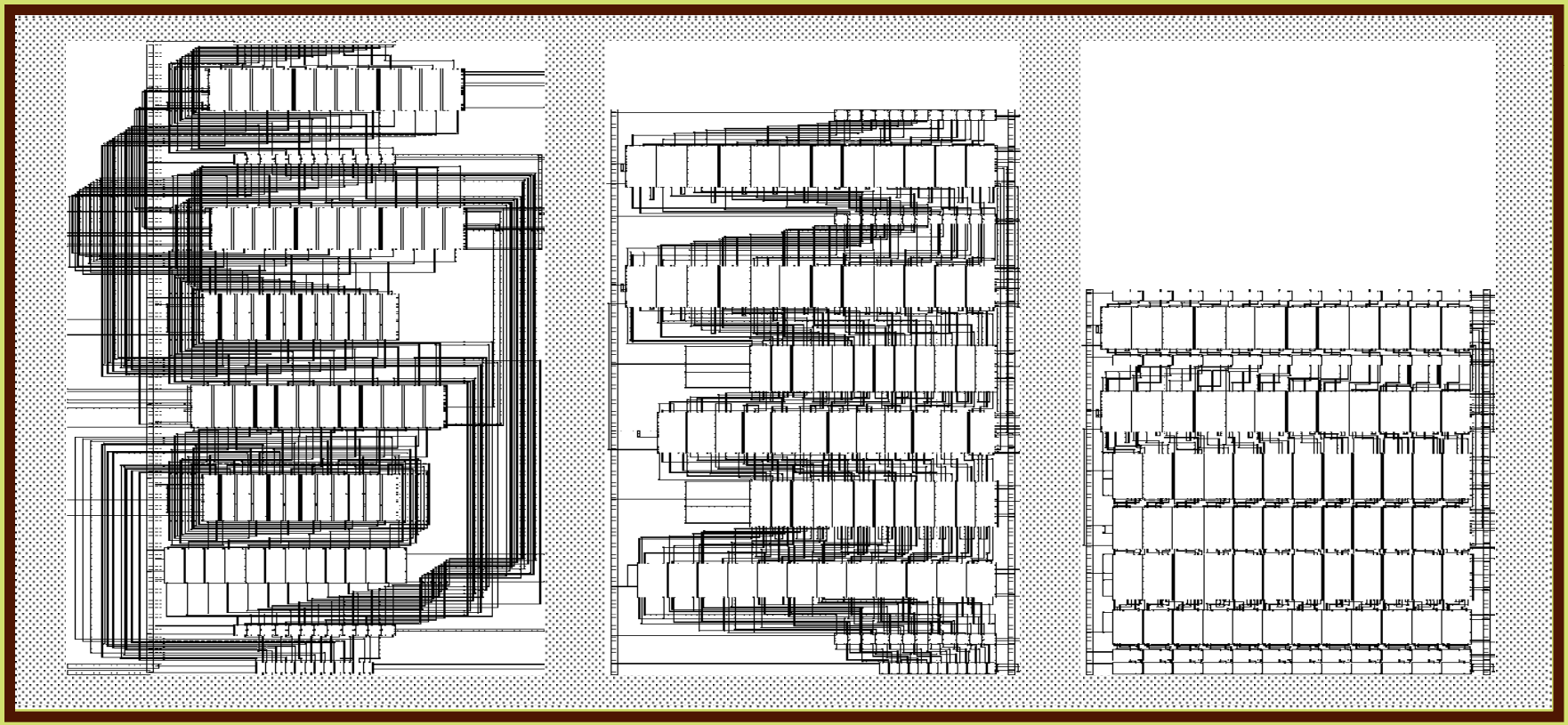


Layout of Bit-sliced Datapaths

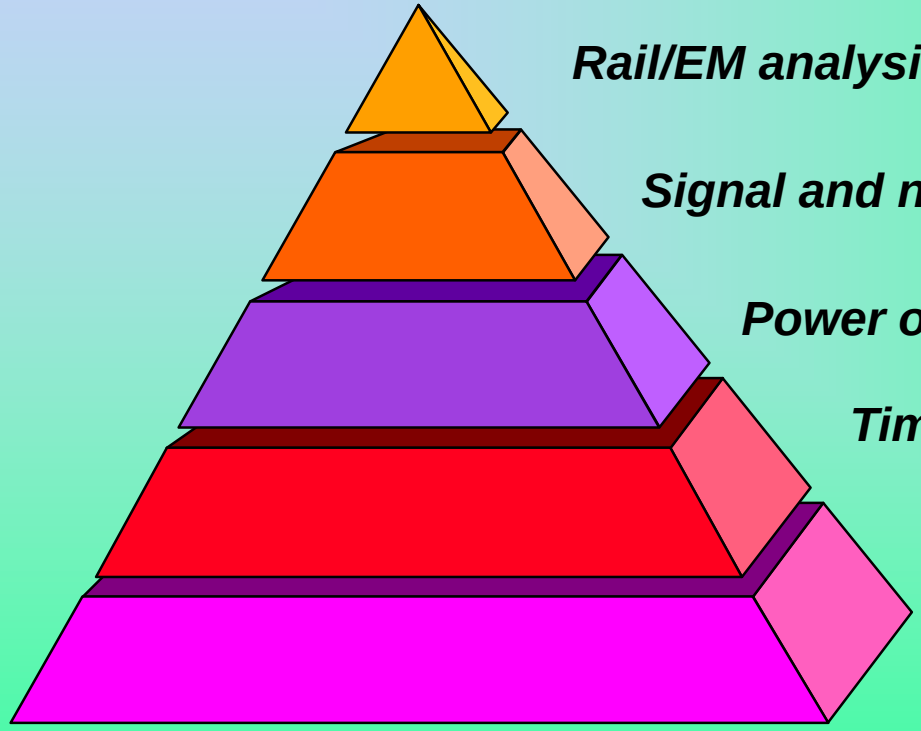
(a) Datapath without feedthroughs and without pitch matching (area = 4.2 mm^2).

(b) Adding feedthroughs (area = 3.2 mm^2)

(c) Equalizing the cell height reduces the area to 2.2 mm^2.



Vision for Design Closure



Rail/EM analysis, power grid design (*)

Signal and noise integrity

Power optimization

Timing optimization

Foundation of accurate 3-D interconnect modeling

(*) Roadmap

DSM design issues : A closer look

- **10 - 100 M Gates by year 2004**
  - **System/s on Chip**

- **High Frequency Interconnect-centric design**
  - **Performance limited by dispersion of signals**
  - **Reliability strong function of Design**

- **IP incorporation and verification**
- **Power dissipation in 10-120 watt per IC part**
- **Gigabytes of design database**
- **Informal design flows with loss of information at each abstraction**
- **Designer inexperience with DSM electrical issues and design methods**