Introduction

- VLSI realization process
- Verification and test
- Ideal and real tests
- Costs of testing
- Roles of testing
- A modern VLSI device - system-on-a-chip

Course outline

Part I: Introduction to testing
Part II: Test methods
Part III: Design for testability
VLSI Realization Process

Customer’s need

Determine requirements

Write specifications

Design synthesis and Verification

Test development

Fabrication

Manufacturing test

Chips to customer
Definitions

- **Design synthesis:** Given an I/O function, develop a procedure to manufacture a device using known materials and processes.

- **Verification:** Predictive analysis to ensure that the synthesized design, when manufactured, will perform the given I/O function.

- **Test:** A manufacturing step that ensures that the physical device, manufactured from the synthesized design, has no manufacturing defect.
Verification vs. Test

- Verifies correctness of design.
  - Performed by simulation, hardware emulation, or formal methods.
  - Performed once prior to manufacturing.
  - Responsible for quality of design.

- Verifies correctness of manufactured hardware.
  - Two-part process:
    1. Test generation: software process executed once during design
    2. Test application: electrical tests applied to hardware
  - Test application performed on every manufactured device.
  - Responsible for quality of devices.
Problems of Ideal Tests

- Ideal tests detect all defects produced in the manufacturing process.
- Ideal tests pass all functionally good devices.
- Very large numbers and varieties of possible defects need to be tested.
- Difficult to generate tests for some real defects. Defect-oriented testing is an open problem.
Real Tests

- Based on analyzable fault models, which may not map on real defects.
- Incomplete coverage of modeled faults due to high complexity.
- Some good chips are rejected. The fraction (or percentage) of such chips is called the yield loss.
- Some bad chips pass tests. The fraction (or percentage) of bad chips among all passing chips is called the defect level.
Testing as Filter Process

Good chips
Prob(good) = y
Prob(pass test) = high
Prob(fail test) = low
Mostly good chips

Fabricated chips

Defective chips
Prob(bad) = 1 - y
Prob(pass test) = low
Prob(fail test) = high
Mostly bad chips
Costs of Testing

- **Design for testability (DFT)**
  - Chip area overhead and yield reduction
  - Performance overhead

- **Software processes of test**
  - Test generation and fault simulation
  - Test programming and debugging

- **Manufacturing test**
  - Automatic test equipment (ATE) capital cost
  - Test center operational cost
Design for Testability (DFT)

DFT refers to hardware design styles or added hardware that reduces test generation complexity.

Motivation: Test generation complexity increases exponentially with the size of the circuit.

Example: Test hardware applies tests to blocks A and B and to internal bus; avoids test generation for combined A and B blocks.
Present and Future*

<table>
<thead>
<tr>
<th>Feature size (micron)</th>
<th>1997 - 2001</th>
<th>2003 - 2006</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transistors/sq. cm</td>
<td>4 - 10M</td>
<td>18 - 39M</td>
</tr>
<tr>
<td>Pin count</td>
<td>100 - 900</td>
<td>160 - 1475</td>
</tr>
<tr>
<td>Clock rate (MHz)</td>
<td>200 - 730</td>
<td>530 - 1100</td>
</tr>
<tr>
<td>Power (Watts)</td>
<td>1.2 - 61</td>
<td>2 - 96</td>
</tr>
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* SIA Roadmap, IEEE Spectrum, July 1999
Cost of Manufacturing Testing in 2000AD

- 0.5-1.0GHz, analog instruments, 1,024 digital pins: ATE purchase price
  \[= \$1.2M + 1,024 \times \$3,000 = \$4.272M\]

- Running cost (five-year linear depreciation)
  \[= \text{Depreciation} + \text{Maintenance} + \text{Operation}\]
  \[= \$0.854M + \$0.085M + \$0.5M\]
  \[= \$1.439M/\text{year}\]

- Test cost (24 hour ATE operation)
  \[= \$1.439M/(365 \times 24 \times 3,600)\]
  \[= 4.5 \text{ cents/second}\]
Roles of Testing

- Detection: Determination whether or not the device under test (DUT) has some fault.
- Diagnosis: Identification of a specific fault that is present on DUT.
- Device characterization: Determination and correction of errors in design and/or test procedure.
- Failure mode analysis (FMA): Determination of manufacturing process errors that may have caused defects on the DUT.
A Modern VLSI Device System-on-a-chip (SOC)

![Diagram showing the components of a modern VLSI device: DSP core, RAM ROM, interface logic, mixed-signal Codec, data terminal, transmission medium.]

Figure 18.5 (page 605)
Course Outline

Part I: Introduction

- Basic concepts and definitions (Chapter 1)
- Test process and ATE (Chapter 2)
- Test economics and product quality (Chapter 3)
- Fault modeling (Chapter 4)
Course Outline (Cont.)
Part II: Test Methods

- Logic and fault simulation (Chapter 5)
- Testability measures (Chapter 6)
- Combinational circuit ATPG (Chapter 7)
- Sequential circuit ATPG (Chapter 8)
- Memory test (Chapter 9)
- Analog test (Chapters 10 and 11)
- Delay test and IDDQ test (Chapters 12 and 13)
Course Outline (Cont.)
Part III: DFT

- Scan design (Chapter 14)
- BIST (Chapter 15)
- Boundary scan and analog test bus (Chapters 16 and 17)
- System test and core-based design (Chapter 18)
VLSI Testing Process and Equipment

- Motivation
- Types of Testing
- Test Specifications and Plan
- Test Programming
- Test Data Analysis
- Automatic Test Equipment
- Parametric Testing
- Summary
Motivation

- Need to understand some Automatic Test Equipment (ATE) technology
  - Influences what tests are possible
  - Serious analog measurement limitations at high digital frequency or in the analog domain
  - Need to understand capabilities for digital logic, memory, and analog test in System-on-a-Chip (SOC) technology

- Need to understand parametric testing
  - Used to take setup, hold time measurements
  - Use to compute $V_{IL}, V_{IH}, V_{OL}, V_{OH}, t_r, t_f, t_d, I_{OL}, I_{OH}, I_{IL}, I_{IH}$
Types of Testing

- Verification testing, characterization testing, or design debug
  Verifies correctness of design and of test procedure – usually requires correction to design
- Manufacturing testing
  Factory testing of all manufactured chips for parametric faults and for random defects
- Acceptance testing (incoming inspection)
  User (customer) tests purchased parts to ensure quality
Testing Principle

INPUT PATTERNS
---11
---00
-----
-----
---01

DIGITAL CIRCUIT

STORED CORRECT RESPONSE

COMPARATOR

OUTPUT RESPONSES
10---
00---
-----
-----
01---

TEST RESULT
Automatic Test Equipment Components

- Consists of:
  - Powerful computer
  - Powerful 32-bit Digital Signal Processor (DSP) for analog testing
  - Test Program (written in high-level language) running on the computer
  - Probe Head (actually touches the bare or packaged chip to perform fault detection experiments)
  - Probe Card or Membrane Probe (contains electronics to measure signals on chip pin or pad)
Verification Testing

- Ferociously expensive
- May comprise:
  - Scanning Electron Microscope tests
  - Bright-Lite detection of defects
  - Electron beam testing
  - Artificial intelligence (expert system) methods
  - Repeated functional tests
Characterization Test

- **Worst-case test**
  - Choose test that passes/fails chips
  - Select statistically significant sample of chips
  - Repeat test for every combination of 2+ environmental variables
  - Plot results in Schmoo plot
  - Diagnose and correct design errors

- **Continue throughout production life of chips to improve design and process to increase yield**
Schmoo Plot

* Acceptable Reading Combination
@ Unacceptable Reading Combination
Manufacturing Test

- Determines whether manufactured chip meets specs
- Must cover high % of modeled faults
- Must minimize test time (to control cost)
- No fault diagnosis
- Tests every device on chip
- Test at speed of application or speed guaranteed by supplier
Burn-in or Stress Test

- **Process:**
  Subject chips to high temperature & over-voltage supply, while running production tests

- **Catches:**
  Infant mortality cases – these are damaged chips that will fail in the first 2 days of operation – causes bad devices to actually fail before chips are shipped to customers
  Freak failures – devices having same failure mechanisms as reliable devices
Incoming Inspection

- Can be:
  - Similar to production testing
  - More comprehensive than production testing
  - Tuned to specific systems application

- Often done for a random sample of devices
  - Sample size depends on device quality and system reliability requirements
  - Avoids putting defective device in a system where cost of diagnosis exceeds incoming inspection cost
Types of Manufacturing Tests

- **Wafer sort or probe test** – done before wafer is scribed and cut into chips
  - Includes test site characterization – specific test devices are checked with specific patterns to measure:
    - Gate threshold
    - Polysilicon field threshold
    - Poly sheet resistance, etc.
- **Packaged device tests**
Sub-types of Tests

- **Parametric** – measures electrical properties of pin electronics – delay, voltages, currents, etc. – fast and cheap

- **Functional** – used to cover very high % of modeled faults – test every transistor and wire in digital circuits – long and expensive – main topic of tutorial
Two Different Meanings of Functional Test

- ATE and Manufacturing World – any vectors applied to cover high % of faults during manufacturing test
- Automatic Test-Pattern Generation World – testing with verification vectors, which determine whether hardware matches its specification – typically have low fault coverage (< 70 %)
Test Specifications & Plan

- **Test Specifications:**
  - Functional Characteristics
  - Type of Device Under Test (DUT)
  - Physical Constraints – Package, pin numbers, etc.
  - Environmental Characteristics – supply, temperature, humidity, etc.
  - Reliability – acceptance quality level (defects/million), failure rate, etc.

- **Test plan generated from specifications**
  - Type of test equipment to use
  - Types of tests
  - Fault coverage requirement
Test Programming

- **DEVICE SPECIFICATIONS**
  - **TEST PLAN**
  - **VECTOR EDITOR**
  - **TEST PROGRAM GENERATOR**
  - **ARCHITECTURAL & LOGIC DESIGN, VERIFICATION & TEST GENERATION**

- **TEST PROGRAM**
  - Tester data, Types of tests, timing specs., etc.
  - Vectors
  - Pin assignment, Wafer map, etc.
Test Data Analysis

- Uses of ATE test data:
  - Reject bad DUTS
  - Fabrication process information
  - Design weakness information
- Devices that did not fail are good only if tests covered 100% of faults
- Failure mode analysis (FMA)
  - Diagnose reasons for device failure, and find design and process weaknesses
  - Allows improvement of logic & layout design rules
Automatic Test Equipment (ATE)
T6682 ATE Specifications

- Uses 0.35 \( \mu \)m VLSI chips in implementation
- 1024 pin channels
- Speed: 250, 500, or 1000 MHz
- Timing accuracy: +/- 200 ps
- Drive voltage: -2.5 to 6 V
- Clock/strobe accuracy: +/- 870 ps
- Clock settling resolution: 31.25 ps
- Pattern multiplexing: write 2 patterns in one ATE cycle
- Pin multiplexing: use 2 pins to control 1 DUT pin
Pattern Generation

- **Sequential pattern generator (SQPG):** stores 16 Mvectors of patterns to apply to DUT, vector width determined by # DUT pins

- **Algorithmic pattern generator (ALPG):** 32 independent address bits, 36 data bits
  - For memory test – has address descrambler
  - Has address failure memory

- **Scan pattern generator (SCPG):** supports JTAG boundary scan, greatly reduces test vector memory for full-scan testing
  - 2 Gvector or 8 Gvector sizes
Response Checking and Frame Processor

- Response Checking:
  - Pulse train matching – ATE matches patterns on 1 pin for up to 16 cycles
  - Pattern matching mode – matches pattern on a number of pins in 1 cycle
  - Determines whether DUT output is correct, changes patterns in real time

- Frame Processor – combines DUT input stimulus from pattern generators with DUT output waveform comparison

- Strobe time – interval after pattern application when outputs sampled
Probing

- Pin electronics (PE) – electrical buffering circuits, put as close as possible to DUT
- Uses pogo pin connector at test head
- Test head interface through custom printed circuit board to wafer prober (unpackaged chip test) or package handler (packaged chip test), touches chips through a socket (contactor)
- Uses liquid cooling
- Can independently set $V_{IH}$, $V_{IL}$, $V_{OH}$, $V_{OL}$, $I_H$, $I_L$, $V_T$ for each pin
- Parametric Measurement Unit (PMU)
Probe Card and Probe Needles or Membrane

- **Probe card** – custom printed circuit board (PCB) on which DUT is mounted in socket – may contain custom measurement hardware (current test)

- **Probe needles** – come down and scratch the pads to stimulate/read pins

- **Membrane probe** – for unpackaged wafers – contacts printed on flexible membrane, pulled down onto wafer with compressed air to get wiping action
T6682 ATE Software

- Runs Solaris UNIX on UltraSPARC 167 MHz CPU for non-real time functions
- Runs real-time OS on UltraSPARC 200 MHz CPU for tester control
- Peripherals: disk, CD-ROM, micro-floppy, monitor, keyboard, HP GPIB, Ethernet
- Viewpoint software provided to debug, evaluate, & analyze VLSI chips
Specifications

- Intended for SOC test – digital, analog, and memory test – supports scan-based test
- Modular – can be upgraded with additional instruments as test requirements change
- enVision Operating System
- 1 or 2 test heads per tester, maximum of 1024 digital pins, 1 GHz maximum test rate
- Maximum 64 Mvectors memory storage
- Analog instruments: DSP-based synthesizers, digitizers, time measurement, power test, Radio Frequency (RF) source and measurement capability (4.3 GHz)
Multi-site Testing – Major Cost Reduction

- One ATE tests several (usually identical) devices at the same time
- For both probe and package test
- DUT interface board has > 1 sockets
- Add more instruments to ATE to handle multiple devices simultaneously
- Usually test 2 or 4 DUTS at a time, usually test 32 or 64 memory chips at a time
- Limits: # instruments available in ATE, type of handling equipment available for package
Electrical Parametric Testing
Typical Test Program

1. **Probe test (wafer sort)** – catches gross defects
2. **Contact electrical test**
3. **Functional & layout-related test**
4. **DC parametric test**
5. **AC parametric test**
   - Unacceptable voltage/current/delay at pin
   - Unacceptable device operation limits
DC Parametric Tests
Contact Test

1. Set all inputs to 0 V
2. Force current $I_{fb}$ out of pin (expect $I_{fb}$ to be 100 to 250 $\mu$A)
3. Measure pin voltage $V_{pin}$. Calculate pin resistance $R$
   - Contact short ($R = 0 \ \Omega$)
   - No problem
   - Pin open circuited ($R$ huge), $I_{fb}$ and $V_{pin}$ large
Power Consumption Test

1. Set temperature to worst case, open circuit DUT outputs

2. Measure maximum device current drawn from supply $I_{CC}$ at specified voltage
   - $I_{CC} > 70$ mA (fails)
   - $40$ mA < $I_{CC}$ ≤ 70 mA (ok)
Output Short Current Test

1. Make chip output a 1
2. Short output pin to 0 V in PMU
3. Measure short current (but not for long, or the pin driver burns out)

   Short current > 40 \( \mu \text{A} \) (ok)
   Short current \( \leq 40 \mu \text{A} \) (fails)
Output Drive Current Test

1. Apply vector forcing pin to 0
2. Simultaneously force $V_{OL}$ voltage and measure $I_{OL}$
3. Repeat Step 2 for logic 1

$I_{OL} < 2.1$ mA (fails)
$I_{OH} < -1$ mA (fails)
Threshold Test

1. For each I/P pin, write logic 0 followed by propagation pattern to output. Read output. Increase input voltage in 0.1 V steps until output value is wrong

2. Repeat process, but stepping down from logic 1 by 0.1 V until output value fails
   - Wrong output when $0 \text{ input} > 0.8 \text{ V}$ (ok)
   - Wrong output when $0 \text{ input} \leq 0.8 \text{ V}$ (fails)
   - Wrong output when $1 \text{ input} < 2.0 \text{ V}$ (ok)
   - Wrong output when $1 \text{ input} \geq 2.0 \text{ V}$ (fails)
AC Parametric Tests
Rise/fall Time Tests

![Diagram showing voltage changing over time with fall and rise times marked]
Set-up and Hold Time Tests

![Diagram showing set-up and hold time tests with voltage, input waveform, and clock waveform.](image)
Propagation Delay Tests

1. Apply standard output pin load (RC or RL)
2. Apply input pulse with specific rise/fall
3. Measure propagation delay from input to output
   - Delay between 5 ns and 40 ns (ok)
   - Delay outside range (fails)
Summary

- **Parametric tests** – determine whether pin electronics system meets digital logic voltage, current, and delay time specs
- **Functional tests** – determine whether internal logic/analog sub-systems behave correctly
- **ATE Cost Problems**
  - Pin inductance (expensive probing)
  - Multi-GHz frequencies
  - High pin count (1024)
- **ATE Cost Reduction**
  - Multi-Site Testing
  - DFT methods like Built-In Self-Test