

## List of Projects

### Behavioral Testing

1. Design an 8-bit microprocessor similar to i8080 or 6800 using VHDL/Verilog BEHAVIORAL MODELING. Verify the correctness of your design by executing the instruction set. You must introduce behavioral-level fault model in your microprocessor behavioral model and test the microprocessor for various behavioral faults.

### Board Testing

2. Design a digital system at the board-level using VHDL/Verilog. Use Boundary Scan Test (BST) protocol to develop a design and test methodology of your system. You may use design for testability features.

### Functional Testing

3. Design an 8-bit microprocessor similar to i8080 or 6800 using VHDL/Verilog STRUCTURAL MODELING and design the microprocessor at gate level. Verify the correctness of your design by executing the instruction set. You must test the microprocessor for all stuck-at faults. Use Scan path.

4. Design an 8-bit microprocessor similar to i8080 or 6800 using VHDL/Verilog STRUCTURAL MODELING and design the microprocessor at gate level. Verify the correctness of your design by executing the instruction set. You must test the microprocessor for all stuck-at faults. Use Built-in Self Testing using LFSR and MISR.

### FPGA Testing

5. Design a testing methodology for FPGAs using symmetrical array architecture/ row-based architecture/ sea-of-gates architecture.

### Memory Testing #1

6. Design a Verilog/VHDL model for self-testable Multiport/FIFO/VRAM memories. Your design should be parameterizable in the sense that it can test memory arrays of variable size. Show the CMOS implementation of the BIST circuit and estimate the overhead of the BIST circuit as a function of memory size.

### Memory Testing #2

7. Design the most compact layouts for automatically generating a set of functional algorithms (select the algorithms after discussing with the instructor). Compare the layout overhead with fault coverage. Your BIST circuit must be parameterizable and it should dissipate very low power and it should have minimum interconnect overhead.

### Memory Testing #3

8. Develop BIST circuits for IDDQ and SDD testing in SRAM memories.

### Memory Self-Repair#4

9. Combine BIST with automatic replacement of faulty cells by invoking spare rows and/or columns.

### IP Core Testing #4

10. Develop test strategies for hard/firm/soft IP modules.

## **Deep Submicron Fault Modeling**

11. Thorough literature survey of the effect of scaling on device electrical parameters. Apply on an SRAM cell and show the behavior through SPICE simulation. This work is not as easy as you may think.

### **Test Generation #1**

12. Design a Test Generator for domino CMOS circuit testing.

### **Test Generation #2**

13. Design a Test Generator for CMOS delay fault testing.

### **Test Generation #3**

14. Design a Test Generator for CMOS IDDQ testing.