Workshop on NSF Nanoelectronics: Circuits, Systems, and CAD Tools

Hilton Arlington, October 15 – 16, 2007

National Science Foundation
Computer and Information Science and Engineering (CISE)
Computing and Communications Foundations (CCF)
Emerging Models and Technologies for Computation (EMT)

Report Compiled by: Kathleen Meehan, Virginia Tech

NSF Program Manager: Pinaki Mazumder

2008

Acknowledgements

We wish to thank Dr. Pinaki Mazumder, Program Director of the Emerging Models and Technologies for Computation (EMT) for his sponsorship of and his help in planning this workshop, Allison Smith, Program Assistant in Computing and Communications Foundations (CCF) for her administrative and technical support. On behalf of Dr. Pinaki Mazumder, we would like to thank the distinguished speakers for their pivot role in providing their insights into the field. We also acknowledge the contributions of the more than 80 workshop participants, including the invited speakers, who provided the research foundations for the discussions that were held throughout the two day workshop, contributing thoughtful comments and useful recommendations during and after the workshop, and responded to the draft of the breakout session and workshop report. We are grateful for the time and effort expended by Dr. Paul Rothemund and Dr. Chris Dwyer (DNA-Based and Molecular Electronics), Dr. Alan Seabaugh (Evolutionary and Revolutionary Nanoarchitecture), Dr. Marco Saraniti and Dr. Jan Rabaey (CAD Tools for Nanoelectronics), and Dr. John Savage (Management of Uncertainties and Processing Induced Defects) for their leadership as chairs of the breakout sessions and in organizing the breakout session reports.

Executive Summary

A two-day workshop on Nanoelectronics Circuits, Systems, and CAD tools was held on October 15-16, 2007 in Arlington, Virginia. The workshop was funded by a National Science Foundation grant from the Emerging Models and Technologies for Computation (EMT) Program (Dr. Pinaki Mazumder, NSF Program Director) to Dr. Kathleen Meehan and Dr. Yong Xu, Virginia Polytechnic Institute and State University (also known as Virginia Tech). The primary objective of this workshop was to allow the current principal investigators and leading researchers in the field of nanoelectronic systems to review the impacts of the EMT Program for the Nanoelectronics program element on various fronts: research, technology transfer culminating into better competitiveness of the USA and establishing new start-up companies, undergraduate and graduate education, promotion of cross-disciplinary teaching and research activities, training of engineers, and societal benefits, namely engendering enthusiasm amongst high school students and society in general. To achieve this objective, Dr. Mazumder invited twenty distinguished nanoelectronics researchers to share their vision of the future research directions in nanoelectronics. He also requested the workshop participants during the breakout sessions to evaluate the success of the current research projects supported via grants from the EMT program, overviews of which were given by the PIs during brief talks and poster sessions, in meeting the past and future needs in this field. The insights into the field from these internationally recognized leaders in nanoelectronics research and the principal investigators in the EMT program and their recommendations on the areas in which research should be focused to address the critical needs of the field have compiled into this report.

The workshop speakers included an array of highly regarded researchers who provided their vision of nanoelectronics by sharing their own research work, current principal investigators who described the research projects that have been funded by the EMT, and attendees who studied the written materials, presentation slides, and posters of the principal investigators. Nineteen invited talks were given by national and international experts in the field, from academia and industry, including the Semiconductor Research Corporation, which recently established a consortium of companies from the Semiconductor Industry Associated called the Nanoelectronics Research Initiative. These presentations provided a review of the accomplishments achieved to date, an overview of the technical challenges that still need to be addressed to attain the promise of molecular, DNA, and other nanoelectronic approaches, and described a number of new research directions that have the potential to overcome some of these challenges. The names and contact information of workshop participants and attendees is listed in Appendix A and the workshop agenda is provided in Appendix B.

This report is organized into four major sections that cover major research thrusts in the area of nanoelectronics devices and assembly techniques, nanoarchitecture, computer-aided design tools for nanoelectronics, and management of uncertainty and defects in quantum devices. In each section, a short review of the state-of-the-art with highlights of the research sponsored by the EMT Program and its impacts is provided. The significant challenges within each research thrust area are described. Recommendations are made to guide the EMT Program, the National Science Foundation, and the nanoelectronics research community as a roadmap of the emerging nanoelectronic circuits, systems and CAD tools as the EMT Program and NSF develop plans to move this field forward.

The EMT Program clusters stand out in the Computing and Communications Foundations (CCF) Division as a lone and small cluster in contrast with other big clusters. Therefore, it is useful to understand the perspectives and aspirations of the research community through this workshop and then make a managerial decision as to the future of the EMT Program. In addition to the recommendations to support the research needs of the nanoelectronics community, the recommendations from this workshop will help NSF make an informed decision regarding critical issues: whether the EMT Program should be retained in its present form, whether it should be altered sufficiently to fit into the re-clustering schemes within the CCF Division, or whether some small changes will be necessary to more effectively manage this variegated, multidisciplinary and often chaotic research program that straddles over the boundaries of various individual research fields in biology, medicine, physics, chemistry, electrical engineering and computer science. The final section of the report addresses the importance of the EMT program to the nanoelectronics community and contains comments and recommendations on how to sustain and grow the interdisciplinary teams needed to support the advancement of nanoelectronics research.

Summary of Recommendations

The needs of the research community were identified for each of the areas discussed in the breakout session. A summary of the highest priority recommendations for each area is provided. Recommendations were also made for the EMT Program in general and are also listed below. The discussions on issues related to each of these recommendations along with additional recommendations are described within workshop report.

Molecular Electronics:

1. Develop reproducibly fabricated systems in which a non-trivial set of molecules can be substituted and achieve a complete chemical, electronic, and structural characterization of molecular junctions and metal-molecular contacts including chemical and structural stability under a reasonable range of storage and operation conditions. This will likely required support to develop new spectroscopic tools that can identify the type, configuration, and bonding of molecules in junctions.

2. Develop a test suite of approximately ten control experiments that can be run on all molecular electronic systems and support the application of the test suite to probe the behavior of molecules. Results from these tests should lead to the development of a standard definition of yield.

3. Support a long-term, committed effort in the standardization, coordination, and verification of software for electron transport modeling and apply to a simple, repeatable, model system for resonant tunneling devices such that there is agreement between theory, experiment, and simulation within in few tens of percent.

4. Support the fabrication of a multi-device circuit from individual molecular electronic devices and the exploration of other electronic effects that molecules can mediate besides

direct electron conduction, including but not limited to the modulation of silicon conduction or the creation of hybrid FETs.

DNA-Based Electronics:

1. Develop new, robust, high yield, linking chemistries for coupling DNA to a wide variety of potential nanodevices, such as silicon nanowires, carbon nanotubes, and semiconductor quantum dots.

2. Develop robust techniques for the placement and orientation of DNA origami or DNA tile arrays on silicon (or other technological substrate) with half micron spacing in high yield (> 90% of positions have a single DNA structure).

3. Stimulate advances in all areas of DNA nanostructure processing, including metallization, dewetting, replica formation, and use as a mask for other materials. Stability analysis of DNA nanostructures under these processes.

4. Support the use DNA self-assembly to create (a) a plasmonic transistor (or at least a plasmonic modulator, without gain), (b) a ring oscillator, and (c) a 2-10 gate logic circuit.

Nanoarchitecture:

1. Study how to utilize nanoelectronic devices based on new state variables. Using charge to represent information will yield excessive heating for extremely small devices. Non-charge variables based on phase transitions, spin or magnetization can require less energy per bit.

2. Develop a quantitative understanding of interfaces to molecules and biology. The connection of conductors with molecules or biological entities needs to be probed at an atomic scale to understand devices.

3. Determine how to embed fault tolerance into nanoelectronic systems. CMOS technology compresses analog voltage ranges to digital bits at each operation. Nontraditional architectures will need new approaches to error correction, at sizes ranging from multiple devices to the system itself.

4. Stimulate the invention of nontraditional architectures that (a) enable new nanoelectronics technology in two- and three-dimensions, (b) that can take advantage of stochastic organization of molecular devices by reprogramming them or measuring the intrinsic circuits they compute, and (c) that enable a wide operating temperature range about room temperature.

CAD Tools:

1. Define a hierarchical (layered) scheme for CAD tool development and define adequate abstraction for each layer of the hierarchy with increased feedback between layers.

2. Identify and incorporate promising state-of-the-art ab-initio models into nanodevice and carrier transport simulations.

3. Improve algorithmic efficiency of transport and device simulation by a factor of at least 100 times.

4. Develop circuit simulation tools that include electro-thermal, soft and liquid state, interconnects, nonlocal parameters.

Managing Uncertainty and Defects

1. Fund nanoscale device research to produce parameterized reliability models for wires and devices assembled using traditional and non-traditional methods and architectural and systems-level research to identify and characterize fault models

2. Support theoretical research to understand the limits of the feasible reliability-capacity design envelope. Important areas for theoretical expansion and exploration include exploitation of differential redundancy, differential complexity between computation and checking, and coding.

3. Support practical research to place existing techniques within the reliability-capacity space and develop new techniques or combination of techniques, which close the gaps in the space.

4. Stimulate strategic collaborative research to redefine the abstraction boundaries from devices to systems to better accommodate the high fault rates. This includes cross-disciplinary education to better allow device scientists and system-level engineers to communication on tradeoffs and to create the next generation of engineers who can navigate in this broader design space where reliability is a parameter rather than an absolute.

EMT Program:

1. Provide supplemental grant support for student exchange programs so that students from one lab can go to another lab and learn a critical piece of technology.

2. Initiate a program to create and support intense, “boot camp”-style summer schools, approximately three weeks in length, where techniques of a field are transferred to all attendees.

3. Support short, interdisciplinary conferences with speakers drawn from the EMT program at which tutorials and/or high level lectures.

4. Modify the calls for interdisciplinary proposals to emphasize small (2-3) investigator teams.

Table of Contents

1. Background

A two-day workshop on Nanoelectronics Circuits, Systems, and CAD tools was held on October 15-16, 2007 in Arlington, Virginia. The workshop was funded by a National Science Foundation grant from the Emerging Models and Technologies for Computation (EMT) Program (Dr. Pinaki Mazumder, NSF Program Director) to Dr. Kathleen Meehan and Dr. Yong Xu, Virginia Polytechnic Institute and State University (also known as Virginia Tech). The primary objective of this workshop was to allow the current principal investigators and leading researchers in the field of nanoelectronic systems to review the impacts of the EMT Program for the Nanoelectronics program element on various fronts: research, technology transfer culminating into better competitiveness of the USA and establishing new start-up companies, undergraduate and graduate education, promotion of cross-disciplinary teaching and research activities, training of engineers, and societal benefits, namely engendering enthusiasm amongst high school students and society in general.

The workshop invited speakers were nineteen nationally and internationally recognized leaders in academic research, government agencies, and industry who provided their vision of nanoelectronics by sharing their own research work. Other speakers included current principal investigators who described the research projects that have been funded by the EMT. Presentations on multi-scale modeling followed by a panel discussion on the evening of October 15, 2007 were organized by Dr. James Ellenbogen of Mitre Corporation. Workshop attendees from academia and industry participated in breakout sessions during the second day of the workshop in which they identified and prioritized the technical challenges that still need to be addressed to attain the promise of molecular, DNA, and other nanoelectronic approaches and described a number of new research directions that have the potential to overcome some of these challenges. The names and contact information of workshop participants and attendees is listed in Appendix A and the workshop agenda is provided in Appendix B. The URL for the website containing this material is http://www.ece.vt.edu/optical/NSF_EMT/index.html.

This report is organized into four major sections that cover major research thrusts in the area of nanoelectronics devices and assembly techniques, nanoarchitecture, computer-aided design tools for nanoelectronics, and management of uncertainty and defects in quantum devices. In each section, a short review of the state-of-the-art with highlights of the research sponsored by the EMT Program and its impacts is provided. The significant challenges within each research thrust area are described. Recommendations are made to guide the EMT Program, the National Science Foundation, and the nanoelectronics research community as a roadmap of the emerging nanoelectronic circuits, systems and CAD tools as the EMT Program and NSF develop plans to move this field forward.

2. DNA-based nanoelectronics and molecular electronics

Breakout Session Participants and Report Contributors

Mitra Basu	John Hopkins University	basu@cs.jhu.edu
Tom Beck	University of Cincinnati	thomas.beck@uc.edu
Chris Dwyer (co-Chair)	Duke University	dwyer@ece.duke.edu
Changde Mao	Purdue University	mao@purdue.edu
Ivan Oleynik	University of South Florida	oleynik@shell.cas.usf.edu
Hassan Raza	Cornell University	hr89@cornell.edu
Mark Reed	Yale University	mark.reed@yale.edu (not present, e-mailed comments)
Paul W.K. Rothemund (Chair)	California Institute of Technology	pwkr@dna.caltech.edu
Milan Stoyanovic	Columbia University	mns18@columbia.edu
James Tour	Rice University	tour@rice.edu (not present, e-mailed comments)
Brian Willis	University of Deleware	bgwillis@udel.edu
Erik Winfree	California Institute of Technology	winfree@caltech.edu
Hao Yan	Arizona State University	hao.yan@asu.edu
Hongbin Yu	Arizonia State University	yuhb@asu.edu

The breakout session on DNA-based and molecular electronics included a diverse group of researchers from theorists and experimentalists in molecular electronics to specialists in DNA self-assembly and molecular computation. Because research interests fairly cleanly divided the scientists between those that study molecular electronics and those that study DNA as an engineering material for nanostructure synthesis and molecular computation, here we informally refer to them as the "molecular electronics researchers" and "DNA researchers". At certain places in this document, particular ideas are associated with certain breakout members, who are identified by their initials so that program officers may follow up (and get better articulation of these ideas) by contacting the session member directly. Association with an idea does not indicate endorsement, merely that a particular breakout member expressed strong or interesting opinions on the idea and may have more to say.

2.1 Molecular Electronics

2.1.1 State of the Art

So far, molecular electronic devices have been limited to three types, based on their method of fabrication; molecules inserted into a break junction (a break in an electrode), molecules inserted into gaps in self-assembled monolayers on gold (wherein an STM tip serves as on of the electrodes), and molecules deposited on lithographically defined electronics. The primary material used as the contact for these devices has been gold. Historically, there has been poor characterization of the molecule-electrode interface In several studies, the behavior of "molecular devices" was shown to be independent of the type of molecules in the device; rather, device behavior has been traced to phenomena associated with the contacting electrodes

(electrode migration, for example). In recent years, experiments have reproducibly demonstrated molecular devices with behavior dependent on the type of molecule used in the device – true molecular electronic devices. Still, within the molecular electronic community there is considerable discussion regarding the potential role of molecules in electronic circuits, specifically whether or not molecules will ever play a role as the active state-variable carrying components or whether intrinsic molecular transport of electronics is of mostly academic interest.

2.1.2 Challenges

2.1.2.1 New and better characterized contacts, standard control experiments

On the practical fabrication level, there is a need for new kinds of contacts, other than the standard gold electronics, ones with different work functions (Pt, Ag, Cu, Si, etc.) which will interact with molecules differently, yielding different mechanisms for electron transport and supporting different types of devices (I.O.). Metal electrodes are attractive for their electronic properties. But, the electric field across nanometer-sized gaps are enormous even when voltages are 0.5-1.0 V, and metal electrodes have a tendency to electromigrate, which dominates, masks, changes, or destroys the properties of the molecular device to which they connect. Other electrodes, such as silicon or carbon nanotubes are particularly attractive because they are far less subject to electromigration - up to 1200 read-write-erase cycles have been observed with such electrodes. (J.T.)

On a fundamental level, there is a need for characterization of the molecule-electrode interface. The chemistry of the contact is the domain of surface science. Much used techniques, such as STM and conductive- ARM have taken use far but methods such as tunneling spectroscopy (IETS) will allow us to probe the electronic structure of molecules in detail (B.W., M.R.) In addition, combining IETS with other probes (such as optical excitation, Raman, etc.) will allow for a fundamentally new, in-situ characterization approach. Such studies will also make clear those situations for which we are studying properties of the contact//electrodes or actually probing the electronics of molecules at the single molecular level. And, they will help identify configurations, geometries, impurities, and transport mechanisms. It was noted that problems with the characterization of molecule electrode contacts have also confused and slowed studies of the conductivity of DNA.

With regards to confusion about the sources of device behavior in molecular devices, a suggestion made by both molecular electronics and DNA researchers was to use elaborate “controls” (M.S., P.R.) It may seem ridiculous (and laborious) to fabricate a whole molecular electronic device and leave the molecules out bit these kinds of exhaustive, combinatorial controls are often necessary in molecular systems. Certainly, just such experiments have been used to resole the confusion regarding the performance of molecular electronic devices – the suggestion is that a standard set of such controls be proposed and the culture of doing such exhaustive controls be emphasized within the molecular electronics community.

2.1.2.2 A simple model system for reconciling theory and experiment

Breakout members expressed a need for a simple model system for molecular electronics (‘one

we can all agree on, theorists and experimentalists alike") – a sort of lab-rate for molecular electronics. So far, the best modeled system has been alkanedithiols between two metal electronics (H.R., I.O.). These molecules are fundamentally tunneling-based devices, wherein electron transport is not length dependent- these are the systems that hold most promise as devices and are currently of most interest, Yet, we evidently have no resonant tunneling system that is reproduced reliability from lab to lab and theory has been unable to match the behavior of these devices within a couple orders of magnitude.

2.1.2.3 Standards for calculations, commitment to software development

In bridging the gap between theory and experiment, a good experimental model system is not enough. There is a need for standards for the large pieces of software that are used for theoretical calculations of electron transport (T.B.) When different groups make calculations on the same model system, they often use different numerical techniques and the calculations do not agree. Even given a fixed numerical technique, say density functional theory (DFT) the quality of the calculations can vary greatly based on the quality of the various parameters and assumptions put into the model (say the quality of the DFT functionals and size of the basis set used). A resent study showed, contrary to expectations, that a popular software package' transSIESTA' requires large basis sets for accurate answers and so many studies in the literature are flowed. But, in contrast, some recent DFT calculations do match experiments fairly well (e.g., Nanoletters, volume 4, page 267).

The question becomes, how to compare and rigorously judge the quality of theoretical calculations or even how to know when the assumptions of two different studies are the same or different. There are currently too many 'variables' in calculations so that it is very difficult to identify where error originate. A coordinated, committed effort would work to clarify two kinds of questions:

1. What are the uncertainties in direct comparisons with experiment? What are the essential features of experiments that we need to include in calculations for them to be accurate? What effects are important to include? For example, how sensitive are our calculations to our knowledge of bond geometry? Must we model thermal fluctuations?

2. Given fixed assumptions about the physics of a given experiment, how do we compare the performance of two different modeling techniques? Which technique has better performance and, under what conditions does it give accurate results? Is a technique sensitive (or not) to the amount of computational time given to it, or the quality of its basis set (e.g., for DFT)?

Currently, most of the available code for density functional theory (DFT) electron transport calculations has come out of Europe, especially England, Finland, Denmark, and Spain , rather than the U.S. The most widely used code is tranSIESTA, mainly developed by a physics group in Spain. Code development and verification of the type discussed above requires long-term commitment and, if the U.S. is to contribute to and affect the interplay between theoretical calculations and experiments, there must be support from the NSF.

2.1.2.4 New fabrication methods and scale-up

New, potentially easier methods of molecular device fabrication are sought, as well as methods for combining multiple molecular devices into circuits, and integrating them with conventional electronics. Perhaps, here, DNA self-assembly can play a part for new ways to organize multiple molecular devices.

An Obvious advantage of molecules for electronics is their small size, which is not realized in single devices that use large ensembles of molecules to switch. But realizing this advantage is difficult since our address lines greatly exceed the size of the molecules being tested. If the problems of organizing and addressing multiple molecular electronic devices cannot be solved, new approaches that take advantage of stochastic organization of devices may be found. For example, a randomly connected circuit of molecular devices might have its intrinsic circuit measured and useful subcircuits could be used, or the random circuit might be reprogrammed after fabrication (J.T.)

Combination of devices into circuits may not make sense for molecular devices whose mechanism of electron transport is tunneling. Thus, as a part of scale-up, specific attention must be paid to the creation of devices that exhibit different electron transport behavior (e.g., resonant tunneling devices), and to the establishment of gain n multi-devices structures.

2.1.2.5 What should the future of molecular electronics be?

Because of the aforementioned difficulties in reproducibly making and charactering molecular electronic devices, there has been some reluctance to continue or initiate new studies in molecular electronics. As James Tour noted during this talk at the regular session, even in those systems for which true molecular electronics devices have been demonstrate, the number of switching events that can be observed before the molecules degrade is often just a few, or few hundred.

Tour articulated a way forward for the field: Study systems in which traditional conductors carry the current and the molecules modulate the effect of traditional devices (for example, modulating the threshold voltage of a transistor). This approach would serve to get molecules into labs and under study, perhaps into service in practical devices – a sort of stepping stone to molecular electronics as we become more comfortable with molecules. A complementary way forward was articulated by Mark Reed during his talk, which emphasized molecules integrated with electronics as sensors, sensors for biotechnology and for applications in other fields.

Breakout members noted that these were both valid directions for molecular electronics and complementary to more classical approaches, but expressed concern that the field should not lose sight of its underlying concerns: "To understand the interplay between the atomic structure and electronic structure of molecules and to simultaneously engineer electronic can atomic structure at the molecular/electrode interface. (I.O.) Also expressed was the idea that the NSF should be concentrating on funding basic research and not finding a "killer app" for molecular electronics – that the NSF' goal should be to fund research on the long-time scale, not cater to the short-term interest of industry, for example. It was noted that a search for "killer app" hit the NDA

computation community without a couple of years of its inception and that while no killer apps have yet been found, much important basic research on self-assembly, algorithmic self-assembly, and biochemical circuits has resulted.

It should not be merely because of technical challenges that we back away from the direct study of the electronics of molecular structures. (Note that neither Tour nor Reed made an argument that such studies should be abandoned.) Among the breakout session members, it was generally agreed that there is now a need to "remake the argument for precise control over material structure in molecular systems" within the scientific community, despite the inherent challenges/

Practically, it was noted that problems with yield and stability may affect almost all nanoelectronics systems, and ways to solve thesis issues must be found. Potential solutions range from new, fault-tolerant and degradation-resistant device architectures to approaches from biology: in biological systems molecular machines are susceptible to degradation, but they are constantly recycled and renewed – perhaps molecules in our molecular electronics can be similar continuously replenished.

2.1.2.6 Succinct description for challenges

1. Repeatable fabrication techniques for Cu, Pt, Si, and Ag electrodes and their contacts with molecules. Determine whether electromigration in metal electrodes can be overcome, and develop electrodes that are not subject to electromigration (Si and other semiconductors).

2. For reproducibly fabricated systems, achieve a complete chemical, electronic, and structural characterization of molecular junctions. A system in which a non-trivial set of molecules can be substituted is desired.

3. Develop new spectroscopic tools that can identify the type, configuration, and bonding of molecules in junctions.

4. A simple, repeatable, model system for resonant tunneling devices for which theory and experiment agree within in few tens of percent.

5. A test suite of 10 control experiments that are run on all molecular electronic systems.

6. A set of standard definitions for yield.

7. Many more studies probing the behavior of different molecules within the context of the same type of molecular device and experimental setup

8. A long-term, committed effort in the standardization, coordination, and verification of software for electron transport modeling.

9. Fabrication of a multi-device circuit from individual molecular electronic devices.

10. New device architectures for molecular devices that can take advantage of stochastic organization of molecular devices, by reprogramming them or measuring the intrinsic circuits they compute.

11. Development of methods of stabilizing molecules in molecular devices to give them longer lifetimes.

12. An exploration of other electronic effects that molecules can mediate besides direct electron conduction, including but not limited to the modulation of silicon conduction or the creation of hybrid FETs.

2.2 DNA self-assembly, nanoelectronics and computation

2.2.1 State of the Art

DNA self-assembly techniques have advanced quickly in the last few years and it is now possible to create small (~ 100 nm) rectangular or square structures using either hierarchically assembled DNA tiles (C.D., N.Y.) or DNA origami (P.R.). With numbers of addressable positions in the 60-200 pixel range and resolutions from 20nm down to 6nm, these techniques are very promising for the organization of nanodevices in arbitrary patterns. Well-defined periodic checkerboard patterns of 5 and 10 nm gold nanoparticles have been achieved by a group led by Ned Seeman, Richard Kiehl, and Paul Alivisatos and demonstrated the state of the art in the coupling of nanodevices to DNA nanostructures. We can couple pure preparations of gold nanoparticles to DNA very well, near quantitatively in some instances, but the coupling of quantum dots, carbon nanotubes, and other potential nanodevices is less well developed. The chemistries that we have to work with work well in particular biotin-steptavidin binding, thiol-gold binding, and some click-chemistries (say, azide-alkyne cycloaddition), but the variety of robust and widely practiced reactions is not large. Other ways of using DNA in nanoelectronics are being explored. Progress has been made in metallization of NDA nanostructures, for examples on breakout member (C.M.) has managed to make 7 nm palladium wires using DNA.

Yet the use of DNA self-assembly in nanoelectronics is still limited. Most often, DNA nanostructures are studied on mica, a substrate that is not a so-called “technological substrate” that is amenable to microfabrication processes. And, typical DNA structures either have no devices (and the purpose of an experiment is to demonstrate the creation of a more complex DNA structures) or just single devices or single wires are demonstrated. Wires that are created typically are coarsened to very large sizes, so that the high resolution of DNA patterning is lost, or the wires have the low-conductivity properties of granular metals.

At a fundamental level, the study of self-assembly as an organizing principle for creating structures in a bottom-up fashion has been greatly advanced by the practice of DNA self-assembly. Algorithmic self-assembly, which may embed arbitrarily complex computation into a growth process has been demonstrated in several simple model systems (E.W, P.R.). Hierarchical and uniquely addressed self-assembly have also been explored (H.Y., C.D., P.R.). Buy, self-assembly methods for creating, from molecules, structures that are the size and

complexity of cells have not yet been demonstrated and defect rates (by various measures) for self-assembled structures are still no less than a few percent.

2.2.2 Challenges

2.2.2.1 Integration of devices, integration with microfabrication

"Integration" was often repeated as an important challenge for DNA self-assembly methods. It became clear that integration has at least two meanings: a) quantitative organization of molecular, nanoparticle, nanotubes or nanotubes devices using DNA nanostructures as a template or b) making NDA self-assembly techniques part of a complete microfabrication scheme.

With respect to challenge a), new quantitative and robust methods for coupling potential nanodevices to DNA structures need to be developed. We seek to demonstrate the unique capabilities of NDA to organize and pattern other nanomaterials by scaffolding. For 2-D and 3-D NDA self-assembly may have real advantages over traditional lithography and other methods. In one dimension, bar-code patterns of quantum dots can be grown by molecular beam epitaxy, but the organization of quantum dots in complex 2-D patterns might be best accomplished by DNA scaffolds. For 3-D structures, H.B. has proposed the creation of more compact inductors by metallization of DNA spirals. Also, other biomolecules, peptides, proteins, RNA, and Viruses are all easily incorporated into DNA self-assembly schemes and may add new functions to DNA nanostructures.

For goal b), binding of DNA nanostructures to technological (non-mica) substrates such as silicon or other semiconductors needs to be developed, or methods of growing DNA nanostructures on such surfaces should be developed. Most DNA nanostructures are formed in solution and deposited with random position and orientation on the surface, so methods for positioning and orienting DNA nanostructures are of great interest. While molecular combing techniques work well for long DNA strands, novel techniques may be required for complex 2-D nanostructures, which often fold or rip when applied to surfaces. Similarly, methods for gently dewetting DNA nanostructures, without destroying them, are of great interest to allow further solution-incompatible processing steps. In all processing steps for DNA nanostructures, there must be an emphasis on yield.

It was noted that researchers interested in using DNA for nanoelectronics often ask about the stability of DNA nanostructures (H.Y., C.D.). DNA nanostructures are generally not stable in solutions above 70 ^{o}C. But, apparently little research has been done on their stability, dry or in vacuo, above 100 ^{o}C. It is tempting to assume that, because DNA will not likely play a part in the functioning of the nanodevices that it organizes, it may be "burned away" in subsequent processing steps, as photoresists are stripped away. In fact, people worry greatly about the stability of a photoresist to various processing steps and we must investigate the robustness of DNA nanostructures to a variety of processes. We may need to figure out how to compartmentalize DNA self-assembly steps from pre-assembly organic chemistry and post-assembly conventional fabrication.

2.2.2.2 Creating of functional circuits

Many single particle and single devices have been created at the nanoscale, but few many-device or many-body interactions have been studies. To demonstrate the power of DNA self-assembly for nanoelectronics, an important milestone for the field is to create functioning nanocircuits with 2-10 devices. An ambitious goal would be a ring oscillator, but a circuit of just a couple of gates would be compelling. The circuit need not be a conventional electronics one, any physical mechanism of information processing would suffice. For example gold nanoparticles could be self-assembled into a nanophotonic circuit (H.Y.). If 2-D or 3-D patterns of quantum dots could be arranged with DNA self-assembly, then the resulting structures might be used in quantum information processing for spin-exchange quantum computers. Just such an approach is the subject of a currently funded EMT "DNA patterned colloidal quantum dots, a scalable approach to computing without wires", by PIs Deborah Fygenson (Deborah@physics.ucsb.edu) and Dirk Bouwmeester (bouwmeester@physics.ucsb.edu).

2.2.2.3 New tools for analyzing DNA nanostructures

Defects are common in self-assembled structures. The creation of large, defect-free complex DNA nanostructures must be validated by tools that are capable of scanning large areas with high resolution. In this regard, AFM, the most widely used technique, is slow and not very practical. Development of better instrumentation for nanoscale characterization will benefit other nanoelectronics efforts; as noted by C.D. finding a single defect in a modern Pentium is a difficult task.

2.2.2.4 Greater size and complexity, programmable chemistry and compilers for DNA structures

So far, 2-D periodic DNA structures that are provably single crystals have been relatively small, no more than about 10 microns in size. On a practical level, it is interesting to ask" How large and how perfect a DNA structure can we make?" (E.W.). For practical nanoelectronics, we wish to make structures that are not just a few microns in size, but hundreds of microns or millimeters in size.

At a more fundamental level, many in the field of DNA nanotechnology are interested in programmable chemical systems (E.W., P.R, C.D.). An important goal is to be able to (1) create a description of a desired structure in a high-level programming language and (2) have that description run through a compiler that outputs DNA sequences and an experimental protocol that should generate the desired structure in high yield with few defects. Ideally, we would like to be able to design complex, aperiodic DNA structures with features whose size ranges from the nanometer scale up to the millimeter scale. To do this, we will need to be able to come up with "design rules" analogous to those that are used to create CMOS chips, which restrict the space of designs available to us, in return for guarantees that designs will work with a certain reliability.

For certain DNA self-assembly paradigms, we already have software tools that work at the 100 nm length scale. In particular, we can design 100 nm DNA origami, with arbitrary shapes and patterns, and experimental DNA origami form as predicted (P.R.). More generally, a number of

questions arise: Is there a traditional CMOS design tool, either for layout or simulation, that can serve as a model for a DNA design tool(s) (and design rules) or are DNA design tools going to be something completely different? Are there going to be different design rules for different DNA self-assembly paradigms, (e.g., origami, hierarchical assembly, or algorithmic self-assembly of tiles) or will we wish to integrate these paradigms from the very beginning? Are we even ready for design rules? Have we learned enough to start drawing lines around the playground in which we wish to work?

In her introductory remarks, assistant CISE director Jeannette Wing asked about the role of computation in nanoelectronics and their fabrication, in particular: "How do we make complex things in simple ways or from simple materials?" and "How can we have a complexity theory for the nanostructures that we build?". Algorithmic self-assembly of DNA, as a model for creating nanostructures, is an archetypal example of how computation can be intertwined with physical processes and answer these questions. Algorithmic self-assembly enables an arbitrary computation, any algorithm, to be encoded as a set of DNA tiles, so that the growth process of a DNA crystal created from those tiles performs the desired computation. This allows the formation of complex patterns from simple materials (the tiles) such as Sierpinski triangle fractals, or more practically, the 2-D patterns that underlay circuits such as demultiplexers, or even Hadamard transforms. The number of distinct tiles types required to create a given pattern or shape is a kind of program size complexity, and so the complexity of patterns and shapes inherits many traditional results in computer science. Similarly, the time to self-assemble a pattern or shape is analogous to the running time of a program. As more emerging models are investigated, now models will be able to perform general purpose computation and new connections to computer science will be made.

2.2.2.5 Succinct description of specific challenges:

1. New, robust, high yield, linking chemistries for coupling DNA to a wide variety of potential nanodevices, such as silicon nanowires, carbon nanotubes, and semiconductor quantum dots.

2. The placement and orientation of DNA origami or DNA tile arrays on silicon (or other technological substrate) with half micron spacing in high yield (> 90% of positions have a single DNA structure).

3. Advances in all areas of DNA nanostructure processing, including metallization, dewetting, replica formation, and use as a mask for other materials. Stability analysis of DNA nanostructures under these processes.

4. Use of DNA self-assembly to create a plasmonic transistor (or at least a plasmonic modulator, without gain).

5. Use of DNA self-assembly to create a ring oscillator.

6. Use of DNA self-assembly to create a 2-10 gate logic circuit.

7. Creation of a 100 x 100 micron 2-D DNA crystal with verification of single crystal nature and low defect rate via a new analysis method. Creation and verification of a 1 x 1 mm 2-D DNA crystal.

8. Creation of a DNA compiler and appropriate design rules that allows the design and synthesis of complex, 100 micron DNA shapes and patterns.

9. Support the development of new robust DNA motifs that are capable of organizing the various components. This would include refining origami (whose yields now are low) and extending it to larger periodic or aperiodic arrays, either by simple self-assembly or by hierarchical assembly.

3. Evolutionary and Revolutionary Nanoarchitecture: Challenges and Prospects for Nanoelectronics Architectures

Report Contributors

Supriyo Bandyopadhyay	Virginia Commonwealth University	sbandy@vcu.edu
Larry Cooper	Arizona State University	larry.cooper@asu.edu
André DeHon	University of Pennsylvania	andre@acm.org
Steven Hillenius	Semiconductor Research Corporation	hillenius@src.org
James Klemic	MITRE Corporation	jklemic@mitre.org
Jo-Won Lee	The National Program for Tera-level Nanodevices in Korea	jwlee@nanotech.re.kr
Mike Niemier	University of Notre Dame	mniemier@nd.edu
Garrett Rose	Polytechnic University, Brooklyn	grose@poly.edu
Alan Seabaugh (Chair)	University of Notre Dame	seabaugh.1@nd.edu
Kang Wang	University of California, Los Angeles	wange@ee.ucla.edu
Robert Westervelt	Harvard University	westervelt@seas.harvard.edu

Additional contributors in the breakout session

Wei Lu	University of Michigan	wluee@umich.edu
Vijay Narayanan	Penn State University	vijay@cse.psu.edu
John Prater	Army Research Office	john.t.prater@us.army.mil
Mircea Stan	University of Virginia	mircea@virginia.edu
T. N. Vijaykumar	Purdue University	vijay@ecn.purdue.edu
Hongbin Yu	Arizona State University	yuhb@asu.edu

Research in nanoarchitectures should establish the scientific and technical basis to transition nanoelectronic devices into systems. Systems arising from research in these areas can lead to dramatic reduction in power dissipation in computing and extraordinary immunity to fault tolerance. Realization of non-von-Neumann computing architectures based on developments in nanoelectronics should enable special purpose processors with orders of magnitude improvement in capability, e.g. in image recognition. Research at the interface between nanoelectronics and biology should inspire new ways to couple nanoelectronic, molecular, and biological systems, and lead to discoveries of new ways to organize and engineer systems. A close collaboration of system architects and experimentalists should be sought under this research directive.

3.1 State-of-the-art

For CMOS scaled to 45 nm, the energy dissipation in a logic gate is about 5 pJ GHz/μm[†]. To switch a MOSFET with a 30 nm gate width at 3 GHz requires approximately 5 fJ per cycle. Continued scaling will not significantly lower this energy dissipation for high performance computing applications. Present computing systems based on von Neumann's architecture will

[†] The static dissipation is the product of drain current and power supply voltage, 1 mA/μm of gate width times supply voltage, 1 V.

be limited by the energy dissipation and the ability to remove heat from the semiconductor [1]. Current systems are moving to multiple processing cores as the minimum energy density in the device can no longer be lowered and parallel processing is used to improve performance. Current digital signal processors implement fault tolerance architectures to account for the variability in nanoscale components. The fault tolerance is implemented at three levels: the device level, the circuit level, and through error correction coding.

As CMOS devices approach their limits, leakage currents and power dissipation will limit clock speeds to less than 4 GHz. Intel is exploring InSb-based transistors to utilize the higher on-current at lower bias. Most of the research in III-V materials is supported by the DoD, but little at universities. Asia and Europe are the centers for advanced programs (Intel's InSb device is centered in the UK).

Semiconductor nanowires from group IV and III-V materials, organic and inorganic nanotubes and wires, and graphene have been synthesized by a variety of techniques. Transistors and circuits have been demonstrated. How to effectively utilize these devices in systems is still to be determined.

Resonant tunneling and single electron structures have been formed in both group IV and III-V semiconductors. Resonant tunneling devices have been demonstrated in LSI circuits and can lower circuit power dissipation. Tunneling devices operate at room temperature and are relatively insensitive to temperature.

Nonvolatile memory is a necessary component in low power systems and is constructed from nanoscale devices. Already a considerable amount of area on a CMOS CPU is devoted to memory and it is expected that an increasingly larger fraction of the area of a CPU will be dedicated to on-chip memory. Many concepts are under investigation, all have flaws for use in nanoscale circuits, i.e. repeatability, operating voltage, and required drive currents.

There are many nanoelectronic device paths under investigation for lowering power dissipation relative to the MOSFET. These include low-subthreshold swing devices based on field-effect gating of interband tunneling and nanoelectromechanical FETs. Alternative state variables for computing are under exploration including charge and magnetization in quantum-dot cellular automata, spin devices, and phase-change switching devices.

Currently, the packaging part of nanoelectronics research is underdeveloped. Much research on small scale systems for various applications lack methods to move the concept into a packaged practical whole.

3.2 Research targets for nanoarchitectures.

3.2.1 Increase energy-efficiency, exceeding CMOS.

The minimum voltage that can be utilized in a logic device has been considered by Kish [3]. The thermal noise voltage on the gate capacitor is $\sqrt{kT/C}$. With a clock frequency of a few GHz, the value of V needs to exceed the thermal voltage by a factor of 12 or so to achieve reasonable error

rates [2]. According to this argument, the minimum energy dissipation is approximately 72 *kT*. Today's CMOS dissipates about 40,000 – 50,000*kT* according to the ITRS, so there is considerable room for improvement if the voltage needed to operate the device can be lowered without lowering the drive current. There are opportunities for exploitation of compound semiconductors in nanoelectronics; there are few initiatives in the U.S. to push these materials into systems [3]. Nanowire, tube, and graphene devices may hold possibilities for 3D integration and could be accelerated into use by close-coupling of architectural and device research. New concepts for nonvolatile memory and memory architectures based on nanoelectronic devices should be pushed.

Spin is an alternate state vectors which can be used to represent a logic level. A single electron in a magnetic field has two spin polarizations which can be used to represent the binary bits 0 and 1. To achieve low switching energy, switching requires flipping the spin without physically moving charge in space and causing a current flow. Without current flow, the energy dissipation during switching is the energy separation between two spin eigenstates, $g\mu_B B$, which is the Zeeman splitting, where B is the flux density of the magnetic field. The probability of being in the wrong state is $p = \exp[-g\mu_B B/kT]$, assuming that the spin system is in thermal equilibrium with the surrounding phonon bath [4]. In this case, the energy dissipation is $g\mu_B B = kT\ln(1/p)$, which is the Landauer-Shannon limit; the minimum energy dissipated during a bit flip is $kT\ln(1/p)$. With $p = 10^{-9}$, the energy dissipated is $\sim 21kT$. Spin is an energy-efficient state vector. Research is needed to enable the use of alternate state variable devices and to develop architectural schemes for performing logic with these devices.

The magnetization states in nanomagnets are nonvolatile and could be the basis for nanomagnetic computing. There are various applications for such concepts where remote operations are involved and instant-turn-on computing is required. Thus, power would only be used as required and standby power would be zero. It has been demonstrated that signals represented in the orientation of magnetization can be propagated with arrays of nanomagnets without use of currents, just be coupling of magnetic fields to the magnetization in the nanomagnets. Another variation is the formation of domain walls in nanomagnetic wires. For nanoscale dimensions the domain walls create an external magnetic field. Currents can move the domain walls back and forth along the wire in a controlled fashion. The external fields can be used to modulate currents in adjacently formed semiconductor device structures, which are used to extract the information in the magnetization states. Research is needed to advance these devices into systems.

Energy dissipation in CMOS takes place during switching of logic levels. This energy is $(1/2)CV^2$ where C is the gate capacitance and V is the gate voltage required to switch the transistor from "on" to "off" or vice versa. There are ways to reduce this dissipation even without further reduction in supply voltage, by adopting "adiabatic switching" schemes (e.g. applying the gate voltage in small steps); this requires precise control and is error-prone in current schemes [5]. Adiabatic approaches for minimizing energy in systems should receive further attention.

3.2.2 Realize fault-tolerant architectures in the presence of physical device variability

Fault tolerant architectures are predicated on "collective computation models" where the cooperative activity of many devices acting in unison elicits computational activity as opposed to every single device being critical (e.g. in Boolean logic). From this perspective, neuromorphic architectures are decidedly superior. In the quantum neuromorphic model, proposed by Roychowdhury, et al., the circuit functionality is not impaired even if 30% of the devices fail, i.e. $p = 0.3$, whereas ULSI Boolean circuits cannot work if p exceeds perhaps 10^{-9}.

Nanodevices are inherently irreproducible and error prone. It is difficult to manufacture 10^9 nanodevices that are nominally identical. Therefore, permanent error probabilities are significantly larger than 10^{-9}. Consequently, Boolean logic is by no means the optimal strategy for nanodevices. Neural architectures appear to be much more suitable from the perspective of fault-tolerance. However, these architectures tend to be application specific, rather than general purpose. Support for non-Boolean architectures based on collective computational models is therefore encouraged. The potential for further increases in device density beyond CMOS with further reductions in power may require new architectural perspective in terms of integrating parallel (perhaps even massively parallel) computing systems onto a single die.

Research directions might include careful design partitioning to implement nanoarchitectural blocks in ways that minimize power while also reducing output capacitive loads. Research should also be undertaken to support the utilization of various technologies integrated together (e.g., CMOS and carbon nanotubes) to increase the overall system performance in terms of, e.g., energy and delay. Interfaces for accessing the input and output lines within nanoarchitectures must be developed. As is the case with microelectronic chips on a printed circuit board, the physical interface to the outside world is often a large contributor to both delay and power dissipation.

Several studies for implementation of nanoelectronic devices indicate that small functional circuits, or processing elements, in 2 or 3-dimensional arrays using only local connections, could form the basis for massively parallel computing. Local connectivity eliminates barriers such as clock skew, massive interconnect complexity, and permits nanoscale device integration. An example of this is the Propagated Instruction Processor proposed at University College of London and the Cellular Nonlinear/Neural Network.

There are many applications for digital circuits which do not require more than 8 bit resolution; these could form the basis for locally-connected networks. This allows for implementing analog devices. A particular example of this is the Cellular Neural Network (CNN) architecture which has demonstrated enormous enhancement factors for image or pattern processing. The CNN architecture has not been implemented with nanoscale devices; further research is warranted in this direction. There exist opportunities for integration of nanoscale sensors with nanoelectronic components in a 3-dimensional configuration. CNN is an example of a bio-inspired architecture. The CNN performs a global computation on a pattern or image. Such global computations could be considered for neurocomputing concepts, such has been done for the human retina. A new concept for computing called "wave computing" based on the CNN architecture has appeared in Europe.

Quantitative goals for research in architectures can be expressed generally as follows:

1. in the presence of high-variability of nanoelectronic components, improve the system performance over the state-of-the-art,

2. in the presence of delay variations, avoid the need to provision for worst-case slowdown of devices or increase the delay (the state-of-the-art is to reserve margin for slowdown),

3. in the presence of high persistent defects, circumvent the need to discard parts and pay overhead (the state-of-the-art is to discard defective logic elements or even discard large blocks of logic associated with each defect), and

4. in the presence of high transient faults, avoid the need for large integer factor overhead (the state-of-the-art is to use N-modular redundancy or N-way replication and checking).

3.2.3 Develop robust interfaces to nanoelectronic devices, to connect to biology, molecular, and to realize efficient transducers

Robust interfaces to nano devices are in the very earliest stages of research. Recent work in lab-on-a-chip bionanointerfaces have been the first steps towards this goal. Robust means high yield, reproducible, and long lasting within the context of a device application. These interfaces include bio functionalizing nanoelectronics, connecting proteins, cells, and neurons to nanoelectronics. The transduction of cell responses, the creation of new methods for energy harvesting, the realization of practical methods for coupling molecular and biological materials to electronics should all be considered under architectural research. Optoelectronics and its' coupling to biomaterials is an important area of research already well recognized. Robust methods for optically characterizing bio systems and nanoenabled bio/assay systems, in packaged systems can be a part of this research. At an architectural level, it is important to consider how to achieve robustness at the interfaces of integrated multi scaled cores. New modeling and simulation tools are needed to make significant progress in this area, followed by research in targeted applications.

3.2.4 Demonstrate packagable systems and architectures.

In addition to developing nanoelectronics to exceed the performance of CMOS processors, the development of small special purpose nanoelectronic systems should be encouraged. Many novel nanotechnologies may be more easily integrated into 3-dimensional (3D) systems. Integrating systems in 3D may introduce irregularity, where each layer in the 3D system is regular but the overall system is somehow irregular, could also mean it is heterogeneous. In these systems the full package would be considered. The packaging for nano-circuits must not impair circuit function. For in vivo bio-applications, toxicity may be a consideration. For space applications, radiation hardness may be a consideration.

3.2.5 Develop non von Neumann architectures

There are many opportunities for architectural research based on emerging properties of nanodevices. This includes CNN and autonomous/learning/adaptive architectures. Circuits that can be trained for specific functions are preferable since they are "smart." For this purpose biologically inspired circuit models, e.g. Nagumo-Fitzgerald models for impulse propagation along nerve cell membranes [6], or associative memory, are the ideal architectures. These circuits can be realized with passive devices (resistors, capacitors, etc.) and therefore easier to fabricate. They are also compatible with self assembly, which reduces cost. Research in non von Neumann architectures may be particularly fruitful when closely-coupled to experiment. New paradigms of computing and information processing should arise from research in this area.

An important issue in establishing nontraditional architectures is to establish appropriate models that enable the architectural development to proceed. Statistically-based models, used e.g. in speech recognition and image processing deal with uncertainty and noise. Spatial compute models used e.g. in field-programmable gate arrays (FPGA) allow abstraction for location, so programs will properly optimize and are robust to technology scaling. Models that expose adaptation opportunities and allow it are needed.

3.3 Scientific challenges

A list of the scientific challenges to be overcome in the proposed research follows.

1. How to utilized devices based on new state variables
2. Development of a quantitative understanding of interfaces to molecules and biology
3. How to embed fault tolerance into nanoelectronic systems
4. Invention of nontraditional architectures which enable new nanoelectronics technology
5. How to assemble and utilize nanoelectronic devices in three dimensions
6. How to use nanoelectronic devices for system assurance or cyber security
7. How to enable a wide operating temperature range about room temperature
8. Room temperature operation

3.4 Strategies and mechanisms to address opportunities and technical challenges.

The primary strategy for this research effort should be to work at all levels: devices, circuits, interfaces, and architectures. Encourage interdisciplinary efforts and those that closely couple system architects with researchers developing nanotechnologies. The devices must increase energy-efficiency of the whole system and take advantage of close interactions to increase fault tolerance. The hurdles are to implement new systems from exploratory and nontraditional components.

3.5 References

[1] M. Forshaw, D. Crawley, P.P. Jonker, J. Han, and C. Sotomayor Torres. Nano Arch Review: A Review of the Status of Research and Training into Architectures for Nanoelectronic and Nanophotonic Systems in the European Research Area. FP6/2002/IST/1 (Ext. rep. 507519). London: University College London. 2004.

[2] L. B. Kish. Phys. End of Moore's law: thermal (noise) death of integration in micro and nano electronics. *Physics Letters A*, vol. 305, pages 144-149, 2002.

[3] See commentary in Nature-August-07

[4] S. Salahuddin and S. Datta, Interacting systems for self-correcting low power switching. *Applied Physics Letters*, vol. 90, pages 93503-1-93503-3, 2007.

[5] R. K. Cavin, V.V. Zhimov, J.A. Hutchby, and G.I. Bourianoff. Energy Barriers, Demons, and Minimum Energy Operation of Electronic Devices. *Fluctuation and Noise Letter*s, vol. 5, C29-C38, 2005.

[6] S. Bandyopadhyay, K. Karahaliloglu, S. Balkir, and S. Pramanik. Computational paradigm for nanoelectronics: self-assembled quantum dot cellular neural networks. *IEE Proceedings on Circuits, Devices, and Systems*, vol. 152, pages 85-92, 2005.

4. Computer-Aided Design Tools For Nanoelectronics

Breakout Session Participants and Report Contributors

Petru Andrei	Florida State University	pandrei@eng.fsu.edu
Paul Bergstrom	Michigan Technological University	paulb@mtu.edu
Yu Cao	Arizona State University	Yu.Cao@asu.edu
Jing Guo	University of Florida	guoj@ufl.edu
Niraj Jha	Princeton University	jha@ee.princeton.edu
Ernest Kuh	University of California at Berkeley	kuh@eecs.berkeley.edu
Yehia Massoud	Rice University	massoud@rice.edu
Saraju Mohanty	University of North Texas	smohanty@cse.unt.edu
Nishant Patil	Stanford University	nppatil@stanford.edu
Eric Pop	University of Illinois-Urbana/Champaign	epop@uiuc.edu
Jan Rabaey (Chair)	University of California at Berkeley	jan@eecs.berkeley.edu
Hassan Raza	Cornell University	hr89@cornell.edu
Marco Saraniti (co-Chair)	Arizona State University	Marco.Saraniti@asu.edu
Dragica Vasileska	Arizona State University	vasileska@asu.edu

Computer-aided design (CAD) tools will play a crucial role in the research and development of nanoelectronic devices and systems. The need for a comprehensive set of models and their implementation in effective and user friendly CAD tools clearly emerged from the panel discussion, as well as many of the challenges related to their development. The panelists felt that the diversity of applications and components of nano-scale systems will require within the next decade a significant effort in the definition of a *methodology* for the realization of successful CAD tools.

In particular, the panel defined a layered hierarchical model that should be used as a guideline for the development of effective CAD tools and, *at the same time*, represents the modeling-simulation-design-verification sequence of a generic nanoelectronic system. The generality of such approach is granted by the absence of conceptual constraints in any of the steps (layers) within the sequence, while its functional structure is guaranteed by detailed "protocols" connecting the steps. In other words, the panel attempted the definition of a hierarchy of modeling and simulation approaches in which the choice of the models to be implemented in each step is adaptable, while indicating clearly that the different models should be interrelated in a well defined way.

4.1 State of the art

For the sake of clarity, the panel defined a "nanoelectronic system" as a collection of man-made, natural, or hybrid components with nanometer size. By design, such system interacts in a predictable (but not necessarily deterministic) way with the environment through electrical currents. However, the functionality of the system is achieved by exploiting the structure-function relationship of each individual nano-component, which is not necessarily operating in an "electronic" mode that is by displacing electrons in a controlled way.

In other words, we envision a system whose external interface is electrical, but is made of nano-scale components working by exchanging signals that are not necessarily electrical.

This definition encompasses a set of extremely diverse components realized with materials ranging from crystalline solids to condensed and soft matter. Furthermore, the fabrication processes for such divergent technologies are so different that even the definition of a unified simulative approach is arduous. Existing CAD tools for such nanoelectronic systems are currently limited in scope and do not possess the level of integration capable of addressing the challenges needed for the timely development of such technology.

Indeed, a highly functional and unified set of commercial tools for the CAD of solid-state nanoelectronic systems is currently available to researchers and technologists. These software packages were initially inspired by academic software and have been successfully developed for commercial purposes by several companies as a response to the dramatic evolution of the microelectronic industry. They are computationally robust, they possess coherent and integrated interfaces, and they are successfully employed in all the design steps, including process development, by the microelectronics industry. In particular, circuit simulation codes are definitely a success story because of their compactness and simplicity of use. They supply a level of abstraction that is sufficient to attempt their extension to nonconventional circuit elements, including carbon nanotubes, membrane proteins and transporters. Obviously, their predictive capabilities are as good as the compact models implemented in their circuit element databases.

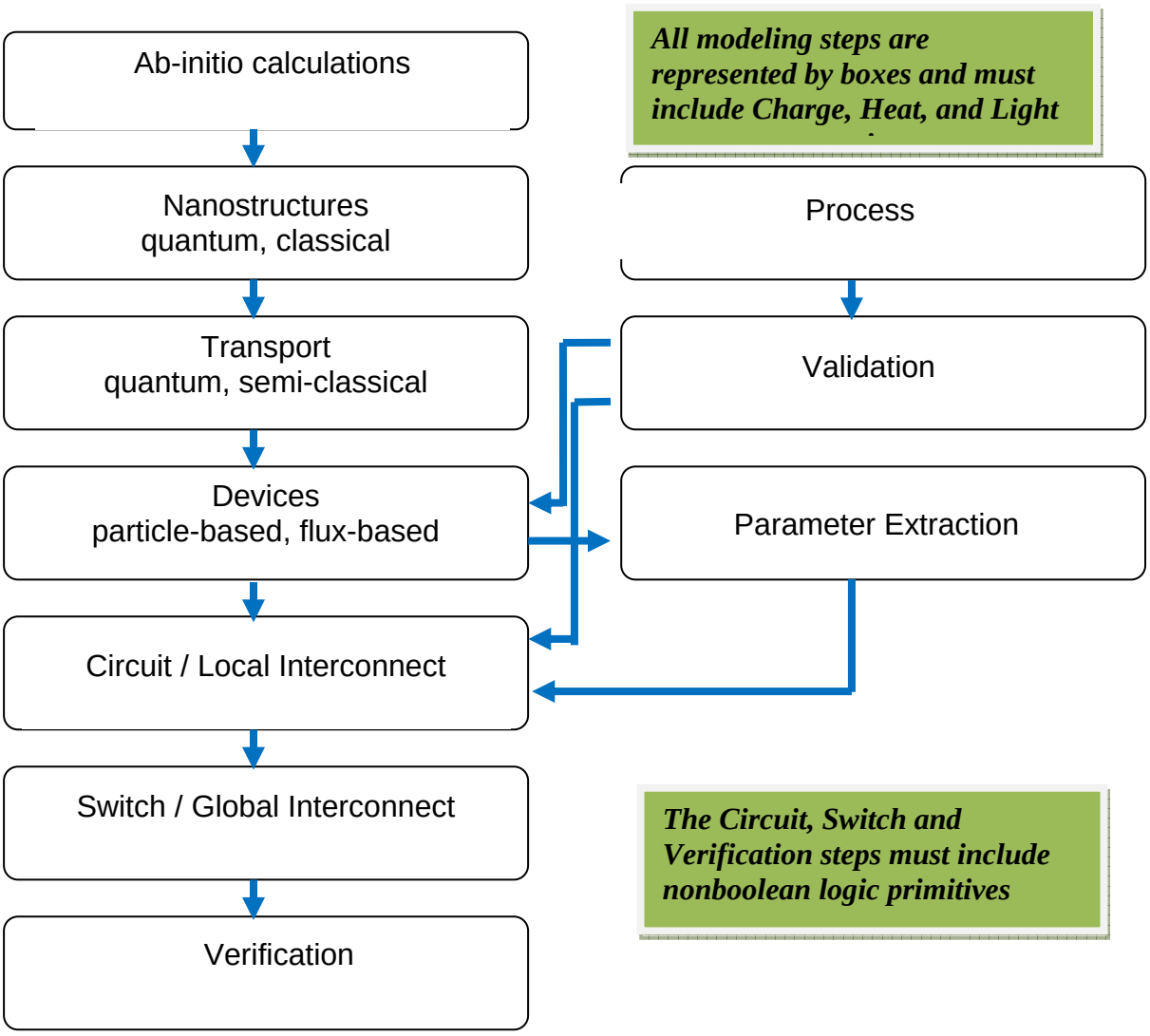
As a whole, commercial CAD software packages do not possess the capability of molecular modeling (either fully quantum-mechanical or semi-classical) which is crucial for the current nanoelectronic technology as defined above. Furthermore, their commercial nature necessarily implies intellectual property issues that make difficult their extension to the non-solid-state technologies that are currently explored.

On the other end, while extremely rich in terms of the physical models it incorporates, the academic software is in general non robust, tends to be application oriented, and is not well engineered in terms of performance or reusability. The open software paradigm is still not adopted by all researchers, and federal funding for the development and integration of medium-sized CAD software projects is sporadic. The current investment of the NSF aimed to the development of a distributed national cyberinfrastructure is significant and goes definitely in the right direction, but some of the panelists feel that a further effort is needed to populate such infrastructure with relevant projects for CAD software.

Recalling the initial definition, the multi-scale and multi-physics nature of CAD tools for nanoelectronics will necessarily require the definition of a hierarchy of models capable of simulating diverse system components with molecular resolution and, at the same time, capable of expressing their structure-function relations with simple laws that can be used to model complete systems (and part of their environment) in a computationally efficient fashion. Designers will definitely need a large set of empirical or semi-empirical models to perform simulation and verification at the system level, and they will also need to continuously calibrate and validate those models with molecular resolution.

4.2 Research targets.

Future nanoelectronics architectures will be made possible by multi-scale CAD tools capable of optimizing their design from the individual molecular components to macroscopic systems of arbitrarily large complexity. Such tools should be organized in a hierarchy of models sorted by increasing time/space scale of the simulated component. Each model should be designed and tuned for a specific individual component or sub-system, and should evolve accordingly to the research on that component/system. The way different models are exchanging parameters must be defined through an adequate level of abstraction; that constitutes one of the major challenges. The panel identified both the overall simulative strategy and the hierarchy of models to be employed, and represented them in the flow-chart below.



In terms of specific research targets, the panelists feel that a major effort is due in order to identify the level of abstraction that each simulative approach must achieve in order to effectively interface with the models it interacts with. For example, any transport modeling effort should be proposed by defining exactly how it will employ data obtained from nanostructure simulation and how it will produce data effectively usable by device simulation. Any new

device simulation tool must define clearly which parameters will be used from charge transport simulation, how device parameters will be extracted, and how they will be supplied to the circuit simulation tools. This crucial methodological requirement should be used to determine the probability of success of each individual proposed modeling approach.
Furthermore, the panelists indicated several research targets for the realization of effective CAD tools for nanoelectronics:

4.2.1 Ab initio approaches for molecular interfaces

Developing and defining ab-initio models, thus far, is mostly a practice of a large quantum chemistry and electronic structure community, used, for example, to design molecules in pharmaceutical industry or to compute the band structure of a material. Two aspects that make nanoelectronics simulation different from quantum chemistry are that the small device channel is attached to large source and drain contacts and the simulation must deal with current flow and a channel under nonequilibrium transport condition. Molecular and solid-state electronics will benefit from the findings of ab-initio calculations. The development of non-periodic polarizable force field schemes for the Brownian and molecular dynamics simulation of electrolyte solutions will be based on parameters extracted from such calculations, as well as all the modeling tools attempting to describe the interface between bulk materials and molecular assemblies or the between solid and liquid components of the hybrid nanoscale systems. Models of charge and heat injection from a classical bath to a quantum system need further development, while ab-initio calculations of electronic structure and phonon spectra of disordered alloys and exotic materials will play a crucial role in spintronics and nanomachines for (bio)energy conversion.

4.2.2 Transport and device simulation

Transport and device simulation must be based on results of ab-initio calculations, and include thermal and optical properties. The capability of modeling realistic 3D geometries in realistic times is also a must. This is a mature field that produced tools that rarely left the academic environment; it can be dramatically improved by adopting unconventional algorithmic solutions in order to achieve higher computational efficiency and, at the same time, higher accuracy. The modeling capabilities of both particle- and flux-based simulations (Ensemble Monte Carlo and Drift-diffusion/Hydrodynamic method, respectively) shall be extended to the liquid-state in order to model hybrid nanosystems.

4.2.3 Circuit and local interconnect

Circuit simulation software will definitely play a pivotal role in transferring the result of sophisticated physical models to the system level. A major effort is needed in order to extend their functionality from electrical to full electrothermal characterization of solid-state devices, and to generalize the parameter sets in order to effectively extend their capability of representing soft and liquid state components. Particular care should be devoted to the inclusion of interconnects, often represented as classical/quantum interfaces.

4.2.4 Switch and Global interconnect

Once more, any of the proposed approach must provide an adequate level of abstraction in order to relate effectively with other tools in the simulation hierarchy illustrated above.

4.3 Scientific challenges.

The main challenge identified by the panel is the related to the obvious difficulty of defining a modeling and simulation approach that is capable of enabling the development of systems based on diverging technologies. We therefore feel that a major task is the definition of appropriate abstractions representing each step in the CAD hierarchy defined above. Each proposed modeling tool must therefore address that issue.

Concerning the individual research targets as defined above, we identified the following challenges as equally important:

4.3.1 Ab initio approaches for molecular interfaces

In part, this challenge is to apply what has been learnt in chemistry to the simulations of nanodevices; yet, significant modifications to the existing approaches must be made to include the nonequilibrium carrier transport and to decrease the computational time required for these simulations to reduce the time required to model these systems. Quantum-mechanical calculations involving large molecular assemblies are arduous, and a significant effort is needed both from the theoretical and the computational viewpoints. The identification of the appropriate approaches and approximations is crucial in this case. For example, the GW method appears to be extremely promising for band structure calculations, magnetic properties of materials, and electron-phonon interactions. Nonequilibrium Green's functions have been successful in determining transport properties of nanostructures. In all these cases, the capability of accurately modeling interfacial properties of the nanocomponents will be crucial.

4.3.2 Transport and device simulation

Charge transport modeling and device simulation approaches need to be extended in order to self-consistently model heat and, possibly, the light generation and transport properties of the simulated components. Furthermore, the modeling capabilities of such approaches must be extended beyond the semi-classical paradigm set by the Boltzmann transport equation. Hybrid particle/flux simulation techniques should be explored. The tools must be capable of simulating transport in both solid and liquid state. Finally, novel, unconventional algorithms should be defined wit the goal of reducing the simulation time by two orders of magnitude. If achieving this goal implies the introduction of specialized computer architectures to execute effectively such algorithms, so be it.

4.3.3 Circuit and local interconnect

Three main challenges are related to this layer of CAD tools: 1) defining a level of abstraction capable of efficiently representing an extremely diverse set of circuit components with a unified

set of parameters, and 2) building interconnect models that account for the transfer of many quantities other than electrical charge (energy, spin, heat, light, ions, etc.) through active interfaces between classical and quantum-mechanical systems; finally, 3) techniques for nonlocal parameter sets must be devised in order to explicitly relate the functionality of many individual components of the system.

4.3.4 Switch and Global interconnect

A proposed approach must provide an adequate level of abstraction in order to relate effectively with other tools in the simulation hierarchy illustrated above.

4.4 Strategies and mechanisms to address the challenges

The strategy addressing the challenges indicated above is defined by the metrics used to quantify the success of a CAD tool. In particular, the effectiveness of a newly proposed modeling/simulation approach should be measured with two main metrics: 1) how well such approach is integrated in the CAD hierarchy defined above; and 2) how well such approach reproduces and predicts some of the components, subsystems, or full systems of interest, including their environment.
The first metrics will estimate the level of abstraction of the model, effectively determining its level of conceptual robustness. We do not envision an individual cad tool as a multi-purpose "black box" that does everything in an acceptable way. At the contrary, each tool can be as specialized as needed, but it must be effectively integrated in the CAD hierarchy in such a way that it can be coupled with or replaced by more capable tools at any time.

The second metric is obviously also needed, even if is more traditional: it defines the quality of a tool in terms of how well it performs its function, rather on its level of integration in the hierarchical CAD structure.

4.5 Schematic Summary

4.5.1 State of the art

1. Two problems: methodology and robustness (applicability) of current CAD tools
2. Physic-based tool development is done for ad-hoc, non general, applications
3. CAD tools are optimized for charge-based solid-state systems
4. Abstraction is not adequate to address emerging (diverging) technology
5. Interfaces and interconnects will play an increasing role
6. Compact models are efficient but too empirical
7. Cyberinfrastructure is funded, CAD software development is not

4.5.2 Research Challenges: Methodology

1. Define a hierarchical (layered) scheme for CAD tool development
2. Define adequate abstraction for each layer of the hierarchy
3. Increase feedback between layers

4.5.3 Research Challenges: Tools

1. Ab-initio: defining promising state-of-the-art models
2. Transport and Device simulation: improving algorithmic efficiency 100 times
3. Circuit: including electro-thermal, soft and liquid state, interconnects, nonlocal parameters
4. Switch: provide an adequate level of abstraction in order to relate effectively with other tools in the simulation hierarchy

4.5.4 Strategy: Define Metrics for the CAD tool hierarchy

1. Level of abstraction of each model in the hierarchy
2. Level of integration of each model within the hierarchy
3. Modeling capabilities of each model in the hierarchy

5. Management of Uncertainty and Defects in Quantum Devices: Understanding the Design Space for Computing in an Uncertain World

Breakout Session Participants and Report Contributors

André DeHon (Vice Chair)	University of Pennsylvania	andre@acm.org
Wei Lu	University of Michigan	wluee@eecs.umich.edu
Kathleen Meehan	Virginia Tech	kameehan@vt.edu
Kartik Mohanram	Rice University	kmran@rice.edu
John Savage (Chair)	Brown University	jes@cs.brown.edu
Sandeep Shukla	Virginia Tech	shukla@vt.edu
Lei Wang	University of Conneticut	leiwang@engr.uconn.edu

As electronics moves to the sub 50nm range and towards the scale of individual atoms, variations in and failures of components are expected to occur at much higher rates than is tolerable today. The challenge facing the research community is to determine under what conditions it will be possible and. ultimately beneficial, to build reliable computers using components which **must** sacrifice traditional device reliability and reproducibility for smaller size, lower energy, less expensive construction, or higher speed operation. We would like to know what tradeoffs are possible among area, energy (power), delay, and reliability. We would also like to have a catalog of methods that can be used at a variety of levels of component reliability, providing system reliability with minimum overhead in key cost metrics (energy, area, delay). Progress will follow with minimum parameterization of reliability along several axes (e.g. magnitude of variation, failure rates, timescale for changes) and the development of a theory and practice for addressing uncertainly and unreliability across this parameterized design space. The education of a cadre of students with the broad knowledge to reach across the many different technological domains and traditional abstraction levels will play an essential role in reliable engineering computation at the nanoscale.

5.1 Introduction

Nanoelectronics, the development of materials, engineering methods, and analysis for electronics at the nanoscale, has led to many advances. These include improvements in CMOS technology, the introduction of new electronic materials with superior properties (e.g., higher mobility, higher conductance, higher and lower dielectric constants, lower energy, nonvolatility), new approaches to their use (e.g., new state-variables), and new method of assembling and analyzing them. Quantum dot systems, single-electron transistors, spin-based devices, nanowire crossbars, carbon nanotubes-based transistors and interconnects, and molecular devices have been introduced.

As CMOS technology rapidly moves to feature sizes below 50nm and new nanoscale technologies are introduced, new issues arise. It is unclear whether the new issues, including reliability, will prevent the semiconductor industry from using smaller conventional devices and the new nanotechnology-enabled technologies. However, it is clear that industry's options will be constrained if the maintain the current paradigm of demanding perfect (or near-perfect) and

identical devices. It is incumbent upon the research community to explore the challenges and opportunities introduced by these technologies and show how new paradigms might allow us to extract new benefits from these different and less reliable technologies.

Our group was charged with exploring the "management of uncertainties and processing induced effects". We interpreted this charge to mean that we should explore the design space for computing under uncertainty. We began by reviewing the uncertainties raised in the talks given at the workshop. These are outlined below. We then outlined our responses, which are detained in subsequent sections.

5.1.1 Uncertainties in Nanoelectronics

1. DNA self-assembly has the potential to provide templates for assembly of nanoelectronics. Errors in self-assembly of DNA strands (e.g., mismatch pairing of bases) occur at a high rate.

2. Molecular electronic devices have been investigated for use as transistors and storage media. An important challenge is to minimize the variation in performance when assembling these devices.

3. As CMOS circuit performance improves, that is, as mean voltages, channel lengths, and oxide thicknesses decline, the standard deviation in all parameters, such as dopant levels, line-edge roughness, oxide thickness, chip speed, and power dissipation increases. Similarly, defects and cost increase as yield decreases. It has become increasingly difficult to build accurate CAD tools for circuit simulation. Coping with failures is just now emerging as an area of concern.

4. Conventional extrapolations of the limits of electron-based computation assume that all the gates in a component must function perfectly for years; if we could relax this assumption, we may be able to drive greater reductions in energy per device and greater levels of nanoscale integration.

5.2 Scientific Challenges and Opportunities

The feature size, λ, of CMOS technologies is decreasing at a steady pace. As λ decreases, device variation and component failure rates increase. Continued scaling depends on economical solutions, which tolerate this failure and variation.

Understanding of tradeoffs between reliability and the size and energy consumption of gates will also benefit the device community. Rather than simply rejecting devices, which may have many beneficial properties (e.g. higher-speed, lower-energy, smaller size) but are inherently less reliable or exhibit higher variation, they can assess if the benefits outweigh the costs. For example, if a novel device is half the size of a conventional device, but increases defect rates from 10^{-9} to 10^{-6}, what is the overhead cost of mitigating against the higher defect rate? If the cost is a factor of 3 with no concomitant decrease in area and power, then this will not be a net benefit. However, if this higher defect rate can be accommodated with only 10% area overhead, say, it will be a net improvement.

While much work has been done on brute-force solutions for reliability (e.g., replication of gates [1], components (e.g., spare cores), or systems (e.g., DNS, Web Servers, quint-redundant (5 copies) flight systems), these conventional fault-tolerance systems spend integer factors of overhead (e.g., >3 for TMR systems, extending to many orders of magnitude for von Neumann-style gate-level redundancy at high fault rates). Even these systems typically deal with relatively low failure rates. Is it possible to tolerate even higher failure rates with more modest (say tens of percent) overhead?

Several opportunities exist that may offer these kinds of economical mitigation, but significant work remains to map out the design space and provide clear guidance on achievable overheads.

- **Reconfiguration** – When component failure is persistent, it is possible to reconfigure around the faulty devices; reconfiguration overheads can be in the few percent range.

- **Differential Reliability** – Selective use of a small number of large, reliable, and area-consuming gates together with a large number of small, less reliable, and area-efficient gates appears to be a promising approach to get beyond the von Neumann-Pippenger limits on failure rates and overheads [1,2]. Differential reliability is used today, if not fully appreciated. It is employed in DRMA memories, where memory cells are much less reliable than the CMOS circuitry used in error-correcting circuits, as well as in disk farms. It is also used in strategic locations in error-critical circuits. The widespread adoption of differential reliability will be a necessity as the reliability of devices decreases.

- **Coding Solution** – For data storage, there is a well-developed theory for error-correcting codes where we can spend a modest amount of overhead to tolerate a large number of errors. Good codes are much more efficient than simple replication. Questions remain as to how well this kind of technique can protect the hardware itself, though there are theoretical results, which suggest that it is possible [3]. In any case, the fact that we can protect memory and computation inexpensively gives us a powerful technique for engineering reliable computations.

- **Checking versus Computation** – Computational theory has identified many cases where we believe that checking the correctness of a computation may be much cheaper than performing the computation (e.g., P vs. NP). This suggests that we may be able to place unreliable computations inside a smaller, reliable control loop that validates the result of the unreliable computation.

This illustrative set of ideas suggests that there are opportunities to de better. We expect continued emphasis on lightweight techniques to tolerate uncertainty will generate additional approaches to extend this list.

5.3 Quantitative Characterization

Coping with unreliable components efficiently requires that we quantify reliability characteristics, identify the techniques appropriate to a particular kind of unreliability, and ultimately understand

how low we can drive the overhead necessary to address a particular quantified level of unreliability.

Key axes in the quantifying unreliability include:

- time-scale over which failure persists or over which changes occur in device parameters (e.g., permanent, single-cycle transients, aging that occurs over years, temperature effects that persist for milliseconds),
- rate at which failures occur – ideally, we would like to understand the error rate as a function of costs (where cost might be area, energy, or number of masks),
- correlation of failures (random vs. bursty, spatial and temporal correlations), and
- magnitude of variations (e.g., variance in device parameters, variance of electrons transferred from cycle-to-cycle).

Ideally, we would like to understand how a particular level of quantified unreliability will impact system-level observables. The system-level observables include:

- energy for computation,
- area of implementation,
- delay (throughput, latency),
- performance variability (average vs. worst-case performance), and
- computation time or complexity of mitigating failures (e.g., up=front time willing to spend mapping device characteristics).

Event without reliability, there is a rich space with tradeoffs among these observables. We need to extend our understanding of the trade space to include various kinds and levels of unreliability.

5.4 Theory and Practice

We need to develop both the theory and practice of computation in the face of unreliable components. By analogy with Information Theory, we need to develop theory that will tell us the limits of achievable overhead at a given unreliability level; these will likely to be stated in terms of tradeoffs between area, quality of solutions, and the effort required to map problems to failure-tolerant architectures (like Shannon's rate-distortion limits or Hamming's sphere-packing bound). We also need to develop a practical body of tools and techniques that get us within quantifiable bounds of the theoretical limits (continuing the Information Theory analogy, Hamming and LDPC codes are practical codes available for use, which approach the identified theoretical bounds). Von Neumann, Pippenger, and others [1, 2, 4] give us bounds for random transient faults using homogeneous, uncoded computations, which is a good start. However, as identified in the previous sections there are many dimensions to characterizing unreliability and

there are many approaches, which give us opportunities to step outside of the original von Neumann model.

A catalog is needed of both existing methods (i.e., design patterns) to handle fault tolerance (e.g., simple replication methods, feed-forward voting, checking circuits, detection and rollback, and codes for one-side errors, such as Berger codes) as well as the emerging techniques. The catalog should also include known special-case techniques and a characterization of their domain of applicability. We need to characterize what parts of the quantified reliability space each technique addresses, and how techniques can be combined to develop complete reliability solutions. New special case and general methods for controlling failures then need to be developed. These may either be elaborations or combinations of existing methods ore new methods based on new ideas.

A key element to understand is how to combine complementary techniques across abstraction levels (e.g., device, gage, microarchitecture, architecture, operation system programming language algorithms, and applications). Models for the effect of failure control at one level in a systems hierarchy are needed so that development of failure control methods at higher level if possible, and so it is possible to perform cross-level engineering.

5.5 From Device to System Level

Success with many of the techniques suggested above in a high failure-rate environment will require rethinking abstractions and models that are currently in use. Design must take into account that occasional failures at one level in a systems hierarchy may be more efficiently handles by applying failure control techniques at the next higher level rather than attempting to squeeze out all failures at the lower level. This is illustrated by failures that are masked by the incoming data and those that produce easily detected catastrophic errors. In both cases, failures can be efficiently handled at the next higher level.

The range of interacting solutions that can be envisioned at multiple levels in an architectural hierarchy is large. Consequently, all level s in the hierarchy can be productively explored. Further, this demands collaboration between the experts at each level. The system designer must help the device scientists understand the system-level impact of deice parameters, and the device scientist must help the system designer understand the tradeoffs available at the device level. Reliability quantification, characterized design space, and the catalog of design options are all tools to help enrich and facilitate the communication.

5.6 Education Programs

The spectrum of problems to be explored form the device to the systems level is very large. To be successful in this area requires a broad range of knowledge, including an understanding of electronics, quantum mechanics, computer architecture, computer systems design, coding theory and tradeoff results in the theory of computation such as those for area and tie on VLSI chips. This requires a broader education that is currently afforded by traditional undergraduate degree programs in electrical engineering or computer science.

5.7 Research Targets

Below we propose four research targets.

1. Nanoscale device research to produce parameterized reliability models for wires and devices assembled using traditional and non-traditional methods. Architectural and systems-level research to identify and characterize fault models

2. Theoretical research to understand the limits of the feasible reliability-capacity design envelope. Important area for theoretical expansion and exploration include exploitation of differential redundancy, differential complexity between computation and checking, and coding.

3. Practical research to place existing techniques within the reliability-capacity space and develop new techniques or combination of techniques, which close the gaps in the space.

4. Strategic collaborative research to redefine the abstraction boundaries from devices to systems to better accommodate the high fault rates. This includes cross-disciplinary education to better allow device scientists and system-level engineers to communication on tradeoffs and to create the next generation of engineers who can navigate in this broader design space where reliability is a parameter rather than an absolute.

5.8 Conclusions

The emergence of nanoelectronics introduces a new concern, namely, coping with a wide range of variation in systems parameters and a concomitant increase in failure rates. Success in this regime requires a) a solid characterization of failure types, b) reflections of those failures to system behavior and achievable system performance, c) new methods of failure managements, d) new paradigms and abstractions to accommodate these failures, and e-The development of both a theory and practice of computing in an uncertain world.

5.9 References

[1] John Von Neumann. Probabilistic logics and the synthesis of reliable organisms from unreliable components. In C.E. Shannon and J. McCarthy, editors, *Automata Studies*, pages 43-98, 1956.

[2] Nicholas Pippenger. On networks of noisy gates. In *Procs. 26th IEEE FOCS Symposium*, pages 30-38, 1985.

[3] Daniel A. Spielman. Highly fault-tolerant parallel computation. In *Procs. 37th IEEE FOCS Symposium*, pages 154-163, 1996.

[4] Nicholas Pippenger. Developments in 'the synthesis of reliable organisms from unreliable components'. In *Proceedings of the Symposia of Pure Mathematics*, volume 50, pages 311-324, 1990.

6. General Concerns for the Emerging Models and Technologies for Computation Program

The members of the DNA-Based and Molecular Electronics breakout session also addressed the questions on the need for the EMT Program and recommendations to stimulate and strengthen interdisciplinary research in nanoelectronics.

6.1 Where is the computation?

An important question regarding the EMT program, from the point of view of the CISE directorate is "There are many materials and fabrication issues involved in the EMT effort, but what role does computation play in EMT?" For DNA assembly, computation is central both to algorithmic self-assembly and to the efforts to create compiler-like design tools for self-assembled DNA structures (see Section 2.2, E.W., P.R., C.D.). In molecular electronics, computation will play an important role in the creation of new fault tolerant "device architectures" for molecular devices. (C.D. notes not to be confused with "computer architecture".) It is important to examine these issues at a theoretical level for different device models and models of fabrication and operating errors, before multiple device structures have been built in the lab- theoretical results may inform the choice of experiments that we make and device architectures that we try.

6.2 Why keep the EMT program?

At the Nanoelectronics workshop, it was disclosed that the future of the EMT program was uncertain – that in a possible reclustering of CCF program clusters, the EMT program might be merged with a larger cluster or fragmented into smaller disconnected programs. Even though the EMT program cluster (nanoelectronics, bio-computation, and quantum computation) has significant overlaps with other CCF programs, several participants voice the opinion that the EMT program cluster should remain as it is, a distinct effort in emerging technologies. Funding emerging technologies for a distinct EMT program means that during a review panel, reviewers will focus on the promise of a proposal as a novel, emerging technology and may make allowances for the immaturity of techniques or high risk. If emerging technology proposals that would go to EMT go to other program clusters, then the proposals may be judged against established, low-risk research in that cluster and may not get funded.

Another supporting view is that "now is exactly the right time to be focusing on and funding emerging technologies". It is an exciting time in nanoelectronics – if one takes as a goal that we are trying to find a technology to complement or augment CMOS in the tasks of performing large scale computation, then among competing technologies there is not clear winner for what the devices will be (silicon nanowires, carbon nanotubes, gold nanocrystals, etc), what their mechanism of operation will be (molecular electronics, nanophotonics, etc.), or what fabrication method will be used (DNA-guided self-assembly, nanoimprint lithography, etc.). It seems that a good approach would be that we "diversify our portfolio" and place lots of small bets – exactly what the EMT program was intended to do (B.W., P.R.). An analogy was drawn with the energy industry for which we have no idea which technology is most promising (solar, new nuclear, biofuel, etc.) and it is the wrong time to solidify efforts behind any one technology at this point.

These diverse technologies and approaches should fall under the single umbrella of MET because of the potential for synergy between them. For example, as has been noted above, there is synergy between the bio-computation track of the EMT program and both the nanoelectronics and quantum information tracks of the EMT program because DNA self-assembly are being used to attempt to create both nanoelectronic circuits and quantum computers (section 2.2.2).

6.3 On promoting interdisciplinary research

Both DNA and molecular electronic researchers in the session agreed that their particular research programs are highly interdisciplinary and need explicit support for the special difficulties that arise in interdisciplinary research. They noted that there were difficulties in getting scientists to speak the same language across disciplines and that it was difficult to transfer knowledge about theoretical and experimental techniques. More specifically, the molecular electronics researchers desired increased interaction between theorist and experimentalist. The DNA researchers desired mechanisms of dispersal of DNA technology to those who could use it for interesting nanoelectronic, physical, material, or biological applications.

The members had three suggestions for strategies to improve the situation:

1. **Supplemental grant support for student exchange programs so that students from one lab can go to another lab and learn a critical piece of technology**. It was noted that this is a slow, serial method for cross-fertilization.

2. **Intense, "boot camp"-style summer schools for, say, three weeks in which the techniques of a field are transferred to all attendees**. This has the benefit that no formal ties need to be forged between labs – the school can operate on a service model and, at the end of the three weeks, people can go home and the are not collaborators. This model has benefits of scale over the student exchange method. The idea is that scientists at all stages from graduate student to PI could participate in the courses. Such a course can provide a mechanism for a PI to switch direction or a lab to take on a field that is totally new to them. Models for this type of program include the courses at Cold Spring Harbor Lab (http://meetings.cshl,edu/courses.html) or the Computing Beyond Silicon Summer School organized at Caltech by E.W. and Nanoelectronics workshop participant André DeHon (andre@acm.org, http://www.cs.caltech.edu/cbsss/schedule/reading.html).

3. **Short, interdisciplinary conferences with speakers drawn from the EMT program at which sort tutorials or high level lectures could allow a scientist to get a taste of a field before committing to deeper involvement**. This type of conference could help scientist learn the language of another discipline, and serve as a mixing place of ideas (I.O.). It would also serve to build the EMT community. (A related and very easy step for building the EMT community could be to prepare a .pdf booklet of abstracts for every proposal funded each year and circulate this to participants so that the EMT PIs in one area get an idea of what other EMT PIs in others are doing.)

6.4 On the size of interdisciplinary teams

Several researchers expressed the idea that they would like calls for interdisciplinary proposals to emphasize small (2-3) investigator teams rather than large 5-10 or more investigator teams (P.R., T.B., E.W.). Clearly, large team grants have their place, when the resources of large teams are required, to establish a new field or for departmental training grants within a single school. However, large team proposals sometimes bring together a constellation of ideas that are only peripherally related, and any strong interdisciplinary research that is accomplished by the teams is attributable to strong and deep pairwise relationships between investigators on the teams. Attempting to make a large team grant appear coherent and then to actually have a coherent theme during its life are difficult challenges and may push researchers to compromise their research interests and research quality to fit into a greater whole. A suggestion is that interdisciplinary calls offer more, smaller awards that would be appropriate for smaller teams.

Also, the question was raised, "What would the source of the many-investigator team trend for interdisciplinary teams?" and there was the suggestion that it may have, in part, come from the scientists themselves (M.B.) – it is an interesting question whether a trend to large teams is driven by the needs of the science, the funding climate, or other factors.

Appendix A

Workshop Participants and Attendees

Petru Andrei
Department of Electrical and Computer Engineering
FAMU-FSU
2525 Pottsdamer St.
Tallahassee, FL 32310
Phone: (850) 410-6589
Email: pandrei@eng.fsu.edu
Webpage: http://www.eng.fsu.edu/~pandrei/

Supriyo Bandyopadhyay
Room 238
Department of Electrical Engineering
Virginia Commonwealth University
601 W. Main Street
Richmond, VA 23284
Phone: (804) 827-6275
Email: sbandy@vcu.edu
Webpage:
http://www.people.vcu.edu/~sbandy/bandy_index1.html

Mitra Basu
Visiting Professor Computer Science Department
Johns Hopkins University
Baltimore, MD 21218
Email: basu@cs.jhu.edu

Sankar Basu
Program Manager
Foundations of Computing Processes and Artifacts
Foundations of Data and Visual Analytics
National Science Foundation
4201 Wilson Boulevard
Arlington, Virginia VA 22230, USA
Phone: 703-292-7843
Email : sabasu@nsf.gov

Chagaan Bataar
Office of Naval Research

Thomas Beck
Department of Chemistry
University of Cincinnati
404 Crosley Tower
PO Box 210172
Cincinnati, Ohio 45221-0172
Phone: 513-556-4886
Email: thomas.beck@uc.edu
Webpage: http://bessie.che.uc.edu/tlb/

Paul Bergstrom
Department of Electrical and Computer Engineering
Michigan Technological University
1400 Townsend Drive, Houghton, Michigan 49931
Main Office Room 121 EERC Building 906-487-2550
Phone: 906-487-2058

Yu Cao
Department of Electrical Engineering
Ira A. Fulton School of Engineering
P.O. Box 9309
Brickyard 6th Floor
Arizona State University
Tempe, AZ 85287-9309
Phone: (480) 965-1472
Email: ycao@asu.edu

Email: paulb@mtu.edu
Webpage:
http://www.ece.mtu.edu/faculty/paulb/Site/Dr._Bergstroms_Homepage_%40_MTU_ECE.html

Webpage: http://www.eas.asu.edu/~ycao/

Almaden Y. Chtchelkanova
Program Director
Division of Computing and Communication Foundation
National Science Foundation
4201 Wilson Boulevard
Arlington, Virginia VA 22230, USA
Phone: 703-292-8910
Email: achtchel@nsf.gov

Larry Cooper
Department of Electrical Engineering
Department of Electrical Engineering
Ira A. Fulton School of Engineering
P.O. Box 9309
Brickyard 6th Floor
Arizona State University
Tempe, AZ 85287-9309
Phone: 480-965-1795
Email: larry.cooper@asu.edu

Shamik Das
MITRE-Washington
7515 Colshire Drive
McLean, VA 22102-7539
Phone: (703) 983-6000
Email: sdas@mitre.org
Webpage:
http://www.mitre.org/tech/nanotech/ourwork/staff.html

André DeHon
Department of Electrical and Systems Engineering
University of Pennsylvania
200 South 33rd Street
Philadelphia, PA 19104
Phone : 215-898-9241
Email: andre@seas.upenn.edu
Webpage: http://www.seas.upenn.edu/~andre/

Chris Dwyer
Department of Electrical & Computer Engineering,
Department of Computer Science.
Duke University
Box 90291
Durham, NC 27708
Phone: (919) 660-5275
Email: dwyer@ece.duke.edu
Webpage: http://www.ece.duke.edu/~dwyer

James Ellenbogen
MITRE-Washington
7515 Colshire Drive
McLean, VA 22102-7539
Phone: (703) 983-6000
Email: ellenbgn@mitre.org
Webpage:
http://www.mitre.org/tech/nanotech/ourwork/staff.html

Michael Foster
Division Director, CCF
National Science Foundation
4201 Wilson Boulevard
Arlington, Virginia VA 22230, USA
Phone: 703-292-8910
Email: mfoster@nsf.gov

Paul Franzon
Department of Electrical and Computer Engineering
North Carolina State University
P.O. Box 7914
Raleigh, NC 27695
Phone: 919-515-7351
Email: paulf@ncsu.edu

Webpage:
http://www.ece.ncsu.edu/erl/faculty/paulf.html

Avik Ghosh
Department of Electrical and Computer Engineering
University of Virginia
351 McCormick Road
PO Box 400743
Charlottesville, VA 22904-4743
Phone: 434-924-8818
Email: ag7rq@virginia.edu
Webpage: http://people.virginia.edu/~ag7rq/

Lawrence Goldberg
Senior Engineering Advisor
Division of Electrical, Communication and Cyber Systems, Directorate for Engineering
National Science Foundation
4201 Wilson Boulevard
Arlington, Virginia VA 22230, USA
Phone: 703-292-8339
Email: lgoldber@nsf.gov

Jing Guo
Department of Electrical and Computer Engineering
NEB 551
P. O. Box 116130
University of Florida
Gainesville, FL, 32611-6130
Phone: 352-392-0940
Email: guoj@ece.ufl.edu
Webpage: http://www.guo.ece.ufl.edu/

James Heath
Department of Chemistry
MC 127-72
California Institute of Technology
1200 East California Blvd.
Pasadena, CA 91125
Phone: 626-395-6079
Email: heath@caltech.edu
Webpage:
http://www.its.caltech.edu/~heathgrp/index.htm

Steven Hillenius
Vice President
Semiconductor Research Corporation
P.O. Box 12053
Research Triangle Park, NC 27709-2053
Phone: (919) 941-9400
Email: Steve.Hillenius@src.org
Webpage:
http://www.src.org/member/about/stevenjhillenius.asp

Niraj Jha
Department of Electrical Engineering
Princeton University
Princeton, NJ 08544
Phone : 609-258-4754
Email : jha@ee.princeton.edu
Webpage: http://www.princeton.edu/~jha/

Rajinder Khosla
Program Director
Active Nanostructures and Nanosystems Electronics, Photonics & Device Technologies
National Science Foundation
4201 Wilson Boulevard
Arlington, Virginia VA 22230, USA

James Klemic
MITRE-Washington
7515 Colshire Drive
McLean, VA 22102-7539
Phone: (703) 983-6000
Email: jklemic@mitre.org
Webpage:
http://www.mitre.org/tech/nanotech/ourwork/

Phone: 703-292-8339
Email: rkhosla@nsf.gov

staff.html

Ernest Kuh
Department of Electrical Engineering and Computer Sciences
University of California at Berkeley
253 Cory Hall MC# 1770
Berkeley CA 94720-1770
Phone: (510) 642-2689
Email: kuh@eecs.berkeley.edu
Webpage:
http://www.eecs.berkeley.edu/~kuh/

Jo-Won Lee
Director
National Program for Tera-level Nanodevices
Korea
Email: jwlee@nanotech.re.kr
Webpage:
http://www.nanotech.re.kr/nanosoja/english/organization_offices.htm

Wei Lu
Electrical Engineering & Computer Science and Applied Physics
The University of Michigan
2405 EECS, 1301 Beal Ave
Ann Arbor, MI 48109-2122
Phone: 734-615-2306
Email: wluee@umich.edu
Webpage:
http://www.eecs.umich.edu/~wluee/

Mark Lundstrom
Purdue University
School of Electrical and Computer Engineering
465 Northwestern Ave.
West Lafayette, Indiana 47907-2035
Phone: 765-494-3515
Email: lundstro@purdue.edu
Webpage:
http://cobweb.ecn.purdue.edu/~lundstro/

Chengde Mao
Department of Chemistry
Purdue University
560 Oval Drive
West Lafayette, IN 47907-2084
Phone: 765-494-0498
Email: mao@purdue.edu
Webpage:
http://www.chem.purdue.edu/people/faculty/faculty.asp?itemID=46

Yehia Massoud
Departments of Electrical and Computer Engineering and Computer Science
2022 Duncan Hall
6100 Main Street, M.S. 380
Rice University
Houston, TX 77005
Phone: 713.348.6706
Email: massoud@rice.edu
Webpage: www.rand.rice.edu

Hiroshi Matsui
Department of Chemistry
Hunter College of CUNY
695 Park Avenue
New York, NY 10065
Phone: 212-650-3918
Email: hmatsui@hunter.cuny.edu
Webpage:
http://www.hunter.cuny.edu/chem/matsui.shtml

Pinaki Mazumder
Program Director
Emerging Models and Technologies
Division of Computing & Communications Foundations
Directorate for Computer & Information Science & Engineering
National Science Foundation
4201 Wilson Boulevard
Arlington, Virginia VA 22230, USA

Phone: 703-292-7898
Email: pmazumde@nsf.gov

Kathleen Meehan
Department of Electrical and Computer Engineering
M/C 0111
Virginia Tech
Blacksburg, VA 24061-0111
Phone: 540-231-4442
Email: kameehan@vt.edu
Webpage: www.ece.vt.edu/optical/

Kartik Mohanram
Department of Electrical and Computer Engineering
Rice University
3029 Duncan Hall
MS - 366 6100 Main Street
Houston, Texas
Phone: (713) 348 6712
Email: kmram@rice.edu
Webpage: http://www.ece.rice.edu/~kmram/

Saraju Mohanty
Department of Computer Science and Engineering
University of North Texas
P.O. Box 311366
Denton, TX 76203-1366
Phone: 940-565-3276
Email: smohanty@cse.unt.edu
Webpage: http://www.cs.unt.edu/~smohanty/

Vijay Narayanan
354D IST Building
Department of Computer Science and Engineering
Pennsylvania State University
University Park, PA 16802
Phone: (814)-863-0392
Email: vijay@cse.psu.edu
http://www.cse.psu.edu/~vijay/

Jun Ni
Department of Radiology
Carver College of Medicine
University of Iowa
Iowa City, IA 52242
Phone: 391-335-9490
Email: jun-ni@uiowa.edu
Webpage: http://www.uiowa.edu/mihpclab/

Michael Niemier
307 Cushing Hall
University of Notre Dame
Notre Dame, IN 46556
(574) 631-3858
Email: mniemier@nd.edu
Webpage: http://www.cse.nd.edu/~mniemier/

Ivan Oleynik
Department of Physics
University of South Florida
4202 East Fowler Avenue
Tampa, Florida 33620-5700
Phone: (813) 974-8186
E-mail : oleynik@shell.cas.usf.edu
Webpage : http://msl.cas.usf.edu

Nishant Patil
Department of Electrical Engineering
Stanford University
161 Packard Building
350 Serra Mall
Stanford, CA 94305-9505
Phone: (650) 723-393
Email: nppatil@stanford.edu

Carl Picconatto
MITRE-Washington
7515 Colshire Drive
McLean, VA 22102-7539

Gernot Pomrenke
Air Force Office of Scientific Research
Phone: 703-696-8426
Email: gernot.pomrenke@afosr.af.mil

Phone: (703) 983-6000
Email: picconatto@mitre.org
Webpage:
http://www.mitre.org/tech/nanotech/ourwork/staff.html

Eric Pop
2258 Micro and Nano Lab
208 North Wright Street
University of Illinois
Urbana IL 61801
Phone: 217-244-2070
Email: epop@uiuc.edu
Webpage: http://poplab.ece.uiuc.edu

Jan Rabaey
545E Cory Hall
University of California at Berkeley
Berkeley, CA 94720
Phone: 510-666-3102
Email: jan@eecs.berkeley.edu
Webpage:
http://bwrc.eecs.berkeley.edu/People/Faculty/jan/

Hassan Raza
Center for Nanoscale Systems
Cornell University
306 Phillips Hall
Ithaca, NY 14850
Phone: 607-255-2163
Email: hr89@cornell.edu
Webpage:
http://www.people.cornell.edu/pages/hr89/

Mark Reed
Becton Center
P.O. Box 208284
Yale University
New Haven, CT 06520
Phone: 203-432-4306
Email: mark.reed@yale.edu
Webpage: http://www.eng.yale.edu/reedlab/

Garrett Rose
Department of Electrical and Computer Engineering
Polytechnic University
Brooklyn, NY 11201 Phone: (718)260-3218
Email: grose@duke.poly.edu
Webpage:
http://www.poly.edu/faculty/rosegarrett/index.php

Paul Rothemund
Senior Research Fellow
Computer Science & CNS
MS 136-93
1200 E. California Boulevard
California Institute of Technology
Pasadena, CA 91125
Phone: 626-390-0438
Email: pwkr@dna.caltech.edu
Webpage:
http://www.dna.caltech.edu/~pwkr/

Rob Rutenbar
Carnegie Mellon University
5000 Forbes Avenue
Pittsburgh, PA 15213-3890
Phone: (412)-268-3334
Email: rutenbar@ece.cmu.edu
Webpage: http://www.ece.cmu.edu/~rutenbar/

Marco Saraniti
Department of Electrical Engineering
Ira A. Fulton School of Engineering
P.O. Box 9309
Brickyard 6th Floor
Arizona State University
Tempe, AZ 85287-9309
Phone: (480) 965-2650

Email: marco.saraniti@asu.edu

John Savage
Computer Science Department
Box 1910
Brown University
Providence, RI 02912
Phone: 401-863-7642
Email: jes@cs.brown.edu
Webpage: http://www.cs.brown.edu/~jes/

Alan Seabaugh
Department of Electrical Engineering
266 Fitzpatrick Hall
University of Notre Dame
Notre Dame, IN 46556-5637
Phone: 574-631-4473
Email: seabaugh.1@nd.edu
Webpage: http://www.nd.edu/~nano/

Ned Seeman
Department of Chemistry
New York University
New York, NY 10003
Phone: (212) 998-8395
Email: ned.seeman@nyu.edu
Webpage: http://seemanlab4.chem.nyu.edu/

Sandeep Shukla
Department of Electrical and Computer Engineering
M/C 0111
Virginia Tech
Blacksburg, VA 24061-0111
Phone: 540-231-2133
Email: shukla@vt.edu
Webpage:
http://fermat.ece.vt.edu/Fermatian_Info/sks.html

Jyuo-Min Shyu
Dean
College of Electrical Engineering and Computer Science (EECS)
National Tsing Hua Univsersity (NTHU)
101, Section 2 Kuang Fu Road
Hsinchu Taiwan, 3005, ROC
Phone: +886-3-5742896
Email: shyu@cs.nthu.edu.tw
Webpage:
http://www.eecs.nthu.edu.tw/english/people/people.htm

Mircea Stan
Department of Electrical and Computer Engineering
Thornton Hall
University of Virginia
351 McCormick Road
PO Box 400743
Charlottesville, VA 22904-4743
Phone: (434) 924-3503
Email: mircea@virginia.edu
Webpage:
http://www.ee.virginia.edu/~mrs8n/

Milan Stojanovic
Division of Nephrology
Columbia University
22 W 168th Street
4th Floor
PH4124
New York, New York 10032
Phone: 212-305-1890
Email: mns18@columbia.edu
Webpage:

Ulrich Strom
Executive Officer
National Science Foundation
4201 Wilson Boulevard
Arlington, Virginia VA 22230, USA
Phone: 703-292-4938
Email: ustrom@nsf.gov

http://www.cumc.columbia.edu/dept/medicine/BasicResearchers/Stojanovic.html

James Tour
Rice University
Smalley Institute for Nanoscale Science and Technology, MS222
6100 Main Street, Houston, Texas 77005
Phone: 713-348-6246
Email: tour@rice.edu
Webpage: http://www.jmtour.com

Dragica Vasileska
Department of Electrical Engineering
Ira A. Fulton School of Engineering
P.O. Box 9309
Brickyard 6th Floor
Arizona State University
Tempe, AZ 85287-9309
Phone: (480) 965-6651
Email: vasilesk@impa2.asu.edu
Webpage: http://www.eas.asu.edu/~vasilesk/

T.N. Vijaykumar
School of Electrical and Computer Engineering
Department of Computer Science
Purdue University
ECE/EE 465 Northwestern Avenue
West Lafayette, Indiana 47907-1285
Phone: (765) 494-0592
Email: vijay@ecn.purdue.edu
Webpage:
http://cobweb.ecn.purdue.edu/~vijay/

Kang Wang
University of California - Los Angeles
Engineering IV Building
Room 63-109
420 Westwood Plaza
Los Angeles, CA 90095-1594
Phone: 310-825-1609
Email: wang@ee.ucla.edu
Webpage: http://drl.ee.ucla.edu/

Lei Wang
Electrical & Computer Engineering
University of Connecticut
371 Fairfield Road U-2157
Storrs, CT 06269-2157, USA
Phone: 860-486-3066
Email: leiwang@engr.uconn.edu
Webpage:
http://www.engr.uconn.edu/~leiwang/

Paul Werbos
Program Manager
Emerging Frontiers in Research & Innovation
National Science Foundation
4201 Wilson Boulevard
Arlington, Virginia VA 22230, USA
Phone: 703-292-8339
Email: pwerbos@nsf.gov

Robert Westervelt
Division of Engineering and Applied Physics
Harvard University
Cambridge MA, 02138
Phone: (617) 495-3296
Email: westervelt@deas.harvard.edu
Webpage: http://meso.seas.harvard.edu/

Jacob White
Dept of Electrical Engineering & Computer Science
Massachusetts Institute of Technology
Room 36-817
77 Massachusetts Avenue
Cambridge, MA 02139
Phone: (617) 253-2543
Email: white@mit.edu
Webpage:

http://www.rle.mit.edu/cpg/people_faculty.htm

Brian Willis
Department of Chemical Engineering
University of Delaware
331 Colburn Laboratory
150 Academy Street
Newark, Delaware 19716
Phone: 302-831-6856
Email: bgwillis@udel.edu
Webpage:
http://www.che.udel.edu/directory/facultyprofile.html?id=7950

Erik Winfree
Computer Science
Computation and Neural Systems
California Institute of Technology
MS 136-93, Moore 204B
Pasadena, CA 91125 [USA]
Phone: (626) 395-6246
Email: winfree@caltech.edu
Webpage:
http://www.dna.caltech.edu/~winfree/

Jeannette Wing
Assistant Director
Computer & Information Science &
Engineering Phone: CISE-Directorate
National Science Foundation
4201 Wilson Boulevard
Arlington, Virginia VA 22230, USA
Phone: 703-292-8900
Email: jwing@nsf.gov

Yong Xu
Department of Electrical and Computer
Engineering
M/C 0111
Virginia Tech
Blacksburg, VA 24061-0111
Phone: 540-231-2464
Email: yong@vt.edu
Webpage:
http://www.ee.vt.edu/~photonics/Yongpage.html

Hao Yan
Department of Chemistry & Biochemistry
Biodesign Building A 120 FB
Mail Code 1604
Arizona State University
Tempe, AZ 85287
Phone: 480-727-8570
Email: Hao.Yan@asu.edu
Webpage :
https://sec.was.asu.edu/directory/person/734863

Chen Yang
Department of Chemistry
Purdue University
560 Oval Drive
West Lafayette, IN 47907-2084
Phone: 765-496-3346
Email: yang@purdue.edu
Webpage:
http://www.chem.purdue.edu/people/faculty/faculty.asp?itemID=81

Hongbin Yu
Arizona State University
Department of Electrical Engineering
Department of Electrical Engineering
Ira A. Fulton School of Engineering
P.O. Box 9309
Brickyard 6th Floor

Luping Yu
929 East 57th Street
GCIS E 419A
University of Chicago
Chicago, IL 60637
Phone: 773-702-0805
Email: lupingyu@uchicago.edu

Arizona State University
Tempe, AZ 85287-9309
Phone: (480) 965-4455
Email: yuhb@asu.edu
Webpage :
https://sec.was.asu.edu/directory/person/866744

Webpage:
http://chemistry.uchicago.edu/fac/yu.shtml

Mona Zaghloul
Department of Electrical and Computer Engineering
George Washington University
801 22nd Street NW
Suite 607
Washington DC 20052
Telephone: (202) 994-6083
Phone: 202 994-3772
Email: zaghloul@gwu.edu
Webpage:
http://www.ece.gwu.edu/people/mona.htm

Tong Zhang
Electrical, Computer and Systems Engineering Department
Rensselaer Polytechnic Institute
CII 6015 - CIE
110 8th St.
Troy, NY 12180
Phone: 518-276-2945
Email: tzhang@ecse.rpi.edu
Webpage:
http://www.ecse.rpi.edu/homepages/tzhang

Workshop on NSF Nanoelectronics:
Circuits, Systems, and CAD Tools

Program

Monday, October 15, 2007
Hilton Arlington Hotel Gallery 2

8:00 *Registration and refreshments*

8:20 – 8:35 **Jeannette Wing**
Assistant Director, Computer & Information Science and Engineering
Welcome from the CISE Directorate

8:35 – 8:45 **Michael J. Foster**
Division Director, Computing and Communication Foundations
Welcome from the CCF Division

8:45 – 8:55 **Lawrence Goldberg**
Welcome from the Engineering Directorate

8:55 – 9:05 **Ulrich Strom**
Executive Officer, Div. of Materials Research
Welcome from the MPS Directorate

9:05 – 9:25 **Pinaki Mazumder**
Program Director, Emerging Models and Technologies
Welcome from the EMT Program

Session 1. ***DNA Self-Assembly for Nanoelectronics***
Chair: **Prof. Ernest Kuh, University of California**

9:25 – 9:50 **Steven Hillenius**
Vice President, Semiconductor Research Corporation
Current Perspective and Future View of Nanoelectronics Research for the Semiconductor Industry

9:50 – 10:15 **Ned Seeman**
Margaret and Herman Sokol Professor of Chemistry, New York University
DNA: Not Merely the Secret of Life

10:15 – 10:40 **Paul Rothemund**
Senior Research Fellow, Department of Computer Science & CNS, California Institute of Technology
DNA Origami and Nanofabrication

10:40 – 11:00 **Erik Winfree**
Associate Professor of Computer Science, California Institute of Technology
Progress in Algorithmic Self-Assembly

11:00 – 11:10 *Coffee Break*

Session 2. ***Molecular Computing***
Chair: **Lawrence Goldberg, Program Director, NSF**

11:10 – 11:35 **Mark Reed**
Harold Hodgkinson Professor of Engineering and Applied Science, Yale University
The Next Frontier: Bioelectronic Interfaces

11:35 – 12:00 **James Tour**
Chao Professor of Chemistry and Professor of Computer Science and of Mechanical Engineering, Rice University
Silicon/Molecule Hybrid Devices

12:00 – 12:20 **Jyuo-Min Shyu**
Dean, College of Electrical Engineering and Computer Science, National Tsing Hua University, Taiwan
Nanotechnology Opportunities from a System Application Perspective

12 :20 – 12 :30 Break

12:30 – 1:30 Panel discussion on the future directions of research on Nanoelectronics at lunch (working);
Panel Moderator: **Michael Foster, CCF Division Director, NSF**

Session 3. ***Design Automation***
Chair: **Sankar Basu, Program Director, NSF**

1:30 – 2:00 **Ernest Kuh**
William S. Floyd, Jr. Professor Emeritus in Engineering and Professor in the Graduate School, University of California – Berkeley
Past, Present and Future of the EDA Research

2:00 – 2:25 **Jacob White**
Cecil H. Green Professor of Electrical Engineering and Computer Science, Massachusetts Institute of Technology
Design Tools for Emerging Technologies

2:25 – 2:50 **Rob Rutenbar**
Jatras Professor of Electrical and Computer Engineering, Carnegie Mellon University
Toward Tools for Emerging Nanoelectronics

2:50 – 3:10 **Mark Lundstrom**
Don and Carol Scifres Distinguished Professor of Electrical and Computer Engineering, Purdue University
CAD for Nanoelectronics: What's Needed and When

3:10 – 3:20 *Coffee Break*

Session 4 ***Nanosystems I***
Chair: **Almadena Chtchelkanova, Program Director, NSF**

3:20 – 3:50 *Talk withdrawn, speaker was unable to attend*
George Bourianoff
Senior program manager in the Strategic Research Group, Intel Corporation
Scientific Challenges Facing the Nanoelectronics Industry

3:50 – 4:15 **Robert Westervelt**
Mallinckrodt Professor of Applied Physics and Professor in the Division of Engineering and Applied Sciences, Harvard University
Future Devices

4:15 – 4:40 **Kang Wang**
Professor of Electrical Engineering and Director of the Functional Engineered Nano Architectonics (FENA) Focus Center, University of California at Los Angeles
Nanoelectronics Options -- From Nanodevices to Nanosystems

4:40 – 5:15 **Jan Rabaey**
Donald O. Pederson Distinguished Professor of Electrical Engineering and Computer Science, University of California – Berkeley
A System Perspectives on the Post-Silicon Era

5:15 – 5:40 **Jo-Won Lee**
Director of the National Program for Tera-level Nanodevices in Korea,
Efforts to Achieve Tera-Level Nanoelectronics in Korea

Rump Session
Room: Gallery Ballroom

7:30 – 10:00 *Poster Session*

7:30 – 9:00 Oral presentations

9:00 – 10:30 Panel Discussion on ***Multi-Scale Modeling***
Panel Chair: **Paul Werbos, Program Director, NSF**

9:00 – 9:05 **James Ellenbogen/Paul Werbos**
Introduction of Multi-Scale Modeling

9:05 – 9:25 **Avik Ghosh**
Assistant Professor of Electrical Engineering and Computer Science, University of Virginia
Multiscaling Non-equilibrium Properties: Coupling Current Flow at Interfaces

9:25 – 9:45 **Thomas Beck**
Professor of Chemistry, University of Cincinnati
Real-Space Multiscale Methods for Electronic Structure and Electron Transport

9:45 – 10:05 **Jun Ni**
Associate Professor of Radiology and Computer Science, University of Iowa
A Multi-scale Model for Simulations of Crystallization/Solidification in the Formation of Nanostructured Materials on Large-scale Parallel Computing Systems

10:05 – 10:25 **James Ellenbogen**
Senior Principal Scientist, Nanosystems Group, The MITRE Corporation
New Laws of Physics for the Multiscale Modeling of Materials and Nanoelectronic Systems: Application to the Bandgap Engineering of Molecular Devices

October 16, 2007
Hilton Arlington Hotel Ballroom

Session 5 ***Nanosystems II***
Chair: **Gernot Pomrenke, Program Manager, AFOSR**

8:00 – 8:20 *Refreshments*

8:20 – 8:50 **James Heath**
Elizabeth W. Gilloon Professor of Chemistry, California Institute of Technology
A Systems Approach to Molecular & Nanoelectronics

8:50 – 9:15 **John Savage**
Professor of Computer Science, Brown University
Nanowire Decoders

9:15 – 9:40 **Larry Cooper**
Research Scientist, Arizona State University
Another View of Nanoelectronics and its Applications

9:40 – 10:05 **Gernot Pomrenke**
Air Force Scientific Research Office
Nanophotonics and Silicon Photonics: Advancing chip-scale control of light

10:05 – 12:00 Oral Presentations with Poster Session

12:00 – 2:30 Breakout Session I (lunch will be provided)
Rooms: Ballroom, Renoir Room, Rembrandt Room
DNA-based and molecular electronics (Chair: Dr. P. Rothemund)
Evolutionary and revolutionary nanoarchitectures (Chair: Prof. A. Seabaugh)
CAD tools for nanoelectronics (Chair: Prof. J. Rabaey)
Management of uncertainties and processing induced defects (Chair: Prof. J. Savage)

2:30 – 3:00 *Coffee Break*

3:00 – 5:00 General discussion of the final document. The discussion will address the major challenges of research on nanoelectronics, its intellectual merits and broader impact. Means of improving and enhancing the cross-disciplinary collaboration will be discussed, as well as the areas where NSF and the EMT program in particular are making a major impact and what the scientific community expects from the NSF and

	the EMT program in the future. The first draft of the final document of the workshop will be prepared. The document will be finalized after the workshop and will be circulated among the participants.
5:00	Adjournment

Speakers for 10 minute oral presentations (in alphabetical order)

Supriyo Bandyopadhyay, Collective Computation with Self Assembled Quantum Dots, Nanowires and Nanodiodes/Single Spin Logic: Spin Based Computing with Organic Nanostructures

André DeHon, Paradigm Shifts for Computing with Nanoscale Electronics

Paul Franzon, Molecular and Nanodot Devices

Niraj Jha, NATURE: A Hybrid Nanotube/CMOS Dynamically Reconfigurable Architecture

Chende Mao, DNA nanostructures: Self-Assembly and Pattern Transfer

Subhasish Mitra, H-S Philip Wong, and Nishant Patil, Imperfection-Immune Computing Fabrics using Carbon Nanotubes

Vijay Narayanan, System Design Using Nanoelectronics: Opportunities and Challenges

Michael Niemier, Applications, Architectures, and Circuit Design for Nano-scale Magnetic Logic Devices

Ivan I. Oleynik, Theory and Modeling of Single Molecular Nanoelectronic Devices

Sandeep Shukla, Scalable Techniques for Reliability Evaluation for Defect-Tolerant Nano-Architectures

Mircea Stan, Challenges and Opportunities with Graphene-based Devices and Circuits

Milan Stojanovic, DNA Computing and Robotics

Lei Wang, Performance Limits of Molecular Electronic Computing

Hao Yan, Combinatorial Self-assembly of Nanocircuits on Addressable DNA Nanoscaffolds

Luping Yu, Molecular Diodes Based on Diblock Conjugated Oligomers

Hongbin Yu and Yu Cao, Self-Assembled Nanoscale Device: A New Paradigm for Nanoelectronics Design