EECS 498/598: Nanocircuits and Nanoarchitectures

Instructor: Prof. Pinaki Mazumder

Tuesday and Thursday @ 3:00 – 4:30 p.m.

Lecture 1: Introduction to Nanoelectronics

Fall 2006 **Prof. P. Mazumder**

EECS 498/598: Nanocircuits and Nanoarchitectures

Lecture 1: Introduction to Nanotelectronic Devices **(Sept. 5)**

Lectures 2: ITRS Nanoelectronics Road Map **(Sept 7)**

Lecture 3: Nanodevices; Guest Lecture by Prof. Lu **(Sept. 12)**

Lecture 4: Overview of Photonics Device; Guest Lecture by Prof. Ku **(Sept. 14)**

Lectures 5: Quantum Device Modeling for Nano-CAD **(Sept 19)**

Lectures 6-8: RTD-Based Digital Circuit Design **(Sept 21, 26, 28)**

Lectures 9-12: Class Presentations (ITRS) **(Sept. 30, Oct. 3, Oct. 5, Oct. 10)**

Lecture 13: Cellular Nonlinear Network Nanoarchitectures **(Oct 12)**

Lecture 14: Quantum-Dot Based Logic and Local Computational Models **(Oct 19)**

Lectures 15 & 16: Molecular Electronics Circuits **(Oct 24, Oct 26)**

Lectures 17-21: Class Presentations **(Oct. 31, Nov 2, Nov 7, Nov 9, Nov 14)**

Lecture 22: Nano Tube/Nano Wire Based Digital Logic Design **(Nov 16)**
Lectures 23 & 24: Quantum Cellular Array Based Logic Circuits **(Nov 21, Nov 28)**
Lectures 25: Miscellaneous Topics like Photonics, Plasmonics, Quantum Computing, etc. **(Nov 28)**
Lectures 26-29: Project Presentations **(Dec 1, Dec 5, Dec 7, Dec 12)**

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Lecture #1

How small is Nano? (A movie)
What is Nanotechnology?
What is Nanoelectronics?
What are Emerging Devices?
About the Course

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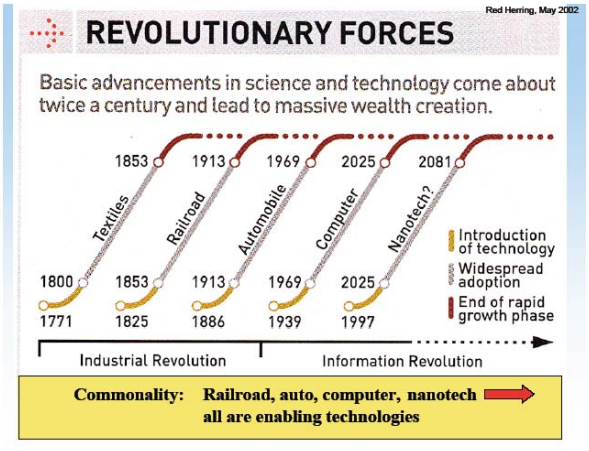
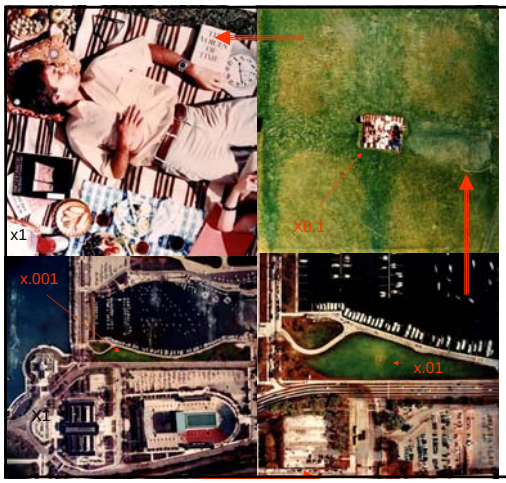
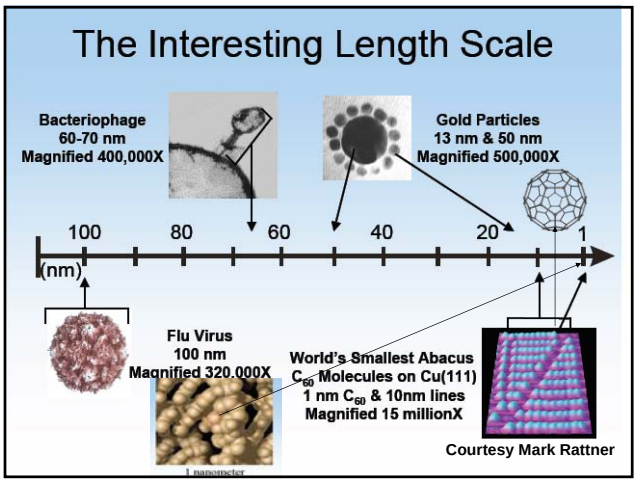
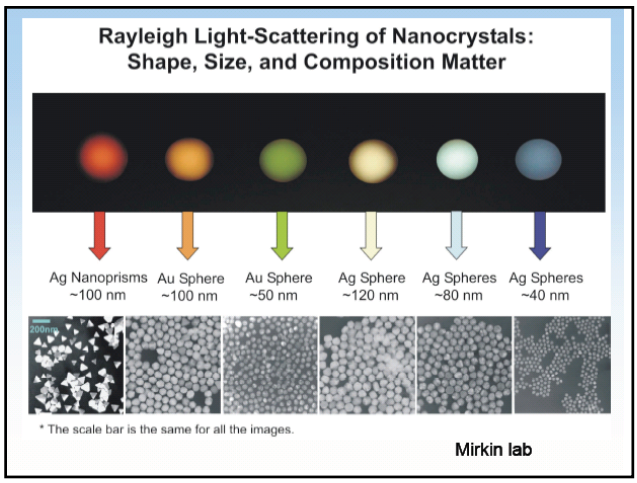




Power of 10

A sense of nanoscale





Definition of Nanotechnology

"Working at the atomic, molecular, super-molecular levels, in the length scale approximately **1-10** nm range, in order to understand and create materials, devices and systems with fundamentally new properties and functions because of their small structure" **--- Mike Roco, National Nanotechnology Initiative (NNI).**

However, Intel prefers the range from 1-100 nm so that conventional CMOS devices (< 90 nm) are part of Nanoelectronics Evolution.

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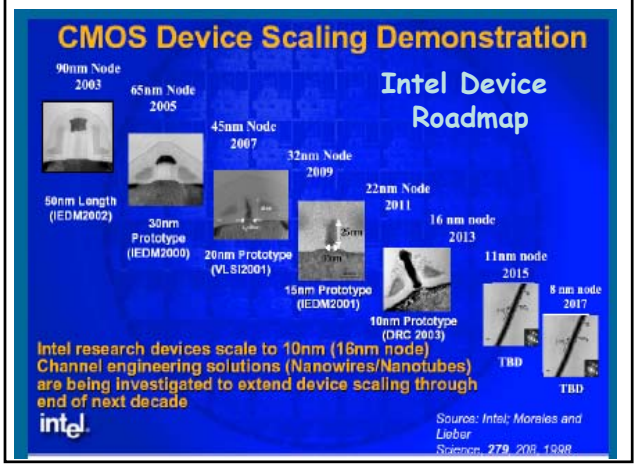
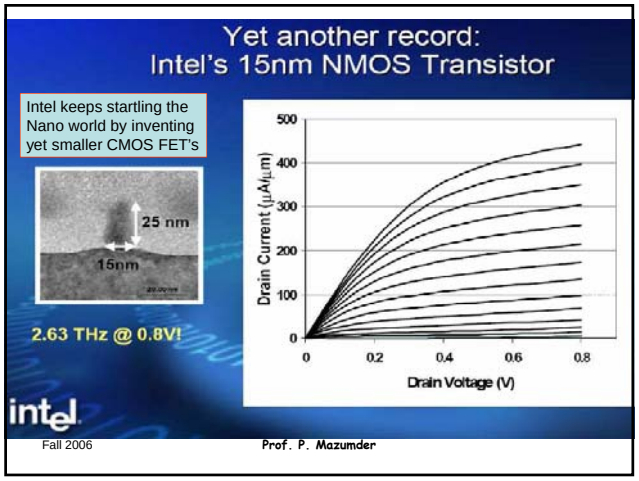
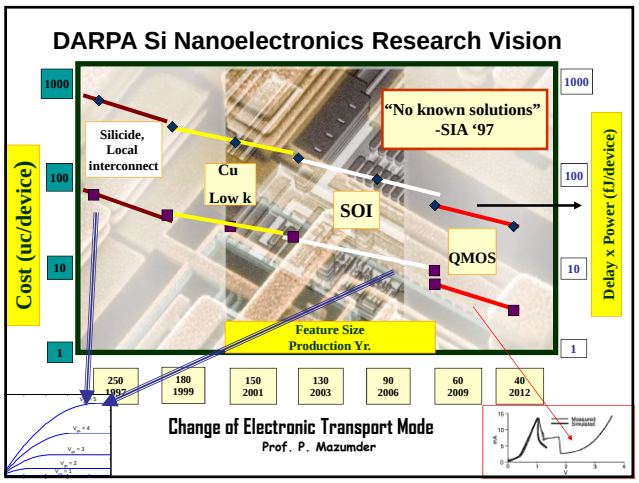
Multiple Perspectives of Roadmap for Nanoelectronics

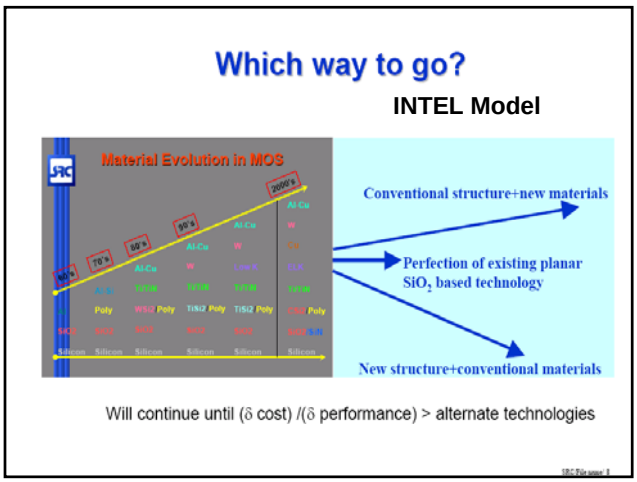
- Intel Perspective (shrinking driven) → Nano-scale CMOS, Nanowire FET, Carbon Nano Tube (CNT) FET
- Brick Wall Perspective → Post CMOS Devices in post-shrinking era
- Concurrent Advancements (ITRS Roadmap)
- Evolutionary v. Revolutionary Devices

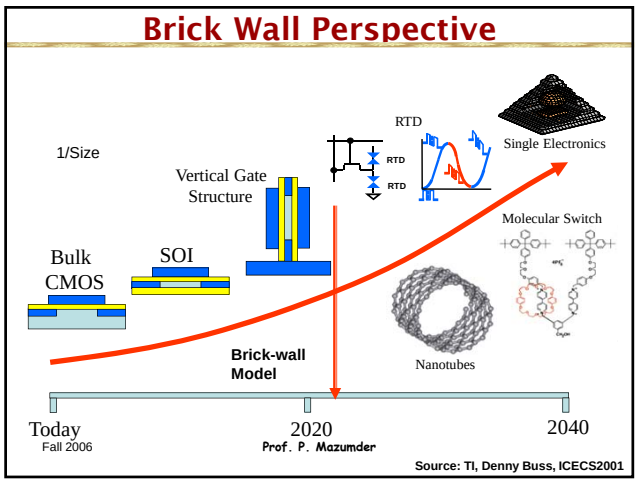


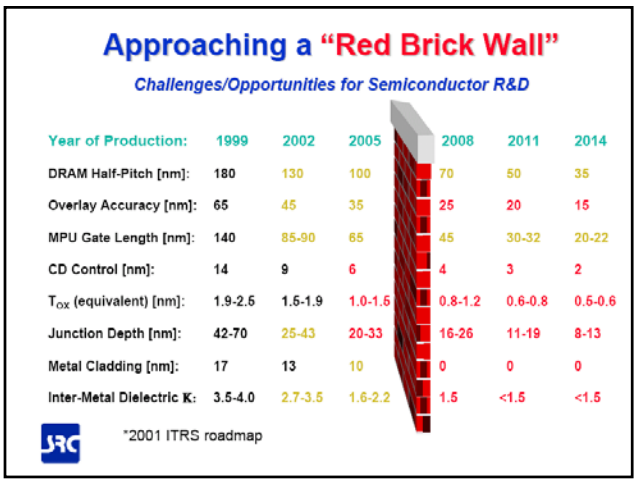


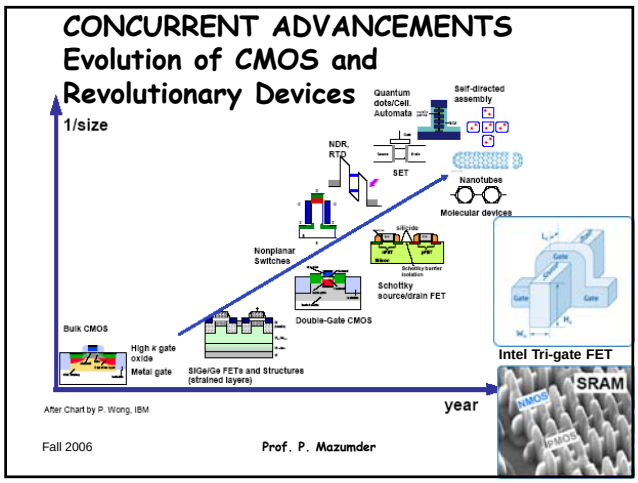
Extracted from a talk by Dr. David Tennenhouse (V.P. for Research, Intel Corporation) entitled "Three Challenges" at a joint CIA/DARPA conference on The Global Computer Industry Beyond Moore's Law


DARPA Si Nanoelectronics Research Vision
Cost (uc/device)
Delay x Power (fJ/device)
1000
100
10
1
"No known solutions"
-SIA '97
Silicide, Local interconnect
Cu
Low k
SOI
QMOS
Feature Size
Production Yr.
250 1997
180 1999
150 2001
130 2003
90 2006
60 2009
40 2012
Change of Electronic Transport Mode
Prof. P. Mazumder


Which way to go?
INTEL Model
Material Evolution in MOS
Conventional structure+new materials
Perfection of existing planar SiO2 based technology
New structure+conventional materials
Will continue until (δ cost) /(δ performance) > alternate technologies


Brick Wall Perspective
1/Size
Vertical Gate Structure
RTD
Single Electronics
Molecular Switch
Bulk CMOS
SOI
Nanotubes
Brick-wall Model
Today
Fall 2006
2020
2040
Prof. P. Mazumder
Source: TI, Denny Buss, ICECS2001


Approaching a "Red Brick Wall"
Challenges/Opportunities for Semiconductor R&D
Year of Production: 1999 2002 2005 2008 2011 2014
DRAM Half-Pitch [nm]: 180 130 100 70 50 35
Overlay Accuracy [nm]: 65 45 35 25 20 15
MPU Gate Length [nm]: 140 85-90 65 45 30-32 20-22
CD Control [nm]: 14 9 6 4 3 2
Tox (equivalent) [nm]: 1.9-2.5 1.5-1.9 1.0-1.5 0.8-1.2 0.6-0.8 0.5-0.6
Junction Depth [nm]: 42-70 25-43 20-33 16-26 11-19 8-13
Metal Cladding [nm]: 17 13 10 0 0 0
Inter-Metal Dielectric K: 3.5-4.0 2.7-3.5 1.6-2.2 1.5 <1.5 <1.5
*2001 ITRS roadmap


CONCURRENT ADVANCEMENTS
Evolution of CMOS and Revolutionary Devices
1/size
year
Quantum dots/Cell. Automata
Self-directed assembly
NDR, RTD
SET
Nanotubes
Molecular devices
Nonplanar Switches
Schottky source/drain FET
Double-Gate CMOS
Bulk CMOS
High κ gate oxide
Metal gate
SiGe/Ge FETs and Structures (strained layers)
Intel Tri-gate FET
SRAM
NMOS
PMOS
After Chart by P. Wong, IBM
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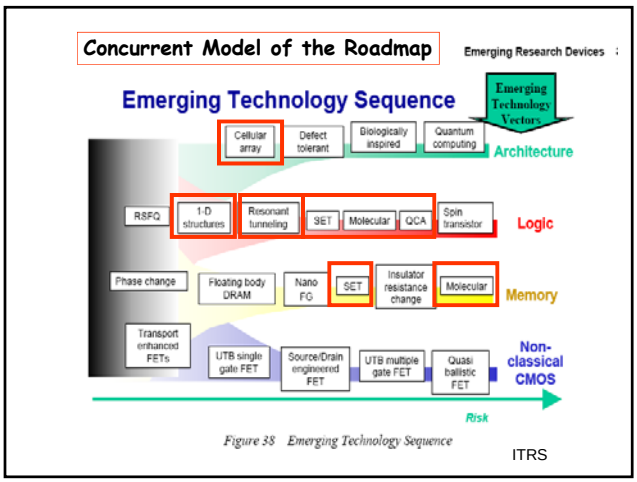
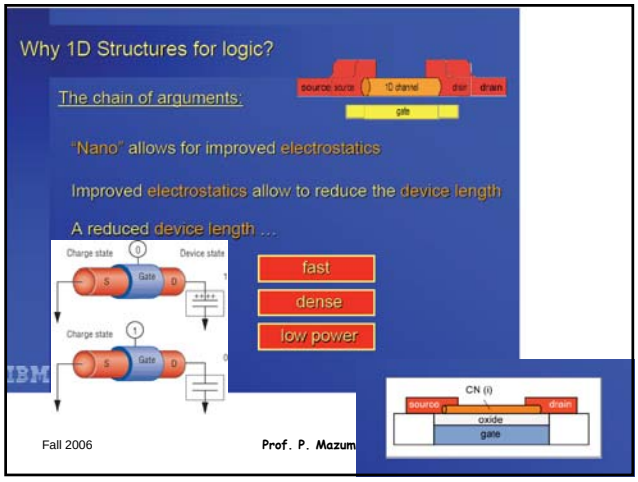

Concurrent Model of the Roadmap
Emerging Research Devices
Emerging Technology Sequence
Emerging Technology Vectors
Cellular array
Defect tolerant
Biologically inspired
Quantum computing
Architecture
RSFQ
1-D structures
Resonant tunneling
SET
Molecular
QCA
Spin transistor
Logic
Phase change
Floating body DRAM
Nano FG
SET
Insulator resistance change
Molecular
Memory
Transport enhanced FETs
UTB single gate FET
Source/Drain engineered FET
UTB multiple gate FET
Quasi ballistic FET
Non-classical CMOS
Risk
Figure 38 Emerging Technology Sequence
ITRS


Why 1D Structures for logic?
The chain of arguments:
"Nano" allows for improved electrostatics
Improved electrostatics allow to reduce the device length
A reduced device length …
fast
dense
low power
CN (i)
source
drain
oxide
gate
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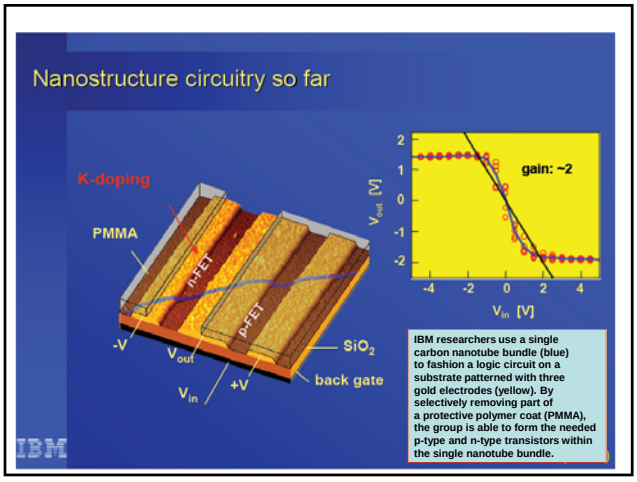
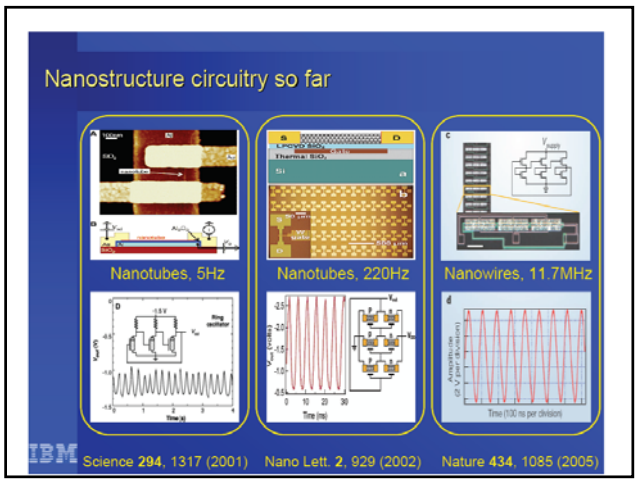
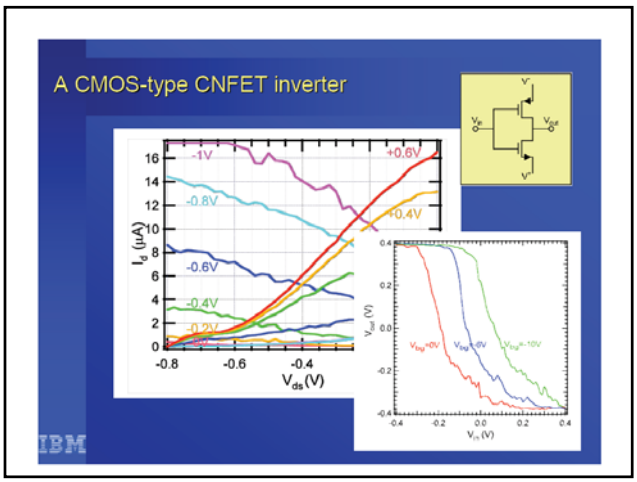
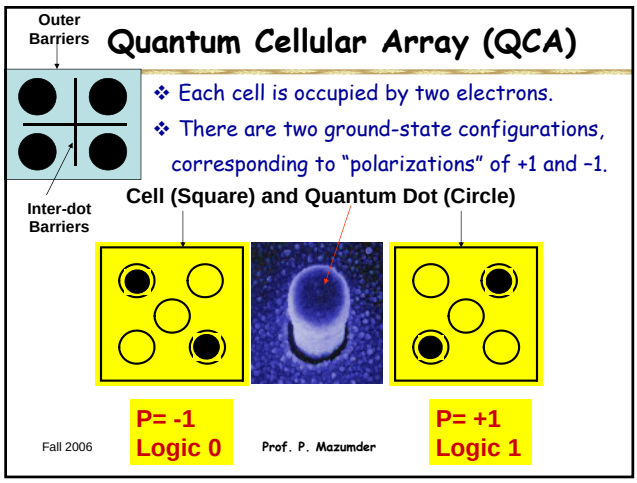

Nanostructure circuitry so far
K-doping
PMMA
n-FET
p-FET
-V
V_out
V_in
+V
SiO2
back gate
gain: ~2
V_out [V]
V_in [V]
IBM researchers use a single carbon nanotube bundle (blue) to fashion a logic circuit on a substrate patterned with three gold electrodes (yellow). By selectively removing part of a protective polymer coat (PMMA), the group is able to form the needed p-type and n-type transistors within the single nanotube bundle.


Nanostructure circuitry so far
Nanotubes, 5Hz
Nanotubes, 220Hz
Nanowires, 11.7MHz
Science 294, 1317 (2001)
Nano Lett. 2, 929 (2002)
Nature 434, 1085 (2005)
IBM


A CMOS-type CNFET inverter
-1V
-0.8V
-0.6V
-0.4V
-0.2V
+0.6V
+0.4V
I_d (μA)
V_{ds}(V)
IBM


Outer Barriers
Quantum Cellular Array (QCA)
Each cell is occupied by two electrons.
There are two ground-state configurations, corresponding to "polarizations" of +1 and –1.
Inter-dot Barriers
Cell (Square) and Quantum Dot (Circle)
P= -1
Logic 0
P= +1
Logic 1
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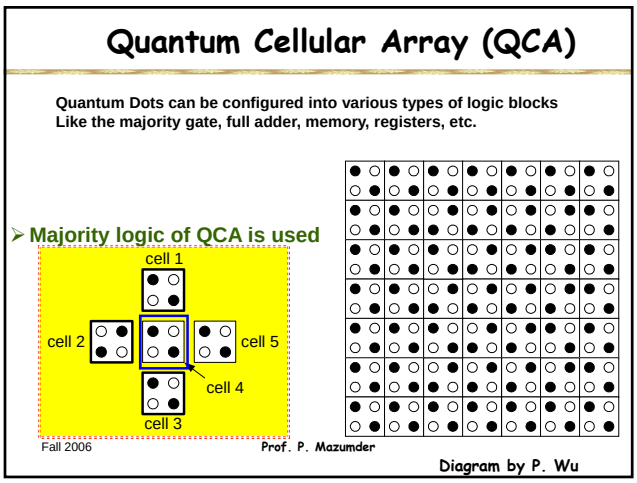
Quantum Cellular Array (QCA)
Quantum Dots can be configured into various types of logic blocks
Like the majority gate, full adder, memory, registers, etc.
Majority logic of QCA is used
cell 1
cell 2
cell 3
cell 4
cell 5
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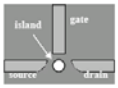
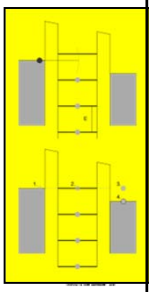
Diagram by P. Wu

Single electron memory

Single electron transistor(SET)
•Electron movements are controlled with single electron precision
•Coulomb blockade effect





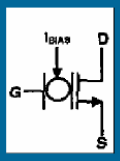
Advantages: high density, low power
Challenges: *low operating temperature*

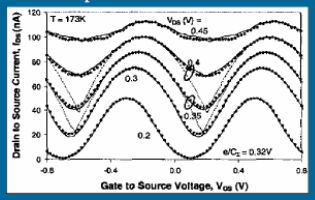
Research needs:
nanoelectronic devices, nonlithographic patterning

SETMOS: A Novel True Hybrid SET- CMOS High Current Coulomb Blockade Oscillation Cell for Future Nano-Scale Analog ICs

ETH, II, UCSB

CMOS (high speed drive, voltage gain)
+ SET (ultra low power consumption)
= SETMOS (dense, low- power, analog circuits, *e.g.*, NDR, NN, ADC)
Coulomb blockade oscillations and operation at- 100C





Malhapatra03

Molecular Electronics

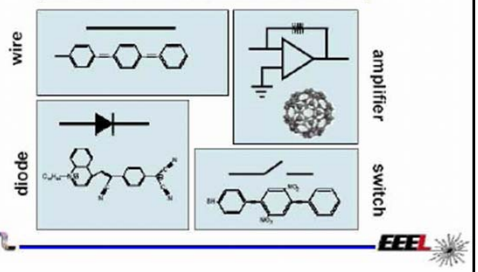
Semiconductor Electronics Division

Emerging Devices and Materials for Beyond CMOS

Slide No. 24

"moletronics"

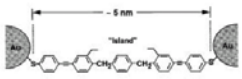
Moletronics: A new technology that uses molecules to perform the function of electronic components.

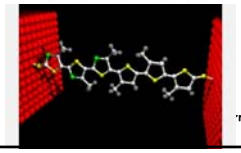


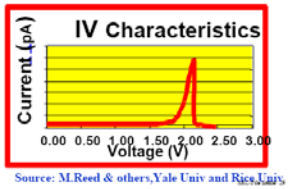
CSR EEEL

Molecular Memory

- Using individual molecules as building block of memory cells
- Data are stored by applying external voltage that cause the transition of the molecule into one of two possible phase states. Reading data is performed by measuring resistance changes in the molecular cell
- It is possible to combine molecular components with existing







Source: M.Reed & others,Yale Univ and Rice Univ.

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Evaluation Criteria:

1. **In-class presentation (2)**
2. **Written assignment related to presentation**
3. **Final project → To be discussed**
   Final Report
   Presentation

Grading: Average grade: A- (undergrad)
Average grade: A → A- (grad)

Points Allocation: Two presentations (30%)
Two assignments (20%)
Final Project (50%)

(distribution is subject to change)

END OF LECTURE 1

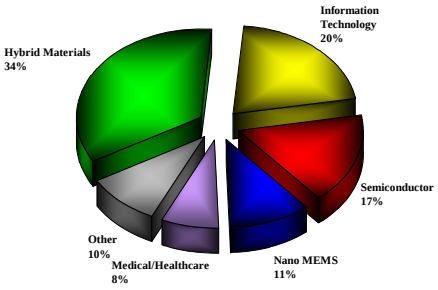
EECS 498/598: Nanocircuits and Nanoarchitectures

Instructor: Prof. Pinaki Mazumder

Tuesday and Thursday @ 3:00 – 4:30 p.m.

Lecture 2: ITRS Roadmap & Nano Devices

Nanotechnology Industry Segmentation



Nanotechnology Magazine http://nanozine.com
http://www.nanotech-now.com
http://www.technolytics.com

Kevin G. Coleman - Senior Fellow & Strategic Management Consultant
Technolytics, McMurray, PA 15317 USA
Contact: kgcoleman@technolytics.com

ITRS ROADMAP FOR EMERGINE MODELS & TECHNOLOGIES

- MEMORY ARRAYS
- LOGIC CIRCUITS
- ARCHITECTURES

RISK & PAYOFF;
CHALLENGES & OPPORTUNITIES

Table 62b Emerging Research Memory Devices—Experimental Parameters

	Baseline 2004 Technologies		*Phase Change Memory**	*Floating Body DRAM*	*Nano-floating Gate Memory*	*Single/Few Electron Memories*	*Insulator Resistance Change Memory [C,D,E]*	*Molecular Memories*
Storage Mechanism								
Device Types	DRAM	NOR Flash	OUM	1TDRAM	Engineered tunnel barrier or nanocrystal	SET	MIM	Bistable switch
Availability	2004	2004	~2006	~2006	>2006	>2007	~2010	>2010
Cell Elements	1T1C	1T	1T1R	1T	1T	1T	1T1R	1T1R
F Value	90 nm	90 nm	100 nm	130 nm[A,B]	80 nm	50 nm[G]	Not known	40–150 nm
Cell Size	$8F^2$ 0.065 μm^2 1T	$12.5F^2$ 0.101 μm^2 1T	~$6F^2$ 0.06 μm^2 1T	9 to $13F^2$ [B]	4 to $10F^2$ 0.04 μm^2	$200F^2$[G] ~0.5 μm^2	80 μm^2[C]	$9F^2$ ~0.01 μm^2[D]
Access Time	<15 ns	~80 ns	<100 ns	3 ns[A,B]	80 ns[F]	Not known	2 ms[C]	Not known
Store Time	<15 ns	~1 ms	<100 ns	3 ns[A,B]	100 ns[F]	5 ns[G]	100 ns[C]	~sec[I]
Retention Time	64 ms	10–20 yrs	>10 yrs	10–15 ms[B] (85°C)	>1 week[F]	>1 min[G]	1 year[D]	440 sec[H] ~month[I]
E/W Cycles	Infinite	>1E5	>1E13	Not known	1E9[F]	Not known	>1E3[D]	1E3[I]

Table 63b Emerging Research Logic Devices—Experimental Parameters

Availability Sequence	**1**	**2**	**2–3**	**2-3**	**4**	**5**	**6**
Device							
	FET	*RSFQ*[Z]	*1D Structures*	*Resonant Tunneling Devices*	*SET*	*Molecular*	*QCA*	*Spin transistor*
Types		JJ	CNT FET[F,G,H]	MOBILE[I] MVL RTT[J]	AND[K] NOT[LMN] OR[O]	2-terminal [V,W,X,Y]	E: QCA[P,Q,R]+ M: QCA[S,T]	Spin-valve[U]
Supported Architectures				See Table 63a				
Cell Size (Spatial Pitch)	100 nm	46 μm	10 μm	3 μm[K]	10 μm[L] 100 μm[L,M] 1 μm[N]	120 nm	E: 5.8 μm[P]* M: 250 nm[S,T]	2 mm
Density (Devices/cm²)	3E9	5E4	Not known	Not known	Not known	6E9	M: 2E9	Not known
Switch Speed	700 GHz	51–80 GHz	220 Hz	700 GHz	1 MHz[K]	2 Hz	Not known	Not known
Circuit Speed	30 GHz	20 GHz	Not known	Not known	Not known	Not known	E: 0.03-0.1 Hz[Q,R,S] M: 27 Hz[T]	Not known
Switching Energy, J^{**}	2×10^{-18}	1.14×10^{-17} [$>8\times10^{-16}$]	10^{-19}	10^{-13} [Z]	8×10^{-17} [] [$>1.3\times10^{-14}$]	10^{-9}	E: 4×10^{-23} [$>8\times10^{-19}$,[R]] M: 6×10^{-18}	Not known

Table 64 Emerging Research Architecture Implementations

Architecture Implementations	Cellular Array Implementations		Defect Tolerant Implementations	Biologically Inspired Implementations	Coherent Quantum Computing
	Quantum Cellular Automata	Cellular Nonlinear Networks			
Application Domain	• Not demonstrated	• Fast image processing • Associative memory • Complex signal processing	• Reliable computing with unreliable devices (such as SETs with background noise) • Historical examples include WSI • Terasac FPGA implementations	• Goal-driven computing using simple and recursive algorithms • High computational efficiency through data compression algorithms	• Special algorithms such as factoring and deep data searches
Device And Interconnect Implementations	• Arrays of nanodots or molecular assemblies	• Resonant tunneling devices	• Molecular switches, • Crossed arrays of 1D structures • Switchable interconnects	• Molecular organic and bio-molecular devices and interconnects	• Spin resonance transistors • NMR devices • Single flux quantum devices • Photonics

< 30 = Σ (PC*RC)
< 40
<50
>50

Table 66 Technology Performance and Risk Evaluation for Emerging Research Memory Device Technologies (Potential/Risk)

Memory Device Technologies (Potential/Risk)	Performance [A]	Architecture compatible [B]*	Stability and reliability [C]	CMOS compatible [D]**	Operate temp [E]***	Energy efficiency [F]	Sensitivity Δ(parameter) [G]	Scalability [H]
Floating Body DRAM	2.3/2.3	3.0/3.0	2.0/2.7	3.0/3.0	3.0/3.0	2.0/3.0	2.3/2.9	2.8/2.7
Phase Change Memory	2.6/2.9	2.2/3.0	2.3/2.2	2.2/3.0	3.0/3.0	1.8/2.7	2.1/2.1	2.7/2.2
Nano-floating Gate Memory	3.0/2.2	2.9/3.0	2.0/2.7	3.0/3.0	3.0/3.0	2.1/2.8	1.6/2.0	2.4/2.0
Insulator Resistance Change Memory	2.4/2.1	2.7/2.7	2.2/2.4	2.1/2.8	3.0/2.9	2.8/2.0	2.1/2.0	2.7/2.4
Molecular Memory	1.6/1.2	1.8/2.0	1.8/1.4	1.9/2.1	2.8/2.3	2.3/1.9	2.1/1.7	2.6/2.2
Single/Few Electron Memory	1.1/1.3	1.9/1.3	1.1/1.0	2.4/1.9	1.3/1.3	2.4/1.2	1.3/1.0	2.6/1.4

Performance Criterion (PC): 3 → better, 2 → comparable, 1 → worse than CMOS
Risk Criterion (RC): 3 → Low Risk, 2 → Moderate Risk, 1 → High Risk

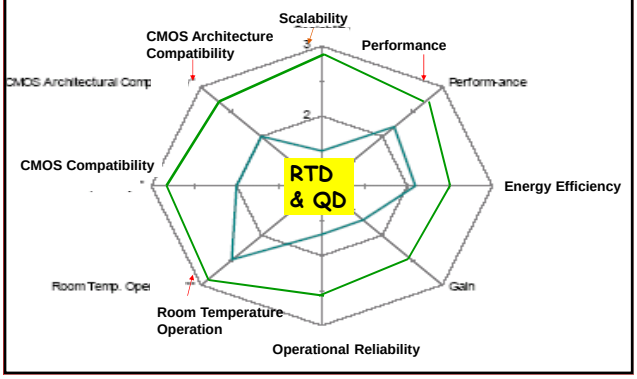
< 30 = Σ (PC*RC)
< 40
<50
>50

Table 67 Technology Performance and Risk Evaluation for Emerging Research Logic Device Technologies (Potential/Risk)

Logic Device Technologies (Potential/Risk)	Performance [A]	Architecture compatible [B]*	Stability and reliability [C]	CMOS compatible [D]**	Operate temp [E]***	Energy efficiency [F]	Sensitivity Δ(parameter) [G]	Scalability [H]
1D Structures	2.3/2.2	2.2/2.9	1.9/1.2	2.3/2.4	2.9/2.9	2.6/2.1	2.6/2.1	2.3/1.6
RSFQ Devices	2.7/3.0	1.9/2.7	2.2/2.8	1.6/2.2	1.1/2.7	1.6/2.3	1.9/2.8	1.0/2.1
Resonant Tunneling Devices	2.6/2.0	2.1/2.2	2.0/1.4	2.3/2.2	2.2/2.4	2.4/2.1	1.4/1.4	2.0/2.0
Molecular Devices	1.7/1.3	1.8/1.4	1.6/1.4	2.0/1.6	2.3/2.4	2.6/1.3	2.0/1.4	2.6/1.3
Spin Transistor	2.2/1.7	1.7/1.6	1.7/1.7	1.9/1.4	1.6/2.0	2.3/2.1	1.4/1.7	2.0/1.4
SETs	1.1/1.2	1.7/1.2	1.3/1.1	2.1/1.4	1.2/1.8	2.6/2.0	1.0/1.0	2.1/1.7
QCA Devices	1.4/1.3	1.2/1.1	1.7/1.8	1.4/1.6	1.2/1.4	2.4/1.7	1.6/1.1	2.0/1.4

Performance Criteria: 3 → superior to, 2 → comparable with, 1 → inferior to CMOS
Risk Criteria: 3 → Low Risk, 2 → Moderate Risk, 1 → High Risk

Evaluation Criteria for an Emergent Technology



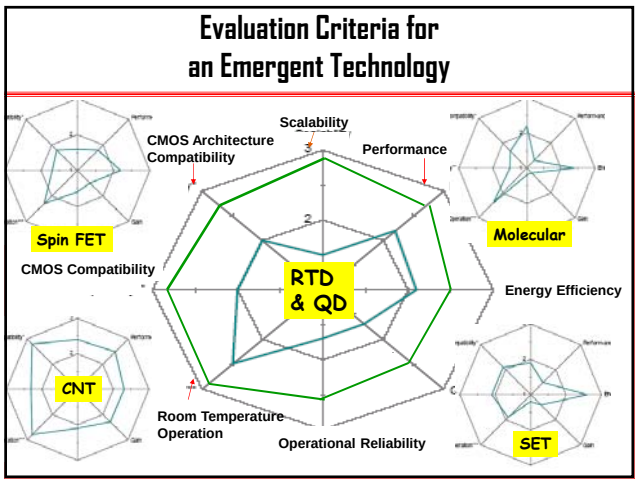


Table 5 Examples of proposed "future" devices and their salient attributes.

Device	*Possible applications*	*Advantages*	*Disadvantages*	*Remarks*
Single-electron transistors (SET)	Logic element	1. Small size 2. Low power	1. Sensitive to background charge instability. 2. High resistance and low drive current. 3. Cannot drive large capacitive (wiring) loads. 4. Requires geometries ≪10 nm for room-temperature operation.	Use of Coulomb blockade in nanocrystal "floating-gate"-type nonvolatile memory demonstrated. May improve retention time.
Quantum dot (quantum cellular automata)	Logic element	Small size	1. Multiple levels of interconnection across long distance difficult. 2. Room-temperature operation difficult. 3. New computation algorithms required. 4. Method of setting the initial state of the system not available. 5. Single defect in line of dots will stop propagation.	Devices demonstrated at low temperatures. QCA architectures extensively investigated.
Resonant tunneling diode (RTD)	1. Logic element 2. Dynamic memory	1. Small size	1. Tunneling process sensitive to small film thickness (tunneling distance) variation, leading to process control difficulties. 2. Requires dc bias, large standby power consumption. 3. Multivalue logic sensitive to noise margin 4. Speed of RTD circuits likely to be determined by the conventional devices required in the circuit.	Small- to medium-scale circuits demonstrated. M demonstrations on III-V compound semiconductor
Rapid single-flux quantum (RSFQ) device	Logic element	Very high speed possible	1. Requires liquid helium temperature. 2. Lacks a high-density random-access memory. 3. Requires tight process tolerance.	Very-high-speed (THz) circuits demonstrated.
Two-terminal molecular devices	1. Logic element 2. Memory	1. Small size	1. No inherent device gain. 2. Scaling to large memory size may be difficult without gain. 3. Placement of molecules in a circuit difficult and not yet demonstrated. 4. Temperature stability of organic molecules may be problematic.	Sixteen-bit cross-point memory demonstrated.
Carbon nanotube FET	Logic element	1. Ballistic transport (high speed) 2. Small size	1. Placement of nanotubes in a circuit difficult and not yet demonstrated. 2. Control of electrical properties of carbon nanotube (size, chirality) difficult and not yet achieved.	Device scaling properties not yet explored. Inverter circuit demonstrated.
DNA computing	Logic element	1. High parallelism	1. Imperfect yield. 2. General-purpose computing not possible.	

Table 65 Estimated Parameters for Emerging Research Devices and Technologies in the year 2016

Technology	T_{min} sec	T_{max} sec	CD_{min} m	CD_{max} m	Energy J/op	Cost min $/gate	Cost max $/gate
Si CMOS	3E-11[123]	1E-6	8E-9	5E-6	4E-18	1E-11	3E-3
RSFQ	1E-12	5E-11	3E-7	1E-6	2E-18	1E-3	1E-2
Molecular	1E-8	1E-3	1E-9	5E-9	1E-20	1E-12	1E-10
Plastic	1E-4	1E-3	1E-4	1E-3	4E-18	1E-7	1E-6
Optical (digital, all optical)	1E-16	1E-12	2E-7	2E-6	1E-12	1E-3	1E-2
NEMS (conservative)	1E-7	1E-3	1E-8	1E-7	1E-21	1E-8[122]	1E-5
Biologically Inspired	1E-13	1E-4	6E-6	5E-5	3E-25	5E-4	3E-1
Quantum	1E-16	1E-15	1E-8	1E-7	1E-21	1E3	1E5

In this table T stands for system cycle time (switching time), CD stands for critical dimension (e.g., physical gate length), Energy is the intrinsic operational energy of one device, and Cost is defined as $ per gate.

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Table 59b Multiple-gate Non-classical CMOS Technologies

Device	Multiple Gate FETs				
	N-Gate (N>2) FETs	Double-gate FETs			
					
Concept	Tied gates (number of channels >2)	Tied gates, side-wall conduction	Tied gates planar conduction	Independently switched gates, planar conduction	Vertical conduction
Application/ Driver	HP, LOP, and LSTP CMOS	HP, LOP, and LSTP CMOS	HP, LOP, and LSTP CMOS	LOP and LSTP CMOS	HP, LOP, and LSTP CMOS
Advantages	▪ Higher drive current ▪ 2× thicker fin allowed	▪ Higher drive current ▪ Improved subthreshold slope ▪ Improved short channel effect	▪ Higher drive current ▪ Improved subthreshold slope ▪ Improved short channel effect	▪ Improved short channel effect	▪ Potential for 3D integration
Particular Strength	▪ Thicker Si body possible	▪ Relatively easy process integration	▪ Process compatible with bulk and on bulk wafers ▪ Very good control of silicon film thickness	▪ Electrically (statically or dynamically) adjustable threshold voltage	▪ Lithography independent L_g
Potential weakness	▪ Limited device width ▪ Corner effect	▪ Fin thickness less than the gate length ▪ Fin shape and aspect ratio	▪ Width limited to <1 μm	▪ Difficult integration ▪ Back-gate capacitance ▪ Degraded subthreshold slope	▪ Junction profiling difficult ▪ Process integration difficult ▪ Parasitic capacitance ▪ Single gate length

Non-classical CMOS Devices

Device	Ultra-Thin Body SOI	Band-engineered Tr	Vertical Tr	FinFET	Double-Gate Tr
Concept	Fully depleted SOI	SiGe or Strained Si channel; bulk Si or SOI	Double-gate or surround-gate structure [No specific temporal sequence for these 3 structures is intended]		
Application/driver	Higher performance; Higher transistor density; Lower power dissipation				
Maturity	Development				
Advantages	- Improved subthreshold slope -Vt controllability better than PD	-Higher drive current - Compatible with bulk and SOI CMOS	- Higher drive current - Lithography independent Lg	-Higher drive current -Improved subthreshold slope - Improved short channel effect	-Higher drive current -Improved subthreshold slope - Improved short channel effect - Stacked NAND
Scaling issues	- Si film thickness - Gate stack - Worse short channel effect than bulk CMOS	- High mobility film thickness, in case of SOI - Gate stack - Integration	- Si film thickness - Gate stack - Integrability -Process complexity - TCAD including QM effect	- Si film thickness - Gate stack - Process complexity - TCAD including QM effect	- Gate alignment - Si film thickness - Gate stack - Integrability - Process complexity - TCAD including QM effect
Design challenges	- Device characterization - Compact model and parameter extraction	- Device characterization	- Device characterization - PD vs. FD - Compact model and parameter extraction		
Timing	Near future →				

*2001 ITRS roadmap

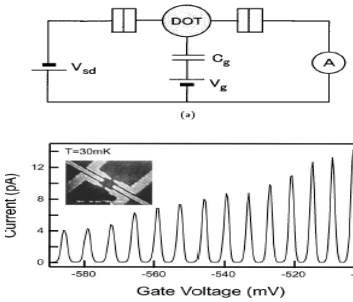

Fig. 1. (a) Circuit model of single electron transistor (SET). The dot is connected to the source and drain electrodes through small tunnel barriers. The potential in the dot can be modified by the gate electrode which is capacitively coupled to the dot. The DC bias (V_{sd}) is applied, and the current is measured as a function of V_{sd} and V_g. (b) Coulomb blockade oscillations of SET. The current is measured at 30 mK as a function of the gate voltage. For this device, $C_g = 27$ aF and $C_\Sigma = 190$ aF. Inset: Scanning electron image of the gate pattern of the SET (example). The Ti/Au metal pattern is formed on the GaAs/AlGaAs surface using electron beam lithography and lift off. Two point contacts are adjusted to form the tunnel barrier.

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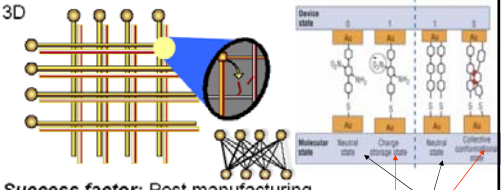
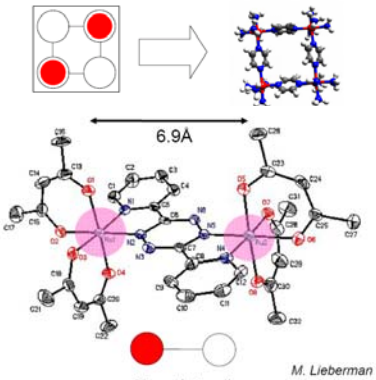
Defect tolerant architecture

- All-memory architecture
- Defect tolerant
- Potentially self-repairing and reconfigurable
- 3D



- ***Success factor:*** Post manufacturing testing/mapping processing. Test Challenge



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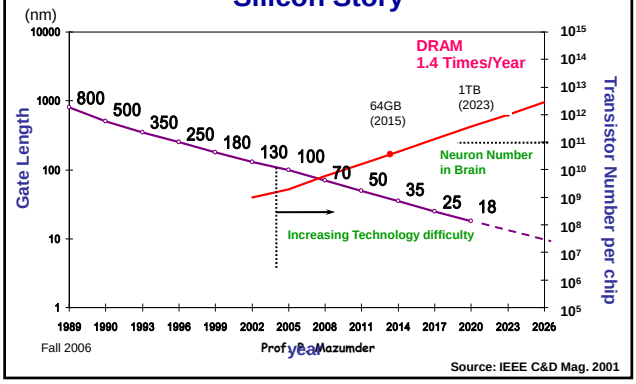
Silicon Nanoelectronics — Nano-CMOS

Silicon Story



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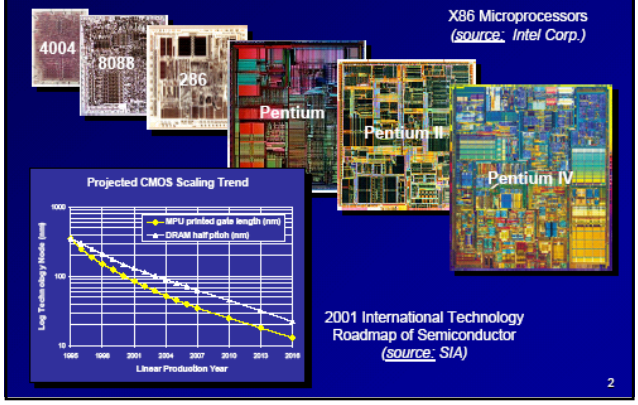
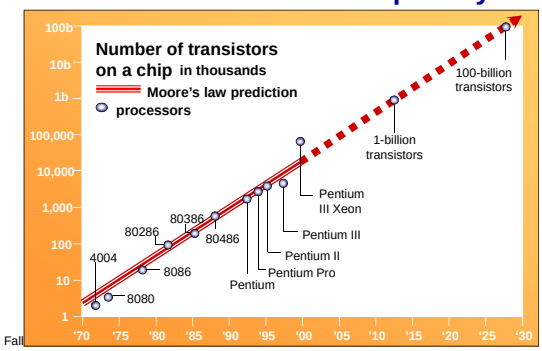
Source: IEEE C&D Mag. 2001

Digital VLSI System Drives CMOS Scaling



Silicon Nanoelectronics — Nano-CMOS

CPU with Multimedia Capability



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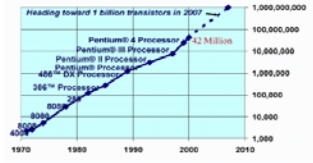
Nanoelectronics and Gigascale Systems Lab.

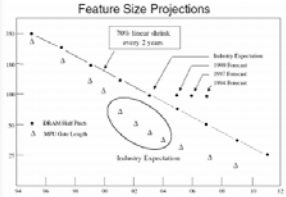
Courtesy: P. Wu

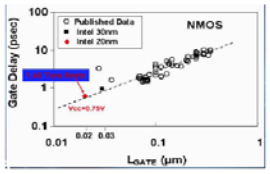
What does a Beyond CMOS technology have to do to replace CMOS?

- >> 10^9 devices
- << 10 nm feature size
- << 1 psec gate delay
- <~ $4B fab
- ~ 10 year reliability

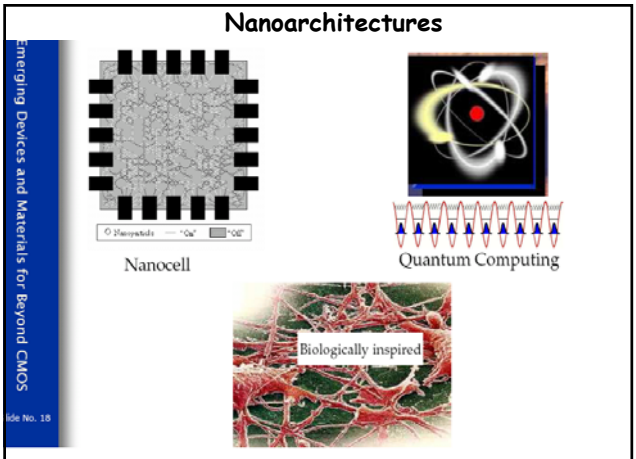


Feature Size Projections





Nanoarchitectures



Emerging Technologies

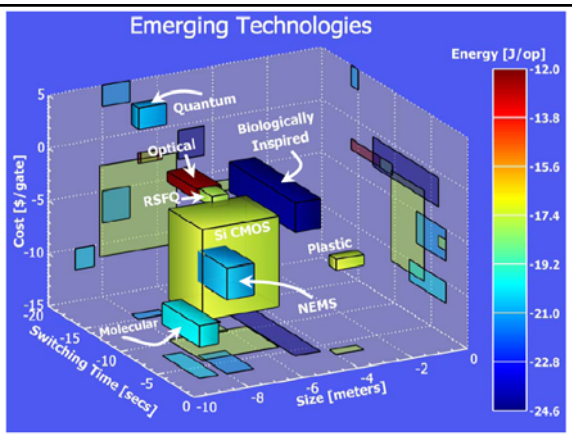


Figure 42 Parameterization of Emerging Technologies and CMOS— Speed, Size, Cost, and Switching Energy

Factor 1 Individual Performance Potential for each Technology Evaluation Criterion

3	Substantially exceeds CMOS * or is compatible with CMOS architecture ** or is monolithically integrable with CMOS wafer technology ***or is compatible with CMOS operating temperature
2	Comparable to CMOS * or can be integrated with CMOS architecture with some difficulty ** or is functionally integrable (easily) with CMOS wafer technology ***or requires a modest cooling technology, T ≥ 77K
1	Substantially (2×) inferior to CMOS * or can not be integrated with CMOS architecture ** or is not integrable with CMOS wafer technology ***or requires very aggressive cooling technology, T < 4K

Factor 2 Individual Risk Assessment for each Technology Evaluation Criterion

3	Solutions to accomplish most of the Technology Evaluation Criteria for the Technology Entry are known resulting in lowest risk
2	Concepts to accomplish most of the Technology Evaluation Criteria have been proposed for the Technology Entry and are judged to be of moderate risk
1	No solutions or concepts have been proposed accomplish most of the Technology Evaluation Criteria for the Technology Entry and are judged to be of highest risk

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Overall Performance and Risk Assessment (OPRA) = Sum [(Performance Potential) x (Risk Assessment)]
(Summed over the eight Evaluation Criteria for each Technology Entry)
Maximum Overall Performance and Risk Assessment (OPRA) = 72
Minimum Overall Performance and Risk Assessment (OPRA) = 8

Overall Performance and Risk Assessment for Technology Entries

Potential for the Technology Entry is projected to be significantly better than silicon CMOS (compared using the Technology Evaluation Criteria) and solutions to accomplish the most of the Technology Evaluation Criteria are known resulting in lowest risk (OPRA ≥ 50)	**Potential/Risk**
Potential for the Technology Entry is projected to be comparable to or slightly less than silicon CMOS (compared using the Technology Evaluation Criteria) and concepts to accomplish most of the Technology Evaluation Criteria have been proposed and are judged to be of moderate risk (OPRA = 40 – 49)	**Potential/Risk**
Potential for the Technology Entry is projected to be comparable to or less than silicon CMOS (compared using the Technology Evaluation Criteria) and concepts to accomplish a few of the Technology Evaluation Criteria have been proposed and are judged to be of higher risk (OPRA = 30 – 39)	**Potential/Risk**
Potential for the Technology Entry is projected to be significantly less than silicon CMOS (compared using the Technology Evaluation Criteria) and no solutions or concepts have been proposed accomplish most of the Technology Evaluation Criteria and are judged to be of highest risk (OPRA < 30)	**Potential/Risk**

Relevance Criteria Notes for Tables 00 and 01:

[A] Performance—Future performance metrics will be very similar to current performance metrics. They are cost, size, speed and energy dissipation.

[B] Architectural compatibility—This criterion is motivated by the same set of concerns that motivate the CMOS compatibility, namely the ability to utilize the existing CMOS infrastructure that currently exists. The architectural compatibly is defined in terms of the logic system and data representation used by the alternative technology. CMOS utilizes Boolean logic and a binary data representation and ideally, the alternative technology would need to do so as well.

[C] Stability and reliability—As devices approach the atomic scale, structural compositional stability to thermal fluctuations becomes a significant concern. Any realistic alternative device must show structural stability at room temperature for at least 7 years.

[D] CMOS compatibility—The semiconductor industry has been based for the last 40 years on incremental scaling of device dimensions to achieve performance gains. The principle economic benefit of such an approach is it allows the industry to fully apply previous technology investments to future products. Any alternative technology will need to utilize the tremendous investment in infrastructure to the highest degree possible.

[E] Room temperature operation—Room temperature operation is desirable because advanced cooling systems can add substantially to the cost.

[F] Energy efficiency—Energy efficiency appears likely to be the limiting factor of any post CMOS device using electric charge or electric current as a state variable. It also appears likely that it will be dominant criterion in determining the ultimate applicability of alternate state variable devices.

[G] Sensitivity to parametric variation—As devices approach the atomic scale, they become very sensitive to manufacturing and environmental variations. Thus parametric sensitivity is an important criterion for evaluation of alternative technologies. The goal should be a device that is affected but not dominated by parametric variations.

[H] Scalability—In order to derive the economic benefit of incrementalism, any alternative technology should be scalable through multiple generations. It will be desirable to make incremental modifications to the alternative technology and achieve integer multiples of performance. In other words, it should be possible to articulate a Moore's law for the proposed technology.

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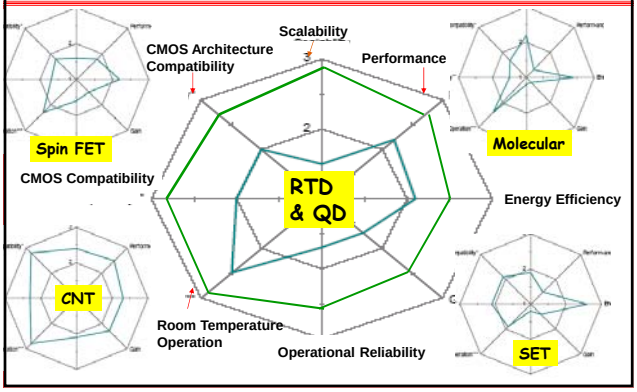
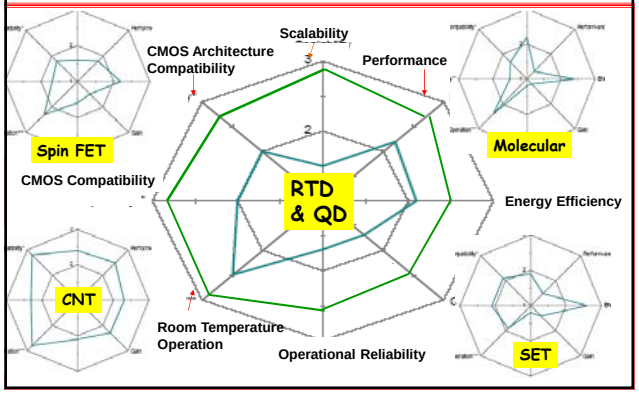
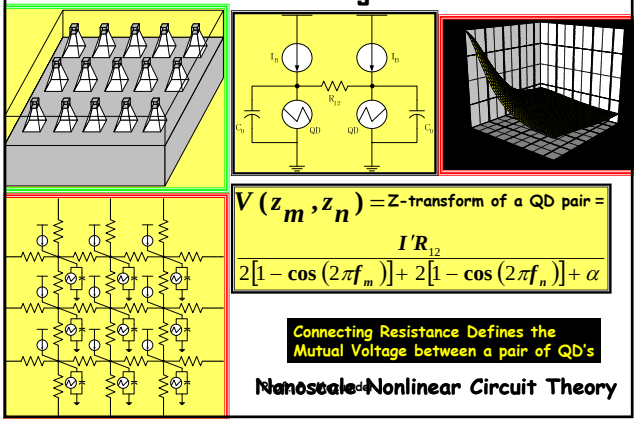
Evaluation Criteria for an Emergent Technology



Evaluation Criteria for an Emergent Technology



Monochromatic Image Processor

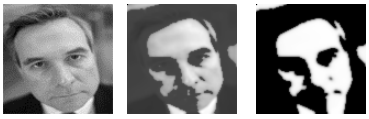


$$V(z_m, z_n) = \text{Z-transform of a QD pair} = \frac{I' R_{12}}{2[1-\cos(2\pi f_m)] + 2[1-\cos(2\pi f_n)] + \alpha}$$

Connecting Resistance Defines the Mutual Voltage between a pair of QD's

Nanoscale Nonlinear Circuit Theory

Edge Detection by QDA



0 ns 1 ns 2 ns

Gray → Binary Conversion

Vertical Line Detection (VLD)

0 ns 6 ns

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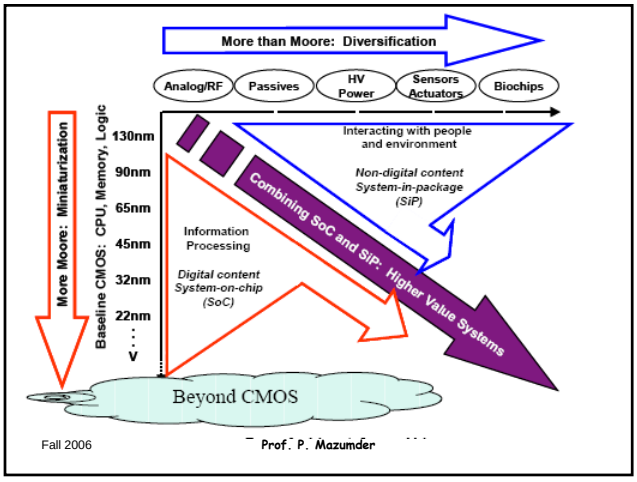
Image Processor is being fabricated and tested under a NIRT project



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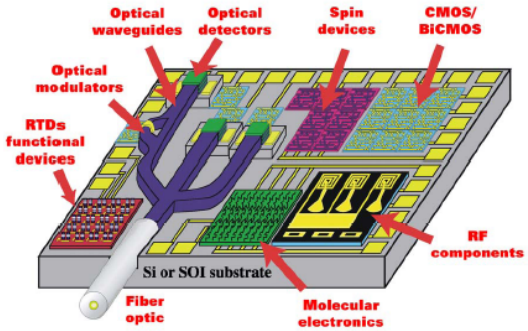

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