EECS 427
VLSI Design

Lecture 11: Dynamic Logic Families

Prof. Pinaki Mazumder

Winter 2013

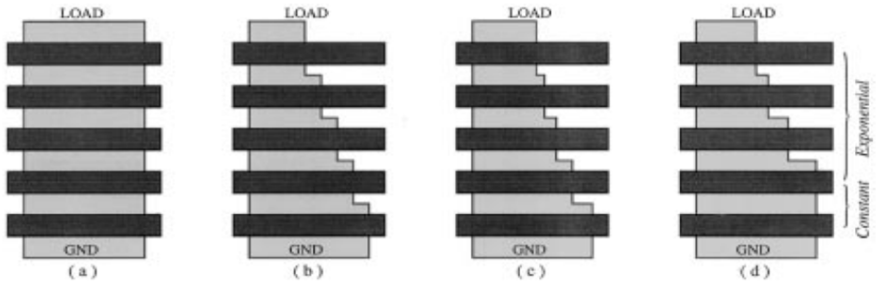
Adapted from Harris, Rabaey, Blaauw, Zhang, Sylvester, and others

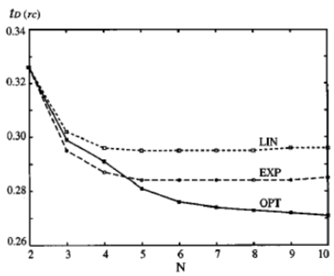
Outline

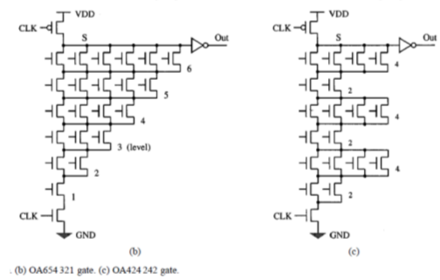
- Basic domino gate
- Issues in dynamic gates
- Domino cascading
- Footless domino
- NORA/Zipper logic
- Multiple-output domino logic
- Compound domino
- Dual-rail domino
- Self-reseting domino
- Limited Switch dynamic logic

On Optimal Tapering of FET Chains in High-Speed CMOS Circuits

Li Ding, *Student Member, IEEE,* and Pinaki Mazumder, *Fellow, IEEE*

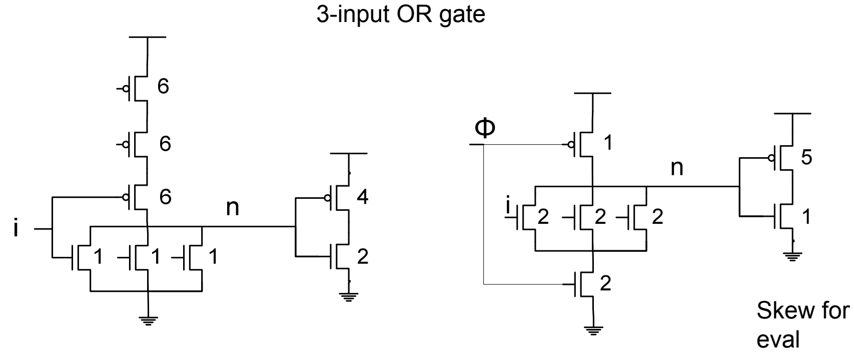






Domino / Static C_{in}/C_{out}

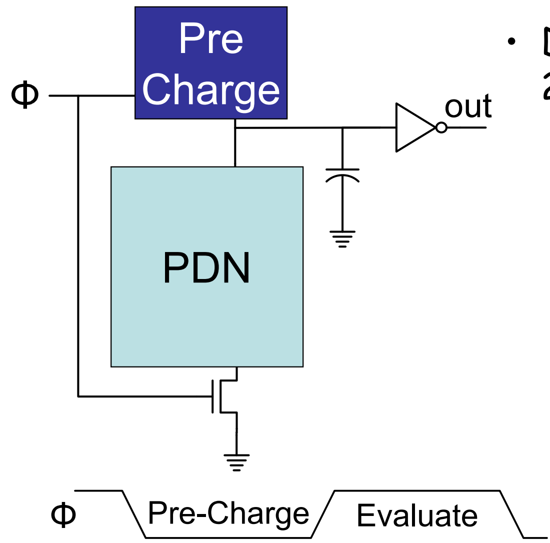
3-input OR gate



Static:
$C_i = 7$
$C_n = 9$

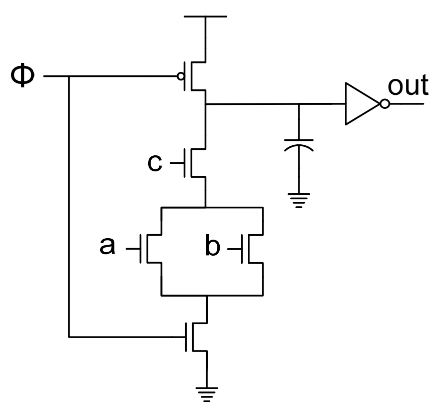
Dynamic:
$C_i = 2$
$C_n = 7$

Basic Domino Gate



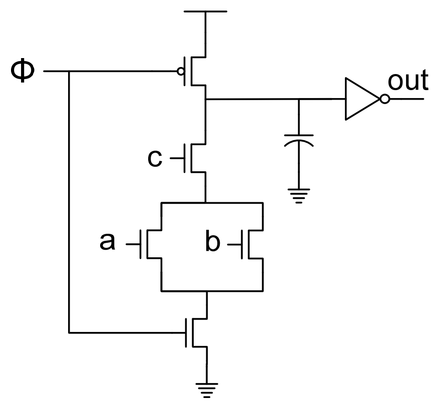
- Divide the clock in 2 phases:
  - Precharge
    - Output Low
    - Dyn. Cap precharge
    - PDN Off
  - Evaluate
    - Conditional discharge
    - Input must be stable and monotonic L→H

Basic Domino Gate



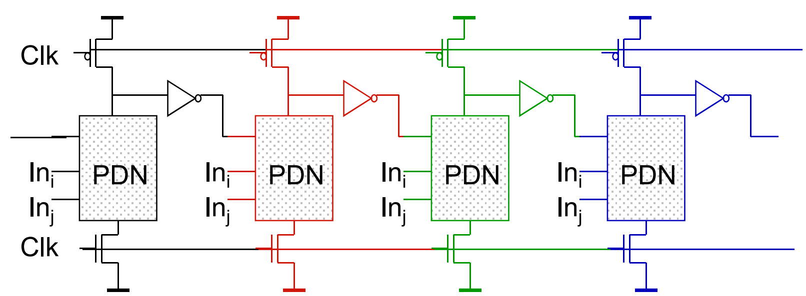
- Advantages:
  - Faster than CMOS
  - Input capacitance is lower
  - Early switch point
  - Inverter P/N > 2 (only rising delay important)

Basic Domino Gate



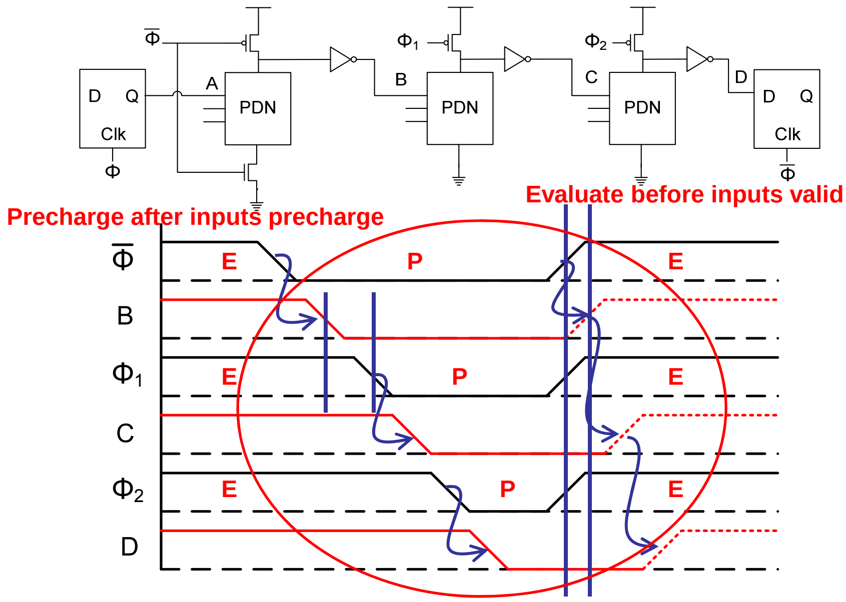
- Disadvantages:
  - Low noise margin
  - Charge sharing
  - Leakage currents
  - Internal capacitance charge sensitive to noise

Why Domino?



Like falling dominos!

Footless Domino



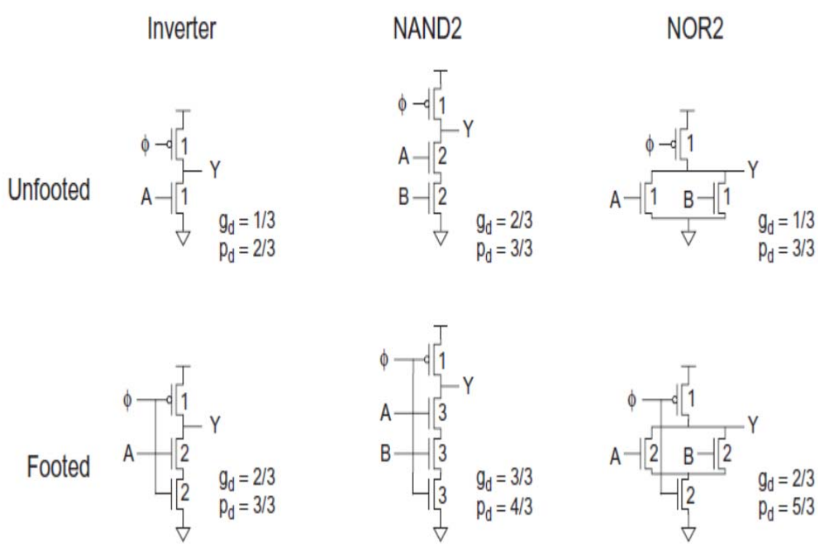
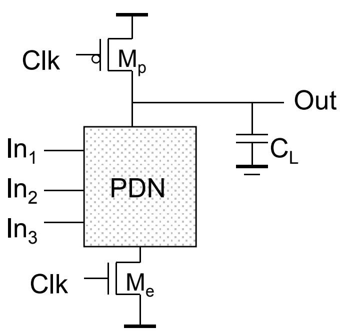


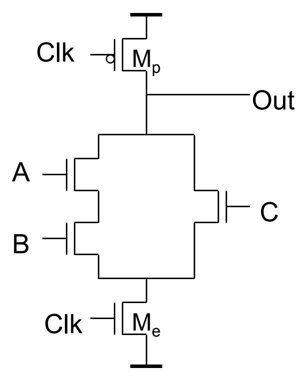
FIGURE 9.25 Catalog of dynamic gates

Dynamic CMOS

- In static circuits at every point in time (except when switching) the output is connected to either GND or V_{DD} via a low resistance path.
  - fan-in of n requires $2n$ (n N-type + n P-type) devices
- Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - requires on $n + 2$ (n+1 N-type + 1 P-type) transistors

Dynamic Gate



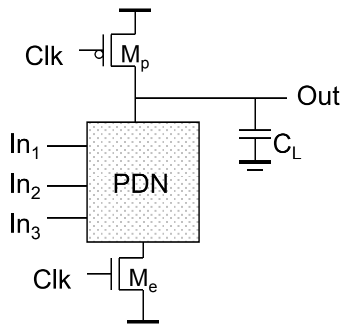


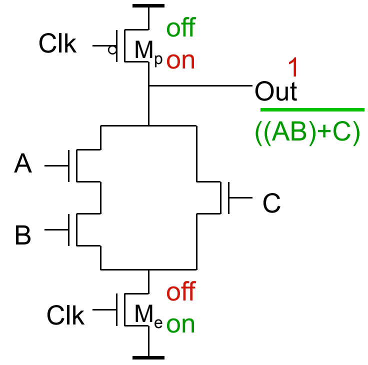
Two phase operation

Precharge (CLK = 0)

Evaluate (CLK = 1)

Dynamic Gate





Two phase operation
Precharge (Clk = 0)
Evaluate (Clk = 1)

Conditions on Output

- Once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.
- Inputs to the gate can make at most one transition during evaluation.
- Output can be in the high impedance state during and after evaluation (PDN off), state is stored on C_L

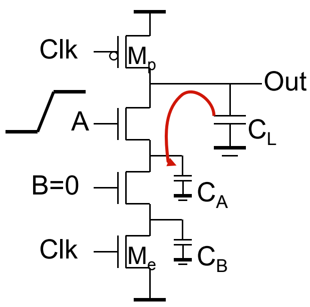
Properties of Dynamic Gates

- Logic function is implemented by the PDN only
  - number of transistors is N + 2 (versus 2N for static complementary CMOS)
- Full swing outputs (V_{OL} = GND and V_{OH} = V_{DD})
- Non-ratioed - sizing of the devices does not affect the logic levels
- Faster switching speeds
  - reduced load capacitance due to lower input capacitance (C_{in})
  - reduced load capacitance due to smaller output loading (Cout)
  - no I_{sc}, so all the current provided by PDN goes into discharging C_L

Properties of Dynamic Gates

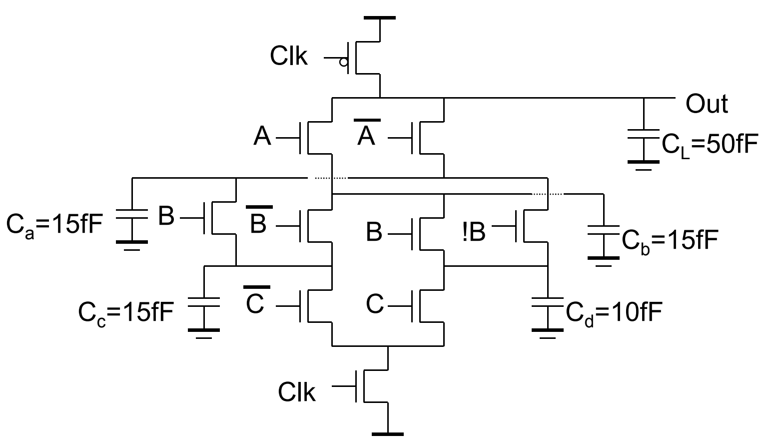
- Overall power dissipation usually higher than static CMOS
  - no static current path ever exists between V_{DD} and GND (including P_{sc})
  - no glitching
  - higher transition probabilities
  - extra load on Clk
- PDN starts to work as soon as the input signals exceed V_{Tn}, so V_M, V_{IH} and V_{IL} equal to V_{Tn}
  - low noise margin (NM_L)
- Needs a precharge/evaluate clock

Issues in Dynamic Design 2: Charge Sharing

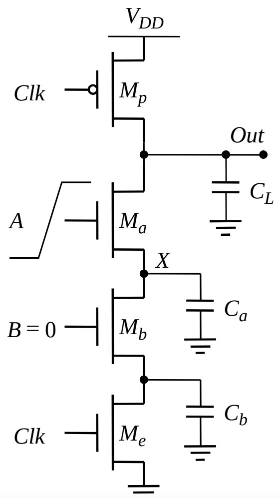


Charge stored originally on C_L is redistributed (shared) over C_L and C_A leading to reduced robustness

Charge Sharing Example



Charge Sharing



case 1) if $\Delta V_{out} < V_{Tn}$

$$C_L V_{DD} = C_L V_{out}(t) + C_a(V_{DD} - V_{Tn}(V_X))$$

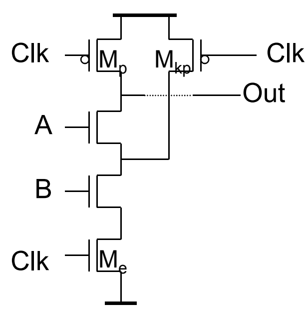
or

$$\Delta V_{out} = V_{out}(t) - V_{DD} = -\frac{C_a}{C_L}(V_{DD} - V_{Tn}(V_X))$$

case 2) if $\Delta V_{out} > V_{Tn}$

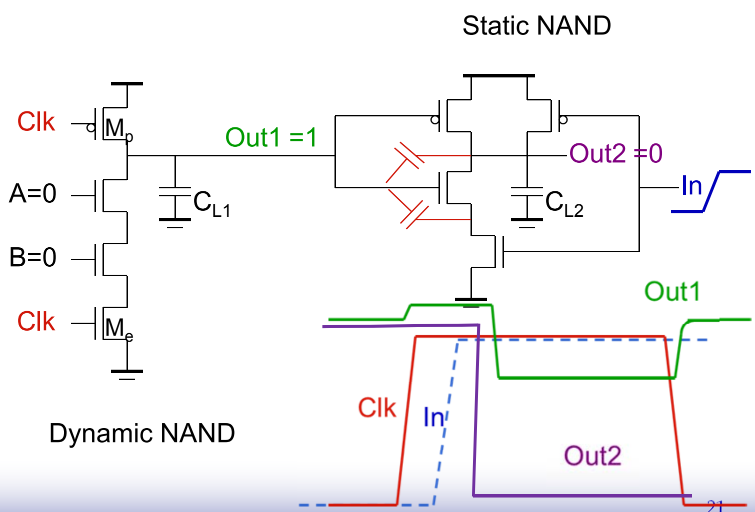
$$\Delta V_{out} = -V_{DD}\left(\frac{C_a}{C_a + C_L}\right)$$

Solution to Charge Redistribution

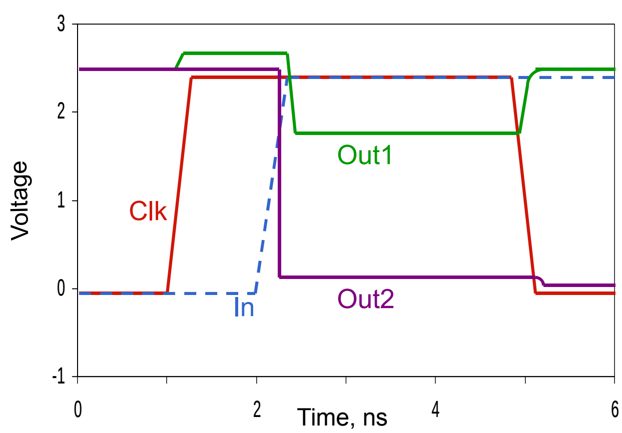


Precharge internal nodes using a clock-driven transistor (at the cost of increased area and power)

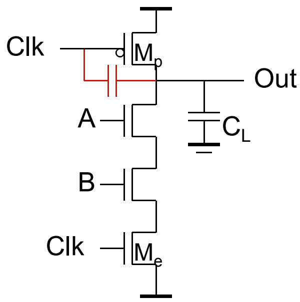
Issues in Dynamic Design 3: Backgate Coupling



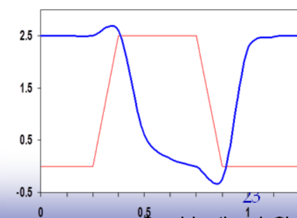
Backgate Coupling Effect



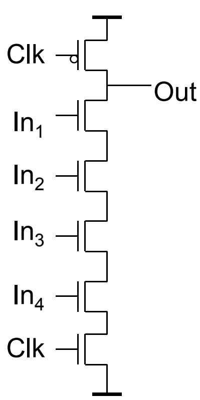
Issues in Dynamic Design 4: Clock Feedthrough

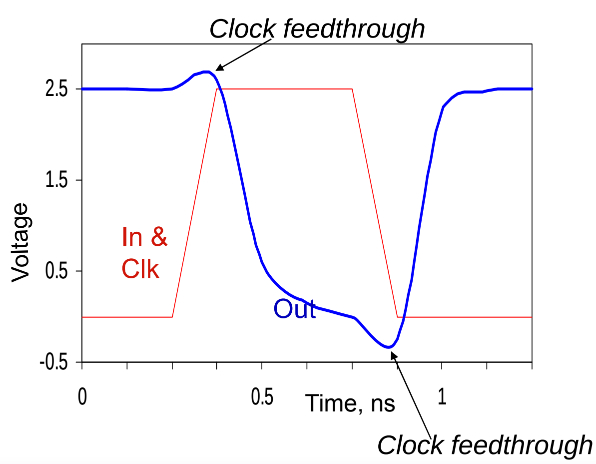


Coupling between Out and Clk input of the precharge device due to the gate to drain capacitance. So voltage of Out can rise above V_{DD}. The fast rising (and falling edges) of the clock couple to Out.

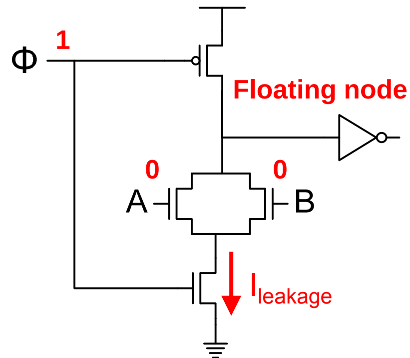


Clock Feedthrough



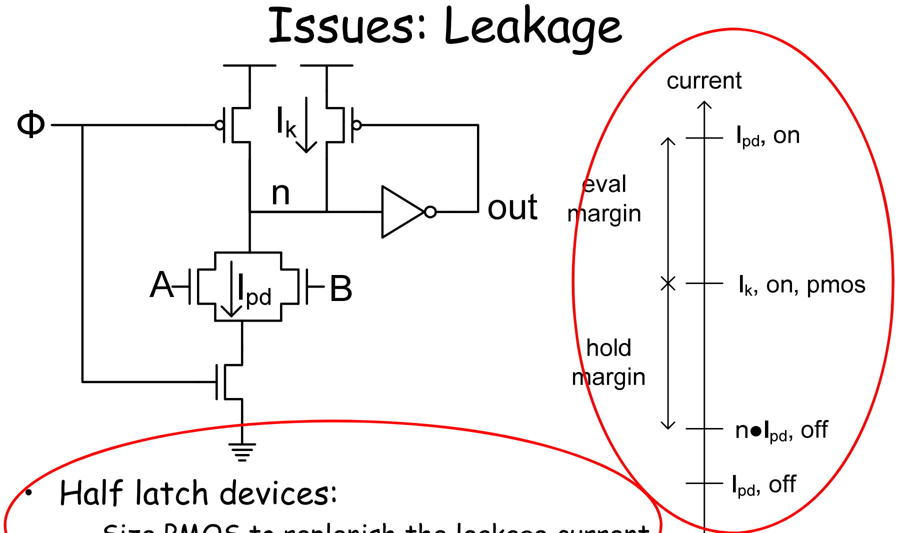


Issues: Leakage



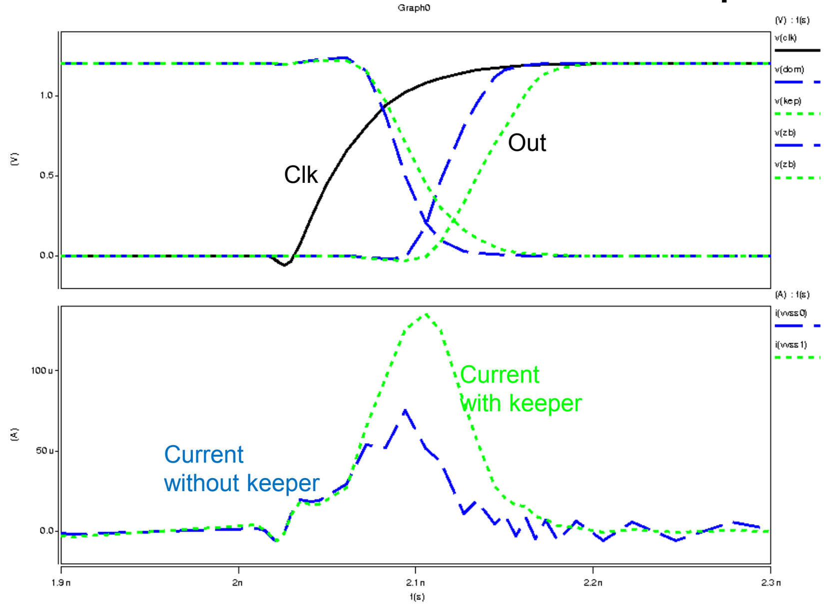
- Dynamic node is floating during evaluation
  - Leakage current of NMOS can discharge it

Issues: Leakage

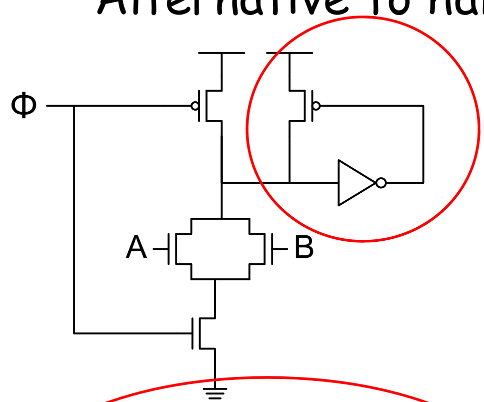


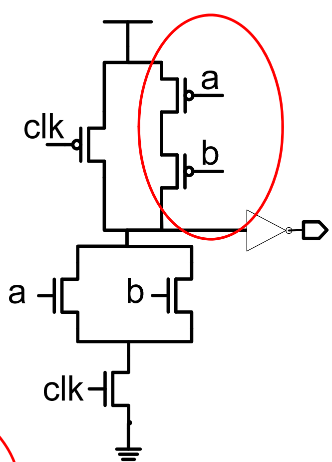
- Half latch devices:
  - Size PMOS to replenish the leakage current
  - Limits width OR gates

Domino – with and without keeper



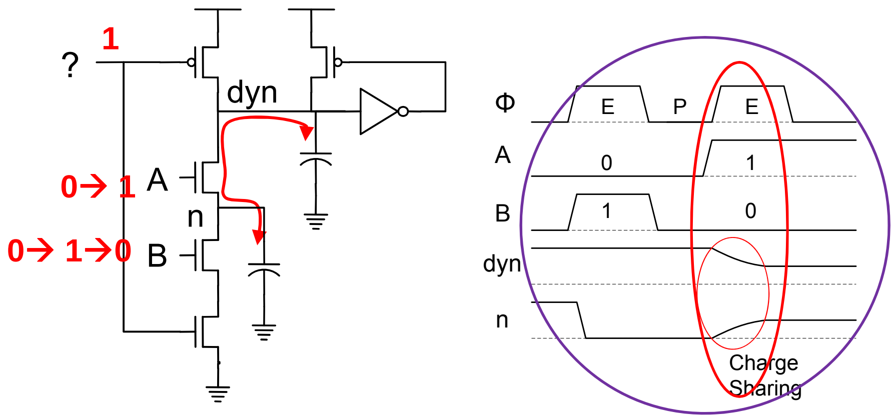
Alternative to half latch device





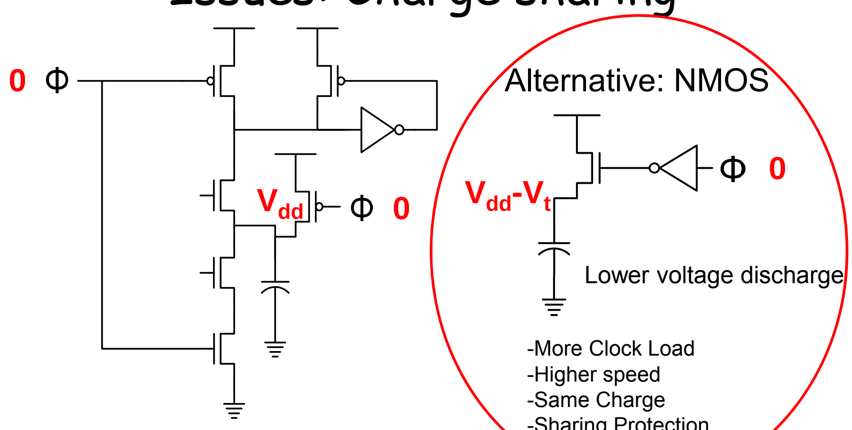
- Eliminates fight
- But only a few PMOS in series
  - More input cap
- OPL?

Issues: Charge sharing



- In evaluate, dynamic node charge is shared with internal node caps
- Node was discharged in previous cycle

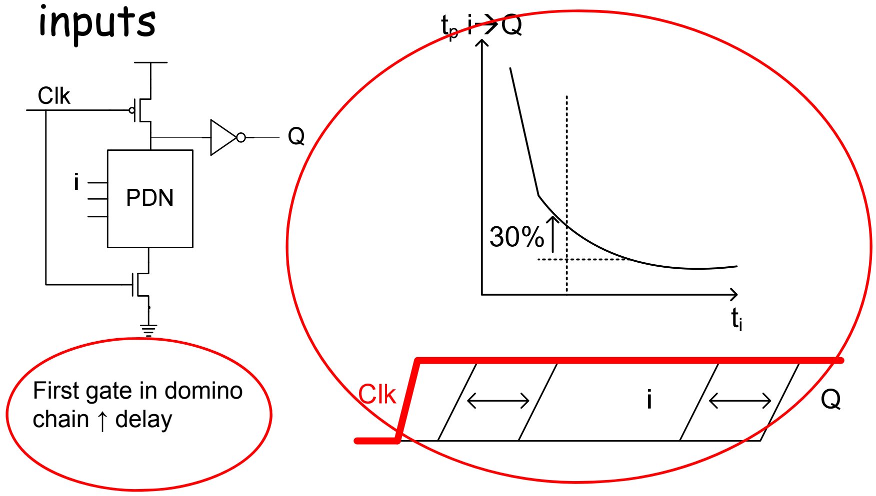
Issues: Charge sharing



- Issues with precharging internal node:
  - PDN becomes slower (more internal cap.)
  - Higher voltage to discharge

Issues: Timing

- Delay is dependent on the timing of inputs



On Circuit Techniques to Improve Noise Immunity of CMOS Dynamic Logic

Li Ding, *Member, IEEE*, and Pinaki Mazumder, *Fellow, IEEE*

Class	Technique	Reference	Illustration	Num. tran.	Input load[a]	Clock load[a]	Dischrg path[a]	DC current[a]	All noises[a]	All func.[a]
A	Always-on keeper	[3]	Fig. 2(a)	*N*	o	o	o	×	o	o
	Feedback keeper	[4]	Fig. 2(b)	*N*	o	o	o	o	o	o
	HS feedback keeper	[5]	Fig. 2(c)	*N*	o	o	o	o	×	o
	Conditional feedback keeper	[7]	Fig. 2(d)	*N*	o	o	o	o	^	o
B	Precharge internal nodes	[9]	Fig. 3(a)	2*N*	o	×	o	o	×	o
	Partial precharge	[10]	Fig. 3(b)	*N*	o	×	o	o	×	o
C	PMOS pull-up	[11]	Fig. 4(a)	*N*	o	o	o	×	o	o
	NMOS pull-up (feedback)	[12]	Fig. 4(b)	*N*	o	o	o	×	o	o
	Mirror technique	[13]	Fig. 4(d)	2*N*	×	o	×	o	o	o
	Twin transistor	[15]	Fig. 4(c)	2*N*	^	o	o	o	o	^
D	Complementary p-network	[17]	Fig. 6(a)	2*N*	×	o	o	o	o	o
	CMOS inverter	[19]	Fig. 6(b)	2*N*	×	o	o	o	o	×
	Gated CMOS inverter	[20]	Fig. 6(c)	2*N*	×	o	o	o	o	×
	Triple transistor	[21]	Fig. 6(d)	3*N*	×	o	×	o	o	o

[a]Symbol o represents 'good' and symbol × represents 'not good'.

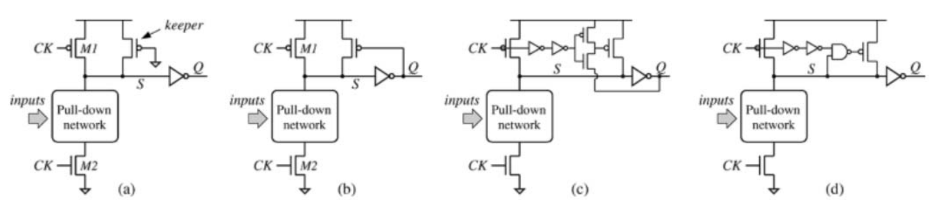
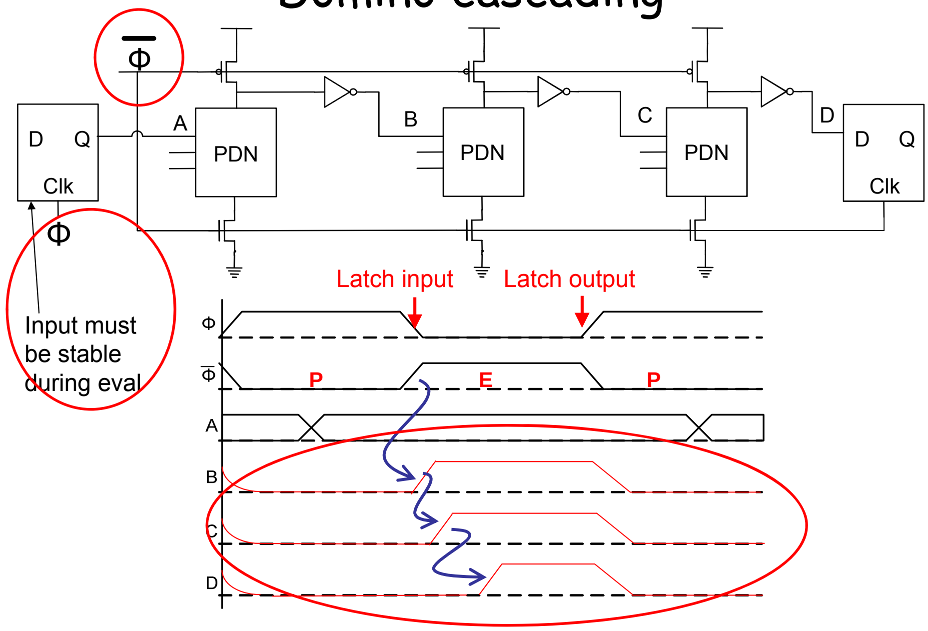
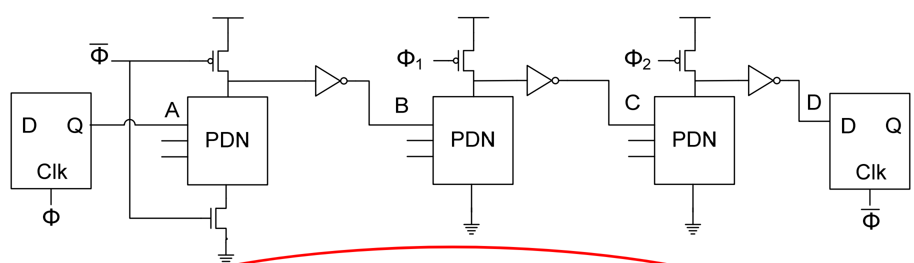


Fig. 2. Improving noise immunity of dynamic logic gates using keeper. (a) Weak always-on keeper [3]. (b) Feedback keeper [4]. (c) HS feedback keeper [5]. (d) Conditional feedback keeper [7].

Domino cascading

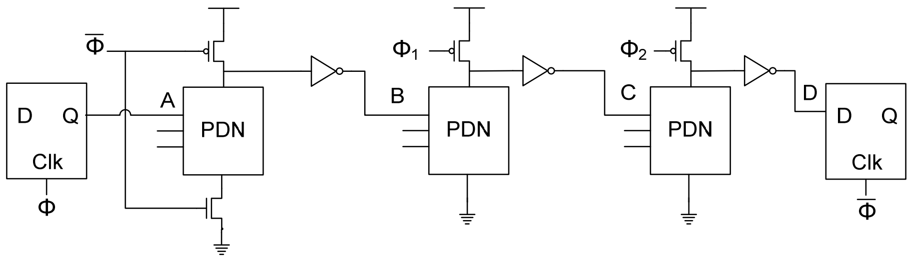


Footless Domino



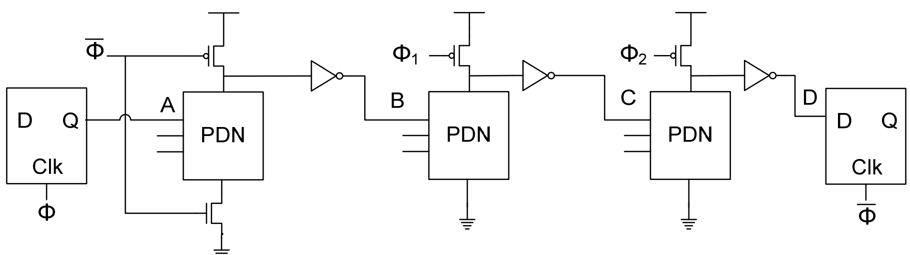
- First stage has footer.
- Footer is not needed for other gates
  - Inputs must precharge low before dynamic node precharge
  - Delay clocks Φ_1, Φ_2

Footless Domino



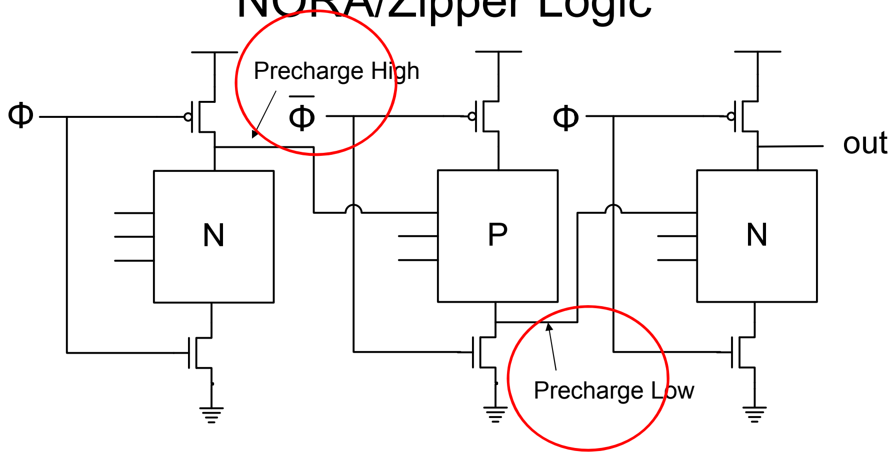
- Advantages:
  - Faster than classic domino → one less NMOS
    - Why is footer necessary in the first stage?
    - Input not guaranteed during precharge

Footless Domino



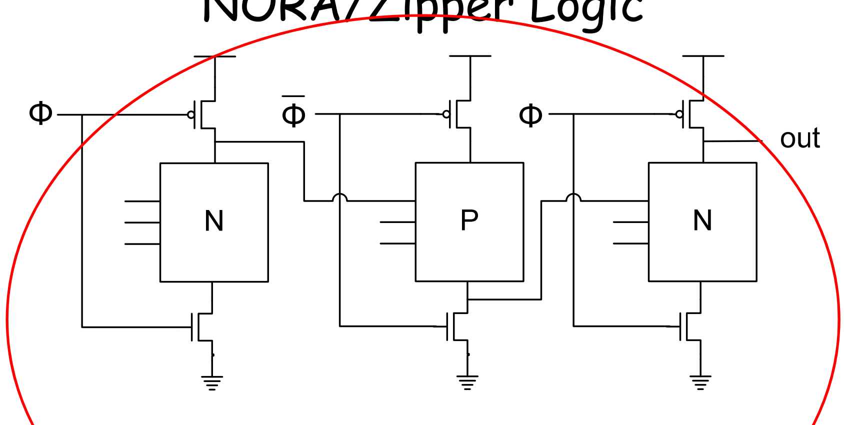
- Disadvantages:
  - Use of different clocks → Can not simply delay the clock (fast inputs during eval)
  - Reduced precharge time for later stages
    - Tradeoff of sizing up PMOS (increase dynamic cap.) vs 1 less NMOS in PDN (footless)
    - But can use a footed stage after a footless stage to recover

NORA/Zipper Logic



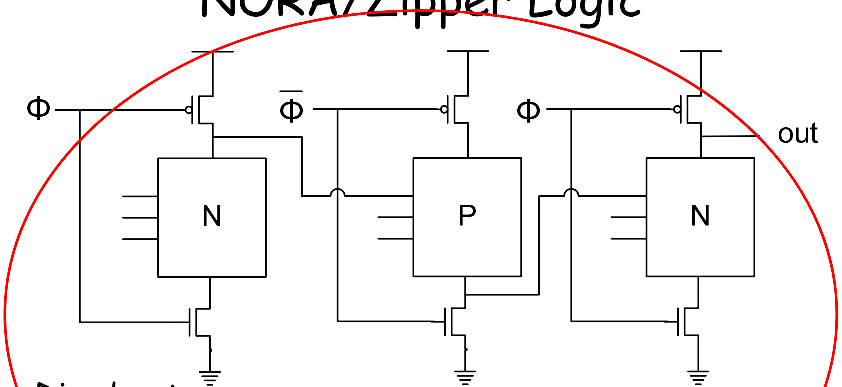
- Cascade basic dynamic gates with different evaluation networks (PDN, PUN)

NORA/Zipper Logic



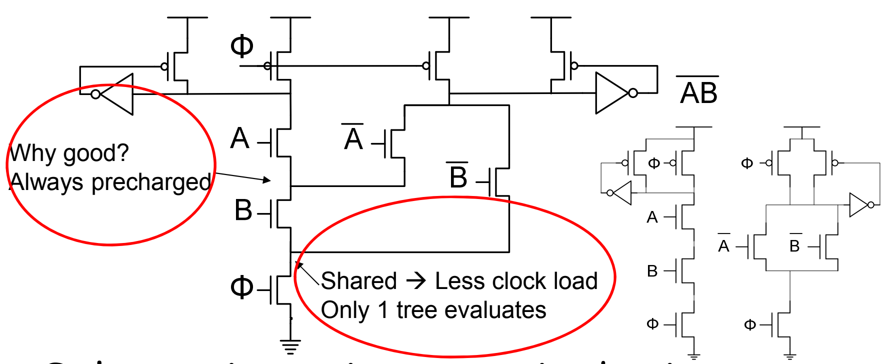
- Advantages:
  - Eliminates the inverter delay (but no drive for long interconnect)
  - Fast

NORA/Zipper Logic



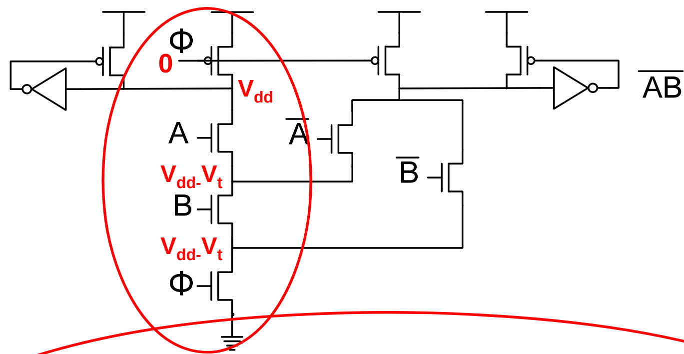
- Disadvantages:
  - Not very good for large output loads (Does not use an output inverter)
  - Big and slow PMOS PUN
  - Bad noise margins → Can add keeper
  - Noise on dynamic node
  - Cannot make arbitrary connections

Dual-Rail Domino



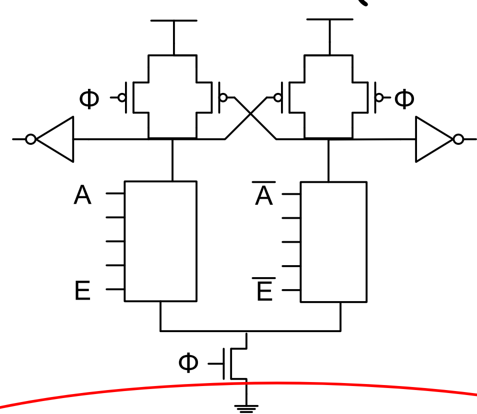
- Only non-inverting gates in domino
  - Dual-rail is required for general logic functions
- Double the number of transistors

Dual-Rail Domino



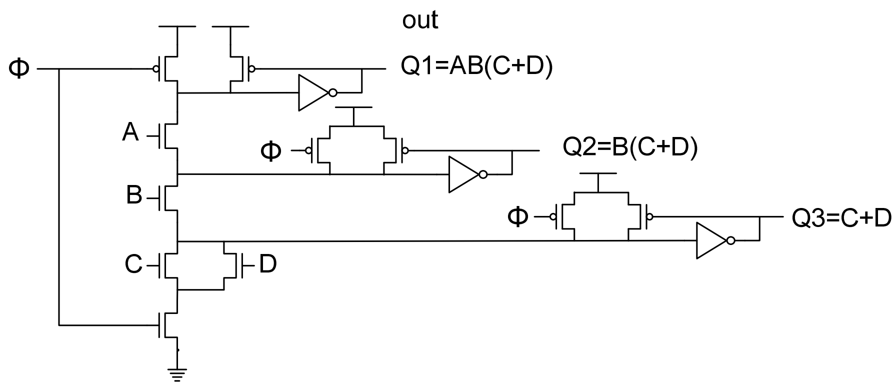
- If evaluation trees are shared, internal nodes are precharged for any input pattern

Dual-Rail Domino (variation)



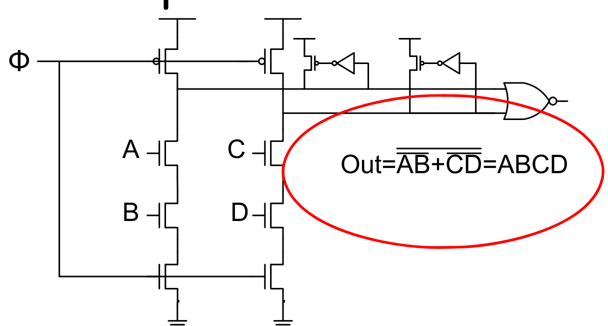
- Not completely safe. Why?
  - No keeper set. On when inputs have not arrived
- No fight

Multiple-Output Domino (MODL)



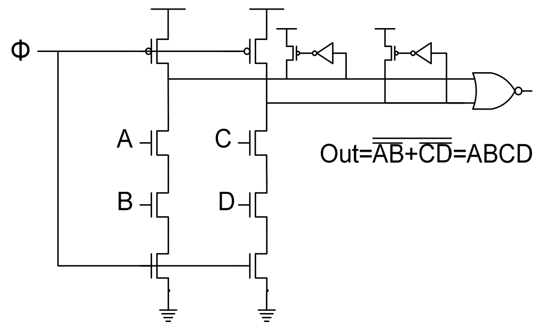
- Implement more logic per domino stage
- Slowdown top output but more work done
- Very common

Compound Domino



- Add static gates to evaluate logic
- Need to add half latches to every output node

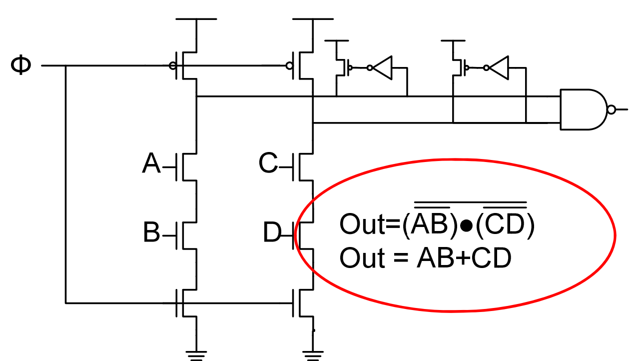
Compound Domino



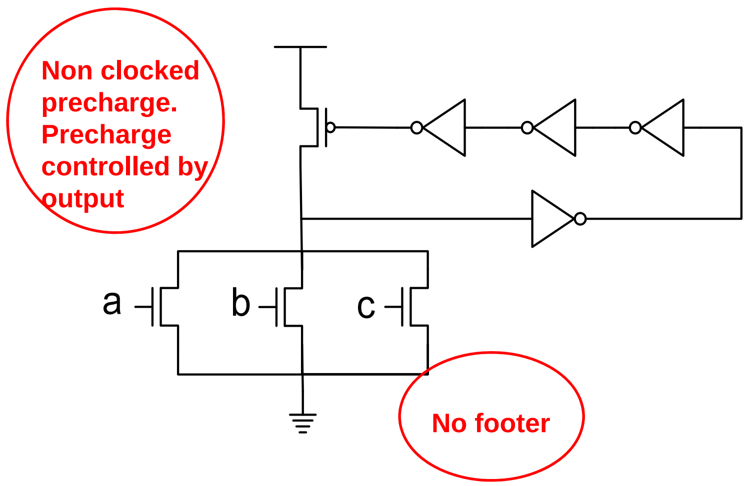
- Reduce the number of transistors in a stack (faster)
  - Due to V_{dd} scaling no more than 4 transistors in a stack ($Vdd{\sim}4{*}V_{dsat}$)
  - But use two PMOS in NOR gate to drive output high

Compound Domino

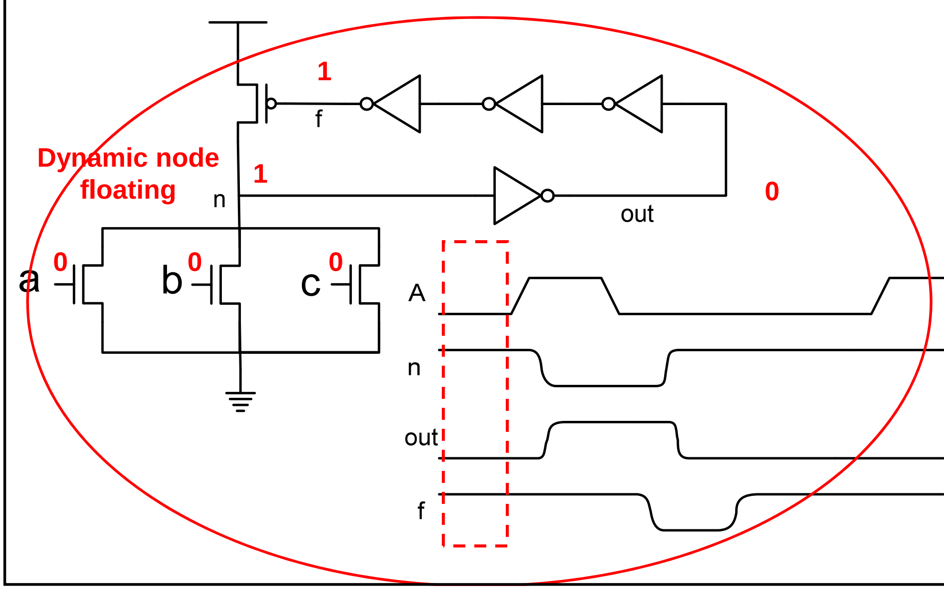
- What static gate can you add?



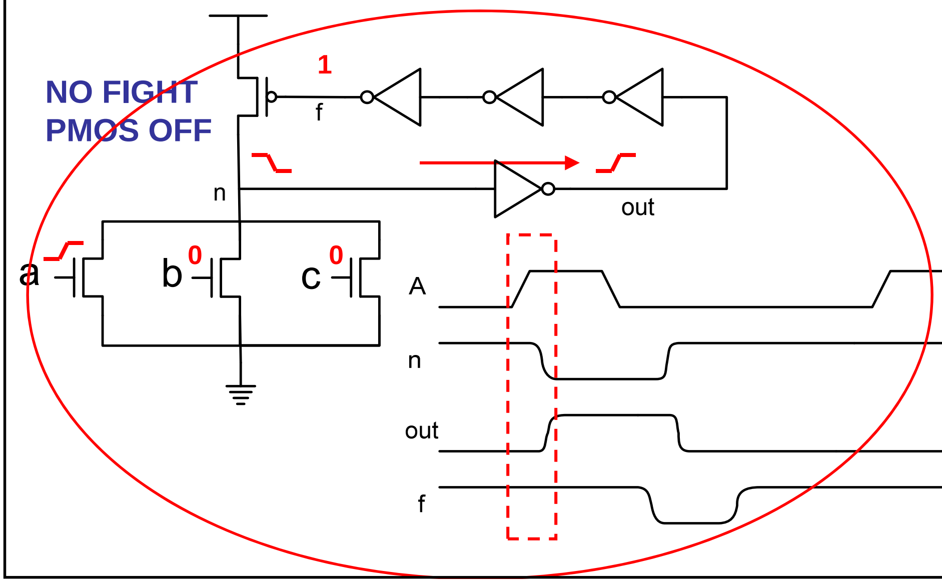
Self Resetting Domino



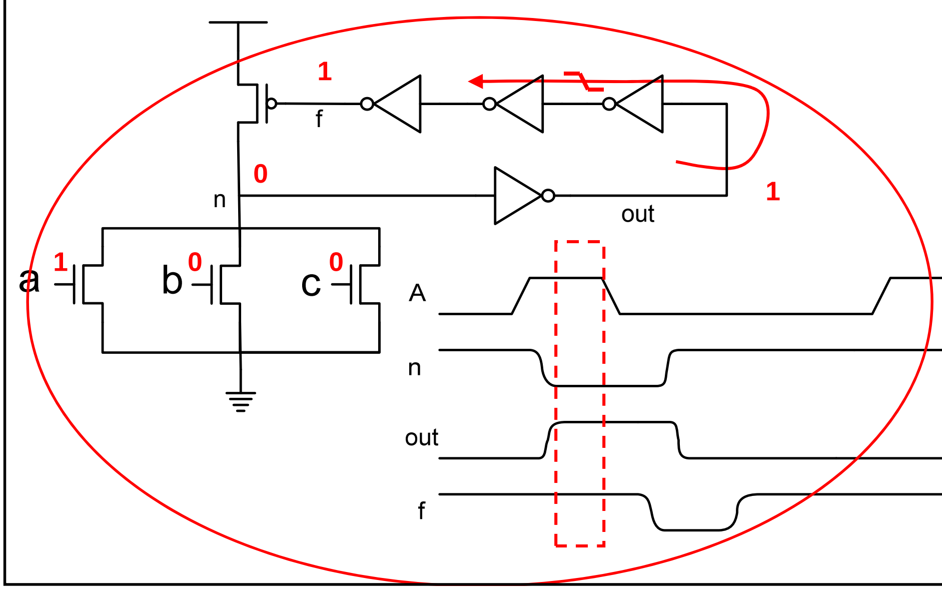
Self Resetting Domino



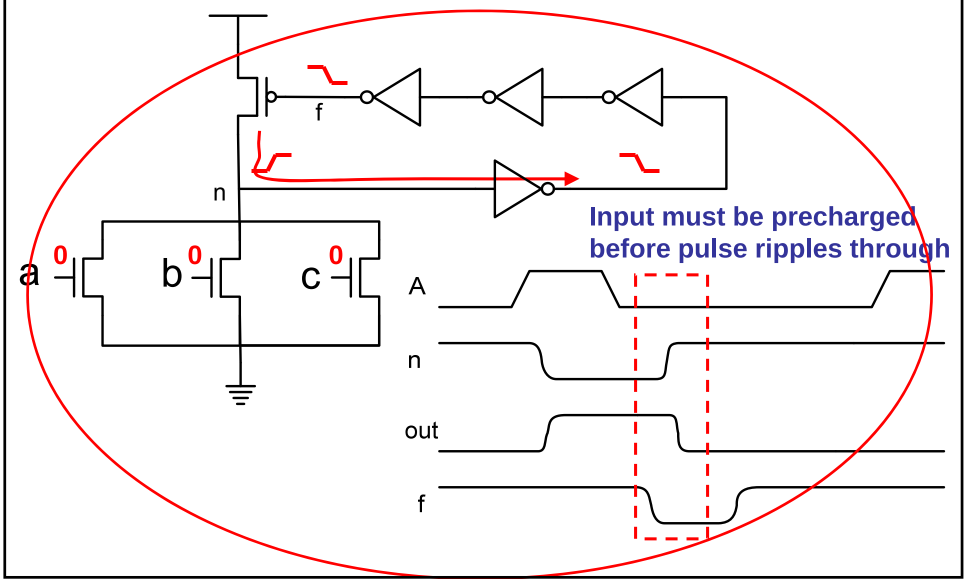
Self Resetting Domino



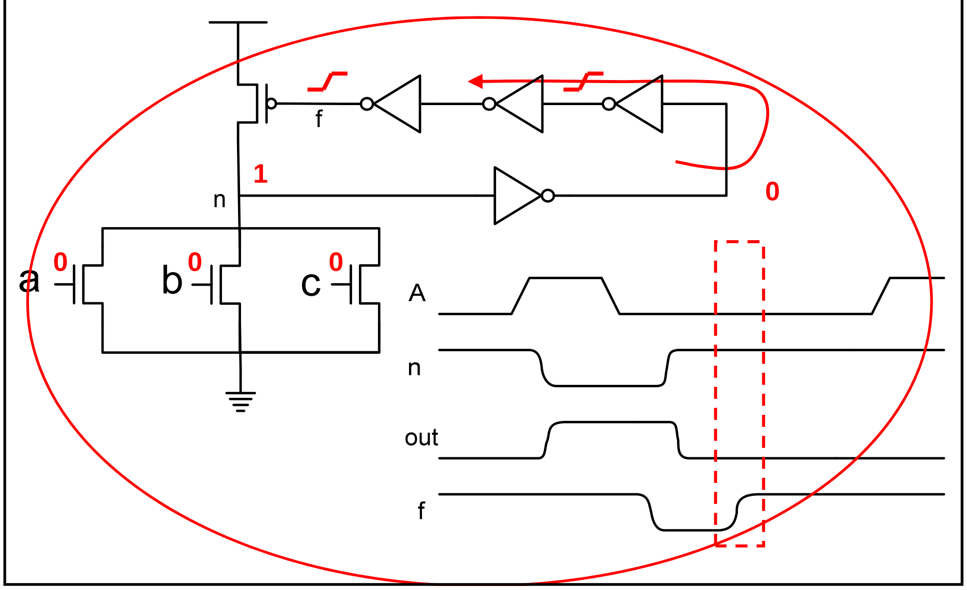
Self Resetting Domino



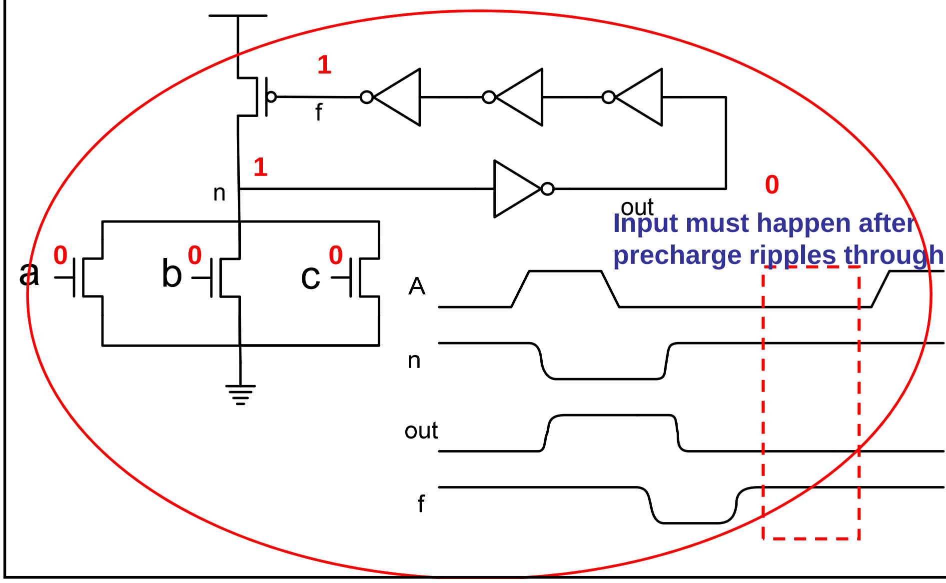
Self Resetting Domino



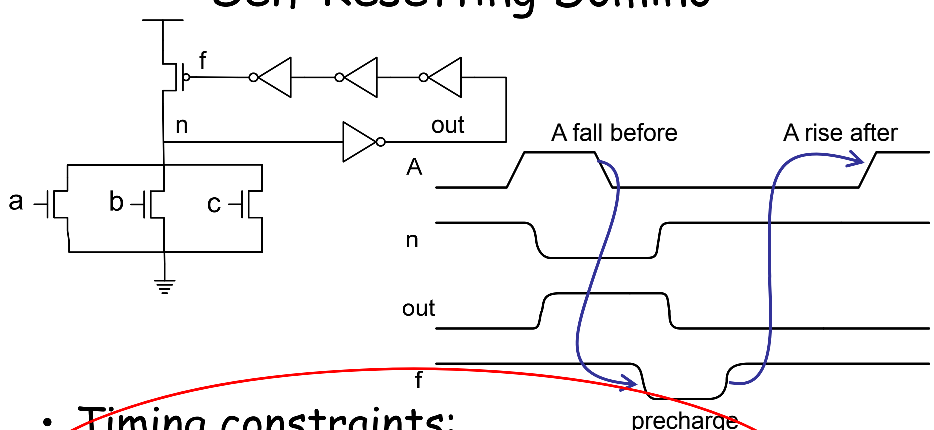
Self Resetting Domino



Self Resetting Domino

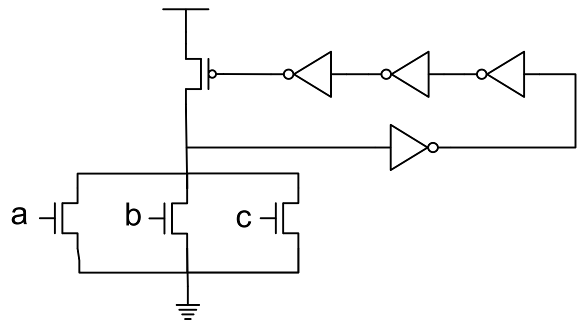


Self Resetting Domino



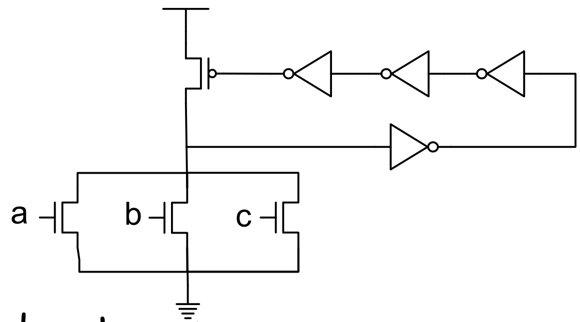
- Timing constraints:
  - f drops after the inputs go low
  - f pulls up before the next input
  - Multiple inputs must line up in time

Self Resetting Domino



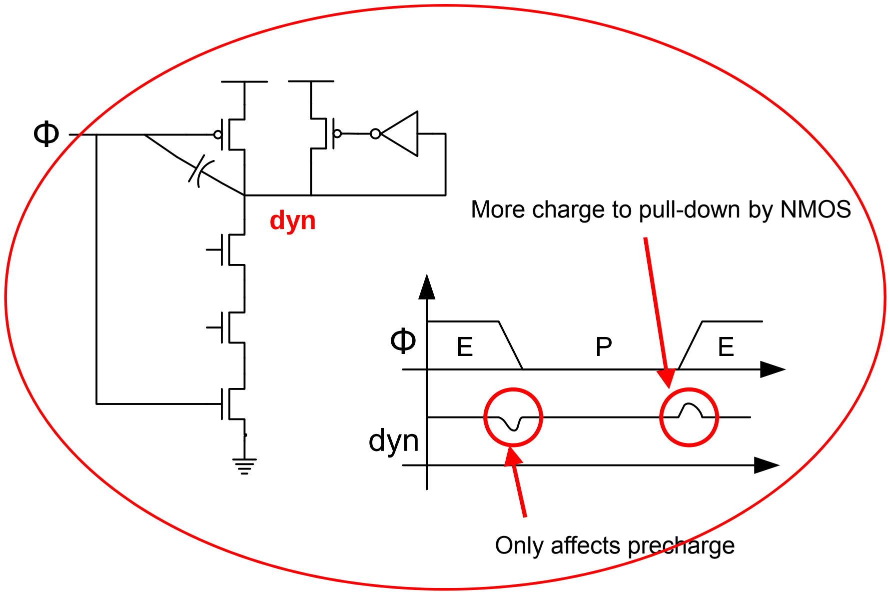
- Advantages:
  - No clock
  - Fast eval because no footer
  - More time for pre-charge than standard footless domino

Self Resetting Domino

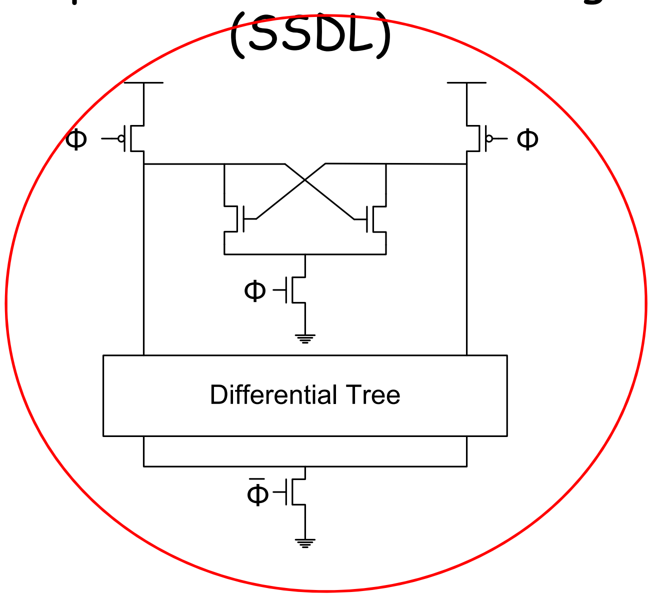


- Disadvantages:
  - Timing constraints
  - Stability after precharge
  - Sensitive to process variations
  - Very difficult in practice → pulse everything

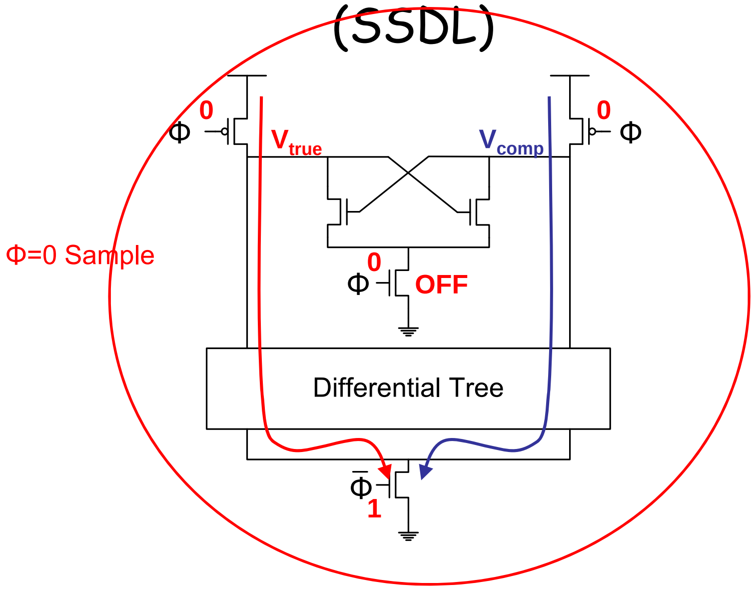
Issues: Miller capacitance



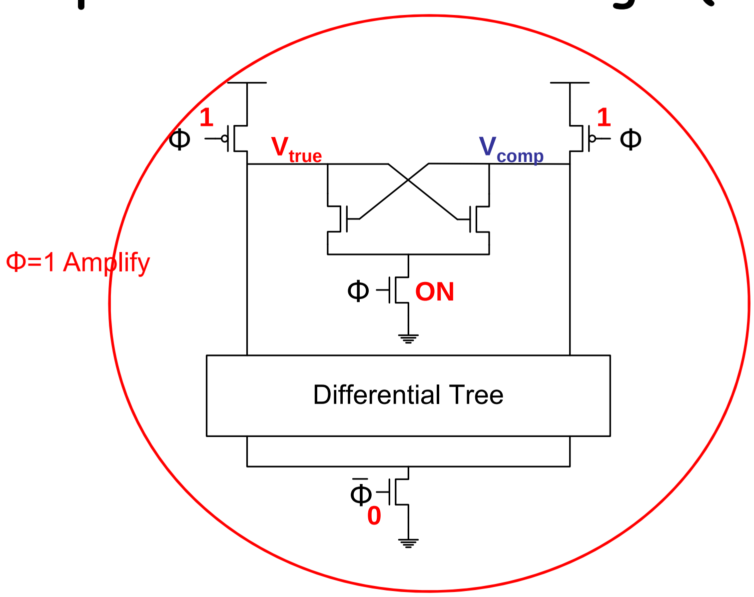
Sample Set Differential Logic (SSDL)



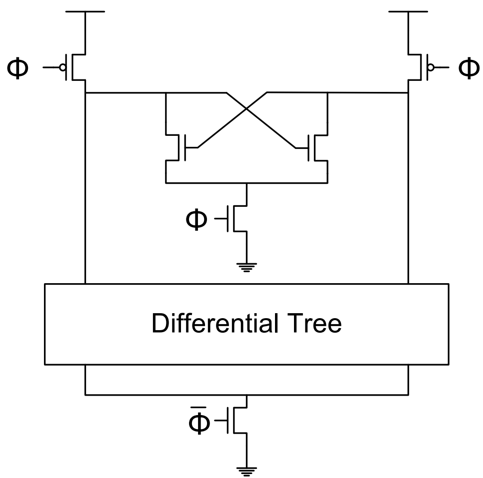
Sample Set Differential Logic (SSDL)



Sample Set Differential Logic (SSDL)

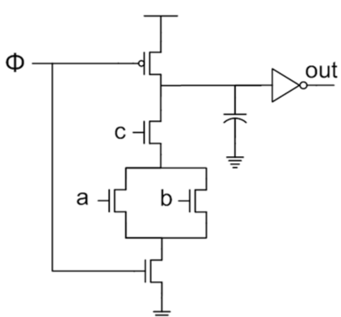


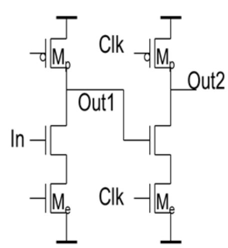
Sample Set Differential Logic (SSDL)

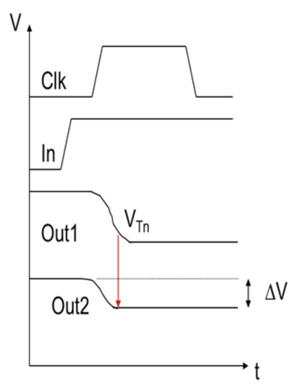


- Advantages:
  - Fast
- Disadvantages:
  - Short circuit power
  - Every gate in one clock phase

Question #1: Why do we use static inverter in domino logic?
Or, why don't we cascade two dynamic logic gates?

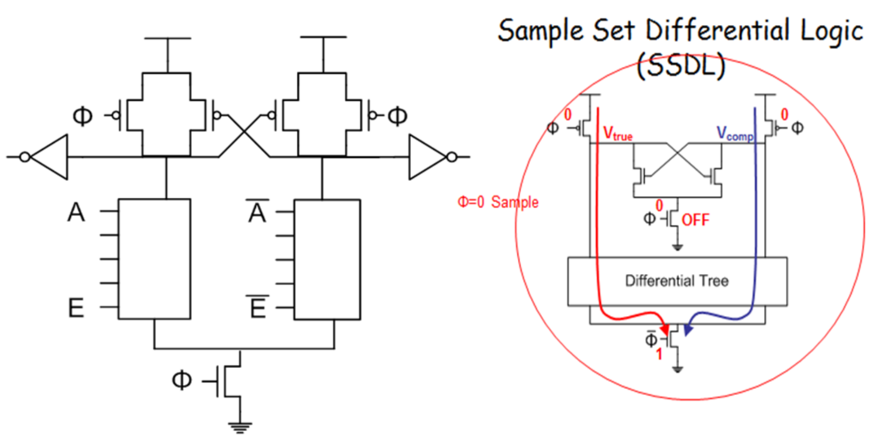






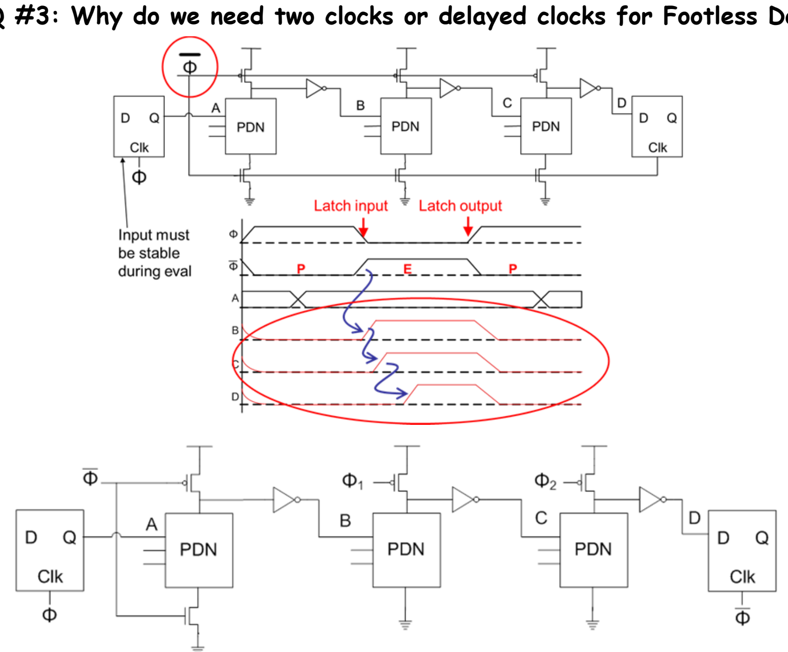
Prof. Pinaki Mazumder at University of Michigan

Question #2: What is the difference between Clocked CVSL and SSDL?



Prof. Pinaki Mazumder at University of Michigan

Q #3: Why do we need two clocks or delayed clocks for Footless Domino?



Lecture 12 –Static Power

WH 5.3

Adapted from Weste & Harris, and Rabaey & Chandrakashan

Prof. Pinaki Mazumder

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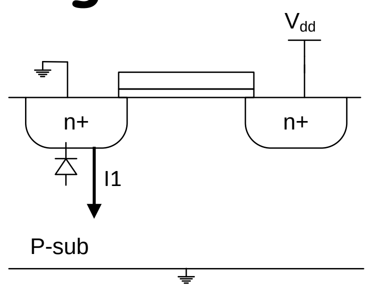
Topics

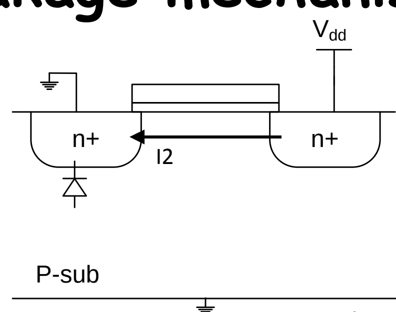
- Leakage mechanisms
  - Subthreshold leakage
  - Gate oxide leakage
- Leakage reduction methods
  - State assignment
  - MTCMOS
  - Dual-Vth design
  - VTCMOS

Leakage mechanisms



- I1: Reverse-bias p-n junction
  - Reverse-biased p-n junctions current: $I_D = I_S\left(e^{\frac{V_D}{V_T}} - 1\right)$
  - Typically < 1 fA/mm^2 (negligible)
  - Depends on area and perimeter of diffusion regions
  - Also: Band to Band tunneling (BTBT)

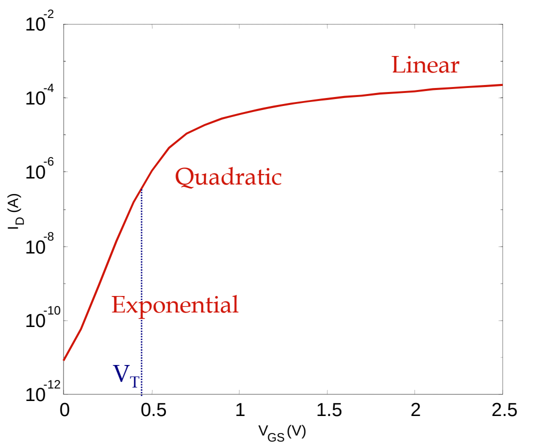
Leakage mechanisms



- I2: Weak inversion or subthreshold leakage current
  - Increased voltage increases drain depletion extending to the source → lowers the potential barrier
  - Dominant effect in modern devices

Sub-Threshold Conduction

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}}\left(1 - e^{-\frac{qV_{DS}}{kT}}\right)$$



The Slope Factor

$$I_D \sim I_0 e^{\frac{qV_{GS}}{nkT}}, \quad n = 1 + \frac{C_D}{C_{ox}}$$

S is ΔV_{GS} for I_{D2}/I_{D1} =10

$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

Typical values for S:
60 .. 100 mV/decade

 Devices

Subthreshold Leakage

- Subthreshold leakage exponential with V_{gs}

$$I_{ds} = I_{ds0} e^{\frac{V_{gs} - V_{t0} + \eta V_{ds} - k_\gamma V_{sb}}{n v_T}}\left(1 - e^{\frac{-V_{ds}}{v_T}}\right)$$

  - n is process dependent – typically 1.3-1.7
  - v_T = kT/q
  - threshold voltage: V_{t0}

See next page for explanation.

$$I_{ds} = I_{off} 10^{\frac{V_{gs} + \eta\left(V_{ds} - V_{dd}\right) - k_\gamma V_{sb}}{S}}\left(1 - e^{\frac{-V_{ds}}{v_t}}\right) \quad S = \left[\frac{d\left(\log_{10} I_{ds}\right)}{dV_{gs}}\right]^{-1} = n v_T \ln 10$$

- S ≈ 100 mV/decade @ room temperature

The threshold voltage decreases with increasing VDS. This effect, called the drain-induced barrier lowering, or DIBL, causes the threshold potential to be a function of VDS

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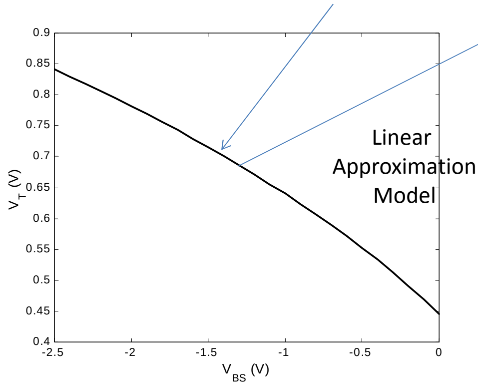
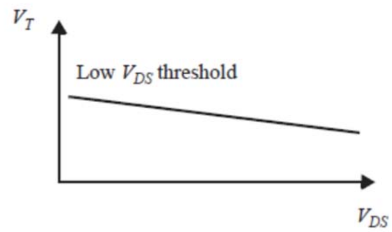
Threshold Voltage

$$V_T = V_{T0} + \gamma\left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}\right) = V_{T0} - K\gamma V_{BS} = -\eta V_{DD} - K\gamma V_{BS}$$





(b) Drain-induced barrier lowering (for low L)

$$I_{ds} = I_{off}\,10^{\frac{V_{gs}+\eta\left(V_{ds}-V_{dd}\right)-k\gamma V_{sb}}{S}}\left(1-e^{\frac{-V_{ds}}{v_t}}\right)$$

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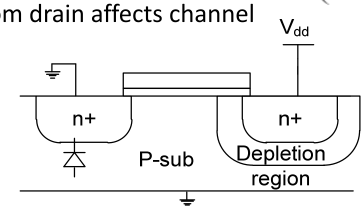
Drain-Induced Barrier Lowering (DIBL)

$$I_{ds} = I_{off}\,10^{\frac{V_{gs}+\eta\left(V_{ds}-V_{dd}\right)-k\gamma V_{sb}}{S}}\left(1-e^{\frac{-V_{ds}}{v_t}}\right)$$

- Electric field from drain affects channel



- More pronounced in small transistors where drain to channel coupling is stronger
- Drain-Induced Barrier Lowering effectively reduces threshold voltage
- High drain voltage causes leakage to increase.

$$V_t' = V_t - \eta V_{ds}$$

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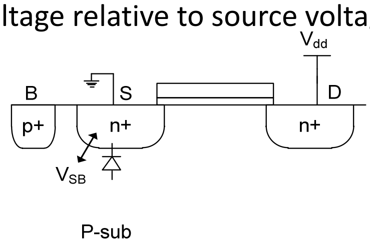
Body Coefficient / Vds Dependence

$$I_{ds} = I_{off} 10^{\frac{V_{gs}+\eta(V_{ds}-V_{dd})-k\gamma V_{sb}}{S}} \left(1 - e^{\frac{-V_{ds}}{v_t}}\right)$$

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

- For NMOS: lower body voltage relative to source voltage (reverse bias)
  - Increases effective Vth
  - Reduces leakage



- Vds dependence
  - For Vds > 4 VT leakage current independent of Vds (other than DIBL)
  - For Vds < 2 VT leakage current drops rapidly with lower Vds

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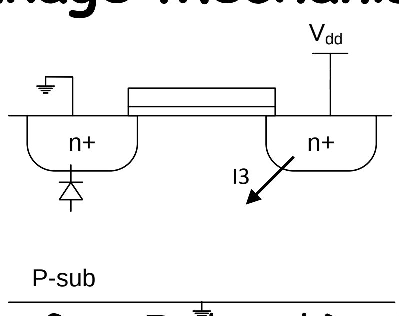
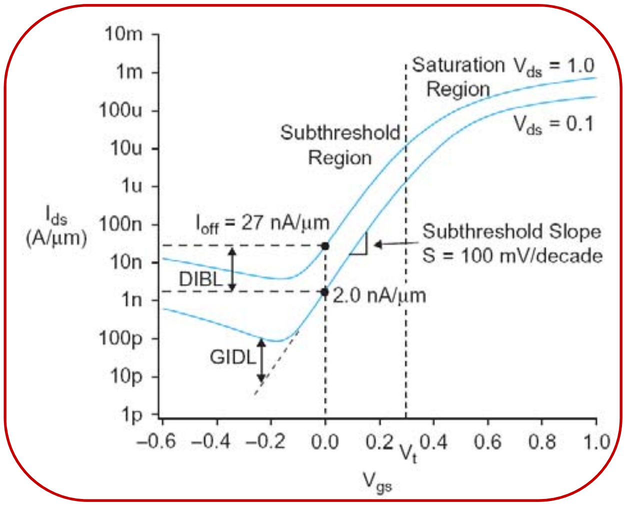
Leakage Mechanisms



- I3: GIDL – Gate Induced Drain Leakage
  - Negative gate / Positive drain
  - Thins out drain depletion causing drain to well leakage near gate
  - Generates a tunneling current

Subthreshold Leakage Roundup



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Subthreshold Leakage

- For V_{ds} > 50 mV

$$I_{sub} \approx I_{off} 10^{\frac{V_{gs} + \eta(V_{ds} - V_{DD}) - k_{\gamma} V_{sb}}{S}}$$

- I_{off} = leakage at V_{gs} = 0, V_{ds} = V_{DD}

Typical values in 65 nm
I_{off} = 100 nA/μm @ V_{th} = 0.3 V
I_{off} = 10 nA/μm @ V_{th} = 0.4 V
I_{off} = 1 nA/μm @ V_{th} = 0.5 V

DIBL coefficient: η = 0.1
Body effect coefficient: k_{γ} = 0.1
S = 100 mV/decade

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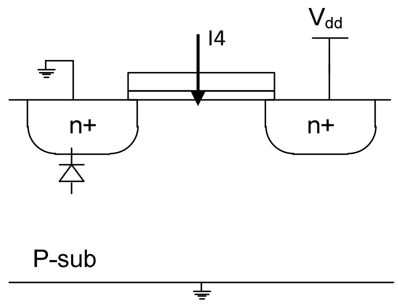
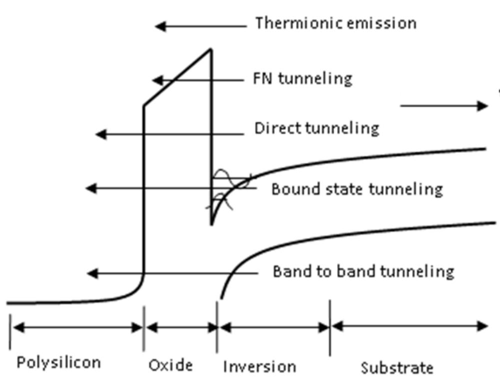
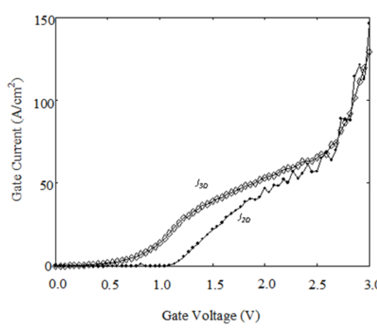
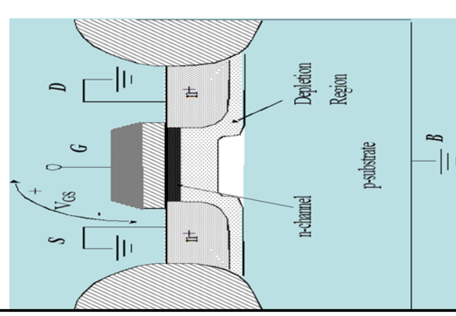
Leakage Mechanisms

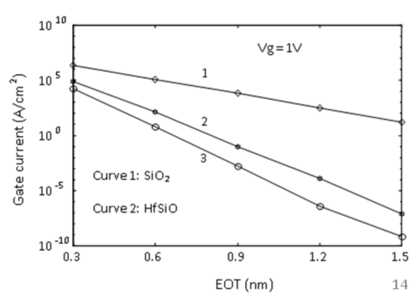


- I4: Gate Oxide tunneling
  - Thinner oxides cause an increase tunneling
  - Highly dependent on oxide material and thickness









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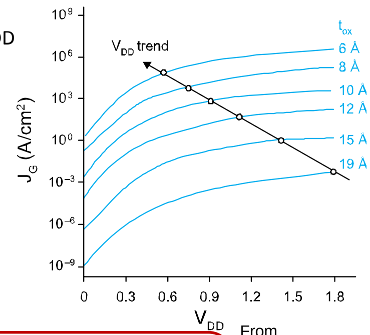
Gate Leakage

- Carriers tunnel thorough very thin gate oxides
- Exponentially sensitive to t_{ox} and V_{DD}

$$I_{gate} = WA\left(\frac{V_{DD}}{t_{ox}}\right)^2 e^{-B\frac{t_{ox}}{V_{DD}}}$$

  - A and B are tech constants
  - Greater for electrons
    - So NMOS gates leak more



From [Song01]

- Negligible for older processes (t_{ox} > 30 Å)
- Critically important at 65 nm and below (t_{ox} ≈ 12 Å)
  - But: improved again with High-K metal gate transistors

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Fundamental Leakage Levers

- Increase Vth: ~10x leakage reduction for every 100mV
  - But: bad for delay

$$\tau \propto \frac{V_{dd}}{(V_{dd} - V_t)^{\alpha}}$$

- Reduce temperature: ~5.2X reduction / 10 degree C

- Stacking transistors

Stack Effect

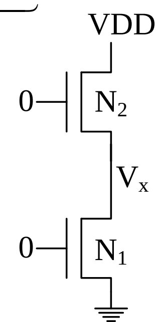
- Series OFF transistors significantly reduce leakage
  - $V_x > 0$, so N2 has negative V_{gs}

$$I_{sub} = \underbrace{I_{off} 10^{\frac{\eta(V_x - V_{DD})}{S}}}_{N1} = \underbrace{I_{off} 10^{\frac{-V_x + \eta((V_{DD} - V_x) - V_{DD}) - k_\gamma V_x}{S}}}_{N2}$$

$$V_x = \frac{\eta V_{DD}}{1 + 2\eta + k_\gamma}$$

$$I_{sub} = I_{off} 10^{\frac{-\eta V_{DD}\left(\frac{1+\eta+k_\gamma}{1+2\eta+k_\gamma}\right)}{S}} \approx I_{off} 10^{\frac{-\eta V_{DD}}{S}}$$

  - Leakage through 2-stack reduces ~10x



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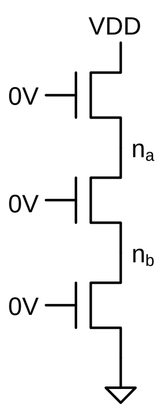
Stacking and Leakage

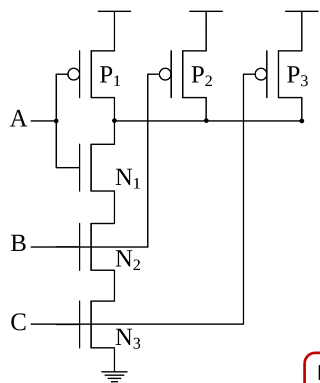


# of stack SVT	Leakage current (pA)	Reduction
1	258	X 1
2	36.1	X 7.1
3	19.8	X 13

# of stack HVT	Leakage current (pA)	Reduction	Reduction per HVT
1	1.25	X 206	X 1
2	0.185	X 1394	X 6.8
3	0.122	X 2115	X 10.3

State Assignment

- Only a few states have significant leakage
  - Dominant leakage states have only one transistor OFF in any path from V_{dd} to Gnd



A	B	C	Leakage Current	Leaking Transistors
0	0	0	10.537	N1, N2, N3
0	0	1	18.534	N1, N2
0	1	0	18.234	N1, N3
0	*1*	*1*	*135.772*	*N1*
1	0	0	20.350	N2, N3
1	*0*	*1*	*102.672*	*N2*
1	*1*	*0*	*100.970*	*N3*
1	*1*	*1*	*192.174*	*P1, P2, P3*

Leakage currents in pA. NMOS width = 480nm PMOS width = 320nm

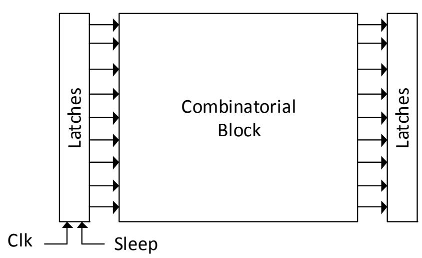
State Dependence of Leakage

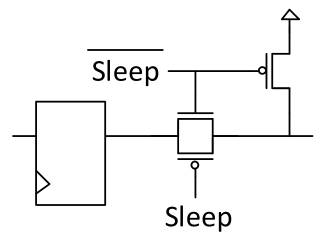
- Circuit state is partially unknown in sleep state
- Leakage variation is less for entire circuit than for individual gates

	Leakage Current (nA)			Max / Min
	Min	Mean	Max	
Adder1	256.8	283.1	309.8	1.2
Control	33.8	45.97	60.23	1.78
Decoder	1702.5	1914.3	2122.1	1.25
Nand4	0.07	0.76	7.1	101.4
OAI21	0.84	7.73	17.78	21.2
Tinv	0.37	1.89	5.76	15.6
AOI21	2.44	8.51	17.23	7.1

State Assignment

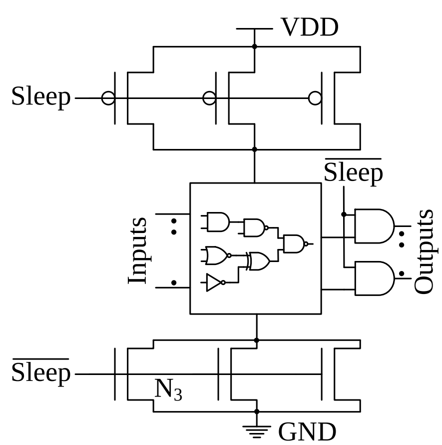
- Since the leakage of a logic gate depends on its input, find the input to a combinational circuit that minimizes leakage
  - 30%-40% leakage variation depending on input vector
- Modify latches
  - Sleep signal moves pre-determined values as inputs into combinational circuit





Power Gating – aka MTCMOS

- Turn OFF power to blocks when they are idle
  - Use virtual V_{DD} and Gnd
  - "Gate" outputs to prevent invalid logic levels at next block
  - Use HVT header/footer
- Voltage drop across sleep transistor during normal operation
  - Size the transistor wide enough to minimize impact
- Switching sleep transistor costs dynamic power
  - Only justified when circuit sleeps long enough



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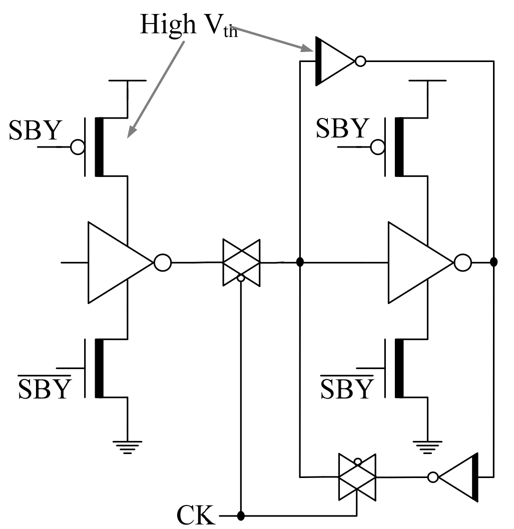
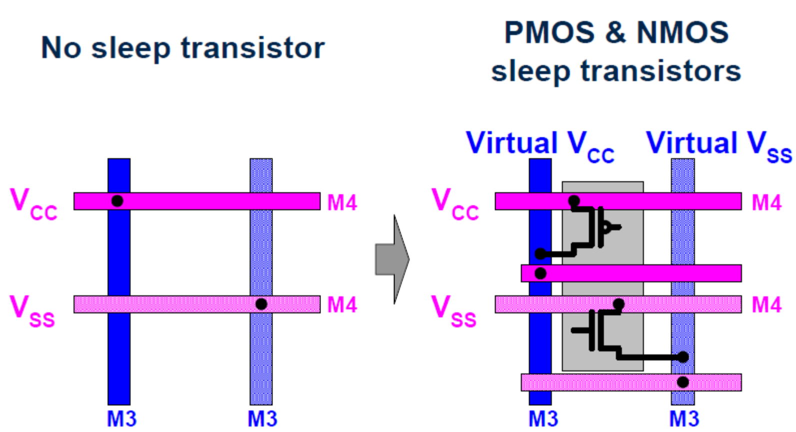
State Retaining MTCMOS Latch



[Mutoh, et al., JSSC 8/95]

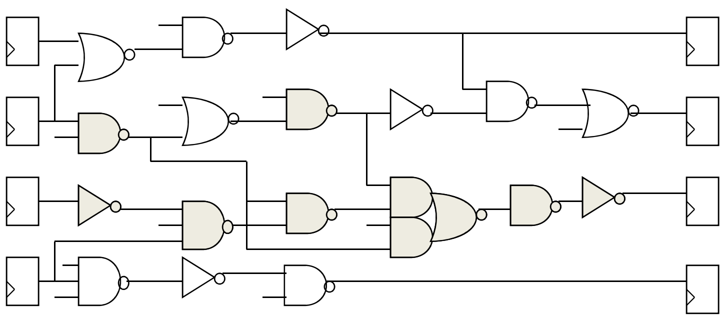
Sleep Transistor Layout



Tschanz, ISSCC'03

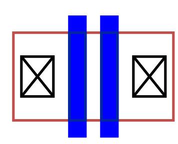
Dual-Thresholds Inside a Logic Block

- Minimum energy consumption is achieved if all logic paths are critical (have the same delay)
- Use lower threshold on timing-critical paths
  - Assignment can be done on a per gate or transistor basis; no clustering of logic is needed
  - No level converters needed



V_{th} Assignment Granularity

- V_{th} assignment can be performed at different levels of granularity
  - Gate level assignment
  - Pull up network / Pull down network based assignment (half gate)
    - Single V_{th} in pull up or pull down networks
  - Stack based assignment
    - Single V_{th} in series connected transistors
  - Individually assignment within transistor stacks
    - Possible area penalty (see right)



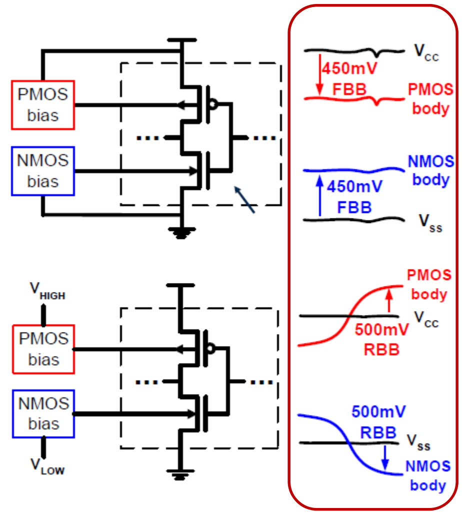
Design rule constraint for different V_t assignment

- Number of library cells increases with finer control
  - Better leakage / delay trade-off
  - Harder for synthesis tools to handle

Dynamic Body Bias

Active mode
Forward body bias

Idle mode
Reverse body bias
Triple well needed



Variable Threshold CMOS (VTCMOS)

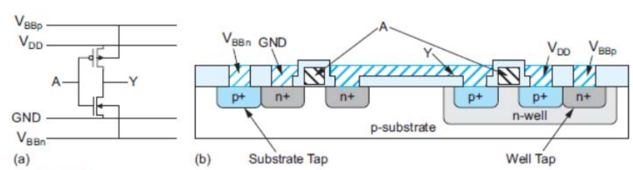
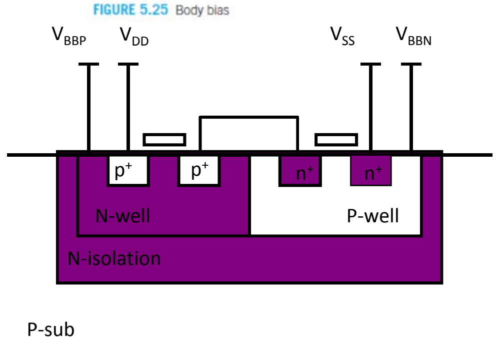
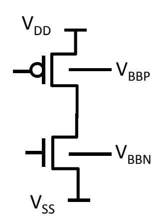
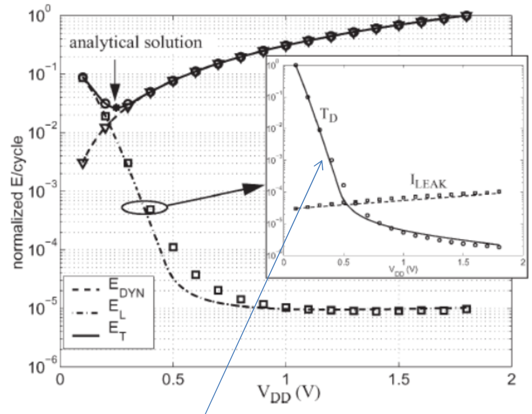


FIGURE 5.25 Body bias

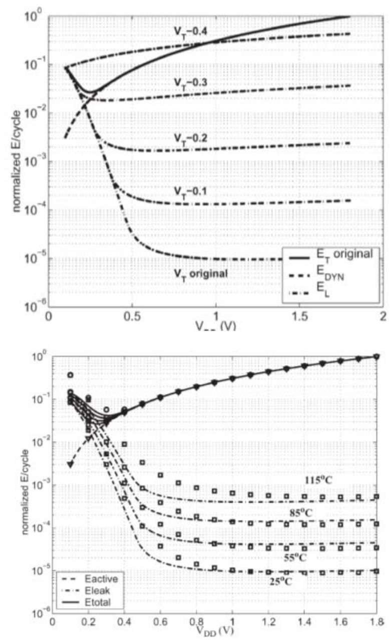




Energy Dissipation at Subthreshold and Superthreshold Voltages

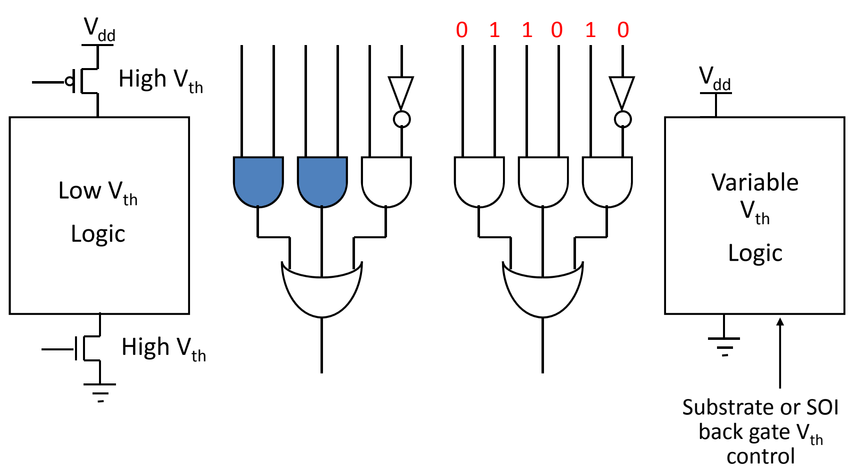


$$t_d = \frac{KC_g V_{DD}}{I_{o,g} e^{(V_{GS}-V_{T,g})/nV_{th}}}$$



Leakage Reduction Overview

MTCMOS | Dual Threshold | State Assignment | Variable V_t



Source: [Johnson, et al., DAC99]

Power and Energy Design Space

	Constant Throughput/Latency		Variable Throughput/Latency
Energy	Design Time	Non-active Modules	Run Time/Adaptive
Active	Logic Design Sizing Low C circuits	Clock Gating	DVFS (Dynamic Freq, Voltage Scaling)
Leakage	Multi-V_{th} Stack effect	Sleep Transistors State assignment Variable V_{th}	Variable V_{th}

Processor Power Management

- Software power control - power management

DOZE	Most units stopped except on-chip cache memory (cache coherency)
NAP	Cache also turned off, PLL still on, time out or external interrupt to resume
SLEEP	PLL off, external interrupt to resume

Deeper sleep mode consumes less power

Deeper sleep mode requires more latency to resume

Mode	66Mhz	80Mhz
No power mgmt	2.18W	2.54W
Dynamic power mgmt	1.89W	2.20W
DOZE	307mW	366mW
NAP	113mW	135mW
SLEEP	89mW	105mW
SLEEP without PLL	18mW	19mW
SLEEP without clock	2mW	2mW

10 cycles to wake up from SLEEP

100us to wake up from SLEEP+

Source: Irwin, 2000

Atom Processor Power Management

C0 HFM:
2 GHz, 1V, 2W

C0 LFM:
0.6 GHz, 750 mV

C6: Sleep
80 mW

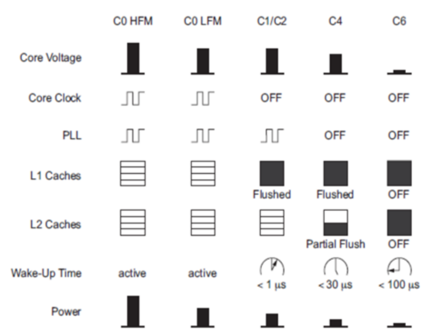
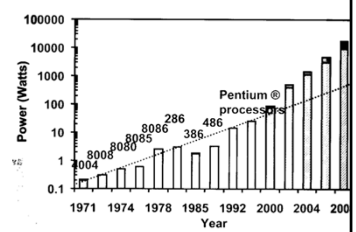


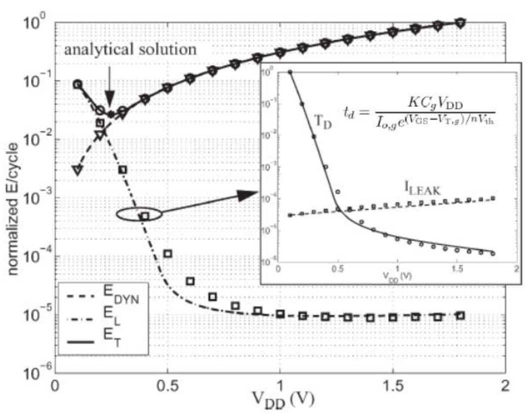
FIGURE 5.30 Atom power management modes (© 2009 IEEE.)

Conclusions

- Lots of recent work on circuit and technology techniques to reduce static power
  - Standby mode leakage reduction can be orders of magnitude, may lose state, takes time to switch in and out of standby mode
  - Active mode leakage reduction is a tougher problem, smaller savings (<50% typically), must be ready for inputs to toggle at any time



Energy Dissipation at Subthreshold and Superthreshold Voltages



$$\frac{\partial E_T}{\partial V_{DD}} = 2C_{eff}V_{DD} + 2W_{eff}L_{DP}KC_gV_{DD}e^{-V_{DD}/nV_{th}} + \frac{-W_{eff}L_{DP}KC_gV_{DD}^2}{nV_{th}}e^{-V_{DD}/nV_{th}} = 0.$$

$$V_{DDopt} = nV_{th}(2 - \text{lambert}W(\beta))$$

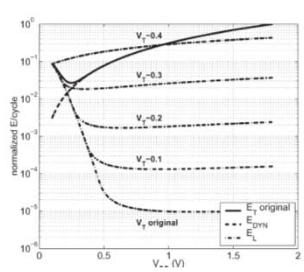
$$\beta = \frac{-2C_{eff}}{W_{eff}L_{DP}KC_g}e^2 > -e^{-1}.$$

Lambert W function, $W = \text{lambert}W(x)$ solution to the equation $We^W = x$,

$$V_{Topt} = V_{DDopt} - nV_{th}\ln\left(\frac{fKC_gL_{DP}V_{DDopt}}{I_{o,g}}\right).$$

$$I_{SUB} = I_o e^{(V_{GS}-V_T)/nV_{th}} \quad I_o = \mu_o C_{ox}\frac{W}{L}(n-1)V_{th}^2$$

$$\begin{aligned} E_{DYN} &= C_{eff}V_{DD}^2 \\ E_L &= W_{eff}I_{o,g}e^{-V_{T,g}/nV_{th}}t_dL_{DP}V_{DD} \\ &= W_{eff}KC_gL_{DP}V_{DD}^2e^{-V_{DD}/nV_{th}} \\ E_T &= E_{DYN} + E_L \\ &= V_{DD}^2\left(C_{eff} + W_{eff}KC_gL_{DP}e^{-V_{DD}/nV_{th}}\right). \end{aligned}$$



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