Overview

• Logistics - Go over syllabus & Course Overview
• Digital ICs are omnipresent: Applications
• The first computers were huge and slow
• Modern Microprocessors and DSP’s
  - Trends of power, complexity, productivity
  - Moore’s law
• Different styles of VLSI Chip Design
• What I expect you to learn in this class
Logistics 1

- Lecture Tuesday/Thursday Chrysler
- Syllabus
- Website is at: https://ctools.umich.edu
  You need your umich password (not EECS!)

- Friday discussion sections led by the GSI, Gregory Brandon
  - Review lecture topics, go through examples, answer questions
  - I may offer supplementary lectures during the discussion hours

- Software labs - Eldo based
  - Will prepare you for future classes where Accusim is used
  - No set time for these labs - do on your own schedule
  - Lab Reports will be, however, due on the indicated dates

Logistics 2

Textbook:
Digital Integrated Circuits: A Design Perspective, 2nd edition by Jan Rabaey, Anantha Chandrakasan, and Bora Nikolic

Lecture notes will be posted online a couple of days in advance before class sessions

I will supplement the ppt slides with handouts from other sources throughout the semester
**Distribution of Points**

- Pay 100% attention to lectures + Discussions
- Read class notes + Handouts regularly
- Try all Homework Problems
- Try all Lab Expts
- Do Design Project

*Late Homework Policy:* 24 hours with 30% penalty and after that no credits.
All Pervasiveness of Digital Integrated Circuits

Global Market Size of Semiconductor Devices:
$250 Billion and heading towards $1 Trillion

Consumer Electronics: Digital TV, DVD, PDA, Video Camera, Games, …
Computers: Notebook, Desktop, Clustered PCs, …
Communications: Cell Phone, Answering Machines, …
Appliances: Washing Machine, Microwave Cooker, Thermostat, ….

Merging of Technologies

Computers
  Embedded Processors
  Microcontrollers
Communication
  Cell Phone
  Internet Voice Service
Consumer Electronics
  Video Camera
  Personal Organizer
  Games
Cell Phones For Voice + Data

Flash Memory Density Growth in Japan

1998 1999 2000 2001 2002
VOICE ONLY PACKETIZED DATA 256 COLOR 4K COLOR JAVA APPS.

Convergence increases silicon usage

Source: NEC, Intel

Converged Cell Phone Integration Opportunities

Communications  Computing  Memory

Radio (RF)  Signal  CPU  Display  Flash
Processing  DSP  Core  Peripherals
Rx  Analog  Power  CMOS (Digital)
Tx  Baseband  Mgmt.
PA

CMOS (Digital, Analog)  CMOS (Digital)  CMOS (Memory)
GaAs/SiGe (for RF)  Display

Intel Developer Forum Spring 2003
Some History

**Detailed History**

- **Invention of the transistor (BJT)** 1947
  - Shockley, Bardeen, Brattain – Bell Labs

- **Single-transistor integrated circuit** 1958
  - Jack Kilby – Texas Instruments

- **Invention of CMOS logic gates** 1963
  - Wantlass & Sah – Fairchild Semiconductor

- **First microprocessor (Intel 4004)** 1970
  - 2,300 MOS transistors, 740 kHz clock frequency

**Very Large Scale Integration** 1978
- Chips with more than ~20,000 devices

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**Larger chips to keep up with more transistors**

Graph showing the die size in mm from 1970 to 2010 with a trend line indicating ~7% growth per year and ~2X growth in 10 years.
## Design Trends

- Smaller transistors
- Bigger chips (dies)
- Faster clock frequencies
- More complex designs
- Higher power consumption
### SIA Roadmap of IC Technology

#### The MARCH Continues

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<tbody>
<tr>
<td><strong>Channel length [nm]</strong></td>
<td>250</td>
<td>180</td>
<td>130</td>
<td>100</td>
<td>70</td>
<td>50</td>
<td>35</td>
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<tr>
<td><strong>Short wire Pitch [μm]</strong></td>
<td>0.75</td>
<td>0.54</td>
<td>0.39</td>
<td>0.3</td>
<td>0.21</td>
<td>0.15</td>
<td>0.10</td>
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<tr>
<td><strong>μP Chip Size [mm²]</strong></td>
<td>300</td>
<td>340</td>
<td>430</td>
<td>520</td>
<td>620</td>
<td>750</td>
<td>901</td>
</tr>
<tr>
<td><strong>μP Transistors [10⁶]</strong></td>
<td>11</td>
<td>21</td>
<td>76</td>
<td>200</td>
<td>520</td>
<td>1400</td>
<td>3600</td>
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<tr>
<td><strong>Global Clock [MHz]</strong></td>
<td>375</td>
<td>1200</td>
<td>1600</td>
<td>2000</td>
<td>2500</td>
<td>3000</td>
<td>3674</td>
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<tr>
<td><strong>Local Clock [MHz]</strong></td>
<td>70</td>
<td>90</td>
<td>130</td>
<td>160</td>
<td>170</td>
<td>175</td>
<td>183</td>
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<tr>
<td><strong>Dissipation [Watt]</strong></td>
<td>2.1</td>
<td>1.7</td>
<td>1.35</td>
<td>1.0</td>
<td>0.75</td>
<td>0.55</td>
<td>0.4</td>
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<tr>
<td><strong>Min Logic Vdd [V]</strong></td>
<td>0.8</td>
<td>1.7</td>
<td>3.3</td>
<td>5</td>
<td>9.2</td>
<td>17</td>
<td>25</td>
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<tr>
<td><strong>Wire length [km]</strong></td>
<td>6</td>
<td>6.7</td>
<td>7</td>
<td>7.8</td>
<td>8.9</td>
<td>9</td>
<td>10</td>
</tr>
<tr>
<td><strong>Wiring levels</strong></td>
<td>6</td>
<td>6-7</td>
<td>7</td>
<td>7-8</td>
<td>8-9</td>
<td>9</td>
<td>10</td>
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<td><strong>ASIC Package Pins</strong></td>
<td>1100</td>
<td>1400</td>
<td>1900</td>
<td>2600</td>
<td>3600</td>
<td>5000</td>
<td>6700</td>
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<tr>
<td><strong>DRAM bits/chip</strong></td>
<td>267M</td>
<td>1.07G</td>
<td>4.29G</td>
<td>17.2G</td>
<td>68.7G</td>
<td>275G</td>
<td>1.10T</td>
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<tr>
<td><strong>μP cost/transistor</strong></td>
<td>30</td>
<td>17</td>
<td>508</td>
<td>206</td>
<td>1.1</td>
<td>0.5</td>
<td>0.22</td>
</tr>
</tbody>
</table>

*Transistor speed > 250 GHz Circuit speed for μP < 10 GHz*

### Transistor Scaling and Research Roadmap

- **90nm Node** 2003
- **65nm Node** 2005
- **45nm Node** 2009
- **32nm Node** 2011
- **22nm Node** 2015

**2015-2019 Research**

- III-V Device Prototype Research
- Nanowire Prototype Research
- Non-planar Tri-Gate Architecture Option
- High-K & Metal-Gate Options
- Uni-axial Strain
- SiGe/S/D PMOS
- 1.2nm Ultra-thin SiO2

Robert Chau, Intel, ICSICT 2004
What does all this mean?

- Chips are getting bigger and harder to design
  - Hierarchical design flow
  - Good design principles needed
- Knowledge of fundamental design practices
- Ability to develop innovative design techniques

- This course is the first step in learning these design principles
  - Next step = 427, then 627, followed by Intel, IBM, or your own start-up

Design Abstraction Levels

EECS 470 & 627 (Verilog)
EECS 427 (Manual)
EECS 270
EECS 312
EECS 320

Verilog & Manual
Design of Large Digital Systems
Device & Circuit Equations
Device Equations
What you will learn in this class

• Transistor level digital circuit design
• How to design and analyze the fundamental building blocks of all large-scale digital ICs
  - CMOS combinational gates
  - Sequential (storage) elements
  - Dynamic circuit families
  - Memories
  - Interconnect-related issues
• Based on the key quality metrics of circuit design:
  - Speed, area, power, cost, reliability

Reading Exercises

• Read Sections 1.1 & 1.2 (pp. 4-15) of your textbook for subject matters of Today's Lecture

• Next lecture: Review of CMOS Logic operation
• Lecture Slides are posted. Study the Slides.
• Read in advance: Textbook pp. 87-115.
EPILOGUE

Main Message of Today’s Lecture:

• CMOS Juggernaut will Continue to Scale down to 20 nm and beyond for another 15 to 20 years!

• No replacement of CMOS is in sight. Non-Silicon Nanotechnologies such as CNT, Moltronics, NMR, Ion-Trap Quantum Computing, … are only good for research.

• Device Physics, Higher Order Physical Effects, Circuit Analysis, Circuit Modeling to Account for Discrepancies Between Analytical Models and SPICE Simulations are Extremely Important for the Nano-scaled CMOS Chip Design. You must learn them in EECS 312 and EECS 427.

Lecture on Sequential Elements

Pinaki Mazumder

Lecture #20

EECS 312
Reading: 7.1.1, 7.2-7.3.1
Exclude 7.2.4
A TYPICAL PROCESSOR ARCHITECTURE

ALU

Shifter

registers

MAR

MDR

PC

16-bit EECS 427 ISA Processor

ALU

Shifter
Sequential Logic

2 storage mechanisms
- positive feedback
- charge-based

Positive Feedback: Bi-Stability

Metastable Point
Meta-Stability

A small perturbation Causes FF to go to A.

Gain should be larger than 1 in the transition region.

Types of Sequential Elements

- **Latch**
  - stores data when CLK is either high or low

- **Register**
  - stores data when CLK rises/falls (edge-triggered)
Types of Latches

- Level-sensitive – A transparent mode and an opaque mode depending on the level of CLK

Timing Metrics

- Timing metrics for sequential elements differ from those of combinational logic
- Set-up time
  - Time that data must be valid before clock transitions
- Hold time
  - Time that data must remain valid after the clock edge
- Propagation delay
  - Can be measured from clock to Q or data to Q
  - Which is more meaningful? Depends…
Register: Timing Definitions

Characterizing Timing
Latch-Based Design

- N latch is transparent when $\phi = 0$
- P latch is transparent when $\phi = 1$

Maximum Clock Frequency

If the data "races" through the logic too fast, the data is contaminated.

Also:

$t_{\text{cdreg}} + t_{\text{cldlogic}} > t_{\text{hold}}$

$t_{\text{cd}}$: contamination delay = minimum delay

Usually $t_{\text{cdreg}} \sim t_{\text{c-Q}}$
Writing into a Static Latch

Use the clock as a decoupling signal that distinguishes between the transparent and opaque states.

Converting into a MUX

Forcing the state (can implement as NMOS-only)

Storage Mechanisms

Static

Dynamic (charge-based)
Mux-Based Latches

Negative latch (transparent when CLK = 0)
Positive latch (transparent when CLK = 1)

\[
Q = \overline{Clk} \cdot Q + Clk \cdot In
\]

T-gate Mux-Based Latch

\[
Q = Clk \cdot Q + \overline{Clk} \cdot In
\]
Pass-transistor Mux-Based Latch

NMOS only
Non-overlapping clocks

Master-Slave (Edge-Triggered) Register

Two opposite latches act to trigger on clock edge
Also called master-slave topology
Advantage: Transparency window is limited and more controllable
Disadvantage: Slower
Master-Slave Register

Multiplexer-based latch pair

High clock load (high switching activity, large power)

Clk-Q Delay
Setup Time Depiction

\[ T_{\text{setup}} = 210\text{ps} \]

\[ T_{\text{setup}} = 200\text{ps} \]

Reduced Clock Load
Master-Slave Register

Only 2 T-gates and 4 INV
New data must now overpower the previously held state

Possible reverse conduction path (keep \( I_4 \) weak)
Latch-Based Design

- latch is transparent when $\phi = 0$
+ latch is transparent when $\phi = 1$

To avoid race conditions, we need to make sure that the clocks are completely non-overlapping.
Otherwise consecutive latches may be transparent simultaneously.

Avoiding Clock Overlap

(a) Schematic diagram

(b) Overlapping clock pairs
Overpowering the Feedback Loop

NOR-based set-reset

Cross-coupled NORs

Adding clock to synchronize

This is not used in datapaths any more, but is a basic building memory cell
Sizing Issues

W/L_2 = 1.5

Output voltage dependence on transistor width

Transient response

Lecture Summary

- Latch topologies are based on cross-coupled inverter pairs to hold state
- New states are overwritten by either decoupling the pair (break the loop) or by overpowering the loop
  - Breaking the loop is cleaner (less contention, power) but results in more complex topologies
- Edge-triggered registers are slower than latches but are more robust/easy to design with since they are only transparent for a very limited duration
Clock Skew in Alpha Processor

- Absolute skew smaller than 90 ps

- The critical instruction and execution units all see the clock within 65 ps