EECS 270 Schedule and Syllabus for Fall 2011 Designed by Prof. Pinaki Mazumder

Week	Day	Date	Lec No.	Lecture Topic	Textbook Sec	Course-pack	HW (Due Date)	Lab (Start Date)
1	W	7-Sep	1	Course Overview, Number Representation	Sec. 1.1-1.3	Pages 1-16		Tutorial
2	M	12- Sep	2	Codes, Addition, 1's & 2's Complements	Sec. 2.5	Pages 16-33		Lab 1: Intro to Quartus
	W	14- Sep	3	Boolean Algebra, Gates, Switching Circuits	Sec. 2.2-2.4	Pages 33-44		
3	M	19- Sep	4	Delay, Timing Diagram and Static Hazards		Pages 47-56		
	W	21-Sep	5	Design Problems, Minimization & Implementation	Sec. 2.6-2.7	Pages 59-67	HW 1	Lab 2: Timing and Delay
4	M	26-Sep	6	Design Problems and Verilog Implementation	Sec 2.8, Sec 9.2-9.4	Pages 69-80		
	W	28-Sep	7	Logic Minimization by Graphical Methods	Sec. 6.2	Pages 83-93		
5	M	3-Oct	8	Decoders, Multiplexers, and Tristate Drivers	Sec. 2.9-2.10	Pages: 96-119	HW 2	Lab 3: Comb. Logic
	W	5-Oct	9	Sequential Design: Flip Flops & Latches	Sec. 4.4	Pages 122-130	Midterm 1 Exam @ 7:00-8:30 pm	
6	M	10-Oct	10	Timing Diagrams using Flip Flops	Sec. 3.1-3.2	Pages 133-152		
	W	12-Oct	11	Counters: Types and Synthesis	Sec. 3.2	Pages 157-173	HW 3	
7	M	17-Oct		Recess				
	W	19-Oct	12	Shift Registers and Register Files	Sec. 4.9	Pages 176-182		Lab 4: Sequential Logic
8	M	24-Oct	13	Analysis of Sequential Circuits	Sec 4.2	Pages 186-198	HW 4	
	W	26-Oct	14	Design of Sequential Circuits	Sec. 3.3-3.5	Pages 186-198		
9	M	31-Oct	15	Serial and Parallel Adder Configurations	Sec. 4.6			Lab 5: Comb Logic
	W	2-Nov	16	Serial and Parallel Multiplier Configurations	Sec 4.3		HW 5	
10	M	7- Nov	17	Synthesis of Large FSM and HLSM Machines	Sec. 3.4-3.7			
	W	9- Nov	18	HLSM & FSM (Continued)	Sec. 5.2-5.4			Lab 6: Sequential Circuit
11	M	14-Nov	19	State Minimization Techniques			HW 6	
	W	16-Nov	20	More FSM, HLSM and RTL Design	Sec 4.5, Sec 5.4-5.6		Midterm 2 Exam @ 7:00-8:30 pm	
12	M	21-Nov	21	Q-M Method of Minimization	Sec. 6.2			Lab 7: Sequential Circuit
	W	23-Nov	22	ROM, PLA, and FPGA	Sec. 8.2-8.6			
13	M	28-Nov	23	Random Access Memories	Sec 8.2-8.6		HW 7	
	W	30-Nov	24	Microprocessor Design	Sec. 6.2, 6.4			
14	M	5-Dec	25	Microprocessor Design	Sec. 6.3			
	W	7-Dec	26	Review of the Course and Exam Syllabus			HW 8	
15	M	12-Dec	27	Discussion of Final Exam Problems				

Final Exam: Friday, December 16 7:00-9:00 pm

Grades are Expected to be Posted: Sunday, December 18.

Introduction to Digital Systems

Lecture #1: Course Overview
and Numeral Systems

Prepared by
Pinaki Mazumder
Professor of Computer Science & Engineering
University of Michigan

Foundation of Digital Systems

- Course Overview
- Grading Criteria
- Goal of EECS 270
- Analog v. Digital Systems
- State-of-the-art of Digital Systems
- Future Trends in Digital Systems
- Merging of Analog and Digital Technologies
- Numeral Systems

People You Need to Know

- Course Instructor
  - Pinaki Mazumder (eecs270.mazum@gmail.com)
- Lab Coordinator
  - Matt Smith (matsmith@umich.edu
- Lecture GSI
  - Zhenghong Sun (zhsun@umich.edu)
- Plus five or so GSI or Lab Assistants

Lecture Office Hours

Instructor

Location: 4765 CSE

> Times: Monday & Wednesday: 1:30 – 3:00pm

- **Lecture GSI**

> Location: CSE 1637

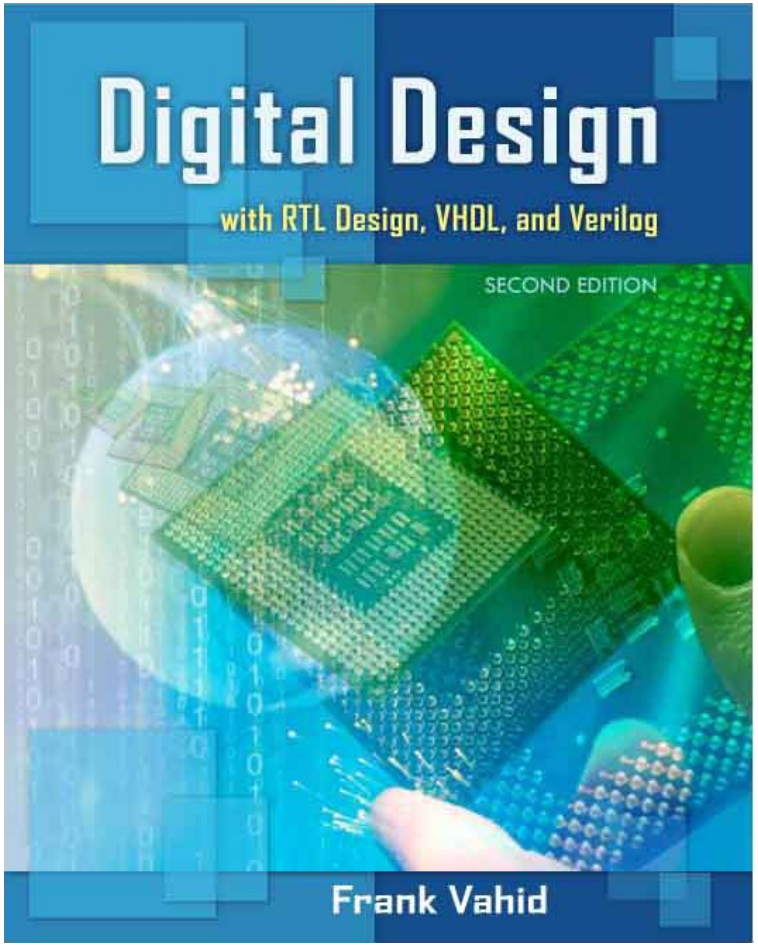
> Times: Monday: 4:00 – 5:00 pm
Tuesday: 2:00 – 3:00 pm, 5:00 – 6:00 pm
Thursday: 10:00 – 11:00 am, 1:00 – 2:00 pm
Friday: 10:00 – 11:00 am

- Lab-related questions should be directed to the lab coordinator and lab assistants

Textbook

F. Vahid: *Digital Design*, Wiley, Second Edition ,2010.

Course-pack by Prof. Mazumder can be purchased from Dollar Bill Copying for the first 15 Lectures. Price: ~ $20.00. Second part will be made available in late October.



EECS 270 Reference Books

1. *Fundamentals of Logic Design* (5th Edition) by Charles H. Roth, Thompson Brooks/Cole

2. *Digital Design: Principles and Practices* (3rd Edition Update) by John F. Wakerly, Prentice Hall Publishing Company

3. *Fundamentals of Digital Logic with Verilog Design* by Stephen Brown and Zvonko Vranesic, McGraw-Hill Higher Education

More Reference Books

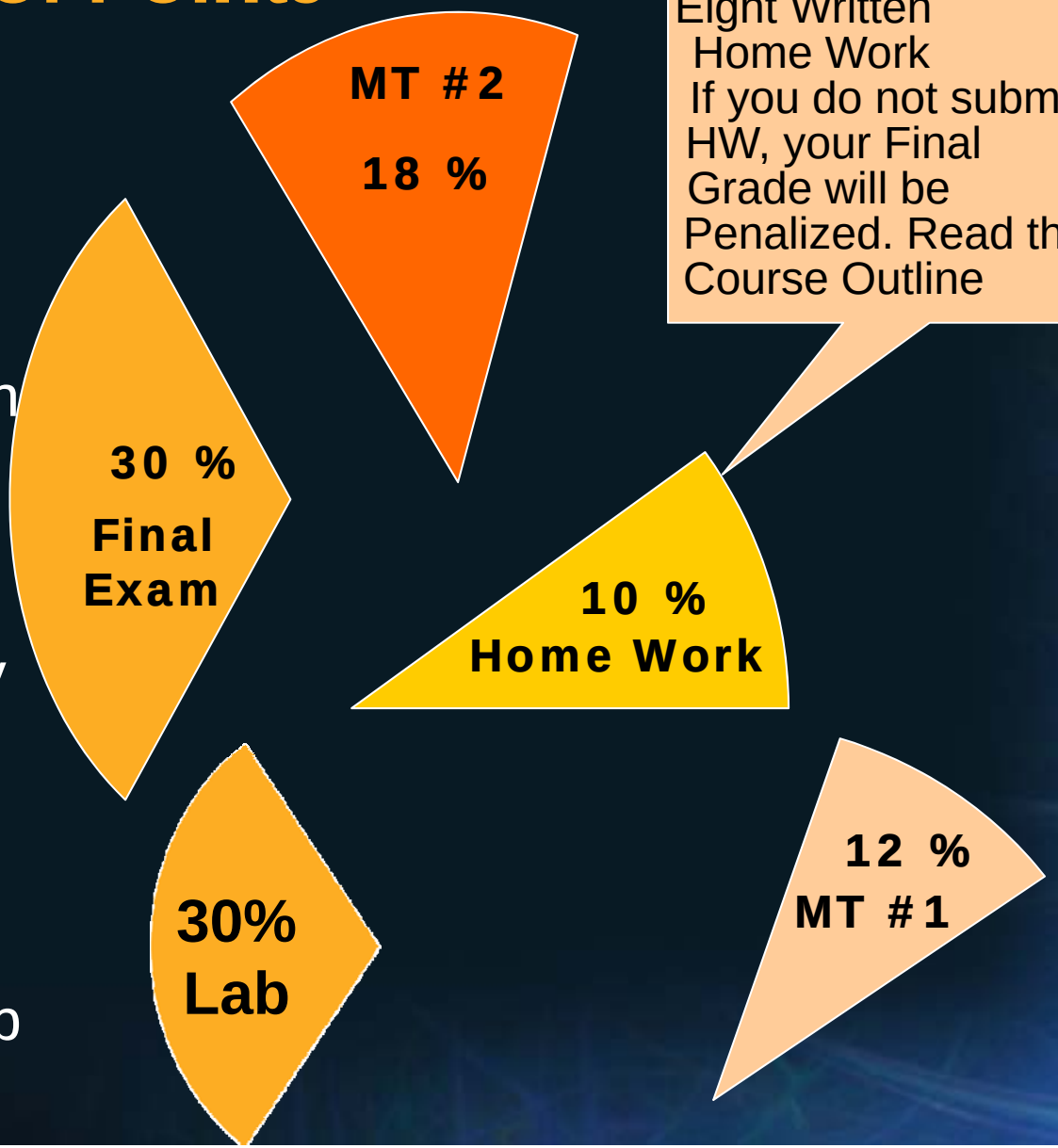
4. *Contemporary Logic Design by R. H. Katz*, Benjamin/Cummings Publishing Company

5. *Logic and Computer Design Fundamentals* by Morris Mano and Charles Kime, Prentice Hall Publishing Company

6. Introduction to Digital Logic Design by *John P. Hayes*, Addison Wesley.

7. *Verilog HDL Synthesis a Practical Primer* by J. Bhasker, Star Galaxy Publishing

Distribution of Points



Tips for Success

- Pay 100% attention to lectures
- Read class notes + Handouts regularly
- Try all Homework Problems
- Do not miss any lab

Very Important Dates

Wednesday, October 5 (7:00-8:30 pm)	Midterm Exam #1
Wednesday, November 16 (7:00-8:30 pm)	Midterm Exam #2
Friday, December 16 (7:00-9:00 pm)	Final Exam

Homework Policies

- Assignments will be posted on the EECS 270 web site
- All homework is to be done by each student individually. The College of Engineering Honor Code applies to all work in this course.
- No late homework will be accepted. However, your lowest homework score will be dropped when computing your overall grade.
- Homework papers should be deposited in the indicated drop box in room 2420 EECS by 5:00 p.m. on the due date
- Graded papers will be returned in room 2431 EECS sorted by lab section number
- Re-grade requests must be submitted within one week after the graded papers are returned, and must have a cover sheet clearly explaining the reason for the request.
- All re-grading requests must be made to the **Lecture GSI** only.

Exam Policies

- The exams will be **"closed book"**. No books, notes or electronic devices of any kind will be allowed.
- The goal of the exams is to test comprehension and problem-solving skills rather than memorization
- To attend a make-up exam (if any) will require a valid and documented excuse, such as a doctor's letter
- All the exams will cover material from:
  - The lectures
  - The textbook reading assignments
  - The lab work
- Re-grade requests (for midterms) must be submitted within one week after the graded exams are returned.
- All re-grading requests must be made to the **Instructor** only.

Course Web Site

- Check the EECS 270 CTools web site regularly
- The web will be the primary way to distribute course information and materials
- Material at the class web site:
  - Lecture slides by the textbook author F. Vahid (all available now)
  - Additional lecture slides and notes used by the instructors will be made available throughout the term
  - Homework assignments and solutions, practice material, etc., will also be distributed throughout the term

Lab Policies

- Lab policies and procedures will be covered by the lab coordinator Matt Smith and his group of lab assistants
- Check the course web site for details and updates, including:
  - Policy for changing or adding a lab section
  - Lab attendance policy
  - Lab work submission policy

Labwork Submission Policy

- **Pre/In/Post-Lab:** Due during assigned lab section of week indicated in table. Submit to any 270 lab assistant during the open or scheduled lab times
- **Late Penalty:** A 10% per day late penalty will be accessed for late lab submissions
- **Incomplete Labs:** It is in your best interest to complete all of the lab assignments!

Goal of EECS 270

- To teach how to design Real World applications of digital logic

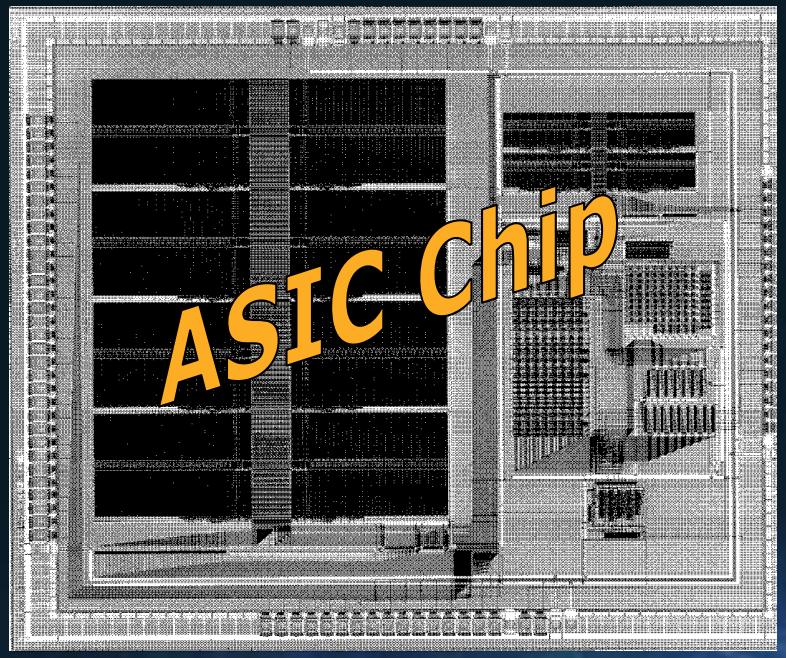
Traffic Light Controller

Vending Machine

Railroad Xing Contoller

Goal of EECS 270

- To teach principles and methodologies of digital logic design
- To provide background for designing complex microprocessors; Application-Specific Integrated Circuits (ASIC) using CAD tools



Goal of EECS 270

To teach how to design Real World applications of Digital Logic

Traffic Light Controller

Simple form: A Ring Counter
Complex Form: Traffic Density Based Fuzzy Controller

Vending Machine

Simple form: Accepts Nickel, Dime & Quarter only
Complex form: Accepts Dollar bills and give changes back

Railway Xing Controller

Senses presence of a train near the Xing, rings bell and lowers crowbar before the train crosses the intersection and lifts the crowbar after the train leaves the intersection.

Analog v. Digital

What is Analog?

Rolex Pricey Watch

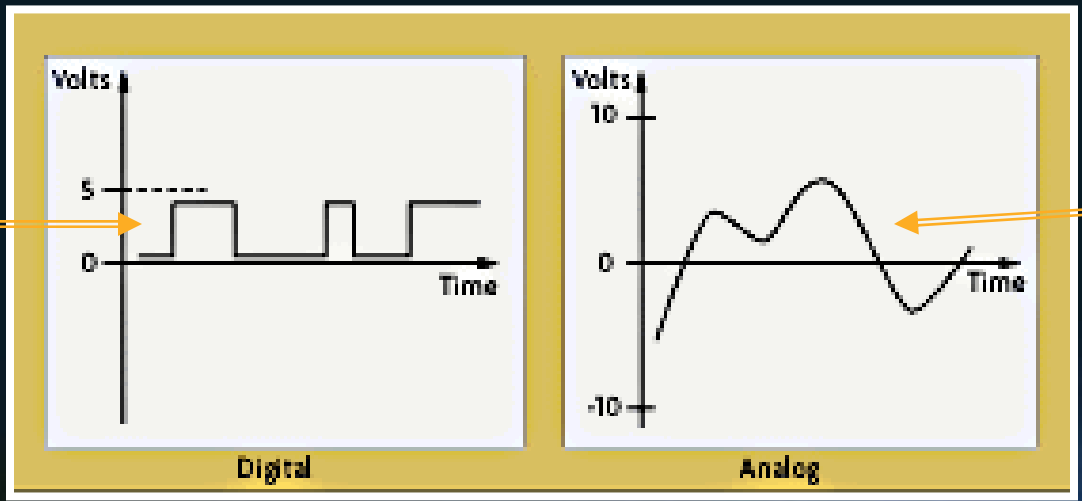
What is Digital?

Timex Quartz Clock

How do Digital and Analog Signals Look Like?

Analog v. Digital

Digital Signal (0 and 1 Pulse Train)



Analog Signal (Contains many frequencies)

Analog v. Digital

Analog

1. Input signal is complex containing many frequencies
2. Signal level varies from < 1mV – 10V
3. Slow Speed: Freq: 1 kHz – 100 MHz

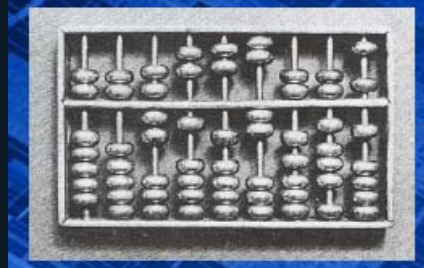
Digital

1. Input signal is a train of pulses
2. Signal is rail-to-rail (0 to Vdd)
3. High Speed: Freq: 1 – 10 GHz

Analog v. Digital (cont'd)

Analog	Digital
4. High power consumption	4. Very low power consumption
5. Low Integration < 10,000 transistors	5. High Integration > 200 Million transistors
6. Must have very low distortions to retain high fidelity	6. Signal Integrity is important to avoid delay induced faults

Explosion of Digital Technologies: From Abbacus to Nanoelectronics



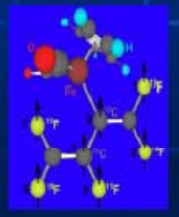
Abbacus 1500 BC

Illiac IV 1954

Moore's Law

Moore's Law

CMOS



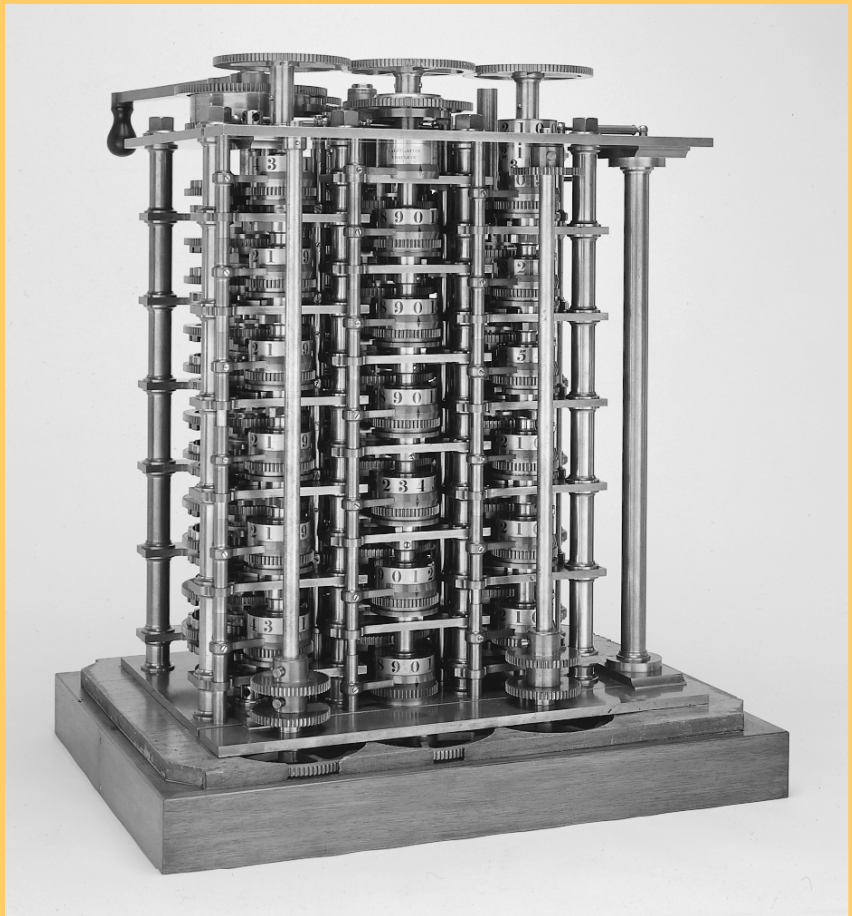
Beyond CMOS 202

Common elements

continue

Intel Nanotechnology
Virtual Open House

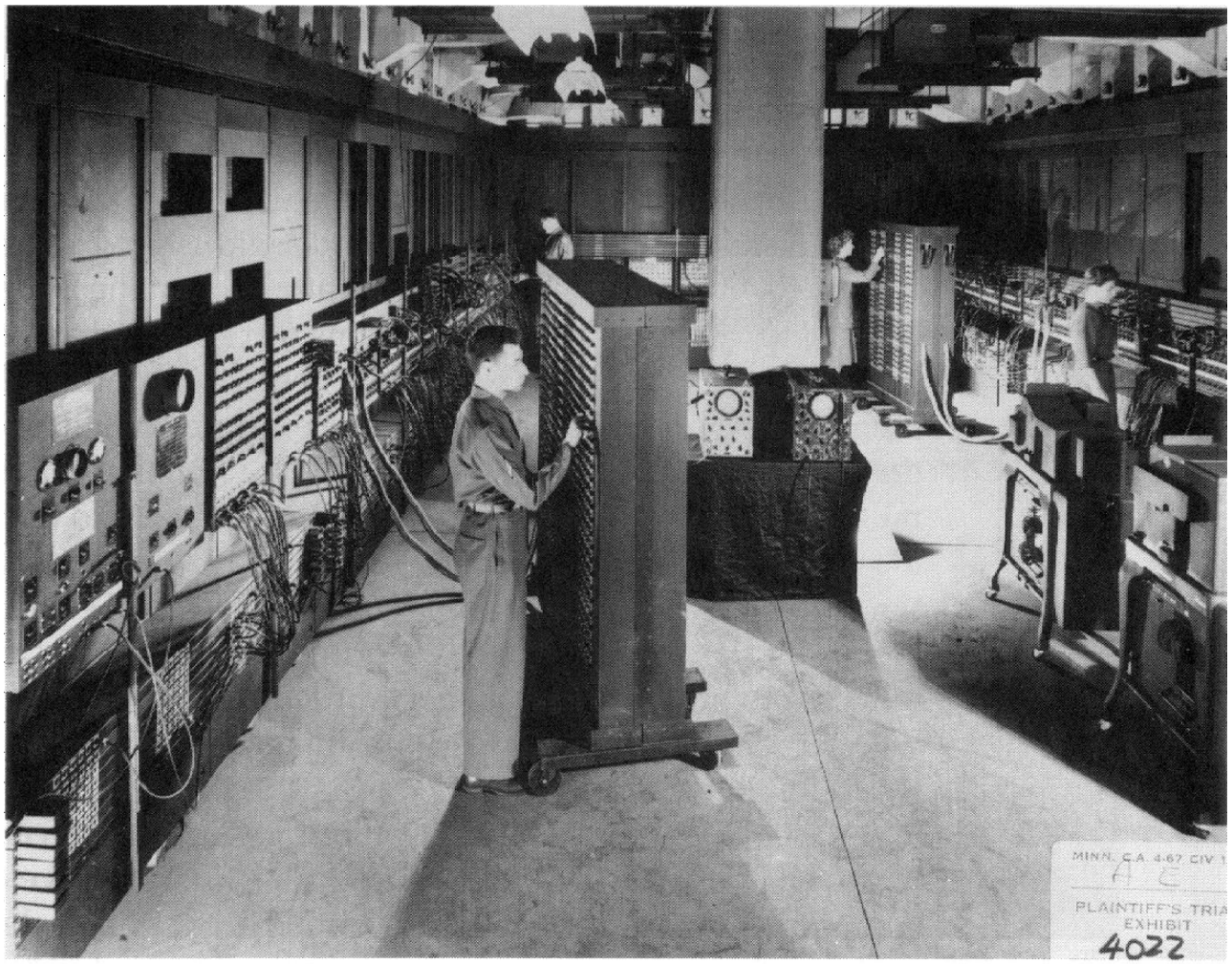
The First Computer



Babbage's Difference Engine 1 (1834)
Consists of 25,000 mechanical parts
It cost: £17,470 (in 1834!)
General-Purpose **Computing Engine**
Two-cycle sequence: Store & Execute
Used pipelining **for addition ops**

Courtesy: Reference 1

ENIAC - First electronic computer v. Pentium Chips



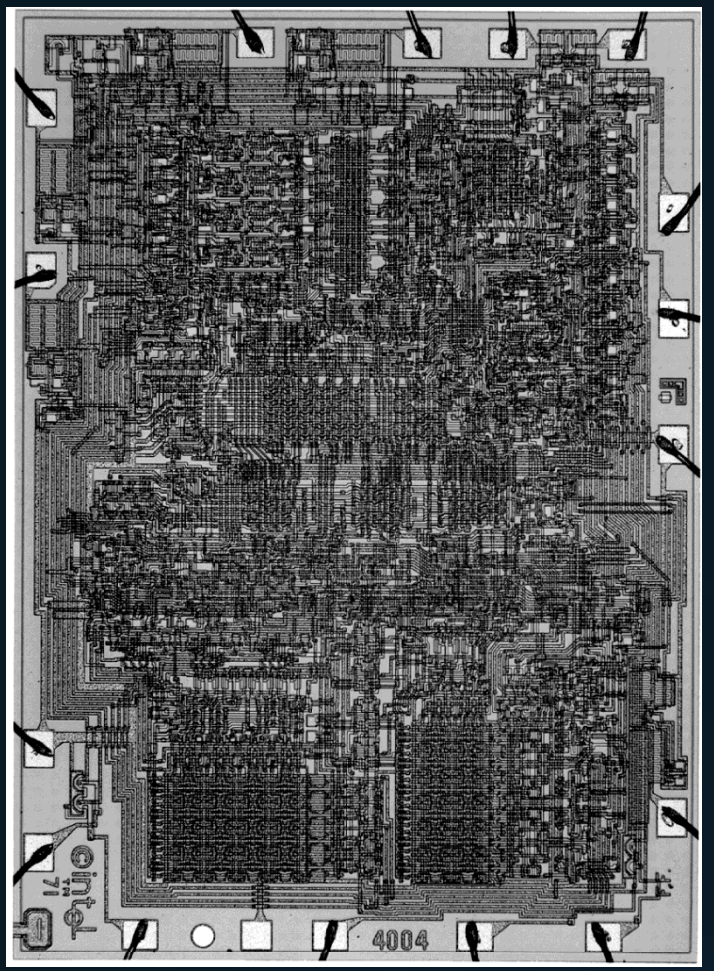
- Built in 1946
- 80 ft long
- 8.5 ft high
- Used 18,000 vacuum tubes

The Multiplier Unit is on display at the atrium of the EECS Dept., The University of Michigan, USA

Courtesy: Reference 1

Intel 4004 Micro-Processor

- First Microprocessor
- 1971
- 2,250

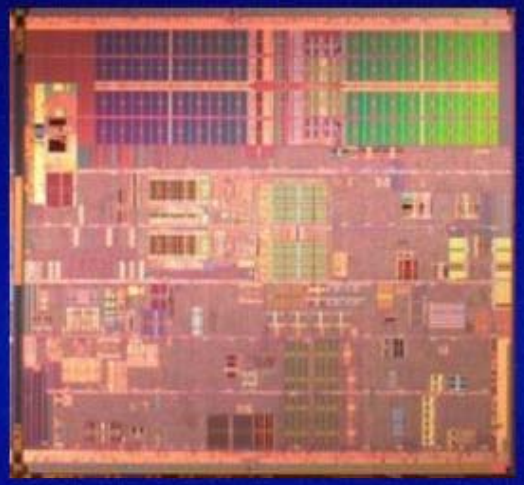


Courtesy: Reference 1

CPU Chips

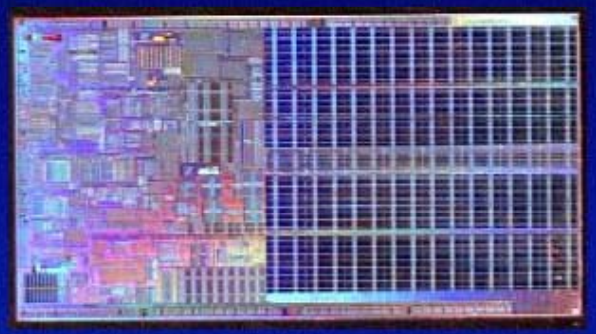
90 nm CPU Chips

Prescott CPU



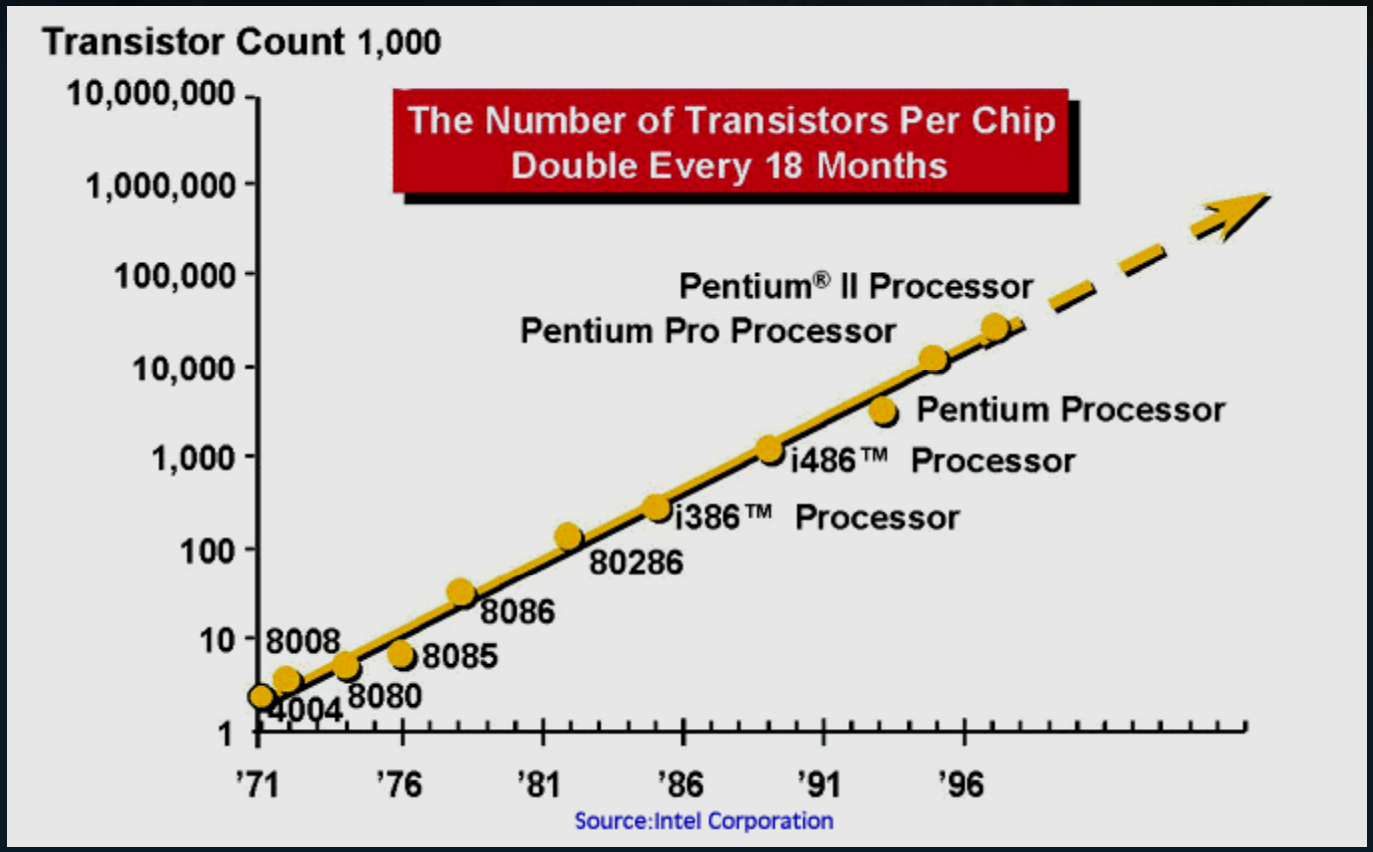
112 mm² die size
125 million transistors

Dothan CPU



87 mm² die size
144 million transistors

90 nm process now ramping on high performance CPU products



- Moores Law
  - $P_n = P_o \times 2^n$

Courtesy: Reference 1

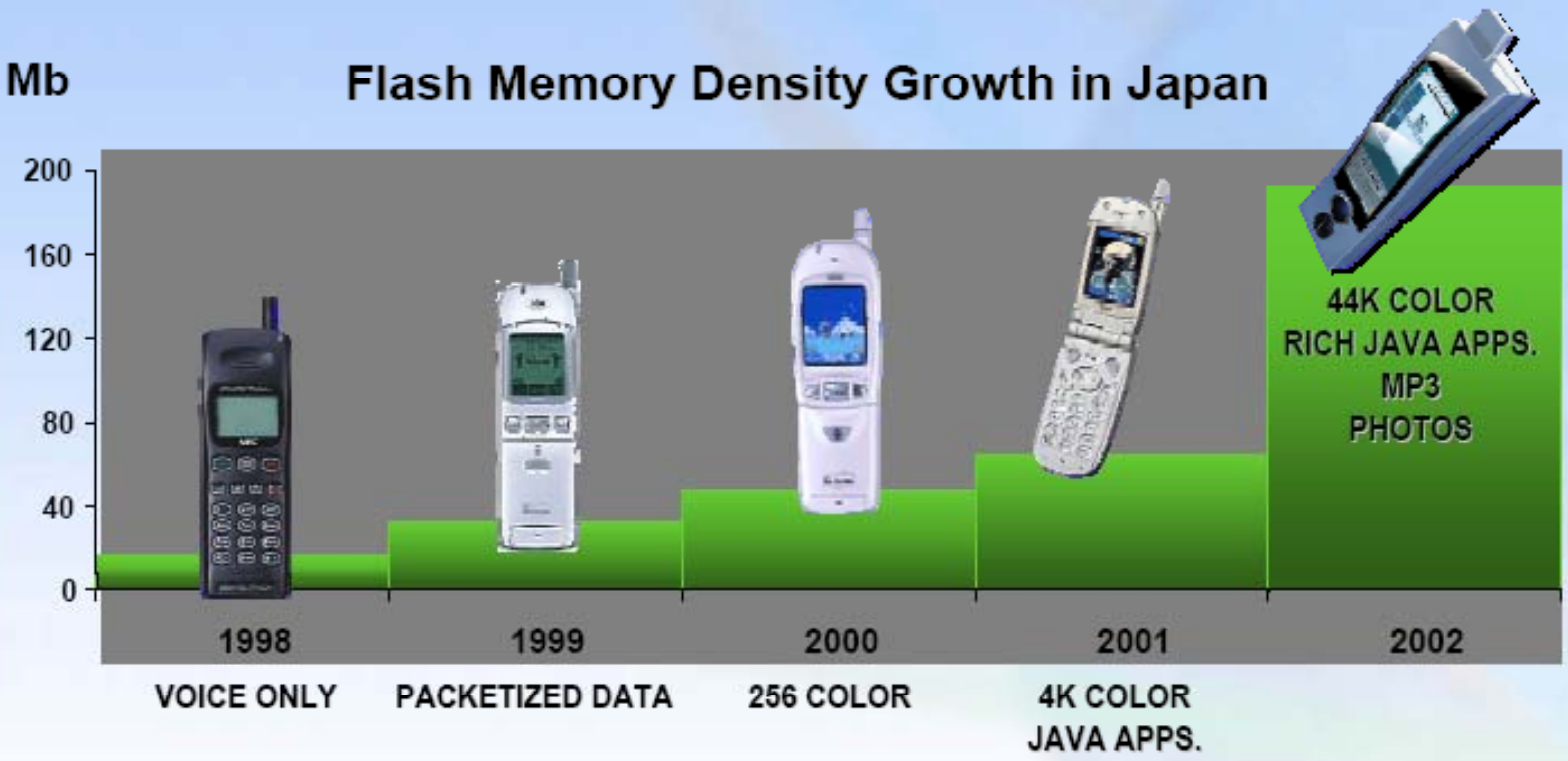
Where

- Pn = computer processing power in future years
- Po = computer processing power in the beginning year
- n = number of years to develop a new microprocessor divided by 2, i.e., every two years

Merging of Technologies

- Computers
  - Embedded Processors
  - Microcontrollers
- Communication
  - Cell Phone
  - Internet Voice Service
- Consumer Electronics
  - Video Camera
  - Personal Organizer
  - Games

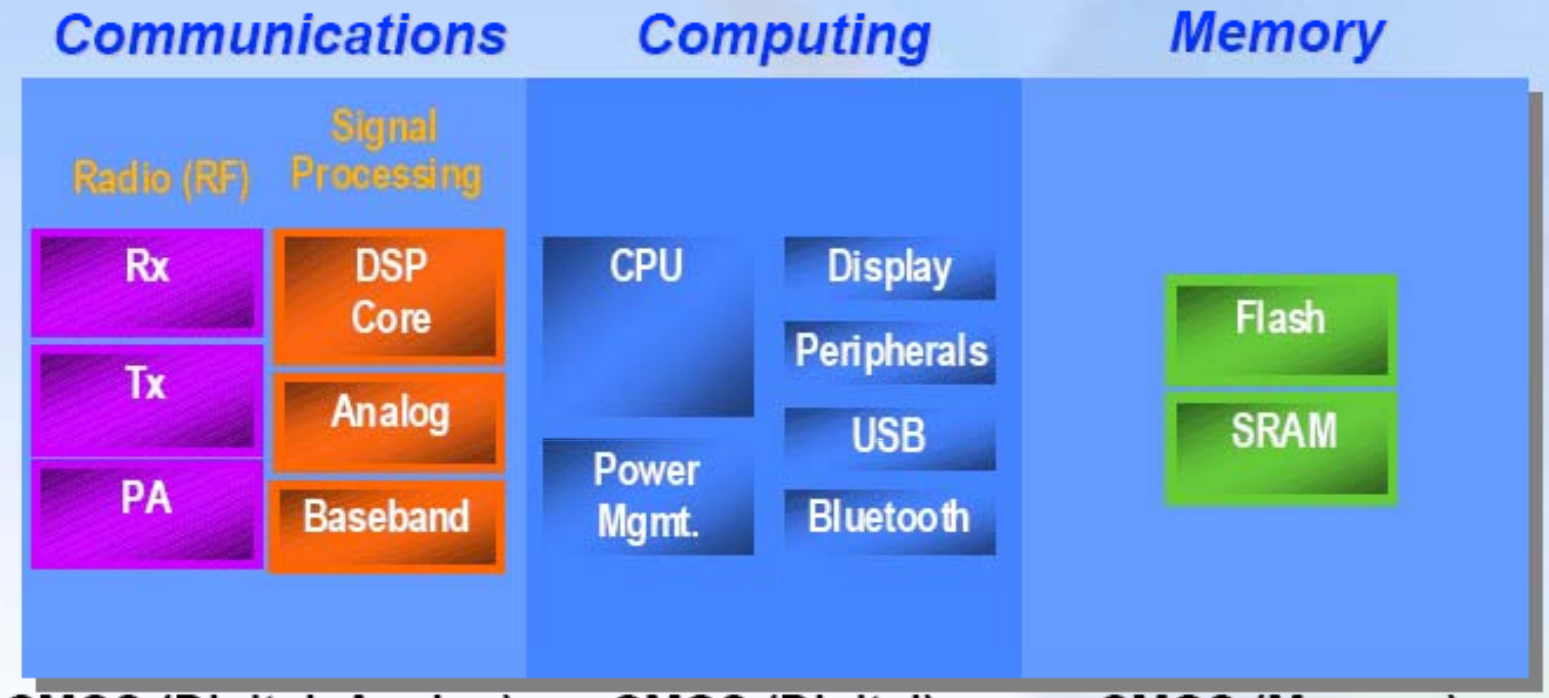
Cell Phones For Voice + Data



Convergence increases silicon usage

Source: NEC, Intel

Converged Cell Phone Integration Opportunities



intel

Intel Developer Forum Spring 2003

Numeral Systems

Beware of missing Info;
Jot down in class

Additionally, Read the Course pack for details