<table>
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<tr>
<th>Week</th>
<th>Day</th>
<th>Date</th>
<th>Lec No.</th>
<th>Lecture Topic</th>
<th>Textbook Sec</th>
<th>Course-pack</th>
<th>HW (Due Date)</th>
<th>Lab (Start Date)</th>
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<td>1</td>
<td>Course Overview, Number Representation</td>
<td>Sec. 1.1-1.3</td>
<td>Pages 1-16</td>
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<td>2</td>
<td>M</td>
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<td>Codes, Addition, 1’s &amp; 2’s Complements</td>
<td>Sec. 2.5</td>
<td>Pages 16-33</td>
<td>Lab 1: Intro to Quartus</td>
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<tr>
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<td>14-Sep</td>
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<td>Boolean Algebra, Gates, Switching Circuits</td>
<td>Sec. 2.2-2.4</td>
<td>Pages 33-44</td>
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<td>3</td>
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<td>Delay, Timing Diagram and Static Hazards</td>
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<td>Sec. 2.6-2.7</td>
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<td>6</td>
<td>Design Problems and Verilog Implementation</td>
<td>Sec. 2.8, Sec 9.2-9.4</td>
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<td>7</td>
<td>Logic Minimization by Graphical Methods</td>
<td>Sec. 6.2</td>
<td>Pages 83-93</td>
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<td>5</td>
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<td>3-Oct</td>
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<td>Decoders, Multiplexers, and Tri-state Drivers</td>
<td>Sec. 2.9-2.10</td>
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<td>Sequential Design: Flip Flops &amp; Latches</td>
<td>Sec. 4.4</td>
<td>Pages 122-130</td>
<td>Midterm 1 Exam @ 7:00-8:30 pm</td>
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<td>6</td>
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<td>10-Oct</td>
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<td>Timing Diagrams using Flip Flops</td>
<td>Sec. 3.1-3.2</td>
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<td>Counters: Types and Synthesis</td>
<td>Sec. 3.2</td>
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<td>Shift Registers and Register Files</td>
<td>Sec. 4.9</td>
<td>Pages 176-182</td>
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<td>Analysis of Sequential Circuits</td>
<td>Sec. 4.2</td>
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<td>Sec. 3.3-3.5</td>
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<td>Serial and Parallel Adder Configurations</td>
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<td>Serial and Parallel Multiplier Configurations</td>
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<td>Synthesis of Large FSM and HLSM Machines</td>
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<td>W</td>
<td>9-Nov</td>
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<td>HLSM &amp; FSM (Continued)</td>
<td>Sec. 5.2-5.4</td>
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<td>Lab 6: Sequential Circuit</td>
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<td>14-Nov</td>
<td>19</td>
<td>State Minimization Techniques</td>
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<td>16-Nov</td>
<td>20</td>
<td>More FSM, HLSM and RTL Design</td>
<td>Sec 4.5, Sec 5.4-5.6</td>
<td>Midterm 2 Exam @ 7:00-8:30 pm</td>
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<td>12</td>
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<td>21-Nov</td>
<td>21</td>
<td>Q-M Method of Minimization</td>
<td>Sec. 6.2</td>
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<td>Lab 7: Sequential Circuit</td>
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<td>ROM, PLA, and FPGA</td>
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<td>13</td>
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<td>28-Nov</td>
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<td>Random Access Memories</td>
<td>Sec 8.2-8.6</td>
<td>HW 7</td>
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<td>24</td>
<td>Microprocessor Design</td>
<td>Sec. 6.2, 6.4</td>
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<tr>
<td>14</td>
<td>M</td>
<td>5-Dec</td>
<td>25</td>
<td>Microprocessor Design</td>
<td>Sec. 6.3</td>
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<tr>
<td>W</td>
<td>7-Dec</td>
<td>26</td>
<td>Review of the Course and Exam Syllabus</td>
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<td>HW 8</td>
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<td>15</td>
<td>M</td>
<td>12-Dec</td>
<td>27</td>
<td>Discussion of Final Exam Problems</td>
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</table>

**Final Exam:** Friday, December 16 7:00-9:00 pm

**Grades are Expected to be Posted:** Sunday, December 18.
Introduction to Digital Systems

Lecture #1: Course Overview and Numeral Systems

Prepared by
Pinaki Mazumder
Professor of Computer Science & Engineering
University of Michigan
Foundation of Digital Systems

• Course Overview
• Grading Criteria
• Goal of EECS 270
• Analog v. Digital Systems
• State-of-the-art of Digital Systems
• Future Trends in Digital Systems
• Merging of Analog and Digital Technologies
• Numeral Systems
People You Need to Know

• Course Instructor
  > Pinaki Mazumder (eeecs270.mazum@gmail.com)

• Lab Coordinator
  > Matt Smith (matsmith@umich.edu)

• Lecture GSI
  > Zhenghong Sun (zhsun@umich.edu)

• Plus five or so GSI or Lab Assistants
Lecture Office Hours

Instructor

Location: 4765 CSE
> Times: Monday & Wednesday: 1:30 – 3:00pm

• Lecture GSI

> Location: CSE 1637
> Times: Monday: 4:00 – 5:00 pm
Tuesday: 2:00 – 3:00 pm, 5:00 – 6:00 pm
Thursday: 10:00 – 11:00 am, 1:00 – 2:00 pm
Friday: 10:00 – 11:00 am

• Lab-related questions should be directed to the lab coordinator and lab assistants

Course-pack by Prof. Mazumder can be purchased from Dollar Bill Copying for the first 15 Lectures. Price: $20.00. Second part will be made available in late October.
EECS 270 Reference Books


More Reference Books

4. *Contemporary Logic Design* by R. H. Katz, Benjamin/Cummings Publishing Company


6. *Introduction to Digital Logic Design* by John P. Hayes, Addison Wesley.

7. *Verilog HDL Synthesis a Practical Primer* by J. Bhasker, Star Galaxy Publishing
Tips for Success

- Pay 100% attention to lectures
- Read class notes + Handouts regularly
- Try all Homework Problems
- Do not miss any lab

Eight Written Home Work
If you do not submit HW, your Final Grade will be Penalized. Read the Course Outline
Very Important Dates

Wednesday, October 5 (7:00-8:30 pm)    Midterm Exam #1

Wednesday, November 16 (7:00-8:30 pm)   Midterm Exam #2

Friday, December 16 (7:00-9:00 pm)      Final Exam
Homework Policies

• Assignments will be posted on the EECS 270 web site
• All homework is to be done by each student individually. The College of Engineering Honor Code applies to all work in this course.
• No late homework will be accepted. However, your lowest homework score will be dropped when computing your overall grade.
• Homework papers should be deposited in the indicated drop box in room 2420 EECS by 5:00 p.m. on the due date
• Graded papers will be returned in room 2431 EECS sorted by lab section number
• Re-grade requests must be submitted within one week after the graded papers are returned, and must have a cover sheet clearly explaining the reason for the request.
• All re-grading requests must be made to the Lecture GSI only.
Exam Policies

- The exams will be "closed book". No books, notes or electronic devices of any kind will be allowed.
- The goal of the exams is to test comprehension and problem-solving skills rather than memorization.
- To attend a make-up exam (if any) will require a valid and documented excuse, such as a doctor's letter.
- All the exams will cover material from:
  - The lectures
  - The textbook reading assignments
  - The lab work
- Re-grade requests (for midterms) must be submitted within one week after the graded exams are returned.
- All re-grading requests must be made to the Instructor only.
Course Web Site

- Check the EECS 270 CTools web site regularly
- The web will be the primary way to distribute course information and materials
- Material at the class web site:
  > Lecture slides by the textbook author F. Vahid (all available now)
  > Additional lecture slides and notes used by the instructors will be made available throughout the term
  > Homework assignments and solutions, practice material, etc., will also be distributed throughout the term
Lab Policies

- Lab policies and procedures will be covered by the lab coordinator Matt Smith and his group of lab assistants.
- Check the course website for details and updates, including:
  - Policy for changing or adding a lab section
  - Lab attendance policy
  - Lab work submission policy
Labwork Submission Policy

- **Pre/In/Post-Lab**: Due during assigned lab section of week indicated in table. Submit to any 270 lab assistant during the open or scheduled lab times.

- **Late Penalty**: A 10% per day late penalty will be accessed for late lab submissions.

- **Incomplete Labs**: It is in your best interest to complete all of the lab assignments!
Goal of EECS 270

- To teach how to design Real World applications of digital logic
Goal of EECS 270

- To teach principles and methodologies of digital logic design
- To provide background for designing complex microprocessors; Application-Specific Integrated Circuits (ASIC) using CAD tools
## Goal of EECS 270

To teach how to design Real World applications of Digital Logic

| Traffic Light Controller | Simple form: A Ring Counter  
Complex Form: Traffic Density Based Fuzzy Controller |
|--------------------------|------------------------------------------------------|
| Vending Machine          | Simple form: Accepts Nickel, Dime & Quarter only  
Complex form: Accepts Dollar bills and give changes back |
| Railway Xing Controller  | Senses presence of a train near the Xing, rings bell and lowers crowbar before the train crosses the intersection and lifts the crowbar after the train leaves the intersection. |
Analog v. Digital

What is Analog?
Rolex Pricey Watch

What is Digital?
Timex Quartz Clock

How do Digital and Analog Signals Look Like?
Analog v. Digital

Digital Signal (0 and 1 Pulse Train)

Analog Signal (Contains many frequencies)
# Analog v. Digital

## Analog

1. Input signal is complex containing many frequencies
2. Signal level varies from $< 1\text{mV} - 10\text{V}$
3. Slow Speed: Freq: $1 \text{kHz} - 100 \text{MHz}$

## Digital

1. Input signal is a train of pulses
2. Signal is rail-to-rail ($0$ to $V_{dd}$)
3. High Speed: Freq: $1 - 10 \text{GHz}$
## Analog v. Digital (cont’d)

<table>
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<th>Analog</th>
<th>Digital</th>
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<tr>
<td>4. High power consumption</td>
<td>4. Very low power consumption</td>
</tr>
<tr>
<td>5. Low Integration &lt; 10,000 transistors</td>
<td>5. High Integration &gt; 200 Million transistors</td>
</tr>
<tr>
<td>6. Must have very low distortions to retain high fidelity</td>
<td>6. Signal Integrity is important to avoid delay induced faults</td>
</tr>
</tbody>
</table>
Explosion of Digital Technologies: From Abbacus to Nanoelectronics
The First Computer

Babbage’s Difference Engine 1 (1834)
Consists of 25,000 mechanical parts
It cost: £17,470 (in 1834!)
General-Purpose Computing Engine
Two-cycle sequence: Store & Execute
Used pipelining for addition ops

Courtesy: Reference 1
ENIAC - First electronic computer v. Pentium Chips

- Built in 1946
- 80 ft long
- 8.5 ft high
- Used 18,000 vacuum tubes

The Multiplier Unit is on display at the atrium of the EECS Dept., The University of Michigan, USA. Courtesy: Reference 1
Intel 4004 Micro-Processor

- First Microprocessor
- 1971
- 2,250

Courtesy: Reference 1
CPU Chips

90 nm CPU Chips

Prescott CPU
112 mm² die size
125 million transistors

Dothan CPU
87 mm² die size
144 million transistors

90 nm process now ramping on high performance CPU products

Intel
**Moores Law**

- \[ P_n = P_o \times 2^n \]

Where

- \( P_n \) = computer processing power in future years
- \( P_o \) = computer processing power in the beginning year
- \( n \) = number of years to develop a new microprocessor divided by 2, i.e., every two years
Merging of Technologies

- Computers
  - Embedded Processors
  - Microcontrollers
- Communication
  - Cell Phone
  - Internet Voice Service
- Consumer Electronics
  - Video Camera
  - Personal Organizer
  - Games
Convergence increases silicon usage

Source: NEC, Intel
Converged Cell Phone Integration Opportunities

**Communications**
- **Radio (RF)**
  - Rx
  - Tx
  - PA
- **Signal Processing**
  - DSP Core
  - Analog
  - Baseband

**Computing**
- **CPU**
- **Power Mgmt.**
- **Display**
- **Peripherals**
- **USB**
- **Bluetooth**

**Memory**
- **Flash**
- **SRAM**

CMOS (Digital, Analog)
CMOS (Digital)
CMOS (Memory)
GaAs/SiGe (for RF)
Numeral Systems

Beware of missing Info;
Jot down in class

Additionally, Read the Course pack for details