Panorama, BISRAMGen, Mellow & Allegro
Next Generation EDA Tools

Design for Manufacturability
Business Proposal

Pinaki Mazumder
Professor, University of Michigan
Ann Arbor, MI 48109-2122
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(Acknowledgement: Members of Mazumder Research Group who Developed BISRAMGen Compiler & Other DFM Tools)
pinakimazum@gmail.com

NanoSys Opportunity

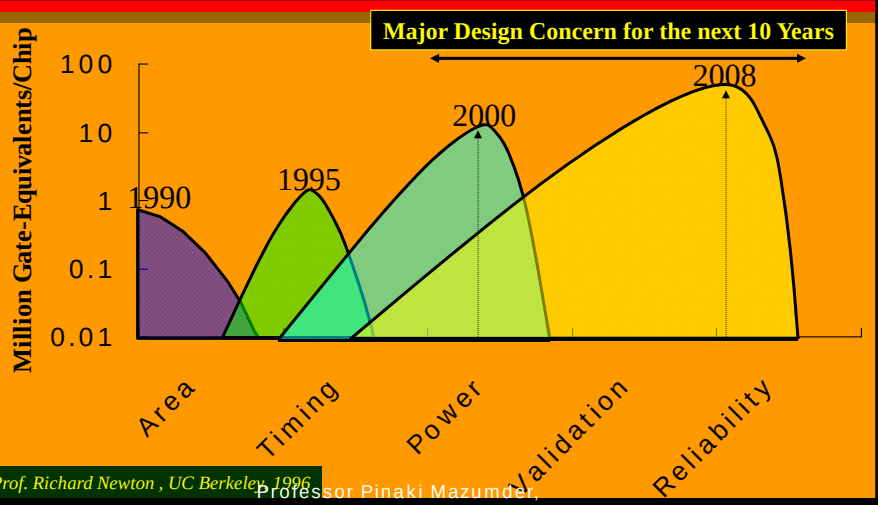
VLSI industry is witnessing rapid shift of Design Paradigm

From 1985-1990: Major design goal - Silicon Real Estate
From 1990-1995: Major design goal - Timing and Speed
From 1994-1999: Major design goal - Power Optimization
From 2000-2009: Major design goal - Chip Reliability

NanoSys introduces *Panorama, a* Deep-Submicron Design Optimization Environment for ULSI Chips

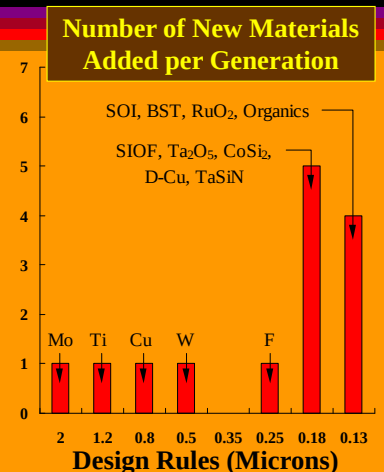
Panorama uses *Concurrent Engineering* at Chip Layout and Compilation phases to improve Yield and Reliability

VLSI Design Goals



Source: Prof. Richard Newton , UC Berkeley, 1996

New Materials Pose Great Reliability Problems



After Jim Owens, Sematech; Source: Nikkei Microdevices/Rose Assoc

Historically

- ***added only one new material in each generation***
- ***took up to 10 years to fully understand reliability***

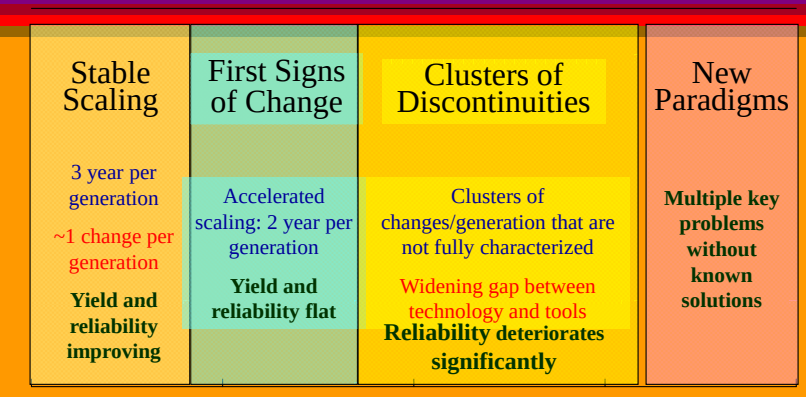
Breaking with history

- ***unprecedented adding of clusters of new materials***
- ***reliability issues of new matls. are not fully understood***

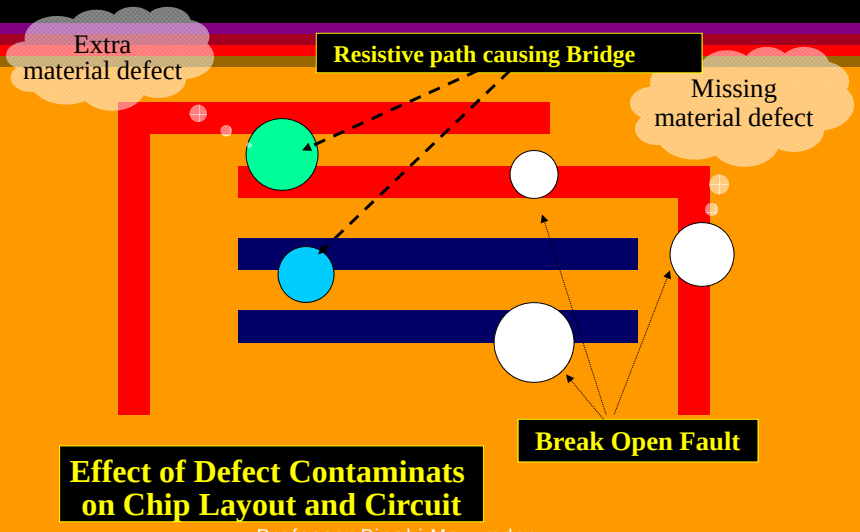
Running an added risk

- ***new failure modes***
- ***that customer reliability requirements won't be met***

Encountering Unprecented Change and Risk

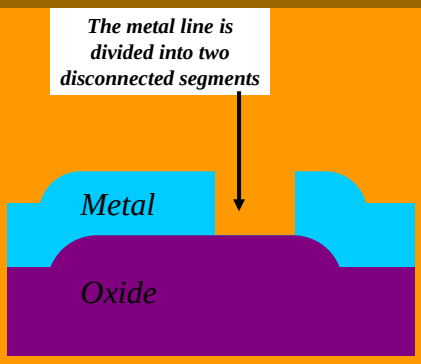


Modeling Contamination In IC Manufacturing



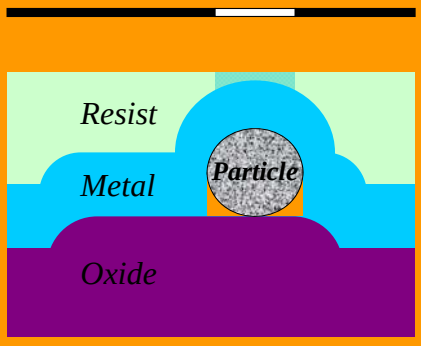
Process Flow for Metal Deposition

Metal Deposition
Resist Spin
Resist Expose
Resist Develop
Metal Etch
Resist Strip



Presence of A Contamination — Before Metal Deposition

Metal Deposition
Resist Spin
Resist Expose



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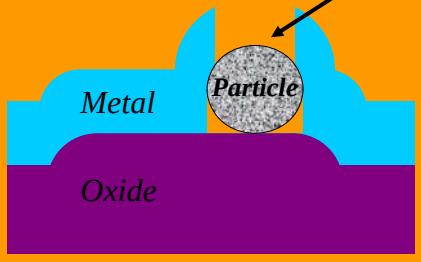
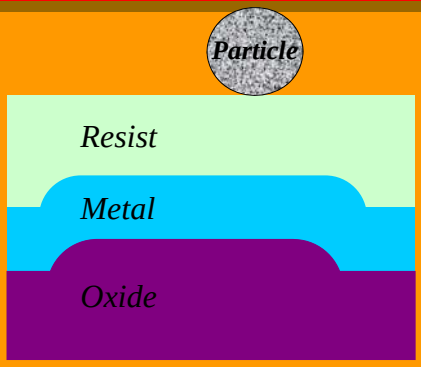


Presence of A Contamination — After Resist Spin-On

Metal Deposition
Resist Spin



Presence of A Contamination — After Resist Spin-On

Metal Deposition
Resist Spin
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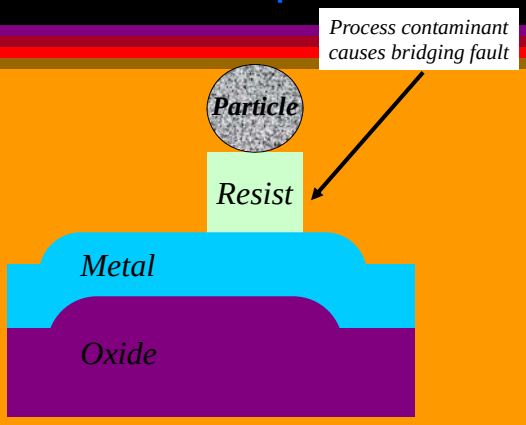
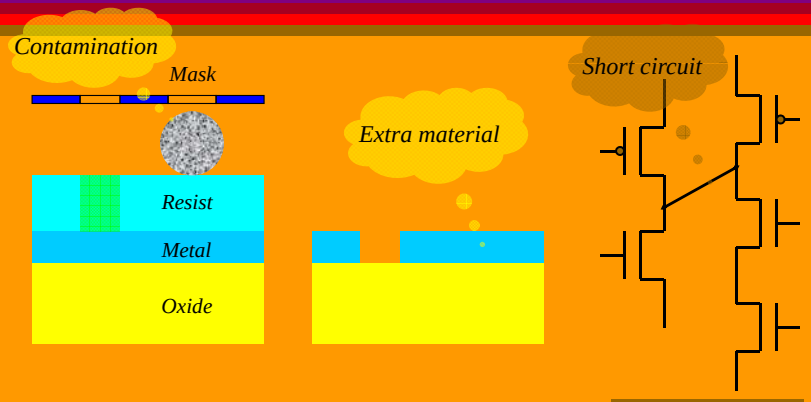
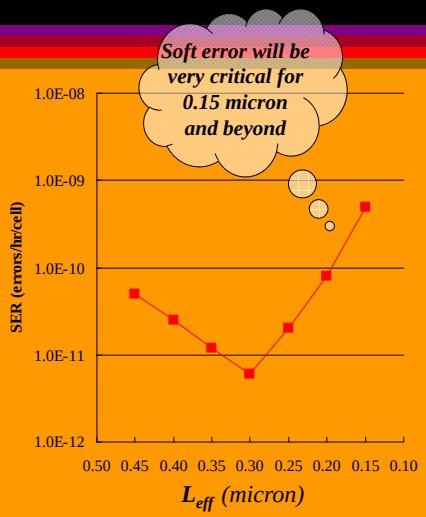


Contamination And Faults



Contamination ***Spot Defect*** ***Circuit Fault***

Soft Error is Critical



Sources of Alpha Particles

- Metal Lines
  Aluminum is contaminated with Thorium and Uranium
- Solder Bumps, Packaging Materials
- Cosmic Rays
  - **SER = 2.15 x 10^6 Airplane altitude**
  - **SER = 3.32 x 10^5 Boulder, Colorado**
  - **SER = 7.70 x 10^4 New York**

NanoSys Solutions To Reliability Problems

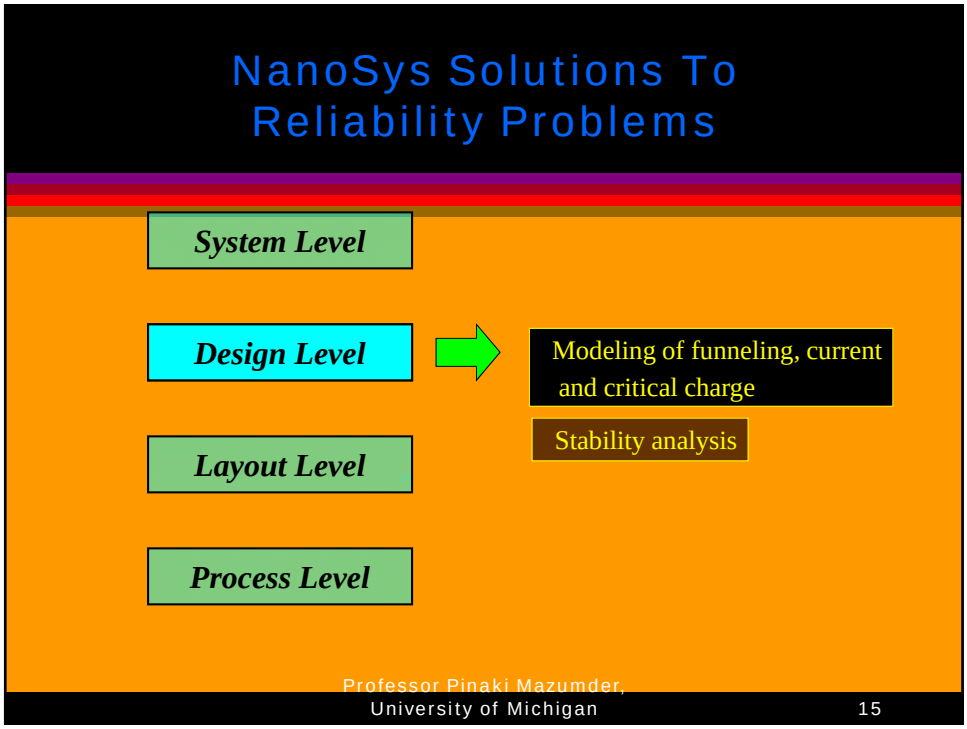
System Level → Self-repair / self-testing; Block-level redundancy

Design Level

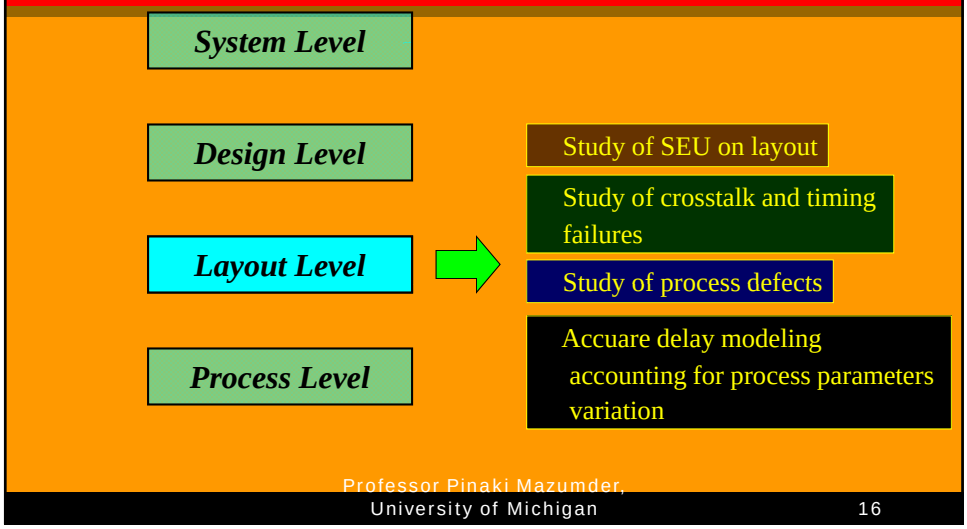
Layout Level

Process Level

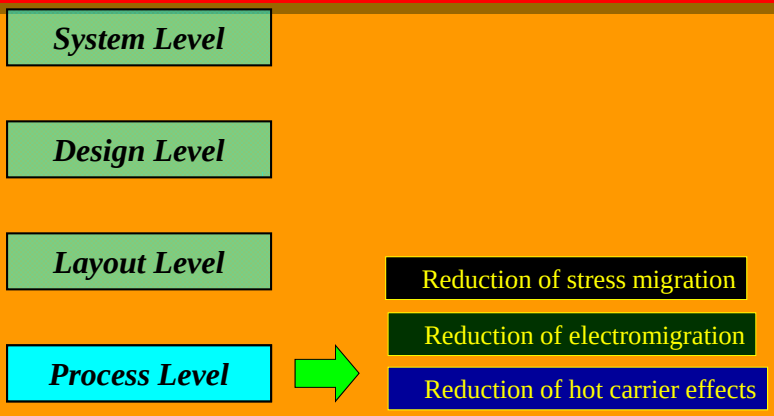
NanoSys Solutions To Reliability Problems



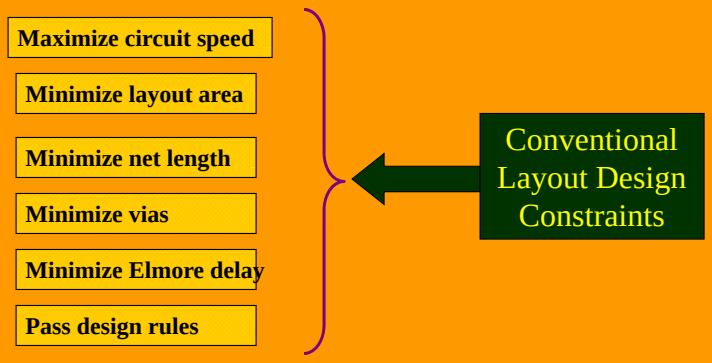
NanoSys Solutions To Reliability Problems



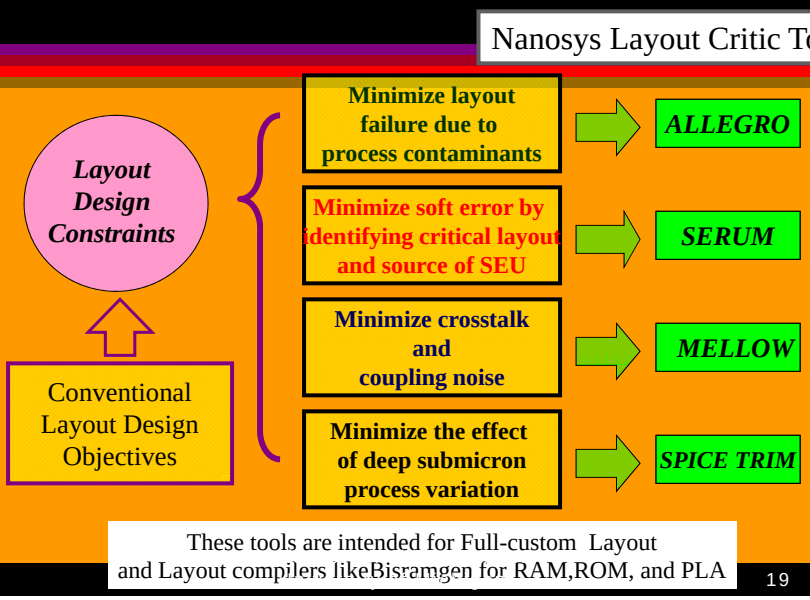
NanoSys Solutions To Reliability Problems



Conventional Layout Design Objectives



Deep-Submicron Layout Design Objectives



Market Size

- Market Size for Memory (SRAM, DRAM and Flash) Compilers and memory modeling at VHDL/Verilog along with Spice Trim for timing analysis is about $200M
- Market Size for Layout Critic Tools for IP vendors and Full-custom designers is about $50M
- Market Size for Yield and Reliabilty analysis is about $50M

Technology

- Currently can support 0.35μ, 0.25μ, and 0.18μ CMOS process technologies
- TSMC, AMI, Orbit and HP process technologies
- Can be extended up to 0.07μ process technology of any vendor
- 2 or more layers of metal + 1 poly

Product Line

FIRST PRODUCT

Panorama - Deep-Submicron Design Optimization Environment

1. *Allegro* - Layout Critic Tool Detects Process Defects
2. *Serum* - Physics Based Layout Critic Tool Detects Alpha Particles Emitting from Chip Materials
3. *Mellow* - Automatic Estimator of Crosstalk Effects
4. *Spice Trim* - Deep-Submicron Timing Analysis Tool
5. *BisramGen* - Robust SRAM Compilers with Self-Testing and Self-Repair Capability

Competitors/Partners

Partners: Cadence, Magma Design Automation, Avanti, Mentor Graphics, Synopsys, Monterey Design Systems, InChip, VLSI Technology, etc.

Competitors: Artisan Components, Virage Logic, Virtual Silicon Technology, Nurlogic Design, Duet Technology, Legend Design Technology

Product Differentiation

BisramGen -

1. Robust SRAM compilers with self-testing and self-repair capability; 2. On-line timing analysis by *Spice Trim* for deep-submicron process parameter scattering and device stress analysis; 3. Cell layout criticing by *Allegro* to eliminate defects resulting from process contaminants; 4. Early estimation of alpha particle induced soft errors and layout refinement by *Serum;* 5. Bit-line coupling and power-bus noise estimation by *Mellow*; 6. VHDL/Verilog Model; 7. GDS and CIF layout output files.

Intellectual Property

Patents: One patent is pending on automatic self-repair of embedded RAM array

Proprietary Techniques: **1. SPICE circuit model reduction technique in Spice Trim, 2. Physics-based alpha particle emission model and plasma discharge mechanism, 3. Defect-based built-in self-testing algorithms, 4. Monte Carlo based 3-dimensional contaminant model and fault classification**

Software Size: **100,000 lines of C code**

Market of First Product

What? 1. BisramGen: A robust memory compiler; 2. Allegro: Layout defect critic tool; 3. Mellow: Crosstalk estimation tool

Where? In USA (Motorola, Lucent Technologies), in Taiwan (TSMC), in Japan (Sony, Fujitsu, Toshiba, NEC, etc.), ...

Who? IP vendors, Full-custom layout tools developers (Avanti, Cadence, Magma, etc.), Silicon synthesis tools developers (Synopsis, Mentor Graphics, etc.)

Market Share

First Product: 1. BisramGen: $8M, 2. Allegro: $10M, 3. SPICE Trim: $1M (Target Date of Introduction: March 31, 2000)

Future Products: 4. Serum, 5. DRAM-Gen, 6. FlashMemGen (Target Date of Introduction: December 31, 2000)

Commercialization

Distribution Plan:

- Direct selling to over 50 IC manufacturers (NEC, Fujitsu, Sony, Samsung, Motorola, Lucent Technologies, etc.)
- Partnership with Layout Companies such as Cadence, Avanti, Magma, Monterey, etc.
- Target market: 400 IC designers who buy Layout design tools

Accomplishment To-date

- 100,000 lines of C Code performing the following:
- BisramGen: Self-testable RAM compiler working at 600 MHz (0.25 μ) **~ $1M**
- Spice Trim: An accurate timing analysis tool that allows reduction of SPICE simulation without ignoring the parasitics **~$0.25M**
- Allegro: Defect analysis and yield modeling tool providing early feedback to layout designers and memory compilers **~$0.75M**

Risks

Intellectual Property: The design concept behind *Allegro*, *Serum* and *Mellow* can be employed by others and similar layout critic tools can be developed, unless NanoSys quickly introduces these products to the market and is recognized as a leader by its customers. NanoSys has a distinct advantage now and must act quickly to market these tools.

Product: *BisramGen* and other compilers developed by NanoSys must retain product differentiation features to penetrate into the market, competing against current *ad hoc* products available in the market. NanoSys must develop memory compilers that will define the industry standards for embedded SRAMs, DRAMs, ROMs and Flash memories. The founder of NanoSys is considered to be a world expert in memory design, testing, repair and compilation.

Risks

Market: The usefulness of *Panorama* will depend on how effective *Allegro*, *Serum* and *Mellow* are in improving the reliability and yield of deep-submicron VLSI chips.Though NanoSys tools will be superior to existing tools like memory compilers, the overall market size of these tools will to a great extent depend on whether NanoSys layout critic tools can also be used for improving the quality of ASIC and high-performance layout tools

Funding: Seed funding will be required to market the initial product. In order to grow rapidly, VC funding of a few million dollars will be needed. The success of NanoSys will not only depend on the quality of its tools, but also on its marketing crew who must develop appropriate marketing strategies to tie up these tools with its partners and to directly reach to the IP core users.

Milestones

- Seed Funding: August 31, 1999
- Beta Version Distribution: January 31, 2000
- Marketing of Panorama: March 31, 2000
- Development Milestones: 1. BisramGen v1 (without self-repair) - November 30, 1999; 2. Allegro v1 - December 31, 1999; 3. Spice Trim v1 - December 31, 1999; 4. Mellow v1 - January 31, 2000; 5. BisramGen v2 (with self-repair) - January 31, 2000; 6. BistROM v1 - March 31, 2000; 7. DRAMGen v1 - May 2000; 8. Serum - June 30, 2000; 9. FlashMemGen v1 - July 31, 2000.

Funding Needs

- Dec. 31, 1999: $650K (5 Engr + 2 Sales) (outcome - Beta version of Panorama)
- Jun. 30, 2000: $2M (1r VC) (20E+5S) (outcome - Marketing of Panorama)
- Dec. 31, 2000: $5M (2r VC) (40E+20S) (outcome - Annual sale of $30M)

Exit Strategies

Strategy 1: (x 7)

- Exit after preparation of Beta version
- Time frame: Mar. 31, 2000
- Seed funding required: $600K; Expected Valuation: $4M

Strategy 2: (x 11)

- Exit after marketing of Initial Product
- Time frame: Dec. 2000
- Funding required: $3.6M; Expected Valuation: $40M

Strategy 3: (x 20)

- Exit after marketing of Few Generations of Products
- Time frame: Aug. 2002
- Funding required: $10M; Expected Valuation: $200M

Mazumder Group Research Team

- **Research Team Members who have Worked on BISRAMGen and Other CAD Tools:** 1. Prof. P. Mazumder, 2. Dr. M. Bhattacharya, Ph.D.; 3. Dr. S. Kulkarni, Ph.D.; 4. Dr. A. Gonzalez, Ph.D.; 5. Mr. V. Warraich, M.S.; 6. Mr. L. Ding, M.S.; 7. S. Mohan, Ph.D. (working at Xilinx for 5 years); 8. K. Chakraborty, Ph.D. (working at IBM for 3 years); 9. J. S.Yih, Ph.D. (working at IBM for 9 years); 10. H. Esbensen, Ph.D. (working at Avanti for 4 years); 11. V. Ramachandran, Ph.D. (working at Cadence for 5 years); 12. A. Gupta; 13. H. Chan, M.S. (working in Intel for 10 years); 14. M. D. Smith, M.S. (working at Intel for 5 years);

Summary

NanoSys will market a suite of CAD Layout Critic and Compilation tools by March 31, 2000

NanoSys initial product will consist of *Panorama*, *BisramGen*, *Allegro* and *Mellow.*

NanoSys requires an initial seed fund of $250K to market its initial product to semiconductor manufacturers

NanoSys plans to grow rapidly and occupy a major percentage of market share. ($200 Billion for world wide semiconductors, with over 15% growth rate.)

Semiconductor Industry Growth

	1995	2030
Semiconductor as % of Electronics	17%	35%
Electronics as % of GWP	4%	8%
Semiconductors as % of GWP	0.7%	3%
CMOS Technology	0.35µm	0.05µm
World Semiconductor Sales	$140B	$12,000B
Annual Growth Rate	16%	8%

Source: Prof. Chenming Hu, UC Berkeley, 1996

Modeling Contamination In IC Manufacturing

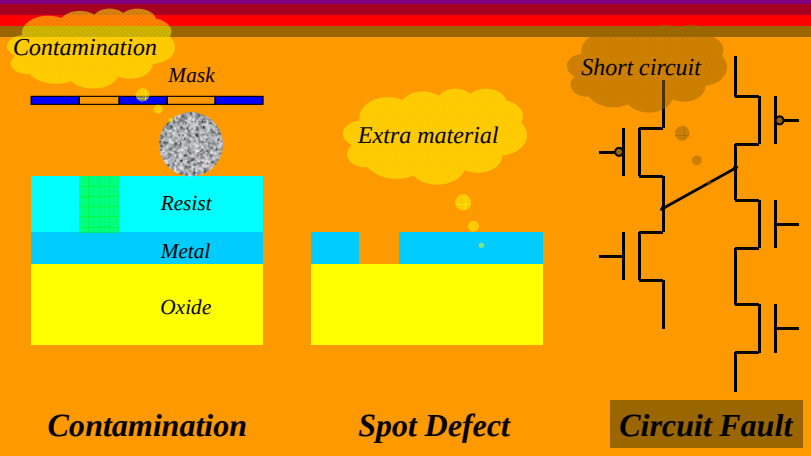
- Terminology

Contamination: any particle or liquid droplet that deposits on the IC during the manufacturing process.

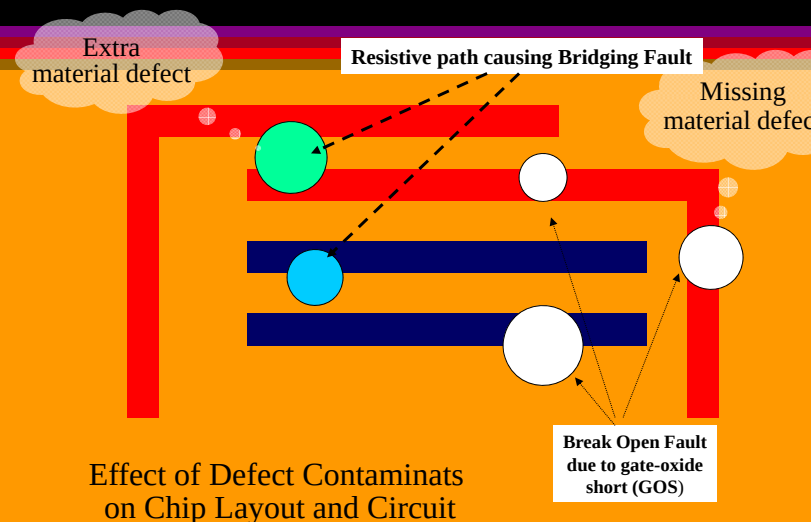
Spot defect: any contamination occurring at appropriate places on the IC that leads to deformation of IC layers.

Fault: A change in the functionality of the IC due to the existence of spot defects.

Relationship Between Contamination, Spot Defects And Faults



Modeling Contamination In IC Manufacturing

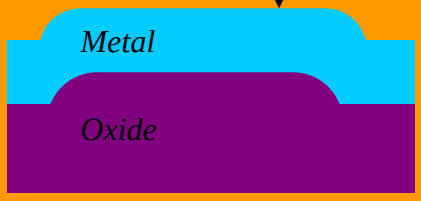


Effect of Defect Contaminats on Chip Layout and Circuit

Process Flow for Metal Deposition

Metal Deposition

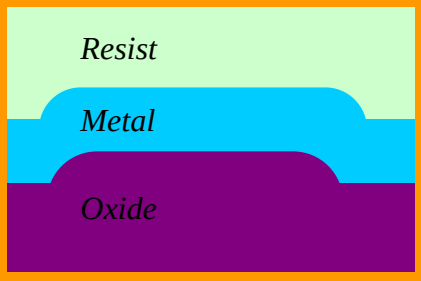
The Objective is to separate Metal into two electrically disconnected segments



Process Flow for Metal Deposition

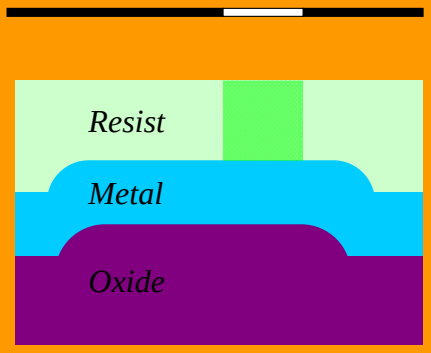
Metal Deposition

Resist Spin



Process Flow for Metal Deposition

Metal Deposition
Resist Spin
Resist Expose



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Metal Deposition
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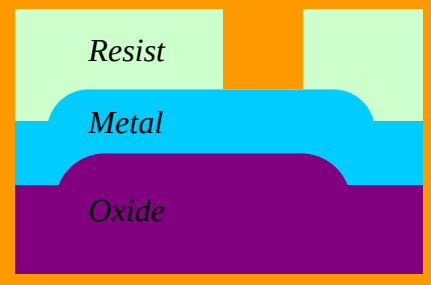
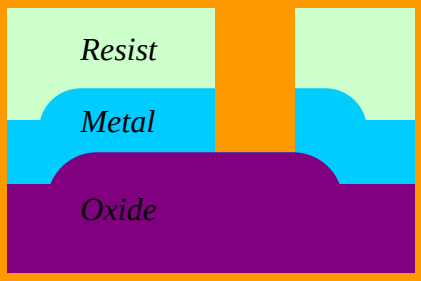


Process Flow for Metal Deposition

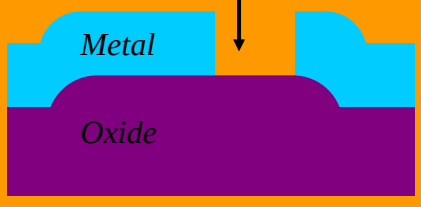
Metal Deposition
Resist Spin
Resist Expose
Resist Develop
Metal Etch



Process Flow for Metal Deposition

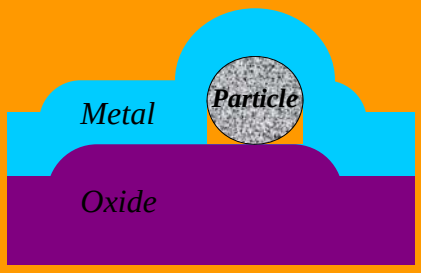
Metal Deposition
Resist Spin
Resist Expose
Resist Develop
Metal Etch
Resist Strip

The metal line is divided into two disconnected segments



Presence of A Contamination — Before Metal Deposition

Metal Deposition



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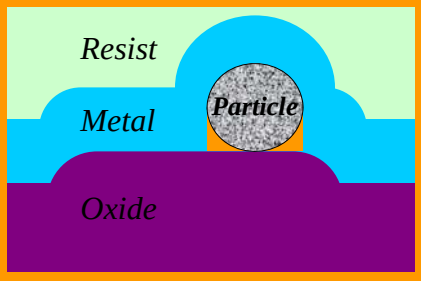

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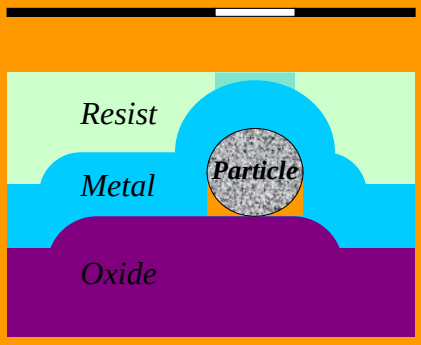
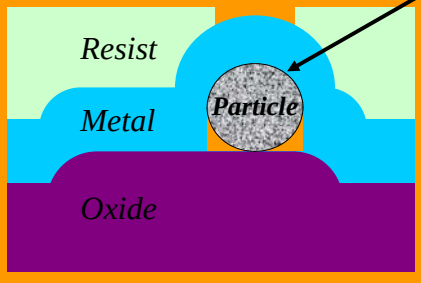


Presence of A Contamination — Before Metal Deposition

Metal Deposition
Resist Spin
Resist Expose
Resist Develop

Process contaminant is present on the oxide layer causing a warp on metal layer at the cut site



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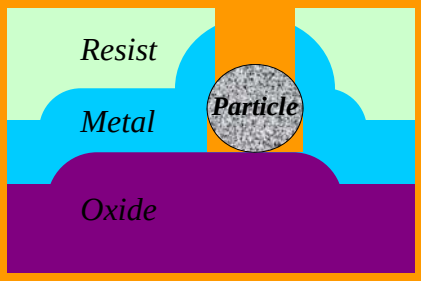

Presence of A Contamination — Before Metal Deposition

Metal Deposition
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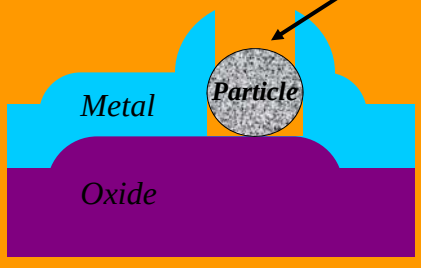
Resist Strip

Process contaminat causes resistive path between metal segments



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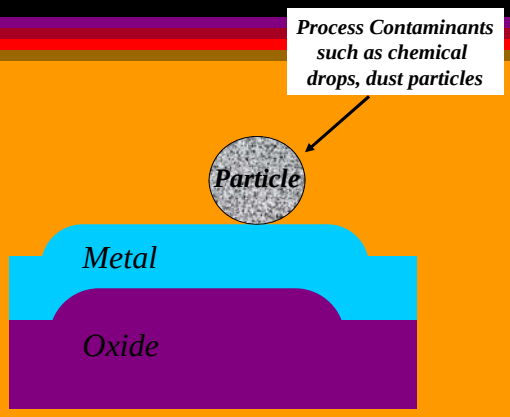

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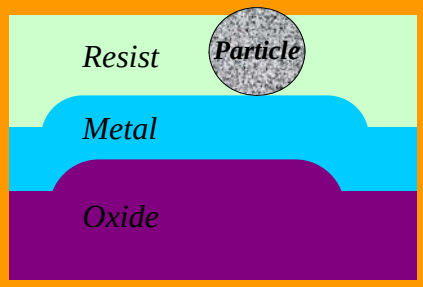

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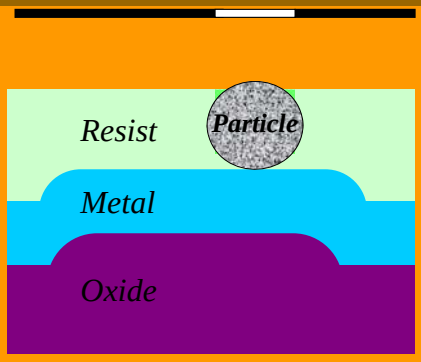

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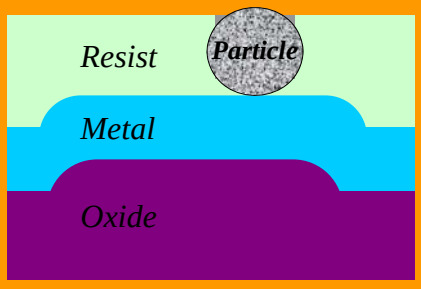
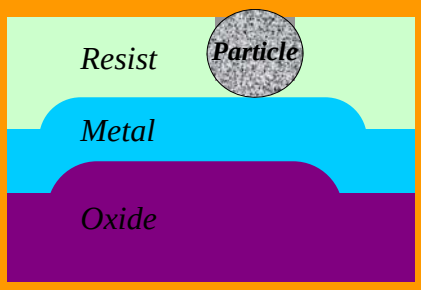


Presence of A Contamination — After Metal Deposition

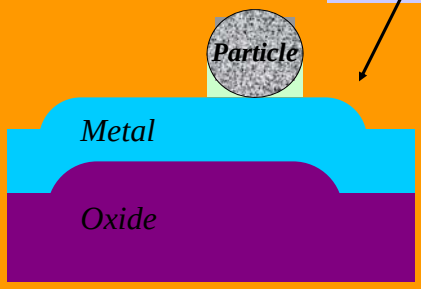
Metal Deposition
Resist Spin
Resist Expose
Resist Develop
Metal Etch



Presence of A Contamination — After Metal Deposition

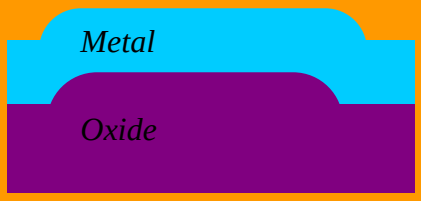
Due to the presence of the process contaminant the metal line remains connected, causing a bridging fault in the circuit

Metal Deposition
Resist Spin
Resist Expose
Resist Develop
Metal Etch
Resist Strip



Presence of A Contamination — After Resist Spin-On

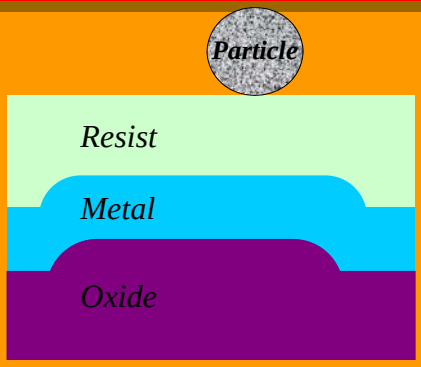
Metal Deposition



Presence of A Contamination — After Resist Spin-On

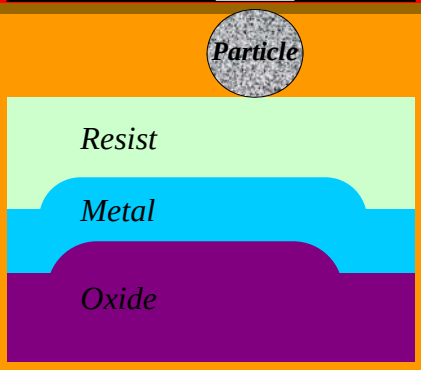
Metal Deposition

Resist Spin



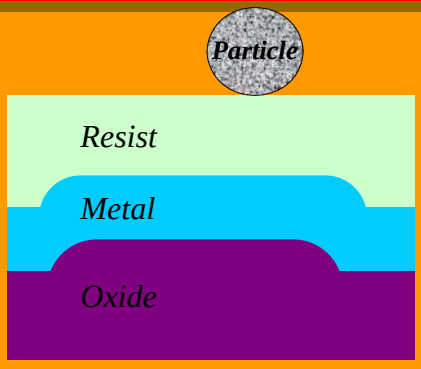
Presence of A Contamination — After Resist Spin-On

Metal Deposition
Resist Spin
Resist Expose



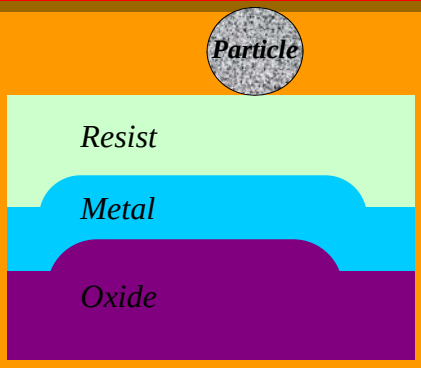
Presence of A Contamination — After Resist Spin-On

Metal Deposition
Resist Spin
Resist Expose
Resist Develop



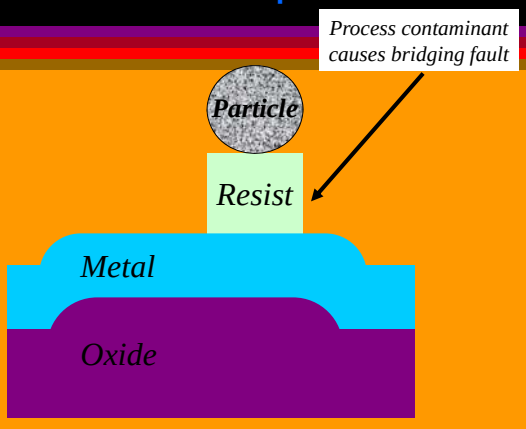
Presence of A Contamination — After Resist Spin-On

Metal Deposition
Resist Spin
Resist Expose
Resist Develop
Metal Etch



Presence of A Contamination — After Resist Spin-On

Metal Deposition
Resist Spin
Resist Expose
Resist Develop
Metal Etch
Resist Strip



Presence of A Contamination — Before Metal Deposition

Metal Deposition

Resist Spin

Resist Expose

Resist Develop

Metal Etch