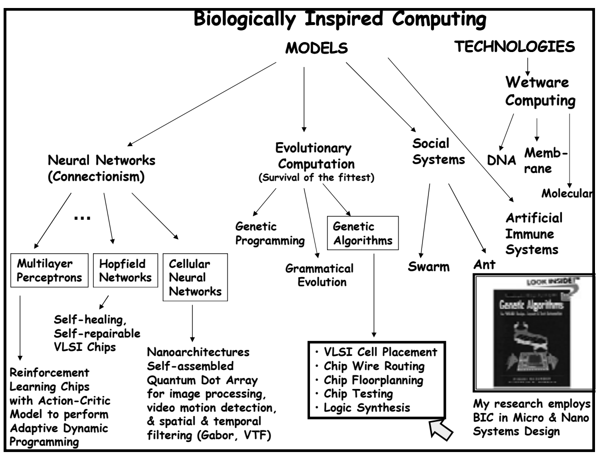
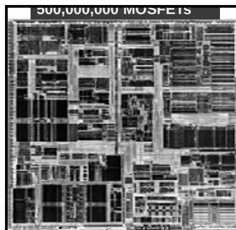
Biologically Inspired Algorithms for Micro and Nano System Design

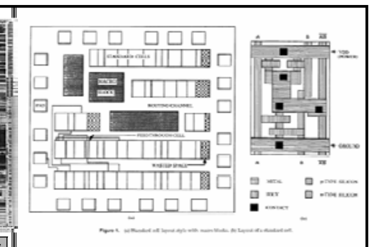
Prof. Pinaki Mazumder,
Univ. of Michigan
Ann Arbor, MI 48105

Outline of the Talk

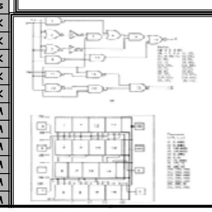
- Evolutionary Approach to Distributed VLSI Layout Synthesis
- Self-Healing of VLSI Chips by Neurally Inspired Hardware Methods
- Neuromorphic Nanoarchitecture using Cellular Nonlinear Network Model
- Reinforcement Learning Hardware



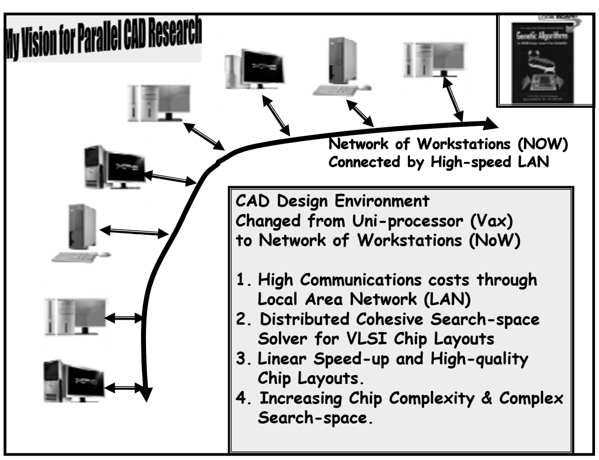


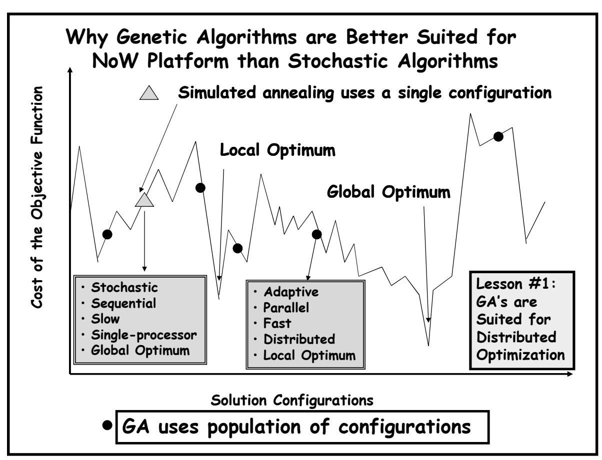


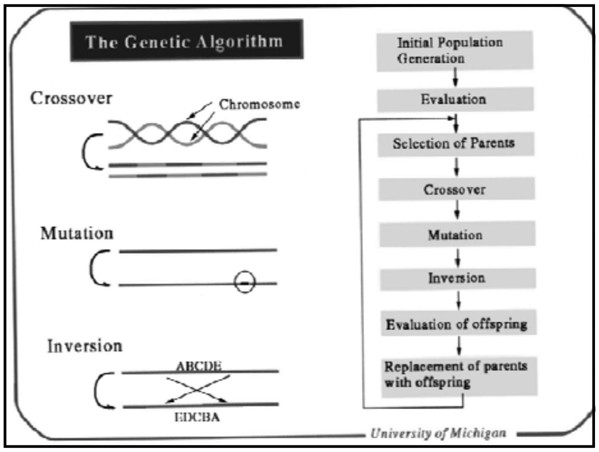
	Year	Transistors
4004	1971	2.25 K
8080	1974	5 K
8086	1978	29 K
286	1982	120 K
Intel386™	1985	275 K
Intel486™	1989	1.1 M
Pentium®	1993	3.1 M
Pentium® II	1997	7.5 M
Pentium® 4	2000	42 M
Itanium®	2002	220 M
Itanium® 2	2003	410 M

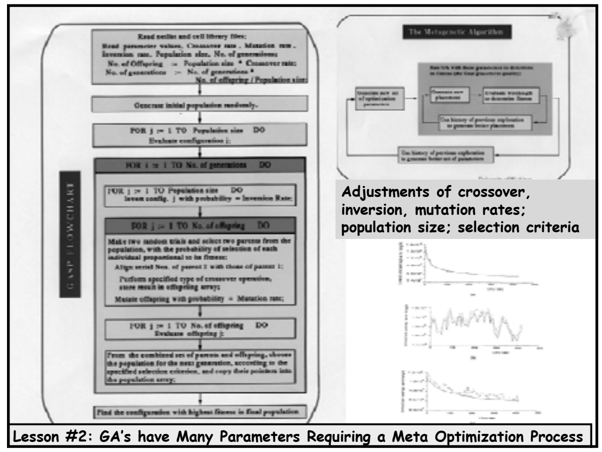


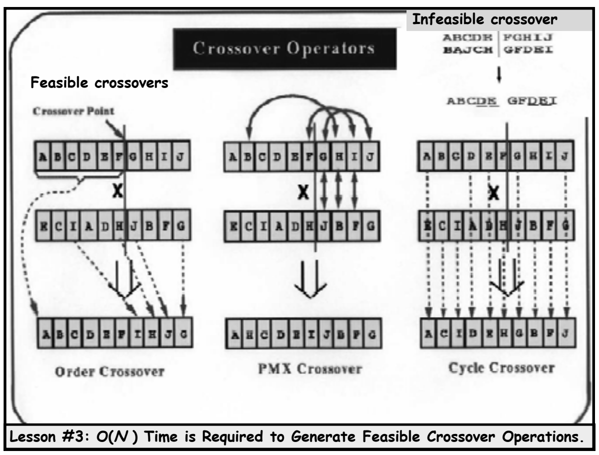
Massive Constrained Permutation Problem with over 250,000 Elements.

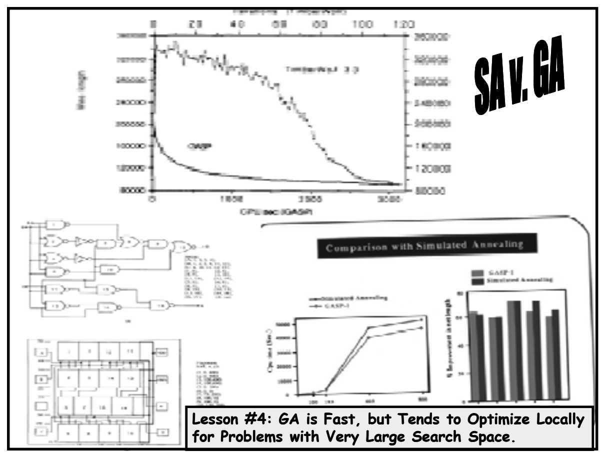


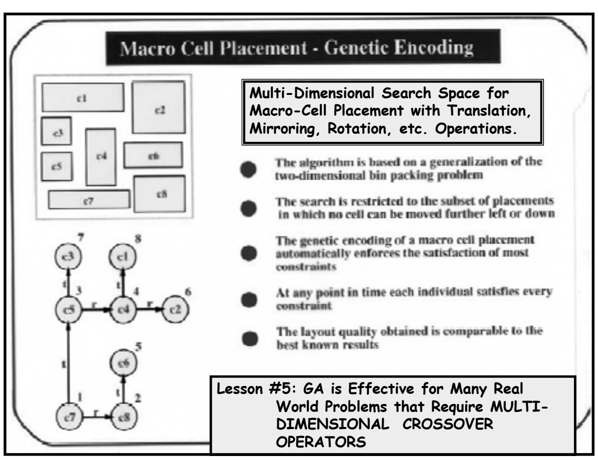



The Genetic Algorithm
Crossover
Chromosome
Mutation
Inversion
ABCDE
EDCBA
Initial Population Generation
Evaluation
Selection of Parents
Crossover
Mutation
Inversion
Evaluation of offspring
Replacement of parents with offspring
University of Michigan


Adjustments of crossover, inversion, mutation rates; population size; selection criteria
Lesson #2: GA's have Many Parameters Requiring a Meta Optimization Process


Infeasible crossover
Crossover Operators
Feasible crossovers
Crossover Point
Order Crossover
PMX Crossover
Cycle Crossover
Lesson #3: O(N) Time is Required to Generate Feasible Crossover Operations.


SA v. GA
Comparison with Simulated Annealing
Lesson #4: GA is Fast, but Tends to Optimize Locally for Problems with Very Large Search Space.


Macro Cell Placement - Genetic Encoding
Multi-Dimensional Search Space for Macro-Cell Placement with Translation, Mirroring, Rotation, etc. Operations.
The algorithm is based on a generalization of the two-dimensional bin packing problem
The search is restricted to the subset of placements in which no cell can be moved further left or down
The genetic encoding of a macro cell placement automatically enforces the satisfaction of most constraints
At any point in time each individual satisfies every constraint
The layout quality obtained is comparable to the best known results
Lesson #5: GA is Effective for Many Real World Problems that Require MULTI-DIMENSIONAL CROSSOVER OPERATORS

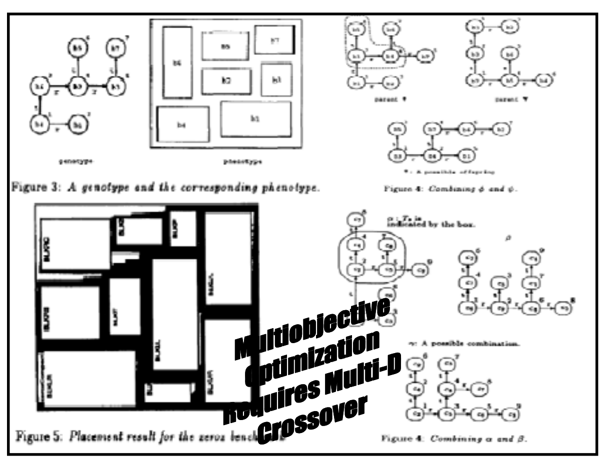
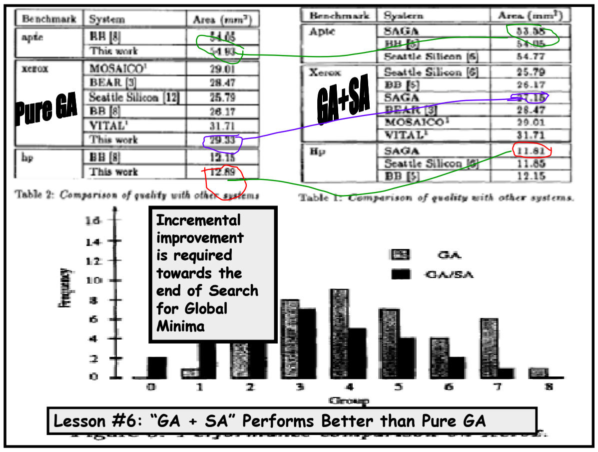


Figure 3: A genotype and the corresponding phenotype.
Figure 4: Combining α and β.
Multiobjective Optimization Requires Multi-D Crossover
Figure 5: Placement result for the xerox benchmark

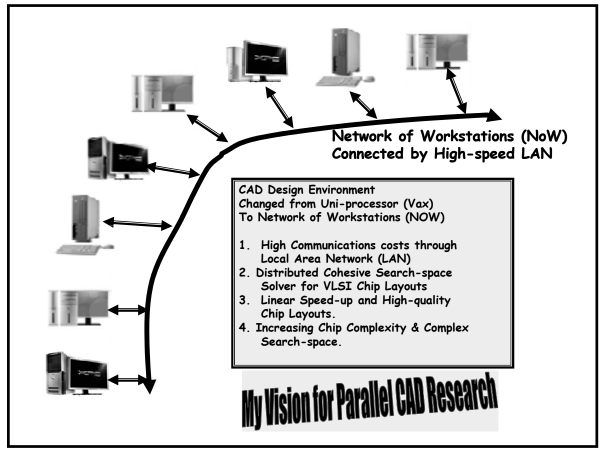


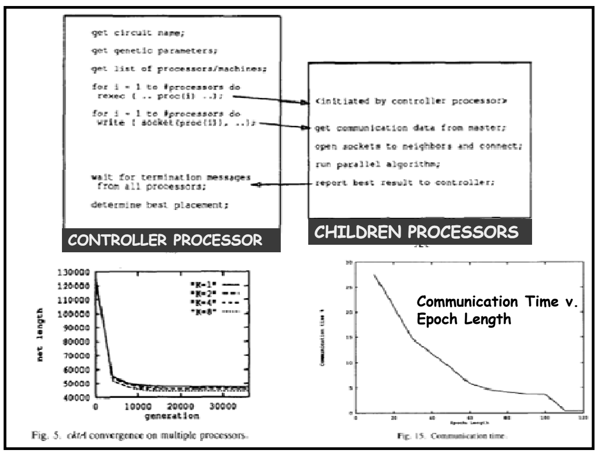
Benchmark	System	Area (mm²)
apte	BB [8]	54.05
	This work	54.93
xerox	MOSAICO[1]	29.01
	BEAR [3]	28.47
	Seattle Silicon [12]	25.79
	BB [8]	26.17
	VITAL[1]	31.71
	This work	29.33
hp	BB [8]	12.15
	This work	12.89

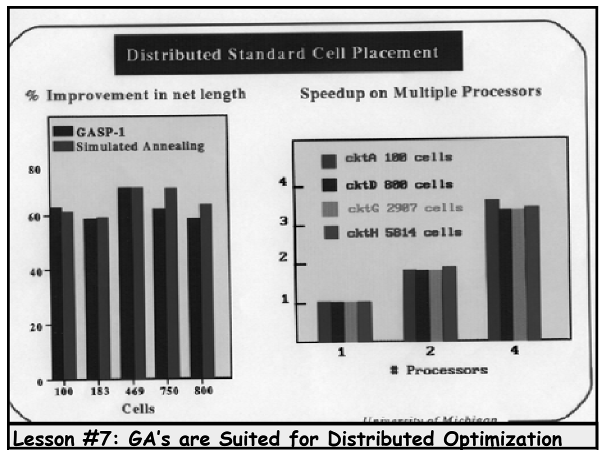
Table 2: *Comparison of quality with other systems*

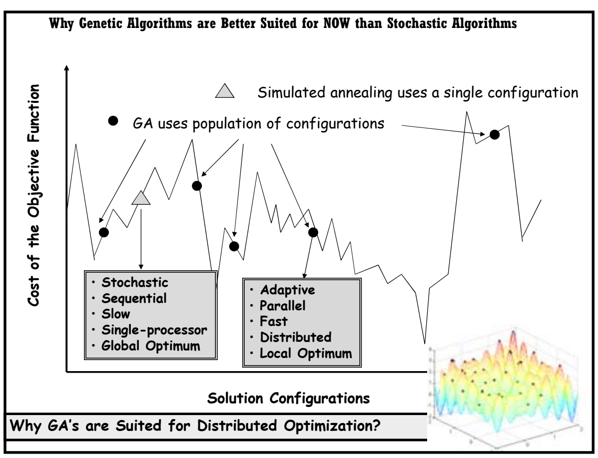
Benchmark	System	Area (mm²)
Apte	SAGA	53.55
	BB [5]	54.05
	Seattle Silicon [6]	54.77
Xerox	Seattle Silicon [6]	25.79
	BB [5]	26.17
	SAGA	27.15
	BEAR [3]	28.47
	MOSAICO[1]	29.01
	VITAL[1]	31.71
Hp	SAGA	11.81
	Seattle Silicon [6]	11.85
	BB [5]	12.15

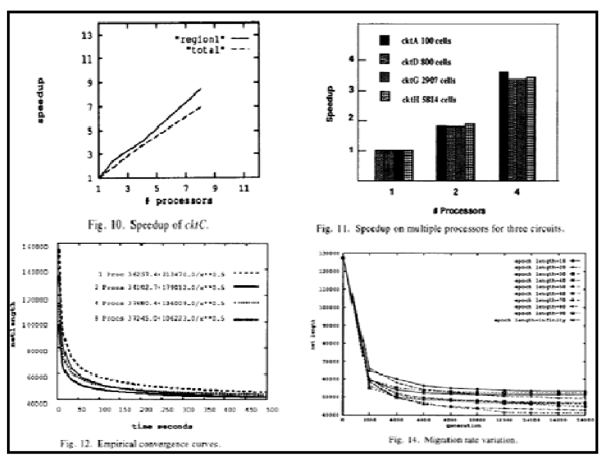
Table 1: *Comparison of quality with other systems.*







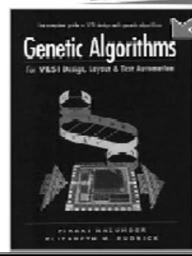




VARIOUS ASPECTS OF GA'S FOR VLSI DESIGN, TEST AND LAYOUT OPTIMIZATION

- Adaptive, learns from experience
- Intrinsic Parallelism
- Efficient for complex problems with hilly search spaces
- Can handle various cost functions and constraints
- Easy to parallelize on a workstation network, without much communication overhead, and with near-linear speedup

University of Michigan



Opportunities for Future Research:

Mathematical Modeling of Genetic Process

Simulated annealing uses Markov Chain to give polynomial time solution.

Probability analysis & Empirical modeling is needed for sequential and distributed Genetic optimization.

- Circuit partitioning
- Macro cell routing, including Steiner problems and global routing
- Standard cell and macro cell placement
- Circuit segmentation, FPGA mapping and pseudo-exhaustive testing
- Automatic test generation including compaction, deterministic/genetic test hybrids and integration of finite state machine sequences
- Peak power estimation

OPEN PROBLEM #1: Markov Chain can be used to model the Simulated Annealing by representing each solution configuration by a State in the Markov Chain and by using the probability of an Incremental transformation as the Transition Probability between different states.

It will lead to a Markov Chain of Length, L such that at the end one can obtain near Global Optimal solution. The Length, L can be controlled by selecting suitable Annealing Parameters and Inner Loop stopping criteria up to 4 or 5 Variables only.

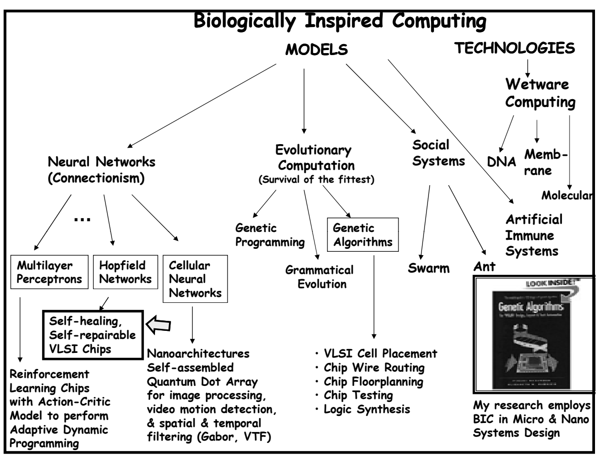
However, the Genetic Algorithm applies Crossover that Causes Multiple Changes in the Chromosome. It cannot be represented by the Markov Chain model. A better way to apply very rigorous Probability Modeling Technique that will simultaneously optimize parameters such as Crossover rate, Mutation rate, Inversion rate, Population Size, etc.

OPEN PROBLEM #2: Distributed Genetic Algorithm will require a more complex Mathematical Modeling to compute the Epoch rate, Search cohesion, Speedup, etc.

OPEN PROBLEM #3: Are GA's suited for Constrained Combinatorial Optimization like in VLSI layouts? How to devise clever Crossover Operators for such cases? Are there advantages of Multidimensional Crossover operators in Multivariate Optimizations?

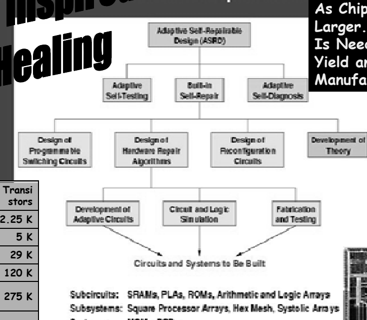
Outline of the Talk

- Evolutionary Approach to Distributed VLSI Layout Synthesis
- Self-Healing of VLSI Chips by Neurally Inspired Hardware Methods
- Neuromorphic Nanoarchitecture using Cellular Nonlinear Network Model
- Reinforcement Learning Hardware



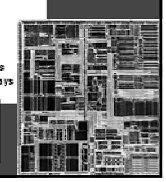
Neural Inspired Chip Healing

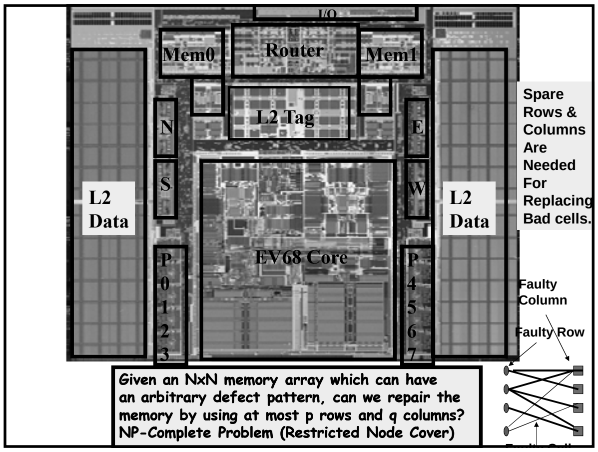
Manufacturing Yield Reduces Dramatically As Chips Become Larger. Self Healing Is Needed to Improve Yield and Reduce Chip Manufacturing Cost.

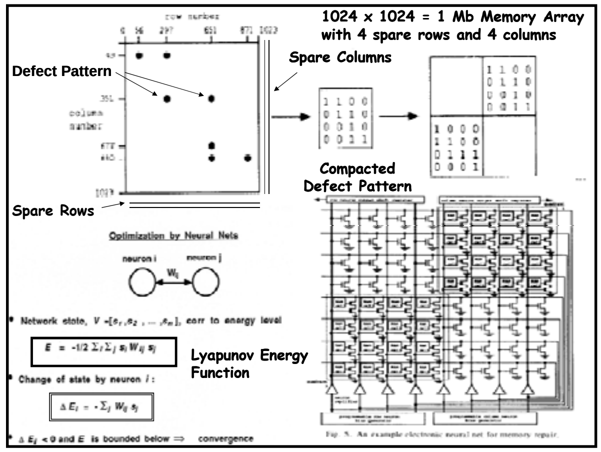


	Year	Transistors
4004	1971	2.25 K
8080	1974	5 K
8086	1978	29 K
286	1982	120 K
Intel386™	1985	275 K
Intel486™	1989	1.1 M
Pentium®	1993	3.1 M
Itanium®	2002	220 M
Itanium® 2	2003	410 M

Objective: Show the concept of self-healing by restructuring a megabit Memory array of RAM







Cost of a Repair Scheme

- Spare Allocation Criteria
  - * To encourage all available spares be used

$$\Rightarrow C_1 = A/2 \left[(\Sigma s_{1i} - p)^2 + (\Sigma s_{2j} - q)^2 \right]$$

  - * To encourage the min. usage of spares

$$\Rightarrow C'_1 = A/2 \left[(\Sigma s_{1i})^2 + (\Sigma s_{2j})^2 \right]$$

- Fault Coverage Consideration
  - * To encourage all defects be covered

$$\Rightarrow C_2 = B \left[\Sigma \Sigma d_{ij}(1-s_{1i})(1-s_{2j}) \right]$$

- Cost Function $C_{MR} = C_1 + C_2$ or $C'_1 + C_2$

Gradient Descent Neural Nets

Let $C_{MR} = E_{NN}$, we get

$$W_{1i,1j} = -A(1-\delta_{ij}), \quad W_{2i,2j} = -A(1-\delta_{ij}),$$
$$W_{1i,2j} = -B\, d_{ij}, \quad W_{2i,1j} = -B\, d_{ji},$$
$$b_{1i} = (p - 1/2) A + B \Sigma_j d_{ij},$$
$$b_{2j} = (q - 1/2) A + B \Sigma_i d_{ij},$$

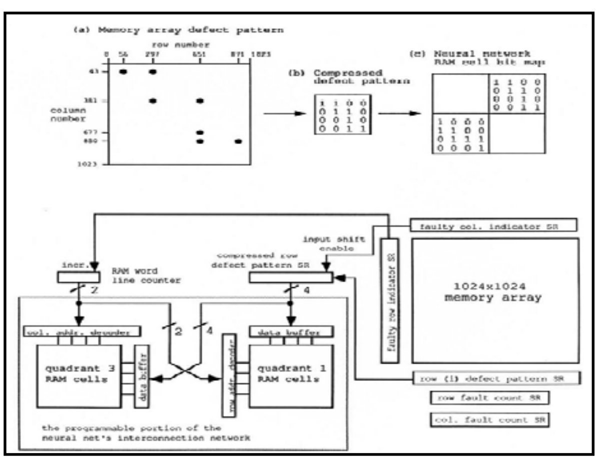
where $\delta_{ij} = 0$ if $i=j$, otherwise 1.

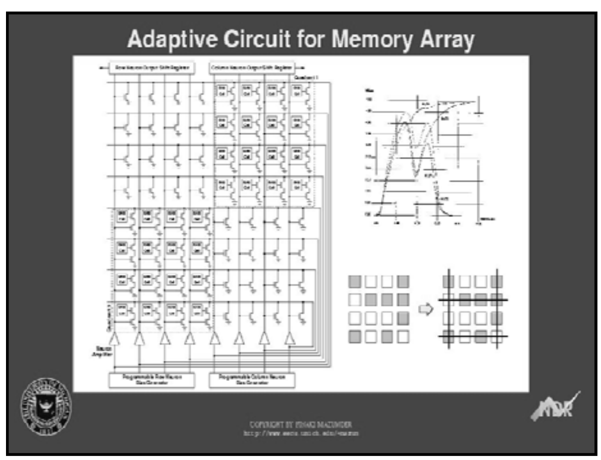
Hill Climbing Neural Nets

Let $C_{MR} = E_{NN}$ with self-feedback allowed, we get

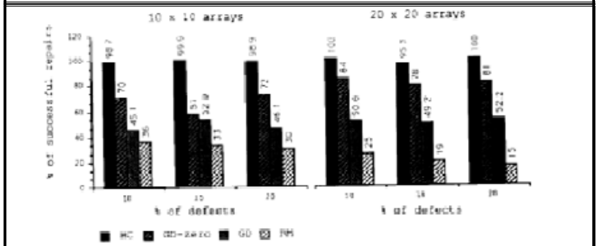
$$W_{1i,1j} = -A, \quad W_{2i,2j} = -A,$$
$$W_{1i,2j} = -B\, d_{ij}, \quad W_{2i,1j} = -B\, d_{ji},$$
$$b_{1i} = p\, A + B \Sigma_j d_{ij},$$
$$b_{2j} = q\, A + B \Sigma_i d_{ij}$$

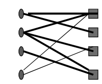
Must have A > B



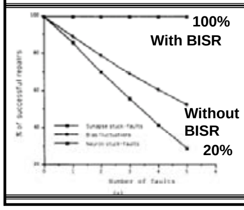


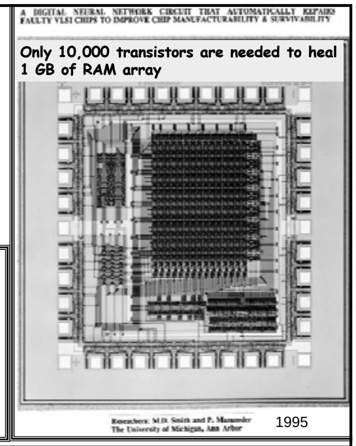
COMPARISON BETWN. NUROMORPHIC v. SOFTWARE TECHNIQUES



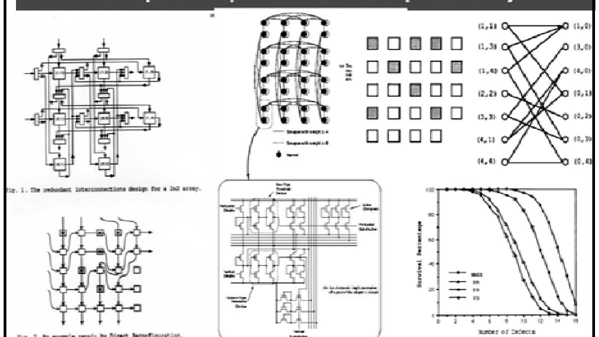


Manufacturing Yield





Adaptive Repair Circuit for Square Array

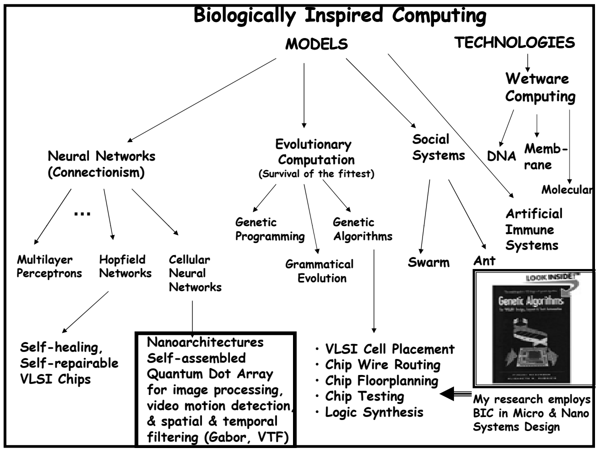


Neural-inspired Maximum Matching Problem on a Bipartite Graph.

Outline of the Talk

- Evolutionary Approach to Distributed VLSI Layout Synthesis
- Self-Healing of VLSI Chips by Neurally Inspired Hardware Methods
- Neuromorphic Nanoarchitecture using Cellular Nonlinear Network Model
- Reinforcement Learning Hardware

Biologically Inspired Computing



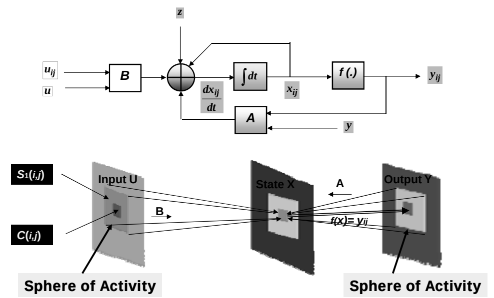
CISE Perspectives of EMT & ITRS Road Map for Architectures are Consistent.

Emerging Research Architecture Implementations

Architecture Implementations	Cellular Array Implementations: Quantum Cellular Automata	Cellular Array Implementations: Cellular Nonlinear Networks	Defect Tolerant Implementations	Biologically Inspired Implementations	Coherent Quantum Computing
Application Domain	• Not demonstrated	• Fast image processing • Associative memory • Complex signal processing	• Reliable computing with unreliable devices (such as SETs with background noise) • Historical examples include WSI • Teramac FPGA implementations	• Goal-driven computing using simple and recursive algorithms • High computational efficiency through data compression algorithms	• Special algorithms such as factoring and deep data searches
Device And Interconnect Implementations	• Arrays of nanodots or molecular assemblies	• Resonant tunneling devices	• Molecular switches, • Crossed arrays of 1D structures • Switchable interconnects	• Molecular organic and bio-molecular devices and interconnects	• Spin resonance transistors • NMR devices • Single flux quantum devices • Photonics

NANO | BIC | QIS

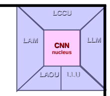
CNN Cell Structure

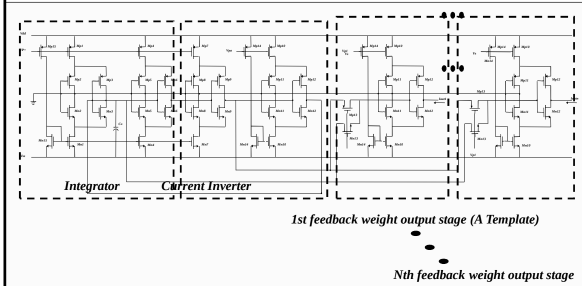


A: Feedback Template
B: Feed-forward Template

$$C\frac{dX_{ij}(t)}{dt} = -h(X_{ij}(t)) + \sum_{C(k,l)\in N_r(i,j)} (AX_{kl} + BU_{kl}) + I$$

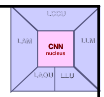
VLSI Implementation – CMOS CNN Nucleus



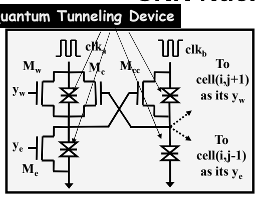


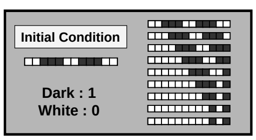
Source: *L. Ravezzi, G.F. Dalla Betta, G. Setti*
Cellular Neural Networks and Their Applications, 1998. (CNNA 1998). Proceedings of the 1998 5th IEEE International Workshop on , April 1998 Pages:253- 258

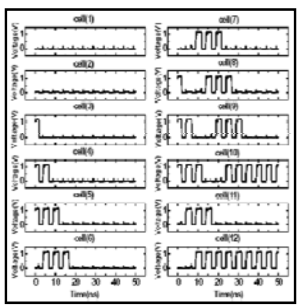
VLSI Implementation – QMOS CNN Nucleus for HCCD



Quantum Tunneling Device

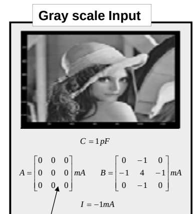


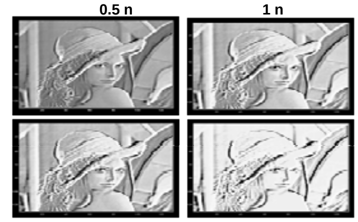




4 transistors & 4 RTDs for one cell

CNN-based Image Processing Edge Extraction-128x128

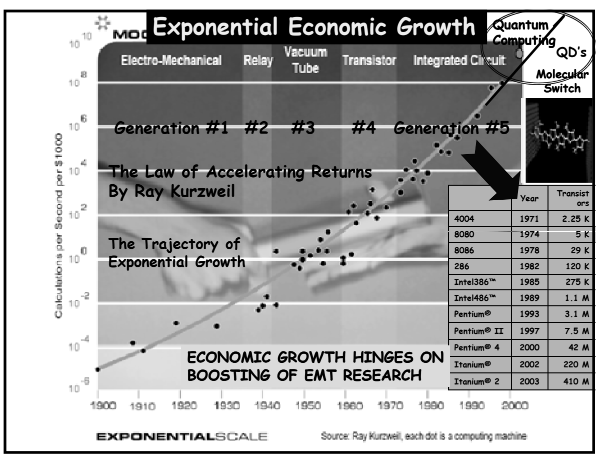




The structure of the synaptic Network between the base cell and neighboring cells.

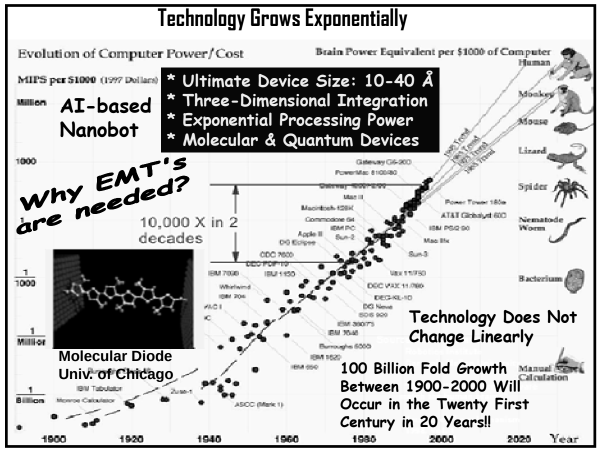
Roadmap

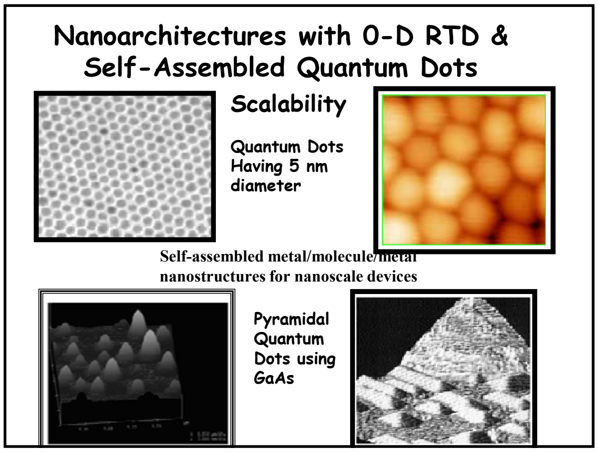
Exponential Economic Growth

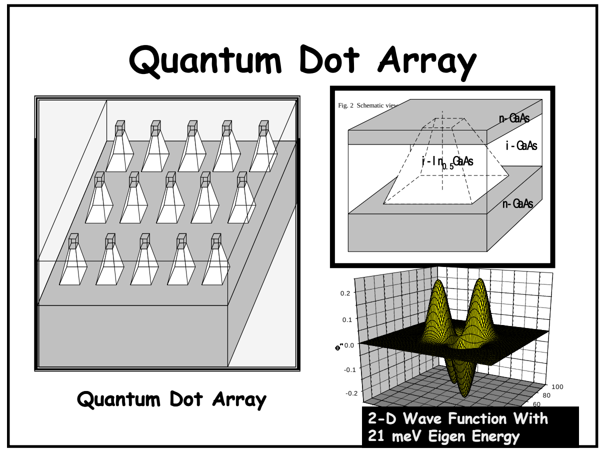


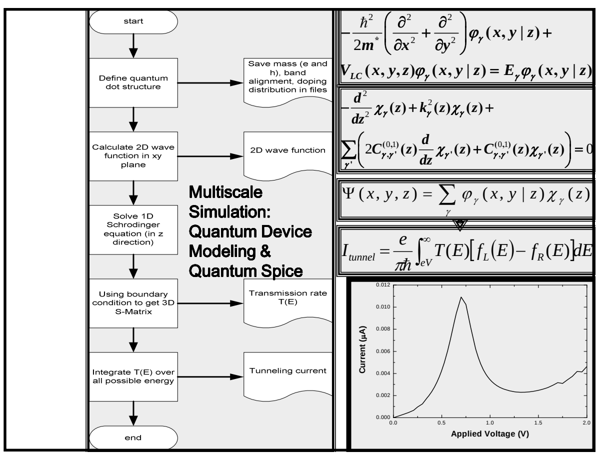
	Year	Transistors
4004	1971	2.25 K
8080	1974	5 K
8086	1978	29 K
286	1982	120 K
Intel386™	1985	275 K
Intel486™	1989	1.1 M
Pentium®	1993	3.1 M
Pentium® II	1997	7.5 M
Pentium® 4	2000	42 M
Itanium®	2002	220 M
Itanium® 2	2003	410 M

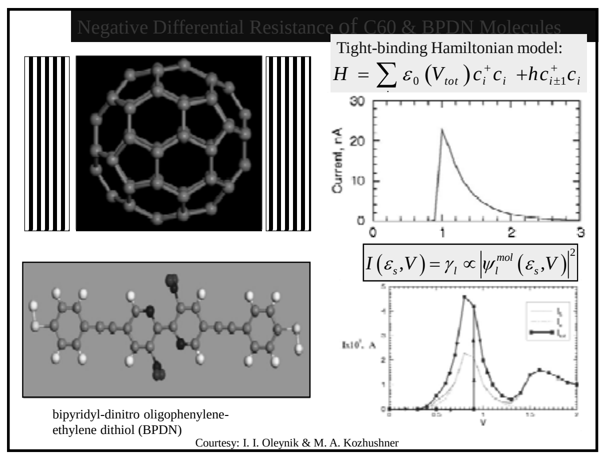
Technology Grows Exponentially

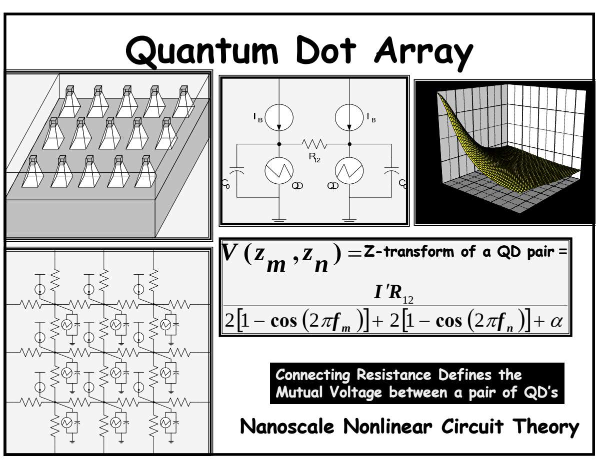


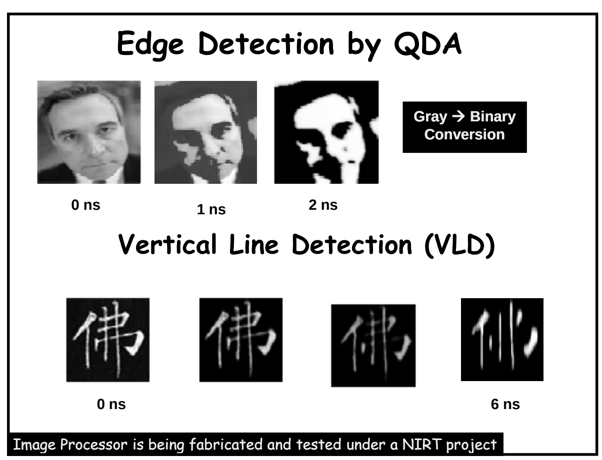

Nanoarchitectures with 0-D RTD &
Self-Assembled Quantum Dots
Scalability
Quantum Dots Having 5 nm diameter
Self-assembled metal/molecule/metal nanostructures for nanoscale devices
Pyramidal Quantum Dots using GaAs

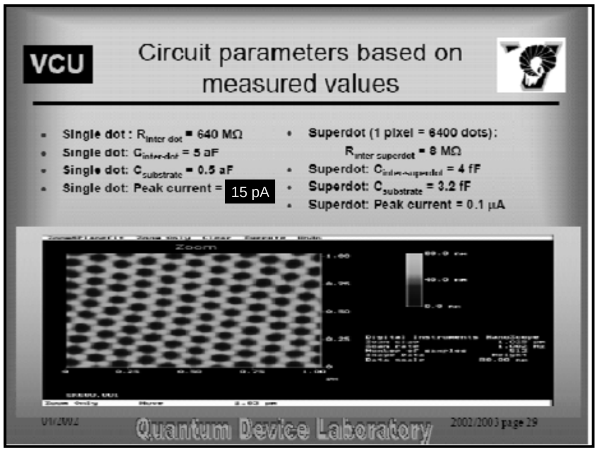

Quantum Dot Array
n-GaAs
i-GaAs
n-GaAs
Quantum Dot Array
2-D Wave Function With 21 meV Eigen Energy

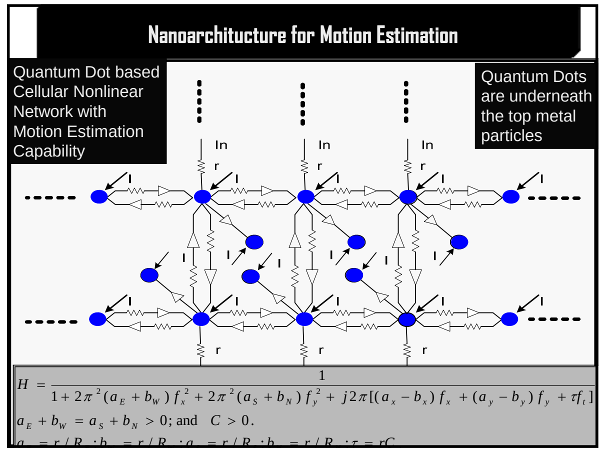

start
Define quantum dot structure
Save mass (e and h), band alignment, doping distribution in files
Calculate 2D wave function in xy plane
2D wave function
Solve 1D Schrodinger equation (in z direction)
Using boundary condition to get 3D S-Matrix
Transmission rate T(E)
Integrate T(E) over all possible energy
Tunneling current
end
Multiscale Simulation: Quantum Device Modeling & Quantum Spice
Current (μA)
Applied Voltage (V)

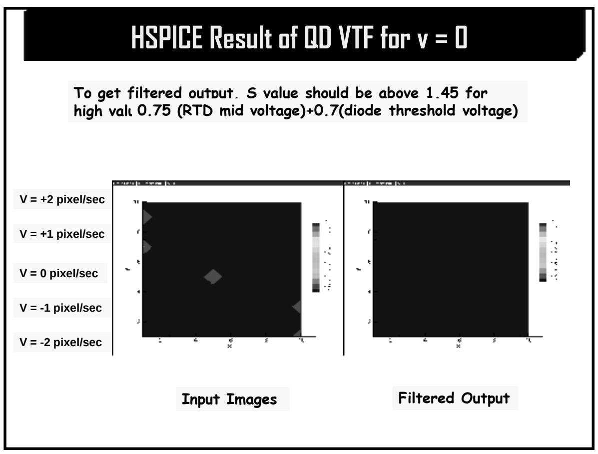

Negative Differential Resistance of C60 & BPDN Molecules
Tight-binding Hamiltonian model:
Current, nA
bipyridyl-dinitro oligophenylene-ethylene dithiol (BPDN)
Courtesy: I. I. Oleynik & M. A. Kozhushner

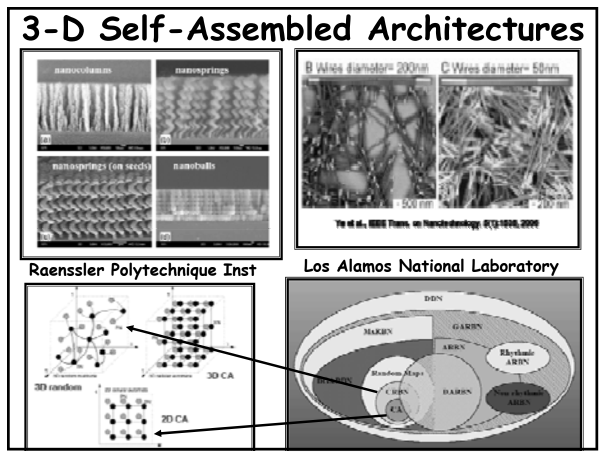

Quantum Dot Array
Z-transform of a QD pair
Connecting Resistance Defines the Mutual Voltage between a pair of QD's
Nanoscale Nonlinear Circuit Theory


Edge Detection by QDA
Gray → Binary Conversion
0 ns
1 ns
2 ns
Vertical Line Detection (VLD)
0 ns
6 ns
Image Processor is being fabricated and tested under a NIRT project







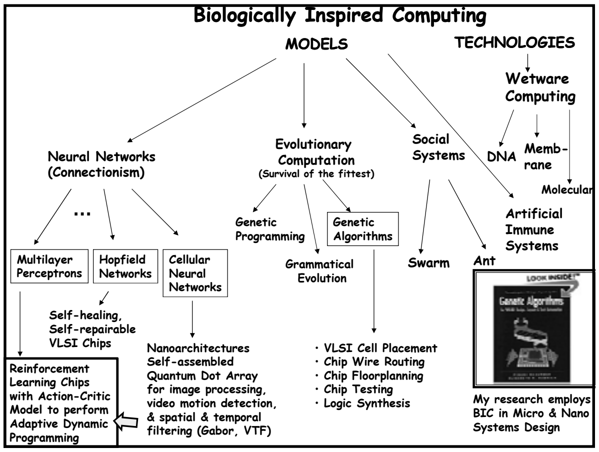


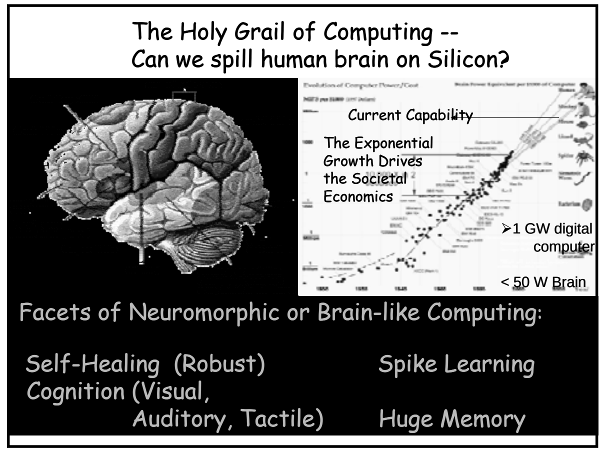
Applications of 3-D Self-Assembled Architectures (Random Boolean Networks)

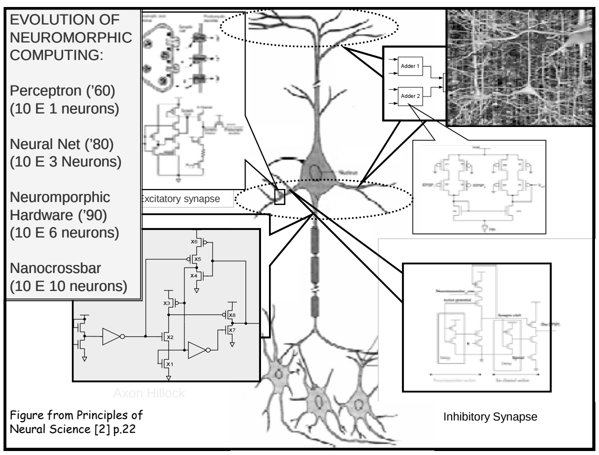
- Genetic Regulatory Networks (Kauffman 1993, Gershenson 2005)
  - Understanding of disease treatment
  - Genomic interaction and data mining
- Evolutionary Computing & Evolvable Hardware (JPL)
- Artificial Neural Networks (Huepe & Aldana, 2002)
- Social Modeling (Shelling 1971)
- Robotics (Quick, et al. 2003)
- Cellular Automata (Wuensche and Lesser, 1992)
- Percolation Theory (Stauffer, 1985)
- Biologically Inspired Computing (Swarm, Ant forage, …)

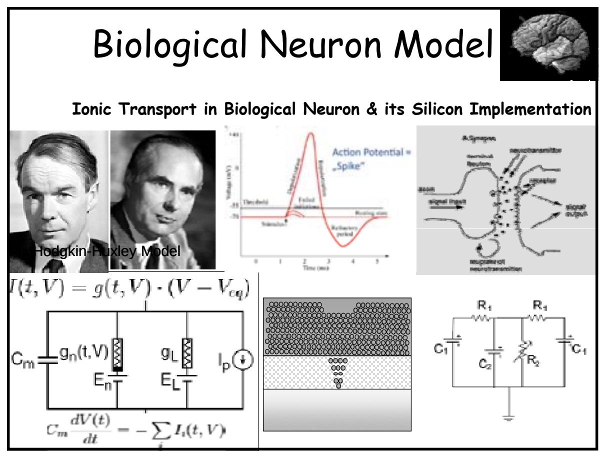
Outline of the Talk

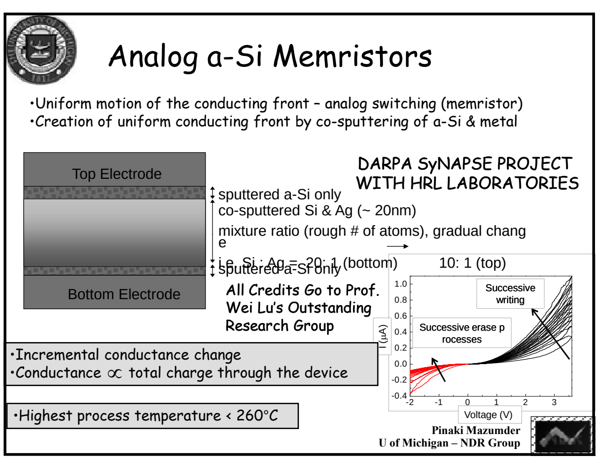
- Evolutionary Approach to Distributed VLSI Layout Synthesis
- Self-Healing of VLSI Chips by Neurally Inspired Hardware Methods
- Neuromorphic Nanoarchitecture using Cellular Nonlinear Network Model
- Reinforcement Learning Hardware ⇦

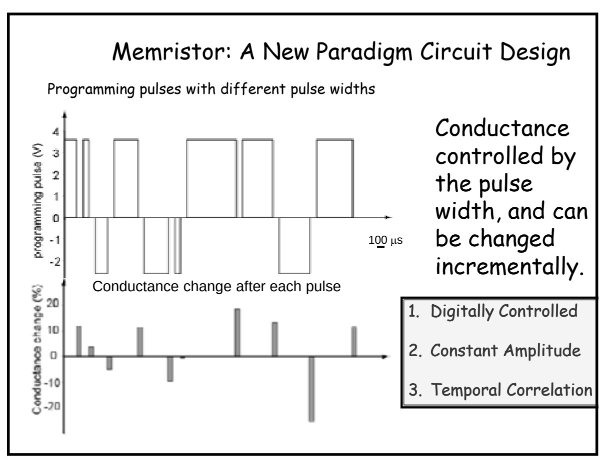

Biologically Inspired Computing
MODELS
TECHNOLOGIES
Wetware Computing
Neural Networks (Connectionism)
Evolutionary Computation (Survival of the fittest)
Social Systems
DNA
Memb-rane
Molecular
Artificial Immune Systems
...
Genetic Programming
Genetic Algorithms
Multilayer Perceptrons
Hopfield Networks
Cellular Neural Networks
Grammatical Evolution
Swarm
Ant
Self-healing, Self-repairable VLSI Chips
Reinforcement Learning Chips with Action-Critic Model to perform Adaptive Dynamic Programming
Nanoarchitectures Self-assembled Quantum Dot Array for image processing, video motion detection, & spatial & temporal filtering (Gabor, VTF)
• VLSI Cell Placement
• Chip Wire Routing
• Chip Floorplanning
• Chip Testing
• Logic Synthesis
My research employs BIC in Micro & Nano Systems Design


The Holy Grail of Computing --
Can we spill human brain on Silicon?
Current Capability
The Exponential Growth Drives the Societal Economics
➤1 GW digital computer
< 50 W Brain
Facets of Neuromorphic or Brain-like Computing:
Self-Healing (Robust)
Spike Learning
Cognition (Visual, Auditory, Tactile)
Huge Memory


EVOLUTION OF NEUROMORPHIC COMPUTING:
Perceptron ('60)
(10 E 1 neurons)
Neural Net ('80)
(10 E 3 Neurons)
Neuromporphic Hardware ('90)
(10 E 6 neurons)
Nanocrossbar
(10 E 10 neurons)
Excitatory synapse
Adder 1
Adder 2
Axon Hillock
Inhibitory Synapse
Figure from Principles of Neural Science [2] p.22


Biological Neuron Model
Ionic Transport in Biological Neuron & its Silicon Implementation
Hodgkin-Huxley Model
Action Potential = „Spike"
$I(t,V) = g(t,V) \cdot (V - V_{eq})$
C_m
$g_n(t,V)$
g_L
I_p
E_n
E_L
$C_m \frac{dV(t)}{dt} = -\sum I_i(t,V)$
R_1
R_1
C_1
C_2
R_2
C_1


Analog a-Si Memristors
•Uniform motion of the conducting front – analog switching (memristor)
•Creation of uniform conducting front by co-sputtering of a-Si & metal
Top Electrode
Bottom Electrode
sputtered a-Si only
co-sputtered Si & Ag (~ 20nm)
mixture ratio (rough # of atoms), gradual change
Sputtered a-Si only
10: 1 (top)
DARPA SyNAPSE PROJECT WITH HRL LABORATORIES
All Credits Go to Prof. Wei Lu's Outstanding Research Group
Successive writing
Successive erase processes
Voltage (V)
I (μA)
•Incremental conductance change
•Conductance ∝ total charge through the device
•Highest process temperature < 260°C
Pinaki Mazumder
U of Michigan – NDR Group

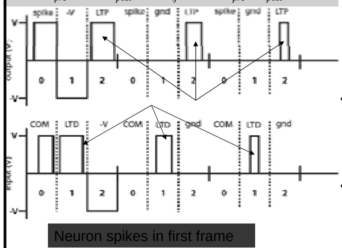

Memristor: A New Paradigm Circuit Design
Programming pulses with different pulse widths
programming pulse (V)
100 μs
Conductance change after each pulse
Conductance change (%)
Conductance controlled by the pulse width, and can be changed incrementally.
1. Digitally Controlled
2. Constant Amplitude
3. Temporal Correlation

Neuron Spiking Signals and STDP Control

Hebbian-Type STDP Learning Model

Neurons that "FIRE" together. also "WIRE" together. – D. Hebb

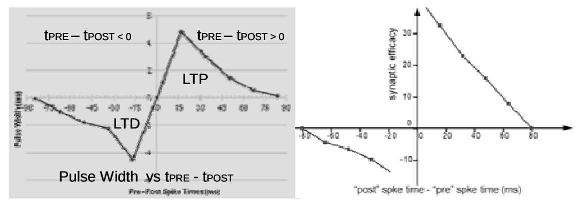
$$\frac{d}{dt} w_{ij}^{LTP} = \gamma^{LTP}.d_a.\exp\left[-\frac{t-t_{pre}}{\tau_a}\right]\times d_b.\exp\left[-\frac{t-t_{post}}{\tau_b}\right]$$
$$\times u(t-t_{pre}).u(t-t_{post}) \Rightarrow w_{ij}^{LTP}\uparrow \text{ if } |t_{pre}-t_{post}|\downarrow$$



- Time Division Multiplexing
  - Events occur at proper timeslots
  - Long Term Potentiation can only occur in the 2nd timeslot
  - Long Term Depression can only occur in the 1st timeslot
  - Inputs are considered only in the 0th timeslot
- Each pulse of amplitude V is not enough to make a significant change to memristance
- When there's a net difference with amplitude 2V, memristance changes

SPDT with Memristor

Pulse Width vs. Pre and Post Neuron Spike Times



Neuron Pulse Width Curves (across a synapse)

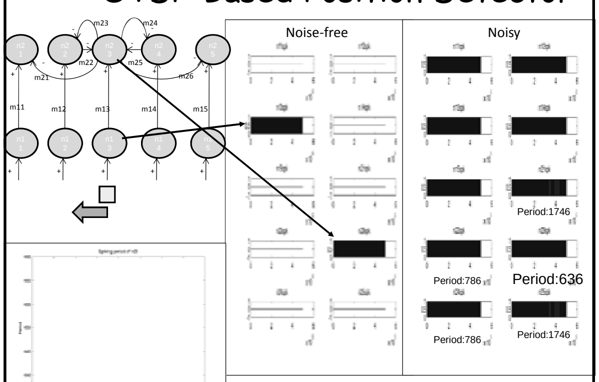
STDP obtained using memristor synapse

For LTP case: The Post neuron is at –V while the Pre neuron at +V

For LTD case: The Pre neuron is at –V while the Post neuron at +V

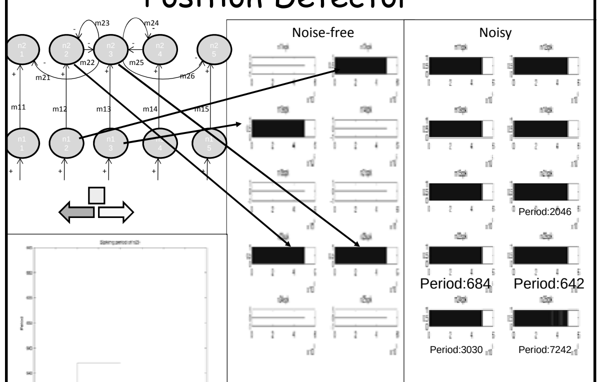
LTP case is taken as positive while the LTD case negative

STDP-Based Position Detector



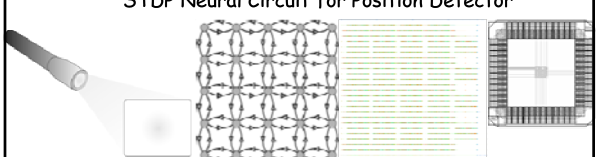
VERILOG SIMULATION

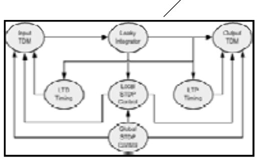
Position Detector



VERILOG SIMULATION

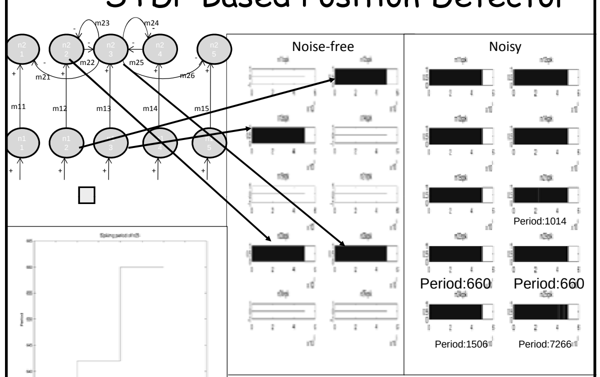
STDP Neural Circuit for Position Detector



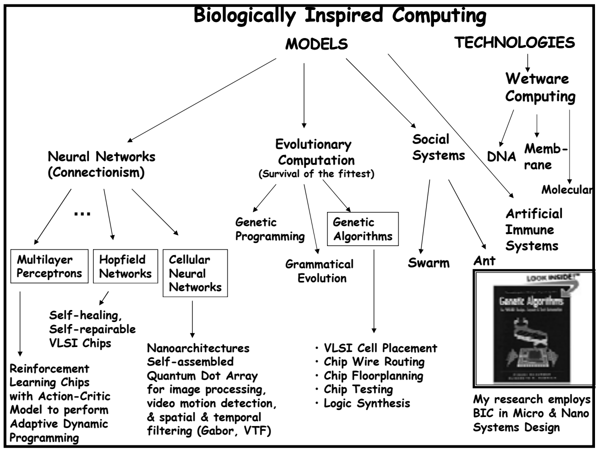


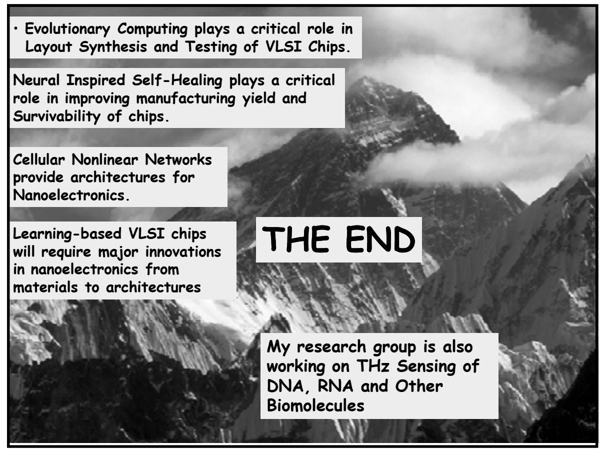
Bases	Memristor Design	CMOS Design
Synaptic area	< (0.5µm x 0.5µm)	17µm x 16µm
Synaptic Density	➢4 devices/µm² x1000	0.0037 devices/µm²
Neuron area	20µm x 10µm	8µm x 12µm
Neuron Density	0.005 devices/µm² x2	0.0104 devices/µm²
Volatility	Nonvolatile	Volatile

STDP Based Position Detector



VERILOG SIMULATION


Biologically Inspired Computing
MODELS
TECHNOLOGIES
Wetware Computing
Neural Networks (Connectionism)
Evolutionary Computation
(Survival of the fittest)
Social Systems
DNA
Memb-rane
Molecular
...
Genetic Programming
Genetic Algorithms
Grammatical Evolution
Swarm
Ant
Artificial Immune Systems
Multilayer Perceptrons
Hopfield Networks
Cellular Neural Networks
Self-healing, Self-repairable VLSI Chips
Reinforcement Learning Chips with Action-Critic Model to perform Adaptive Dynamic Programming
Nanoarchitectures Self-assembled Quantum Dot Array for image processing, video motion detection, & spatial & temporal filtering (Gabor, VTF)
• VLSI Cell Placement
• Chip Wire Routing
• Chip Floorplanning
• Chip Testing
• Logic Synthesis
My research employs BIC in Micro & Nano Systems Design


• Evolutionary Computing plays a critical role in Layout Synthesis and Testing of VLSI Chips.
Neural Inspired Self-Healing plays a critical role in improving manufacturing yield and Survivability of chips.
Cellular Nonlinear Networks provide architectures for Nanoelectronics.
Learning-based VLSI chips will require major innovations in nanoelectronics from materials to architectures
THE END
My research group is also working on THz Sensing of DNA, RNA and Other Biomolecules