Simulated performance of multi-junction parallel array SIS mixers for ultra broadband submillimeter-wave applications

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1. INTRODUCTION

Heterodyne receivers using Superconductor-Insulator-Superconductor (SIS) tunnel junction mixers are the most sensitive at millimeter and submillimeter wavelengths [1]. They are widely employed at ground-based radiotelescopes worldwide, and increasingly in air-borne and space-borne receivers, notably in projects now under development (SOFIA, FIRST, ISS). Today, an important part of the research in this field aims at developing receivers combining ultra wide bandwidths (around 30% relative or more) with ultra low-noise capabilities (a few times the quantum limit), with no mechanical tuning. This goal has been an incentive to explore either new tunnel barrier materials or new types of circuits.

Most mixers use end-loaded single-junction [2,3] or twin-parallel junction [4] designs, where an inductive circuit tunes out the capacitance of the tunnel barrier for the right frequency. In such circuits, the SIS junction's quality factor $Q=\omega RC$ —where R and C are respectively the junction normal resistance and capacitance—sets the maximum achievable relative bandwidth over which the SIS junction can be tuned and impedance-matched to a given source impedance [5]. This matching/tuning bandwidth limitation inevitably translates into conversion gain and mixer noise temperature bandwidth upper limits.

In practice, tuning circuits are integrated with the SIS junctions in thin film technology. They often consist of strongly coupled microstrip structures using either superconductor or normal metal films depending on frequency [6]. A classical circuit with one junction is illustrated in Fig. 1.

Recently, a new kind of SIS mixer based on a distributed array of N (N>2) junctions parallel-connected by microstrip lines was proposed by the Nobeyama Radio Observatory (NRO) group [7] to free the RF coupling bandwidth—and hence the mixer bandwidth—from the junction's RC product. It can also be viewed as the discrete version of the distributed non-linear quasiparticle SIS mixer proposed by Tong et al [8], also offering high sensitivity over wide bandwidths. The very encouraging experimental results reported by the NRO group [9,10] suggest that this type of circuits might be ideal

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to provide tunerless mixers with quantum-limited sensitivities and arbitrarily large bandwidths.

These results have triggered our interest in these circuits as potential solutions for wideband tunerless DSB mixers, such as those needed for FIRST/HIFI. We also believed some optimization could still be done in order to improve the response of the arrays over a particular bandwidth.

2. PECULARITIES OF SIS PARALLEL ARRAY MIXERS

The SIS parallel array proposed by the NRO group [7, 9, 10] consists of a microstripline periodically loaded with identical SIS junctions or, put differently, of a number of cells composed each of a junction and a section of microstrip which will resonate at some frequency. In its principle, such a distributed array strongly resembles the long distributed SIS junction mixer investigated by Tong et al [8,11] which yielded excellent measured heterodyne performance (conversion loss above -3dB and DSB mixer noise temperature around 20 K from 400 GHz to 500 GHz). They have over their cousin one advantage, though, in that they do not require electron beam lithography to fabricate the long junction, and therefore are a much more accessible technology.

In their simulations, Shi et al have changed the length of microstrip line between two adjacent junctions, and the number of junctions. They could show that a parallel array allows—unlike single-junction tuning circuits—mixer bandwidths much larger than ~$1/\omega RC$ and that, the larger the number of junctions, the better the mixer and the wider the bandwidth [7]. In their experiments [8], they could clearly confirm the improvement on noise and bandwidth gained by going from a five- to a ten-junction array. They measured T_{rec} (DSB) around 200 K and at some frequencies as low as 100 K from 320 to 530 GHz, using a 10-junction array with j_c=3.5 kA/cm^2. According to these authors, the bandwidth of arrays with large numbers of junctions (N>5) should be independent on the value of Q, and the length of microstrip between two junctions should not be too critical a tuning factor.

One big advantage of parallel arrays is to alleviate the need for high current density junctions—that one usually confronts with single-junction mixers in an attempt to reduce RC—which not only complicates the SIS device fabrication, reduces the yield, but also degrades the I-V quality. At submillimeter wavelengths one often shoots for 10-20 kA/cm^2 SIS tunnel barriers. At lower current densities, with single-junction tuning, the junction's impedance transformed by the microstrip, $Z_t = R_n/(1+Q^2)$, would become exceedingly small and hard to match to the source. On the other hand we know that at high current densities SIS mixers are doubly penalized: first, their conversion efficiency drops due to the smoother I-V bend and larger subgap leakage current; second, the excess shot noise caused by multiple-Andreev reflections increases, and can up to double the mixer noise [12]. In comparison, parallel arrays then only need a few kA/cm^2. Indeed, if j_{c0} was the current density required for a single-junction tuning circuit mixer, one could use arrays with a current density of only $j_{cN} \approx j_{c0}/N$.

There is a limit to the number of junctions that can be packed in a parallel array mixer, however, since it will be a technological challenge to produce high-quality wafers with *N* identical junctions on every chip when *N* is too high.

Both in simulations and experiments, Shi et al. have noticed ripples across the band, both on the DSB mixer noise (fluctuations of several 100 K) and on the gain (up to 5 dB). We have found similar noise and gain curves (Fig. 2) when we simulated the same arrays with *N*=5 and *N*=10 that were described in [7, 9]. Actually, our mixer noise and gain simulations of parallel arrays—although using a different algorithm—have qualitatively confirmed all features of the mixer performances reported by Shi et al. These authors hinted at a few avenues which could be explored to minimize these ripples, one of them being to play with the array parameters at our disposal: junctions size, spacings between junctions, width of microstrips.

Grossly, a parallel array mixer with *N* SIS junctions functions as a non-linear filter with *N* poles. To take full advantage of this property—and to minimize the ripples—we have made the spacings between two adjacent junctions non-uniform along the array.

3. DESIGN OPTIMIZATION

Obviously, many non-uniform array configurations would be solutions to the problem and would be hard to guess, so we needed a software to efficiently optimize the electrical lengths and characteristic impedances of the striplines connecting the junctions. We did that using HP Libra's optimizer. We fixed the technological parameters (e.g., microstrip dielectric layer, junction's capacitance and normal resistance) and set as free parameters the spacings (electrical lengths) between junctions and the microstrip width (impedance) to run the circuit design optimization. The criteria of convergence were to reach a certain coupling bandwidth and to stay below a certain level of ripple. With similar initial and limit conditions fed into the optimizer, several different array configurations came out.

In previous works, the source impedance was simply assumed to be the characteristic impedance of the microstrip line leading to the array. This is not so in the case of a practical mixer, and the whole embedding impedance, including waveguide cutoff and RF coupling response must be considered. The source impedance assumed for our circuit optimization was derived from independent 3D EM simulations of our tunerless waveguide mixer mount, well suited to broadband applications in the 480 GHz-650 GHz range and available for heterodyne tests [13]. This mixer mount provides the input of the integrated circuits with a nearly constant and real impedance of ~70 Ω over the whole bandwidth, as shown in Fig. 3.

Then, we took these sets of optimized electrical lengths and characteristic impedances of the microstriplines to a Mathcad program, to translate these into physical dimensions. The software computes the *S* parameters of any superconductive 1-D microstrip circuit [6], and takes into account the fringing field via Wheeler's formulas.

The Mattis-Bardeen formalism which describes the RF losses in the superconductor in the vicinity of the gap frequency was not used here. Table 1 provides the geometries of three parallel arrays A, B and C, optimized for slightly different frequencies; as an example, the mask of one is shown in Fig.4. Their expected S_{11} response is shown in Fig5. All have N=5 junctions. We chose this number as a reasonable compromise between fabrication complexity and yield constraints, and parallel array efficiency. In the calculations, we assumed the use of Nb/SiO/Nb microstriplines and of Nb/AlOx/Nb junctions characterized by a current density j_c=10 kA/cm^2 and a specific capacitance C_J= 80 fF/μm^2 (the empirical law $C_J(\mathrm{fF}/\mu\mathrm{m}^2) = 40 + 4 \cdot j_c \ (\mathrm{kA}/\mathrm{cm}^2)$ [1] was used).

Before simulating—or measuring—the heterodyne performance of these array mixers, we needed to apply the same optimization treatment to the design of more conventional single-junction and twin-parallel junction mixers, to make meaningful comparisons. In the single-junction design, the SIS junction impedance is matched to the desired source impedance by one short inductive section of microstrip followed by two cascading 'quarter-wave' sections. All the impedances and electrical lengths of this 'maximally flat' Tchebychev transformer were optimized for our bandwidth using HP Libra, prior to being converted into actual superconductive microstrips dimensions.

A non-periodically SIS loaded transmission line is a strongly non-linear device, however, and our circuit optimization has entirely skipped that fact, oversimplifying the true nature of SIS junctions. On one hand we have neglected the non-linear Josephson tunneling currents. On the other hand we have traded the non-linear, bias- and LO-dependent quasiparticle conductance for the plain normal conductance. Therefore, the array was optimized for energy transfer only, on the basis of its similarity with a passive N-pole filter, and not as a mixing device. But our noise and gain simulations based on quantum theory of mixing will later tell us whether optimizing the junction array this way also optimizes its mixing properties. Let us add that we have used HP Libra not only to optimize the circuits for a given R and C, but also to select these two parameters after a statistical analysis in the case of single-junction circuits. The typical dispersion range on fabrication parameters was plugged in, and the current density and junction area were chosen, not on the basis of the *best results* but instead of the *best yield* to expect for any given run.

Assumed fabrication parameters:	Cell number (N=5)	Optimized cell geometry : L(μm) x w(μm)		
		Circuit 'A'	Circuit 'B'	Circuit 'C'
Junction current density J_c: 10 kA/cm²	1	49.5 / 4.5	44 / 5	58 / 4
Junction capacitance C_J: 80 fF (1μm² area)	2	6 / 5	7 / 7	14 / 5
Penetration depth λ (Nb): 85nm	3	12 / 5	11 / 7	12 / 5
Dielectric constant ε_r(SiO): 5.7	4	42 / 5	44 / 7	58 / 5
Dielectric thickness h:200 nm	5	20 / 5	18 / 7	32 / 5

Table 1. Technological parameters assumed for the design and optimized geometries (i.e. length and width of the microstrip cells) of 5-junction arrays A, B and C.

4. ARRAY MIXER PERFORMANCE ANALYSIS

We have merged the theory of superconductive microstrip lines with the quantum mixing formalism developed by Tucker [1], in the three-port approximation, within a specially developped software allowing us to simulate the heterodyne performances of the SIS mixer circuits, regardless of the number of junctions. The algorithm for the mixer noise temperature and conversion gain calculation is based on the work by Tong et al [11], which was applied to the theory of mixing in superconducting quasiparticle non-linear transmission lines. Figure 6 shows the equivalent circuit corresponding to the calculation. The source admittance Y_s directly relates to the embedding impedance $Z_{emb}(\omega)$ seen by the array at its feeding point. The array is terminated by some admittance Y_t—in our case Y_t=0 for an open circuit. Each cell i corresponds to a small section of microstrip line loaded with the i^{th} junction of admittance $Y_{c,i}+jC_i\omega$, and can be fully modelled by its ABCD matrix, defined in the small signal analysis by:

$$\begin{pmatrix} v_i \\ i_i \end{pmatrix} = \begin{pmatrix} A_i & B_i \\ C_i & D_i \end{pmatrix} \begin{pmatrix} v_{i+1} \\ i_{i+1} \end{pmatrix}$$

In the three-port approximation model, small currents i_n and voltages v_n are 3x1 column vectors projected upon the upper and lower sidebands ($\omega_{+1,-1}$) and the intermediate frequency (ω_0); and every admittance is therefore represented by a 3 x 3 conversion matrix: these matrices are diagonal for linear admittances (Y_s and Y_t), and non-diagonal for all the non-linear quasiparticle admittances $Y_{c,i}$ responsible for frequency conversion. Since the array's dimensions are comparable to the wavelength in the microstrip, all conversion matrices $Y_{c,i}$ must include the LO phase variation at the SIS junction location. The ABCD matrix defining the parallel array circuit is defined by:

$$\begin{pmatrix} v_o \\ i_o \end{pmatrix} = \prod_{n=1}^{N} \begin{pmatrix} A_n & B_n \\ C_n & D_n \end{pmatrix} \begin{pmatrix} v_n \\ i_n \end{pmatrix} = \begin{pmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{C} & \mathbf{D} \end{pmatrix} \begin{pmatrix} v_n \\ i_n \end{pmatrix}$$

Since $i_n=Y_t.v_n$, we can derive the complete conversion admittance matrix of the array:

$$Y_{array} = \frac{i_0}{v_0} = \frac{\left(\mathbf{C} + \mathbf{D} \cdot Y_t\right)}{\left(\mathbf{A} + \mathbf{B} \cdot Y_t\right)}$$

If we define the augmented admittance Y^{aug} as the sum of the source admittance $Y_s(\omega)$ and Y_{array}, we can compute the conversion efficiency of any parallel array mixer:

$$G_{SSB} = 4 \cdot \mathrm{Re}\left(Y_s(\omega_1)\right) \cdot \mathrm{Re}\left(Y_s(\omega_0)\right) \cdot \left|Z_{01}^{aug}\right|^2$$

where $Z^{aug} = (Y^{aug})^{-1}$.

A similar equivalent circuit as in Fig. 6 was used to calculate the single sideband mixer noise of the junction array. We added to each cell m a current source (connected in parallel) modelling the shot noise produced by the m^{th} junction (Again, all small currents and voltages are 3x1 column vectors transformed by the same 3x3 admittance matrices as above). We can legitimately assume that these shot noise sources from different junctions are not correlated, and therefore the total noise produced by the array

at the IF port is merely the sum of the shot noise contributions from all junctions. Since the averaged noise voltage produced at the IF port by any m^{th} junction is

$$\left\langle \left| V_n^m \right|^2 \right\rangle = \sum_{k=-1}^{1} \sum_{k'=-1}^{1} Z_{0k}^m \cdot \left(Z_{0k'}^m \right)^* \cdot H_{kk'}^m,$$

the SSB mixer noise temperature of the whole array can be written:

$$T_{SSB} = \frac{\mathrm{Re}\left(Y_s(\omega_0)\right)}{k_B \cdot G_{SSB}} \cdot \sum_{m=1}^{N} \left\langle \left| V_n^m \right|^2 \right\rangle$$

The algorithm was programmed in C++ and run on a Pentium PC under Linux environment. The software called several input files containing the circuits parameters and geometries, and the complex impedance for all frequencies calculated with CST-Mafia. For each run, the LO pump and the bias voltage could be swept across a chosen range; the output files contained both the noise-optimized data but also the complete set of non-optimized values. The LO voltages across the junctions—calculated using Withington et al's voltage update method [14]—were also stored separately as output data.

5. RESULTS

Using the software, we could compute the mixer gain and noise to expect from all the circuits that had been already optimized with HP Libra, and for any frequency, bias voltage and LO incident power. First, we tested our code using for inputs the technological parameters and the geometry of the circuits analyzed by Shi et al [7], for the same numbers of junctions and equivalent inter-junction spacings (i.e., same $\omega L/R_n$), and having set the source impedance to the same value (a typical microstrip source impedance for the center frequency). Figure 2 provides a sample of these simulations. Our results were strikingly similar to those of NRO, in spite of the different algorithm used; we found the same conversion gain and noise, and in particular, large ripples in those curves at the exact same frequencies where they were observed by the NRO group. Yet, we noticed that our ripples would tend to be rounder and smoother than those, peaking rather sharply—especially in the noise curves, found by Shi et al.

We could confirm the major influence of the spacing lengths on the frequency occurrence of the ripples and the band roll-off. We also investigated junction arrays with spacings across the array non-uniform, and arbitrarily varied. They showed a mixing performance degradation at certain frequencies and an improvement at some other, in an unpredictable manner. Optimizing the non-uniform arrays was the next step to set the roll-off at the right frequency and to contain the noise ripple within acceptable limits.

In order to compare them to the S_{11} calculations, all our mixer noise and gain calculations now assumed the use of one-square-micron junctions with a current density of about 10 kA/cm^2 (R=20 Ω, C=80 fF), regardless of the number of junctions. The

technology parameters (films thicknesses, dielectric constant, fringing field factor) were kept identical.

Fig.7 shows the heterodyne performance to expect from the optimized classical approach: a junction end-loading a three-section Tchebychev transformer, similar to the drawing in Fig.1, superimposed with that of the simplest SIS array of all: a twin-parallel junction circuit designed for the same frequency band. At every frequency, the voltage bias and LO power—the latter being shown on the same figure—were optimized for minimum double-sideband mixer noise. With no surprise, we find that the twin-parallel circuit provides substantially wider bandwidth than the single-junction with its matching transformer, and seems sufficient to achieve a relative 30% bandwidth—at least when one uses a quasioptical antenna or a waveguide mount for which the embedding impedance is almost purely real and constant.

Fig.8 shows the calculated optimum DSB mixer noise temperature, DSB conversion gain, and consumed LO power for the 5-junction array labelled 'A' (see Table 1). The design of this array was particularly aimed at the 480-640 GHz bandwidth. By far, it provides the widest bandwidth of all, clearly extending beyond the 55% relative bandwidth that can be displayed on the graph. The noise bandwidth is therefore larger than what had been projected from Mathcad/HP-Libra S_{11} calculations. On the other hand, the ripples in the noise and gain curves do not quite reproduce what was seen in Fig.5. This is only half a surprise, and it demonstrates the need for a full Tucker mixer analysis to discriminate efficiently between several parallel array circuits prior to fabrication, and obviously, to finely understand the heterodyne results in the laboratory. In particular, it is clear that the predicted array's behaviour is drastically changed when one replaces the constant source impedance usually assumed for mixer analyses by the complex—and more realistic—mixer mount impedance which changes with frequency. The conversion is much better than –8 dB over the whole band, with conversion *gain* possible at some frequencies.

The LO power required to pump optimally a given type of SIS circuit is a major criterion for practical submillimeter-wave receivers. In a single-junction circuit with a three-section transformer, the LO power reaches a maximum of about 250 nW at the center of the band, where the conversion loss and the mixer noise both undergo a local maximum (see Fig. 7); this is a plain consequence of the 'twin-peak'-shaped response of such Tchebychev transformers when stretched to their maximum available bandwidth, and it could already be seen in the S_{11} parameter. The twin-parallel junction offers a slightly broader bandwidth, as expected, a similar LO power of 300 nW with, too, local minima coinciding with the local maxima of the mixer noise and conversion loss.

We see in Fig. 8a that for an optimized 5-junction array, the LO power is not five times higher than that needed for a single junction of same current density, as one could have expected; the LO is almost constant across the band, near 300 nW, about equal to the amount of LO needed for a single-junction mixer at the center of the band. This point is to relate to an important issue in arrays: the uniformity with which the LO power is being absorbed by the junctions. The LO pumping level is a critical factor for the SIS mixer performance, thus it is important to know whether some junctions of the

array are insufficiently or over-pumped; playing a fully passive tuning role; simply contributing noise to the mixer. Because of the phase delays between two adjacent junctions, we expect a non-uniform array to exhibit a complex, non-uniform LO power distribution, changing with frequency. This is precisely what the five curves of Fig. 9 show us in the case of 'A'. They represent, plotted versus frequency, the calculated distribution of the LO voltage (normalized to hf/e) across each of the 5 junctions of an array. The interweaving of the curves as frequency changes seems to corroborate the importance of the LO phase in the array, causing unequal pumping and possibly unequal mixer noise contribution.

From our results, it appears that the arrays were probably correctly optimized for energy transfer (the mixer bandwidth is creectly centered, and larger than expected from the S_{11}), but not necessarily for heterodyne mixing (the conversion loss is a little high; there is more ripple than expected in the conversion gain and in the noise). We conclude, therefore, that a true optimization for sensitivity-bandwidth of the array design requires one to apply a complete mixer analysis to those circuits.

Yet, the non uniform junction distribution resulting from our considering the arrays as bandpass filters and their optimization, looks like a positive step. The ripples are less than in the periodically loaded arrays and the theoretically achievable mixer noise bandwidth is wider. We can safely conclude that with minor improvements the N=5 circuits will provide mixer bandwidths much wider than $1/RC$ with a DSB mixer noise less than three times the quantum limit.

6. PERSPECTIVES

Obviously, more than one parameter can be played with to curtail the broadband response of a parallel array SIS mixer. We have varied the intervals between junctions only, but we could have made the junctions area (hence their capacitance) non uniform as well. We found that the distribution of the LO voltage in the array is non-uniform due to the LO phase, and this needs further investigation. Possibly, certain array configurations, although optimum from the standpoint of the S_{11} response, provide lousy mixer performances because some of the junctions are under- or over-pumped, and merely add noise to the array. Should this turn out to be a problem, we suggest the arrays be optimized not via their spacings between junctions, but via the junctions areas, therefore allowing a uniform—and appropriately defined–electrical length for all microstrip cells.

The Tucker formalism of quantum mixing is most often used in its simplest three-port approximation, generally justified by the large capacitance of SIS junctions, shorting the LO harmonic frequencies at the expense of quasiparticle tunneling. The strongly non-linear response of the parallel array mixer, however, compells us to look into at least the first LO harmonic in the mixer analysis. In another work [15], we report on the analysis of noise and gain in a parallel 3-junction array using both the three-port and the five-port approximations. Comparing the simulation results, we found a

substantial difference in the gain bandwidth, which one could possibly attribute to the importance of the first LO harmonic. We will soon apply this 5-port mixer analysis to arrays with any number of junctions.

Another area of investigation deals with the incidence on mixing performance of the Josephson effet in these devices. One should expect such parallel arrays—analog to a parallel-connected SQUIDs—to exhibit dynamical regimes of the Josephson tunneling current, including fluxon motion, as one applies an external magnetic field. From the standpoint of the electrical model, distributed arrays of small junctions are identical to long Josephson junctions. Hence one should expect their *I-V* characteristics to display the equivalent of well-known features like Zero-field steps and Fiske steps. It remains to be seen, from simulations and experiments, whether these peculiar AC current regimes will be sources of noise or instabilities for the SIS mixer or not. This problem pertains to how one should quench the LO-driven Shapiro steps with an external magnetic field, as currently done with SIS receivers.

7. CONCLUSION

We have used a combination of softwares to optimize the design of parallel-array SIS mixers with N=1, 2 and 5 junctions for the same band 480-640 GHz. The electrical lengths separating two adjacent junctions were made non uniform in order to curtail the bandpass filter-type response of those circuits over a desired band (more than 30 % relative bandwidth around 560 GHz) and in particular to minimize the ripples reported in the case of periodically loaded arrays. We have applied a three-port Tucker mixer analysis to these optimized designs, to investigate their expected mixer noise temperature and conversion gain versus frequency, bias voltage and LO power. We used the embedding impedance of our waveguide mount—computed by a 3D EM software—as the source impedance. We confirm the strong qualitative difference, in terms of mixer noise, conversion gain and LO power needed versus frequency, between the single-junction, twin-parallel junction mixers and the 5-junction array mixers. The level of ripples in the noise is slightly higher than anticipated from the optimization phase. Also, not all three optimized parallel-junction circuits behave identically. Although it seems easier to achieve a flat mixer noise over a 30 % relative bandwidth using the twin-junction mixer, parallel array mixers with N=5 can produce much larger bandwidths at a comparable sensitivity. The required amount of LO power is nearly constant over the whole band and does not exceed that needed by a single-junction mixer at the band center. As anticipated, the distribution of LO voltage within the 5-junction array is not uniform: certain junctions do most of the mixing while others only act as tuning elements; however, in our design, the junctions swap roles as LO frequency changes. This can explain the increase of LO power consumption being non-linear with N as reported by Shi et al.

It may be too early to conclude that multi-junction array mixers are the most solid answer to the need for tunerless broadband mixers. But it is safe to say that they

represent a satisfying alternative to single-junction and twin-parallel junction mixers. Aiming at the specifications we used for the simulations (j_c=10-15 kA/cm^2; 1-μm^2 Nb/AlOx/Nb junctions), we have begun the fabrication of batches of circuits at our facility and will report on the heterodyne measuremens later. In this study, we have chosen N=5 as a reasonable trade-off between performance and complexity, but more—or less—junctions could have been used. Of course, the unique broadband properties of optimized parallel SIS arrays apply not only to heterodyne mixing but also to direct detection.

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FIGURES

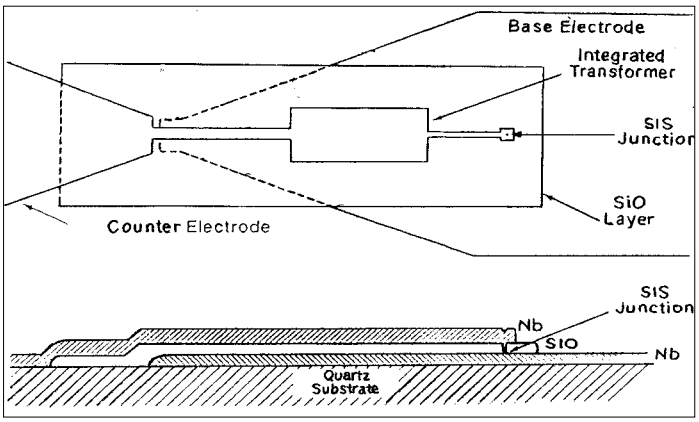


Fig.1. (a) top and (b) cross-sectional view of a typical single SIS junction microstrip tuning circuit, using a Tchebychev transformer.

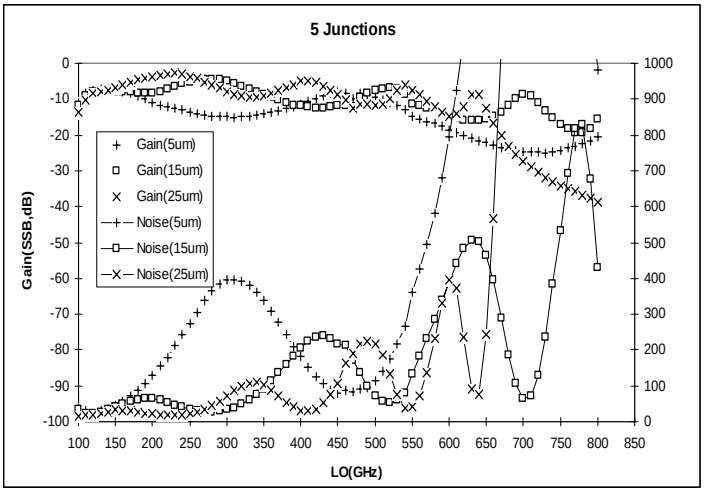


Fig. 2. Simulation of the gain and noise of a periodically loaded 5-junction array mixer, with *d*=15, 20 and 25 μm spacings. The source admittance was set to 8 Ω and assumed frequency independant.

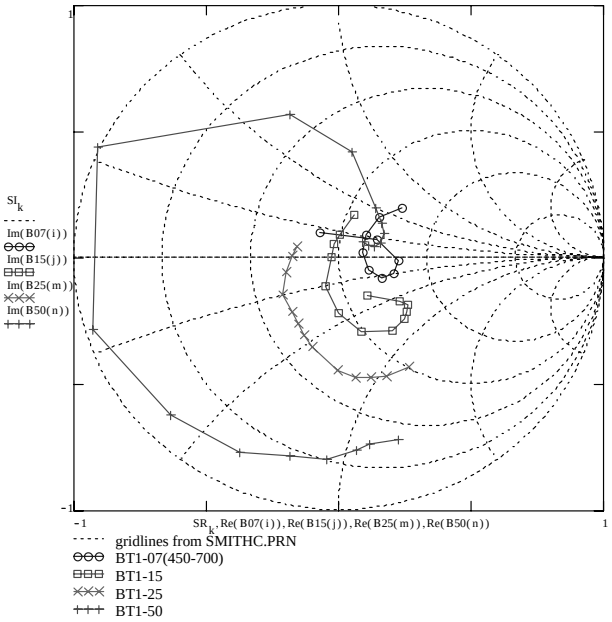


Figure3. Simulated source impedance of the tunerless waveguide mixer mount for different backshort positions. At d=0.07λg, this mixer mount provides the input of the integrated circuits with a nearly constant and real impedance of ~70 Ω over the whole bandwidth.

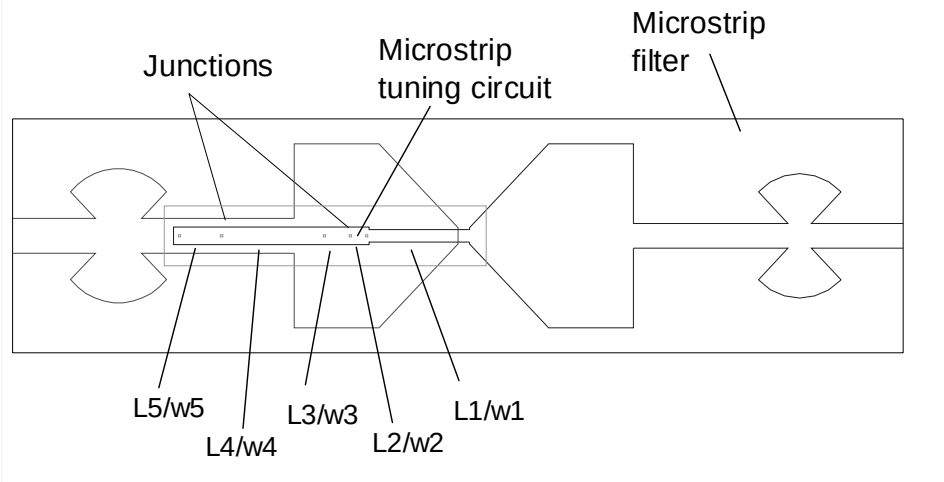


Figure 4. Fabrication mask of a 5-juction array circuit 'A' for 480 - 640 GHz.

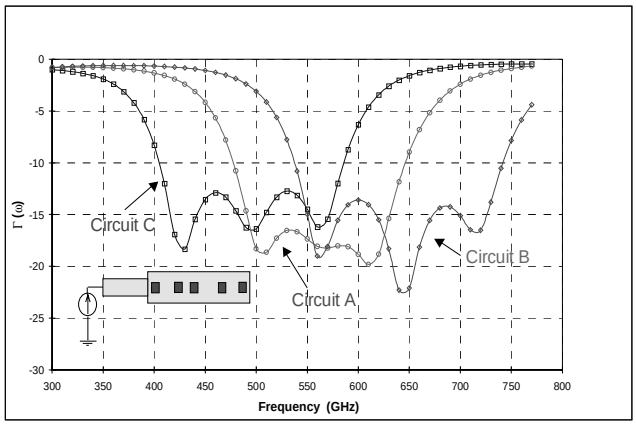


Figure 5. Simulated reflection of three non-uniform 5-junction array circuits designed for a 160 GHz bandwidth at 3 different central frequencies: 520GHz (C), 560GHz (A) and 600GHz (B).

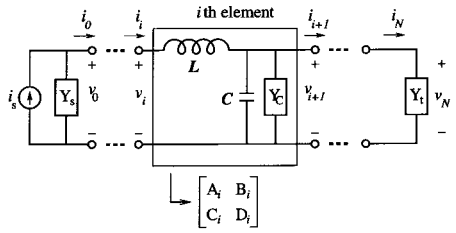


Figure 6. Equivalent circuit of noise analysis in the parallel junction array. The quasiparticle non-linear admittance is represented by its 3 x 3 conversion matrix, and the shot noise produced by the junctions are represented by current sources connected in parallel at the output of each cell.

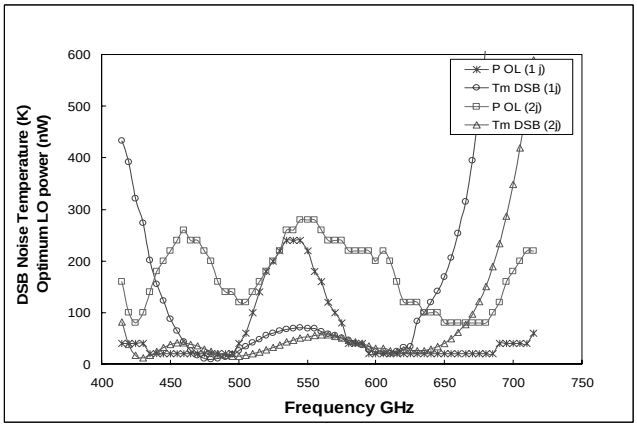
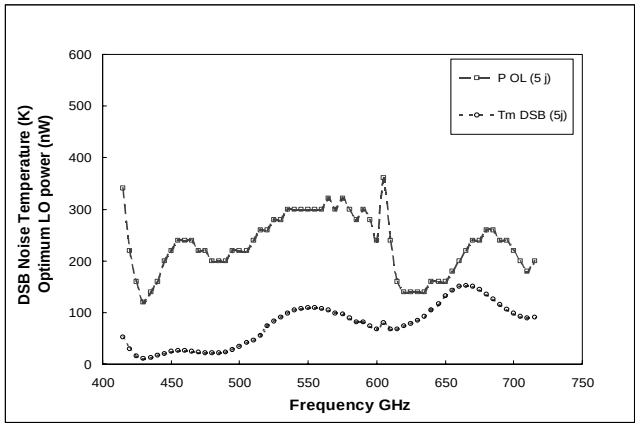


Figure 7. Optimal LO power and double-sideband mixer noise temperature to expect for a single and twin-junction circuits.



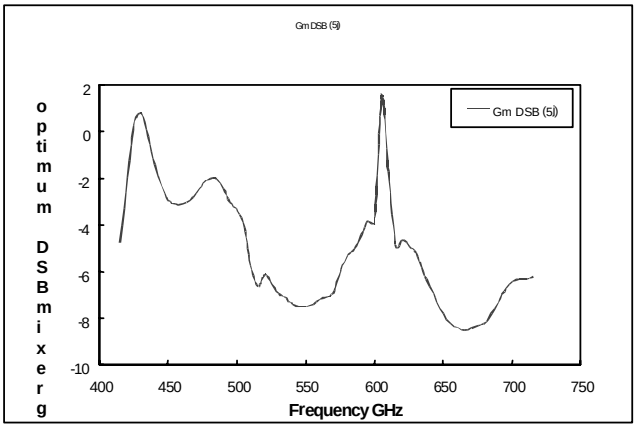


Figure 8. (a) Optimum mixer noise and LO power and (b) optimum conversion gain, calculated for the 5-junction array 'A'.

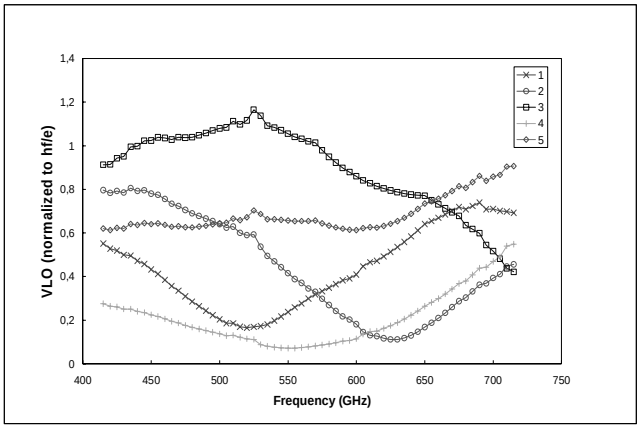


Figure 9. LO voltage distribution within the 5-junction array 'A', versus frequency. The junctions are numbered from 1 (at the entrance) to *N*=5 (at the open end of the array).