# Planar Varactor and Mixer Diodes Fabricated Using InP-Based Materials

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## Abstract

This paper reports on a planar integrated technology which, unlike previous approaches, utilizes InP-based materials and airbridge technology to reduce parasitics by avoiding the use of a bridge-supporting dielectric. Vertical-heterojunction varactors (VHV) and mixers were grown by the in-house Metalorganic-Chemical Vapor Deposition (MOCVD) system on S.I. InP substrates. A novel process is presented which allows fabrication of planar diodes with very short airbridges, a low risk of anode/ohmic undercutting, and without need for replanarization. Methods have been investigated here for replacing the InP substrates with glass and quartz.

Systematic studies on VHV's revealed the effects of varying the barrier thickness ($d_1$), epilayer thickness ($d_2$) and barrier indium concentration (x). Control of $C_{min}$, $C_{max}/C_{min}$, reverse saturation current density ($J_s$), forward and reverse leakage, and Schottky barrier height ($\varphi_{be}$) was demonstrated via choice of device layer structure and alloy composition. The technology allowed demonstration of varactors with leakage currents which could be substantially reduced by design and material choice. Microwave characterization permitted the study of cutoff frequencies ($f_c$) as functions of anode diameter for several values of $d_1$, $d_2$, and x. One μm VHV's showed $f_c$'s in the THz range. First results on the 1 μm InGaAs/InP mixers showed much lower forward turn-on voltages than for similarly-sized GaAs diodes. This suggests the possibility of diode mixing using smaller local oscillator power levels than GaAs diodes.

## II. Introduction

Traditionally, whisker anode contacting technology has been the de-facto standard for submillimeter mixers and varactor multipliers. While whisker contacting produces low parasitics, it is suitable only for discrete devices, has limited reliability, and consequently is difficult to space qualify. To address these problems, GaAs planar diodes have been proposed and demonstrated [1]. In many GaAs-based planar diode technologies [1], [2], anode openings are etched through a film of $SiO_2$ which also supports the evaporated airbridges. Usually, isolation is achieved by laterally undercutting the n+ GaAs under the airbridge. In short-airbridge designs, the isolation etch runs the risk of undercutting the anode. In [2], a solution is proposed using a trench isolation technique in which the trench is anisotropically etched before the airbridge is fabricated. However the trench in [2] also requires a planarizing step.

Planar varactor and mixer diodes have traditionally relied on GaAs and AlGaAs/GaAs material systems to achieve high performance at submillimeter and THz frequencies. In recent years,

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improvements in growth technology have made it feasible to utilize the performance advantages offered by the InP-based material systems. The high mobility and conductivity of InP-based materials (InGaAs) enables the reduction of access resistance ($R_s$). The low barrier heights ($\varphi_{be}$) of mixers using InGaAs and InP Schottky junctions are especially useful in reducing LO power requirements. The InAlAs/InGaAs heterojunction of InP-based varactors achieves an electron barrier of 0.5eV vs. 0.26-0.3eV for AlGaAs/GaAs, resulting in potentially reduced leakage relative to GaAs/AlGaAs varactors. A first demonstration of the InAlAs/InGaAs varactor principle was recently reported by the authors [3].

To gain full advantage of the InP-based system for planar diodes, the authors have developed a novel isolation technique that avoids the use of $SiO_2$ and the BHF $SiO_2$ etch, thus avoiding etching damage to the InAlAs barrier layers used in InP-based varactors. By avoiding use of the $SiO_2$ under the bridge this novel planar diode process also reduces parasitic capacitance by approximately 1fF, which is significant compared to the 3-6fF of 1μm diodes. Furthermore, this process avoids the need of undercutting the airbridge while not requiring a replanarization step.

Section III. of this paper covers layer structures of the demonstrated InP-based varactor and mixer diodes. A novel planar diode fabrication technique is discussed in section IV. Several advantages, such as reduction of parasitic capacitance and ease in dicing accrue from the replacement of the InP substrate. Therefore section V illustrates the replacement of the diodes' InP substrate with glass. Finally, sections VI and VII present measured dc and microwave performance of the planar varactors and mixers.

# III. Varactor and Mixer Layer Structures

Figure 1. illustrates the layer structures for the varactor and mixer diodes. All structures covered here were grown in-house via Metalorganic-Chemical Vapor Deposition (MOCVD) on S.I. InP substrates. The 1μm thick n+ InGaAs layer serves to provide a low sheet resistance and good ohmic contacts.

The heterojunction varactors here use an undoped InGaAs active layer (thickness $d_2$ = 400Å and 800Å) to support a variable-thickness depletion region. In all cases, the InGaAs is lattice-matched to the InP substrate. The $In_xAl_{1-x}As$ barrier layer thickness ($d_1$) is 100Å or 200Å. Decreasing x is expected to increase the electron barrier height, and decrease varactor leakage. To study the impact of x, some varactors have been fabricated with x = 0.4 (strained) and x = 0.52 (lattice-matched). Optimization of the InAlAs significantly affects performance and required a special study as reported in [4] and [5].

The mixer structure uses an 800Å i-InP active layer. The InP/InGaAs heterojunction region is

highly n-doped in an attempt to render it transparent to electron flow so that the diode performs as an InP Schottky while taking advantage of the n+ InGaAs' low sheet and ohmic resistances.

# IV. Topology and Fabrication

Diode topologies such as single-ended, wafer-probeable, antiparallel pair, back-back pair, and strip-anode diodes have been included on the same mask set. Pad sizes vary from 40x70μm to 80x150μm. Wafer-probeable diodes have a pad configuration consisting of 50μm wide ground, signal, and ground (GSG) pads having a 100μm pitch compatible with Cascade® on-wafer microwave probes. These devices allow extraction of microwave characteristics. Antiparallel diode pairs have been designed for application in subharmonic mixers, where the LO frequency is approximately 1/2 that of the RF. These devices consist of two diodes in parallel, with the anode of one connected to the cathode of the second. Back-back diodes provide a symmetric C-V curve useful for varactor tripling. Strip-anode diodes are used to experiment with $R_s$ reduction via an elongated anode. Typical anode diameters vary from 1μm to 5μm diameter. A few large diodes (48μm and 100μm) allow low-frequency C-V characterization. The same mask set is used for both varactors and mixers. This mask set is also includes alignment marks that facilitate the use of

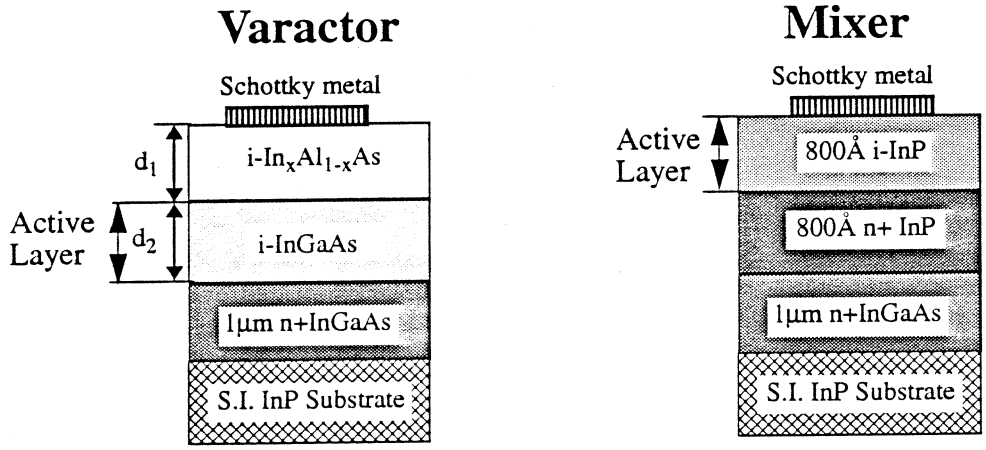


Figure 1. Layer structure of varactor and mixer diodes. The n+ InGaAs layer provides low sheet and ohmic contact resistance, while the i-InAlAs barrier layer provides an electron block for the varactors. In all cases, InGaAs is lattice-matched to InP, while the InAlAs composition is varied to explore the effects of indium content on the varactor leakage and saturation current. The mixer structure addresses the control of $\phi_{be}$ via material choice.

in-house E-beam lithography for submicron diameter anode definition. Seven mask levels are used in the following order, namely: 1. Preposition metal, 2. Mesa etch, 3. Ohmic metal, 4. Interconnect metal, 5. Pillar, 6. Trench isolation etch, and 7. Airbridge. In some cases, mask level 2. is optionally eliminated and the mesa etch step (etch to n+ InGaAs) is replaced by etching of

the ohmic region only.

Figure 2. illustrates the main features of the planar diode process described in this paper. First, the preposition level is deposited. These metal patterns provide the diode alphanumeric labels and an E-beam alignment grid. Next, a mesa etch exposes the n+ InGaAs. Optionally, the mesa pattern may be eliminated. In this case, an ohmic etch exposes the n+ InGaAs beneath the ohmic contacts exclusively. Ohmic contacts of Ge/Au/Ni/Ti/Au are defined and evaporated onto the n+ InGaAs ohmic regions, then annealed via rapid thermal anneal (RTA). Interconnect pads are then defined and evaporated. After this, anodes and airbridge pad attachments are defined via the pillar mask. A conformal hotplate bake is performed, on the pillar photoresist, to ensure good coverage of the evaporated pillar metal. Next, the pillar photoresist is exposed for a second time using the isolation mask, which exposes the region beneath the future airbridge. Pillar metal is then evaporated and followed by airbridge photoresist spun over the pillar metal. The airbridge regions are then opened in the airbridge photoresist. A corner of the sample is also flood exposed and developed to insure a good electrical contact to the pillar metal for gold plating of the airbridges. The top pillar Ti is then removed and the airbridges are Au plated on to a thickness of approximately 3μm. Next, the airbridge photoresist is removed via flood exposure and development. Pillar metal is then etched away, exposing the pillar photoresist. Subsequently, the pillar photoresist is developed for a second time to reveal the isolation patterns. Finally, an isolation etch removes all n+ InGaAs between the diode pads to achieve electrical isolation. Unlike most conventional planar diode processes this novel planar diode process requires no lateral undercutting of the airbridge since the photoresist under the airbridge has been developed away. The probability of anode undercut is further reduced via utilization of device orientation in conjunction with the crystallographic nature of the isolation etch. Diode batches produced with the above process have demonstrated yields greater than 85-

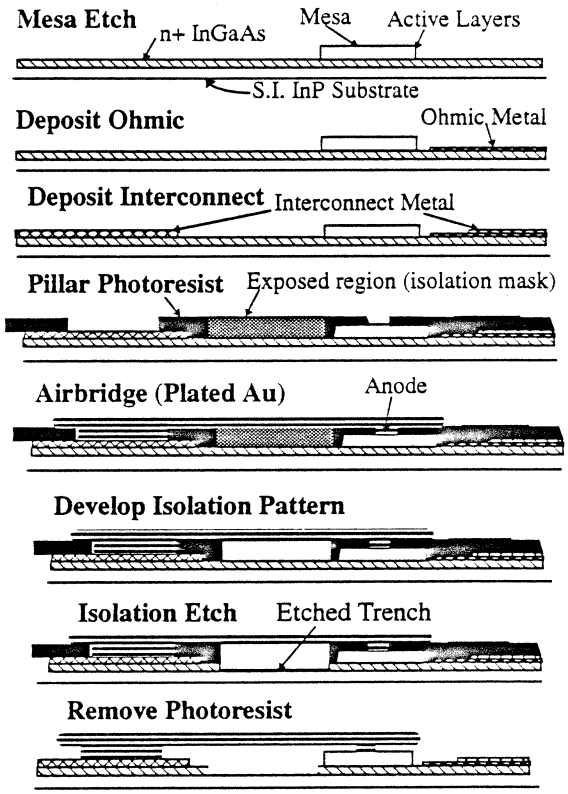


Figure 2. Side view of planar process for InP-based diodes. Active layers had thicknesses on the order of 1000Å. The n+ layer was near 1μm thick. Airbridges are 10-60μm long, 2-4μm wide, and 2-4μm thick. Note that all n+ InGaAs to be etched is uncovered before the isolation etch.

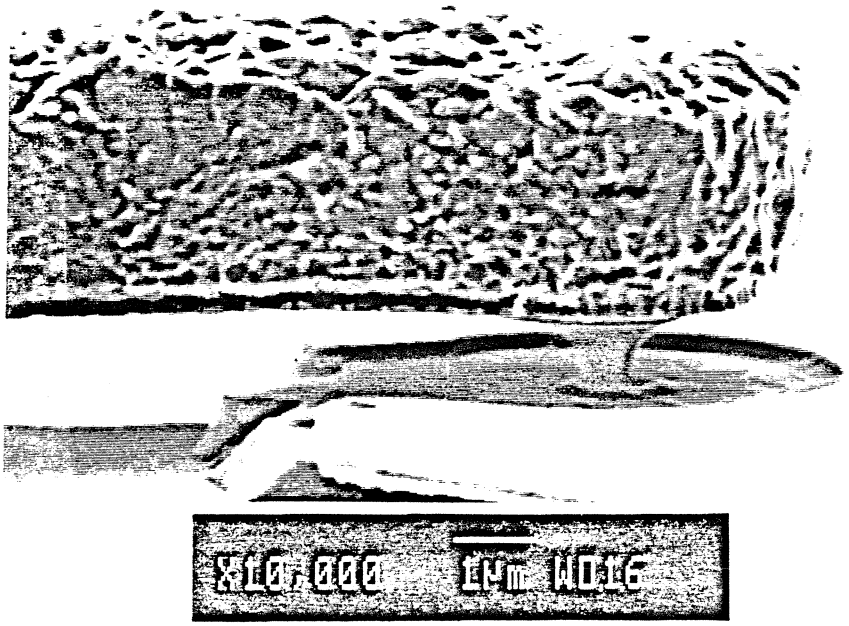

Figure 3. Side-view SEM of diode anode region. Here, the anode diameter is 0.6μm. It appears that there is potential for controlling the anode diameter via exposure, development time, and conformal bake parameters.

90% for regions ~2mm away from the edge (avoiding the photoresist edge bead). Figure 3 shows an InP-based varactor diode fabricated with the above described technology, except that it's isolation etch was performed via undercutting the airbridge. It's anode diameter is 0.6μm.

# V. Epitaxial Lift-Off and Substrate Replacement

It has been found that the mechanical properties of InP give it a tendency towards unacceptable chipping during dicing via dicing saw. Also, the InP's $\varepsilon_r \approx 13$ contributes significantly to pad-pad capacitance. A substrate replacement process using glass, has been studied, to address these problems. It has been found that the glass dices with much greater precision and very little chipping. Furthermore, the glass substrate may be easily removed via BHF or HF.

The wafer frontside is first protected with 4-6μm thick hardbaked photoresist. Next, 1-2mm thick black wax is cut to the wafer's size and oven-baked onto the wafer. The InP substrate is then removed via selective HCl etch under vigorous agitation. This leaves the InGaAs epitaxial layers and devices on the black wax. UV curable glue is then spun on a 50μm thick substrate of cover glass to yield a 2-5μm film. The glue side of the glass slide is then set on the diode side of the black wax and allowed to wet the diodes. A UV and adhesion cure follow next. Finally, the process is completed by removal of the black wax. Optionally, it should be possible to use quartz or another UV transparent substrate in place of the cover glass.

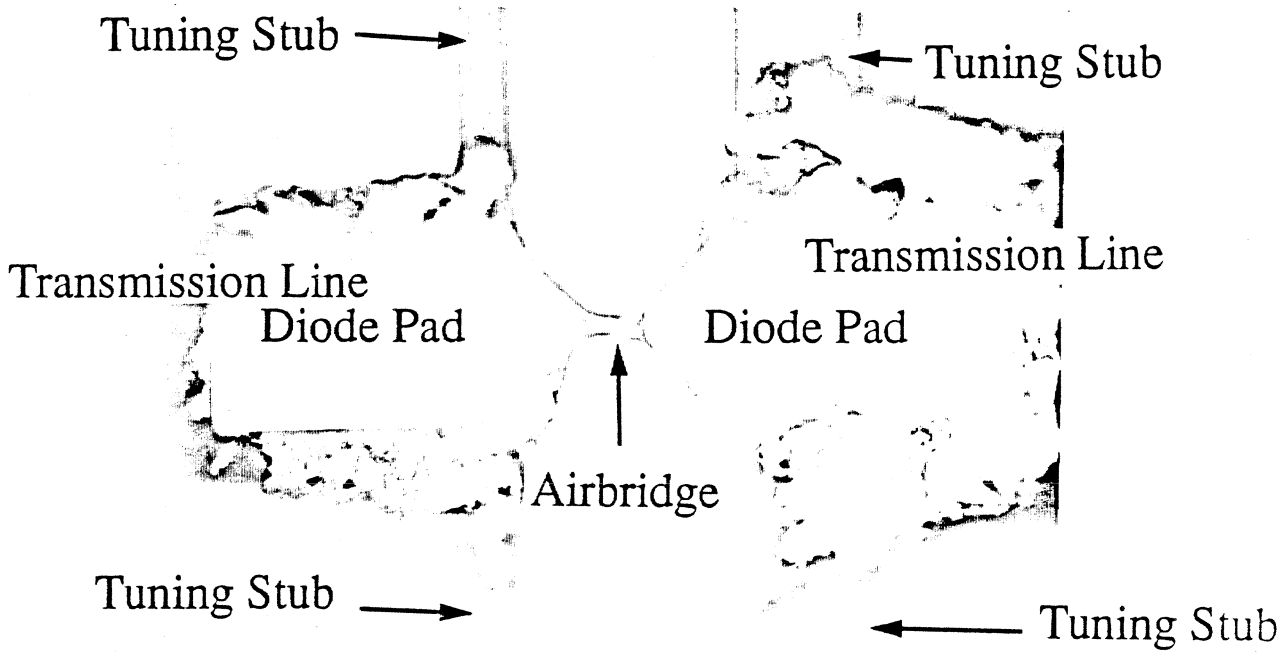


Figure 4. Photograph of varactor diode flip-chip mounted into a quartz multiplier circuit. using conductive epoxy. The active regions are protected with wax or photoresist during substrate removal.

After replacing the InP substrate, the devices may be chemically or mechanically diced and flip-chip mounted into their chip carriers for submillimeter testing. Figure 4 illustrates a diode that has been flip chip mounted using conductive epoxy. The diode's substrate has been etched away while the active layers were protected with photoresist.

# VI. Varactor DC and Microwave Results

Leakage current and ohmic series resistance ($R_s$) both add losses to varactor multipliers which reduce their conversion efficiency. DC I-V characterization of varactors is useful mainly to evaluate their leakage current properties and low-frequency ohmic series resistance ($R_s$).

Varactor I-V curves were characterized at room temperature using an HP4145 parameter analyzer. Measured I-V curves (Figure 5) agree with theory in that for a given barrier thickness, increasing the barrier's Al content (decreasing x) results in reduced forward and reverse leakage currents. The varactor I-V curves also appear to imply the necessity of having the barrier thickness greater than 100Å to obtain reasonable leakage performance. It should also be noted that the reverse current is more strongly affected by $d_1$ while the forward current is more strongly affected by x.

As expected, increasing the Al content (lower x) increases the barrier height. For example, decreasing x increased the effective $\varphi_b$ from 0.48V to 0.54V and reduced $J_s$ from 7.4mA/cm$^2$ to 250μA/cm$^2$.

TLM characterization of the 1μm n+ InGaAs layer indicated sheet resistances from 4.7Ω/□ to 2.8Ω/□, ohmic contact resistances from 9.7x10$^{-3}$Ω•mm to 17x10$^{-3}$Ω•mm and specific ohmic contact resistances of 0.2x10$^{-6}$Ω•cm$^2$ to 10$^{-6}$Ω•cm$^2$.

C-V curves were characterized via two methods namely, low-frequency C-V meter at 4MHz and microwave S-parameters (1-25GHz) in conjunction with EESOF LIBRA® microwave simulation program to fit the S-parameters to the

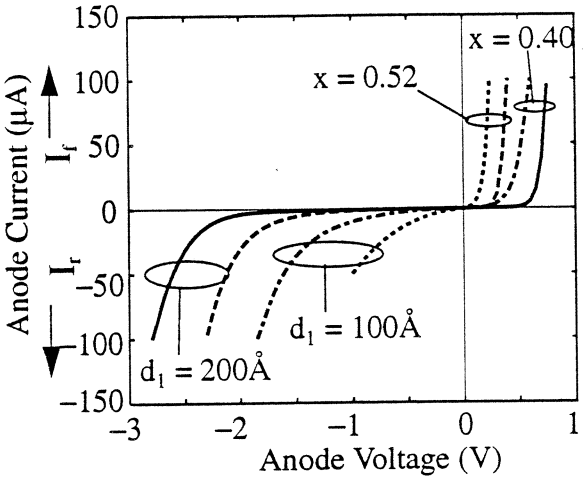


Figure 5. Impact of active layer thickness ($d_1$) and In mole fraction (x) on varactor I-V curves. Reverse current is highly sensitive to $d_1$ while forward current depends more on x. In all cases $d_2$ = 800Å and the anode was 2μm in diameter.

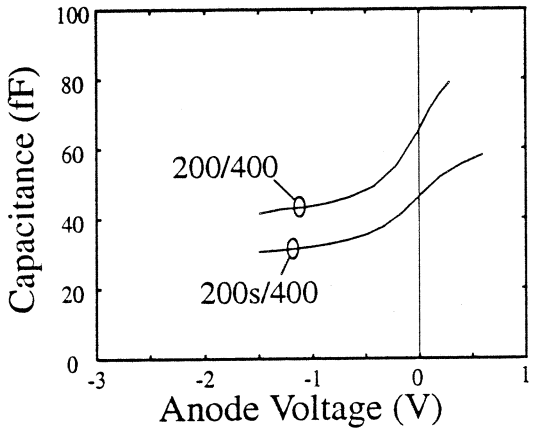


Figure 6a. C-V curves of VHV varactors having $d_1$=200Å, $d_2$=400Å, and 3μm anode diameters. The "s" designates higher Al content in the barrier.

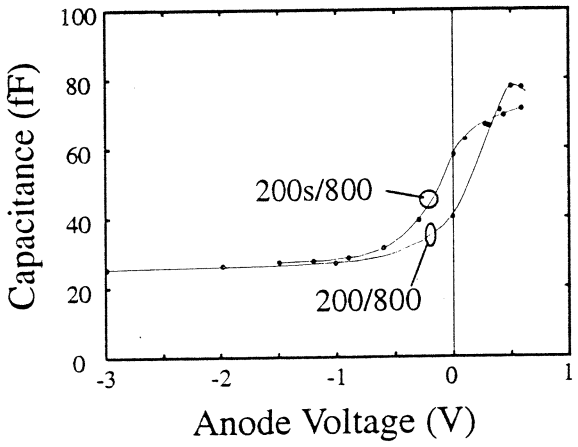


Figure 6b. C-V curves of VHV varactors having $d_1$=200Å, $d_2$=800Å, and 3μm anode diameters. The "s" designates higher Al content in the barrier.

diode model discussed above. The S-parameter derived C-V curves of Figures 6a and 6b illustrate the effects of $d_1$, $d_2$, and Al content on the S-parameter derived C-V characteristics. The useful operation range of these varactors, where leakage currents remained below about 10μA, extends from approximately -1.8V -> -1.4V to 0.26V -> 0.45V. The useful $C_{max}/C_{min}$ ratio of the 200/400, 200s/400, 200/800, and 200s/800 ($d_1/d_2$) (where s means x = 0.4 otherwise x = 0.52) varactors are 1.75, 1.8, 2.5, and 2.55 respectively. Increasing the Al content of the barrier layer increases the useful forward voltage swing and hence $C_{max}/C_{min}$ only slightly. Increasing $d_2$ from 400Å to 800Å

results in the expected trends of decreasing $C_{min}$ from 41.5fF to 26fF and increasing $C_{max}/C_{min}$ from 1.7 to 2.5.

Microwave characterization permitted the study of cutoff frequencies ($f_c$) as functions of anode diameter for several values $d_1$, $d_2$, and x, where: $f_c \triangleq \frac{1}{2\pi R_s C_{ja}}$ and $C_{ja} \triangleq \frac{C_{max}+C_{min}}{2}$. Figure 7 shows $f_c$ of the InGaAs/InAlAs varactors as functions of anode diameter and $d_2$ thickness. For large anode diameters, the perimeter/area ratio declines, making $R_s$ decrease more slowly, whereas $C_{ja}$ continues to increase proportional to anode area. Thus the decrease of $R_s \bullet C_{ja}$ with decreasing anode size, implies an inverse relation between $f_c$ and anode size. The cutoff frequency increased with $d_2$ due to the inverse relation between $d_2$ and $C_{ja}$. One μm varactors, having $d_1$ = 200Å and $d_2$ = 800Å showed $f_c$'s up to 2.4THz.

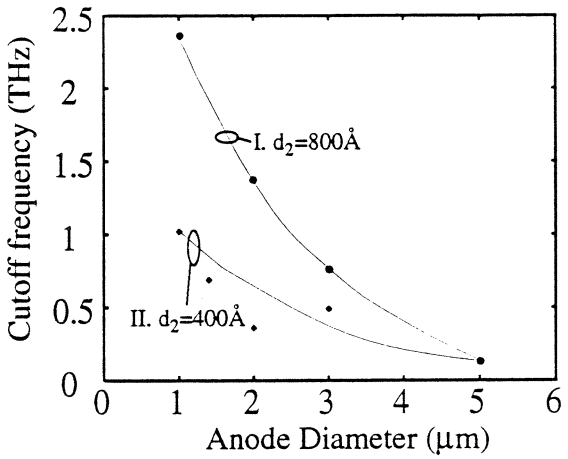


Figure 7. Cutoff frequency as a function of anode diameter and layer structure. In both layers, the In content, x = 0.52 and barrier layer thickness, $d_1$=200Å.

Varactors were also characterized at 4MHz via a low-frequency C-V meter. When 1μm, 3μm, and 48μm varactors with $d_1$, $d_2$ = 200Å and 800Å respectively, were tested, their diameters and pad capacitance could be adjusted to make their normalized C-V (C normalized to anode area) curves agree very well together. Thus, the low-frequency analysis showed that 1μm and 3μm varactors had nearly the same shape of C-V curve indicating that fringing capacitance effects were not significant.

# VII. Mixer Diode Electrical Results

InP mixers were fabricated using the layer structure shown in figure 1 above. The InGaAs/InP heterointerface was submerged in n+ material so as to minimize its effective electron barrier. The Schottky barrier was 0.33eV, as expected for InP. Ideality factors were close to unity. Figure 8 shows that this diode design appears to be promising given its superior ideality factor and reverse

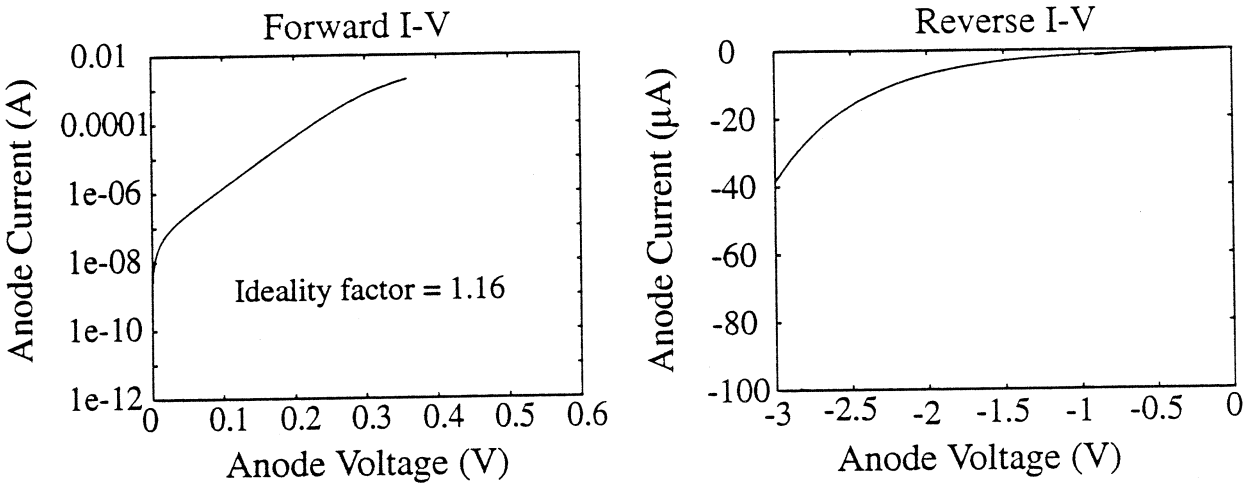


Figure 8. I-V characteristics of an InP/InGaAs mixer diode having an anode diameter = 1μm and the layer structure illustrated in figure 1 above. The $\phi_{be}$ is approximately 0.33eV.The diode exhibits a superior ideality factor lower reverse leakage relative to diodes having the heterointerface in the low-doped active region.

leakage relative to diode designs that have a heterointerface within the low-doped active region.

# VIII. Conclusions

Varactor diodes having cutoff frequencies above 2THz based on InAlAs/InGaAs have been fabricated and characterized. Devices were fabricated using a planar diode process featuring plated airbridges. A novel isolation process has been applied that greatly increases the controllability of the isolation etch and reduces etch time and ohmic metal undercutting. This new isolation process should also nearly eliminate the isolation etch problems of diodes that have very short (10-20μm) airbridges; as is the case for mixers integrated into log-periodic antennae.

An epitaxial lift-off process is under development that should allow the replacement of the InP substrate with glass or quartz substrates to ease dicing and reduce parasitic capacitance.

$C_{max}/C_{min}$ was seen to increase with active layer thickness ($d_2$). Leakage currents had been found to be reduced by increasing barrier thickness ($d_1$) and/or increasing the barrier's Al content. This study indicated that the cutoff frequency could be improved by moderate increases in active layer thickness and/or decreasing the anode diameter. Leakage currents can be reduced by using an Al mole fraction of 0.6 in the barrier layer.

InP/InGaAs mixer structures were also investigated. These results indicate that low ideality factors along with low reverse leakage can be obtained with InP diodes. Additionally, the 1μm InP mixer diode, investigated here, shows a forward current of 1mA at 0.316V which is much less bias than that required for a comparable GaAs diode. These mixer results indicate the possibility

of a substantial reduction of LO power requirements without the need for dc bias and are especially interesting relative to THz subharmonic mixers.

## Acknowledgments:

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